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μPD43501
1,024-CHANNEL TIME DIVISION SWITCH

Description

The μPD43501 is a time-switch device designed for use in a high-performance digital communications network. Features include a time-switch function by which up to 1,024 channels can be exchanged using a 16-bit data width, and a tone output function by which an 8-bit tone signal can be output to an arbitrary channel.

Two planes of 1-kword by 8-bit storage area and one plane of 1-kword by 10-bit control storage area for the time-switch function enable the μPD43501 to realize switching modes in which arbitrary 1,024 or 512 input channels can be connected to arbitrary 1,024 or 512 output channels. The configuration of the tone signal output section, one plane of 64-word by 8-bit tone storage area and one plane of 1-kword by 8-bit tone control storage area, allows the device to output up to 64 different tone signals to an arbitrary output channel as 8-bit voice/tone data.

Ordering Information

Part Number	Data Transfer Rate (max)	Package
μPD43501R	8.192 Mbps	132-pin ceramic pin grid array (PGA)

Features

- ☐ Separate switch storage and control storage to allow construction with one VLSI device of a non-blocking switching network having a maximum capacity of 1,024 channels
- ☐ Selectable operation
  - — 1,024 by 1,024 serial input and output
  - — 1,024 by 1,024 parallel input and output
    - • 16.384 MHz operating frequency
    - • 8.192 Mbps data transfer rate
  - — 512 by 512 parallel input and output
    - • 8.192 MHz operating frequency
    - • 4.096 Mbps data transfer rate
- ☐ Switching flexibility
  - — 8- or 16-bit data width
  - — n by 64 kbps connection
- ☐ Tone signal output function
- ☐ 8 by 8 space switch for an 8.192 Mbps, 128-channel multiplexed line
- ☐ CPU interfaces for the control storage and tone control storage
- ☐ Low power consumption: 1000 mW (typ)
- ☐ TTL-compatible inputs and outputs
- ☐ 132-pin ceramic pin grid array packaging

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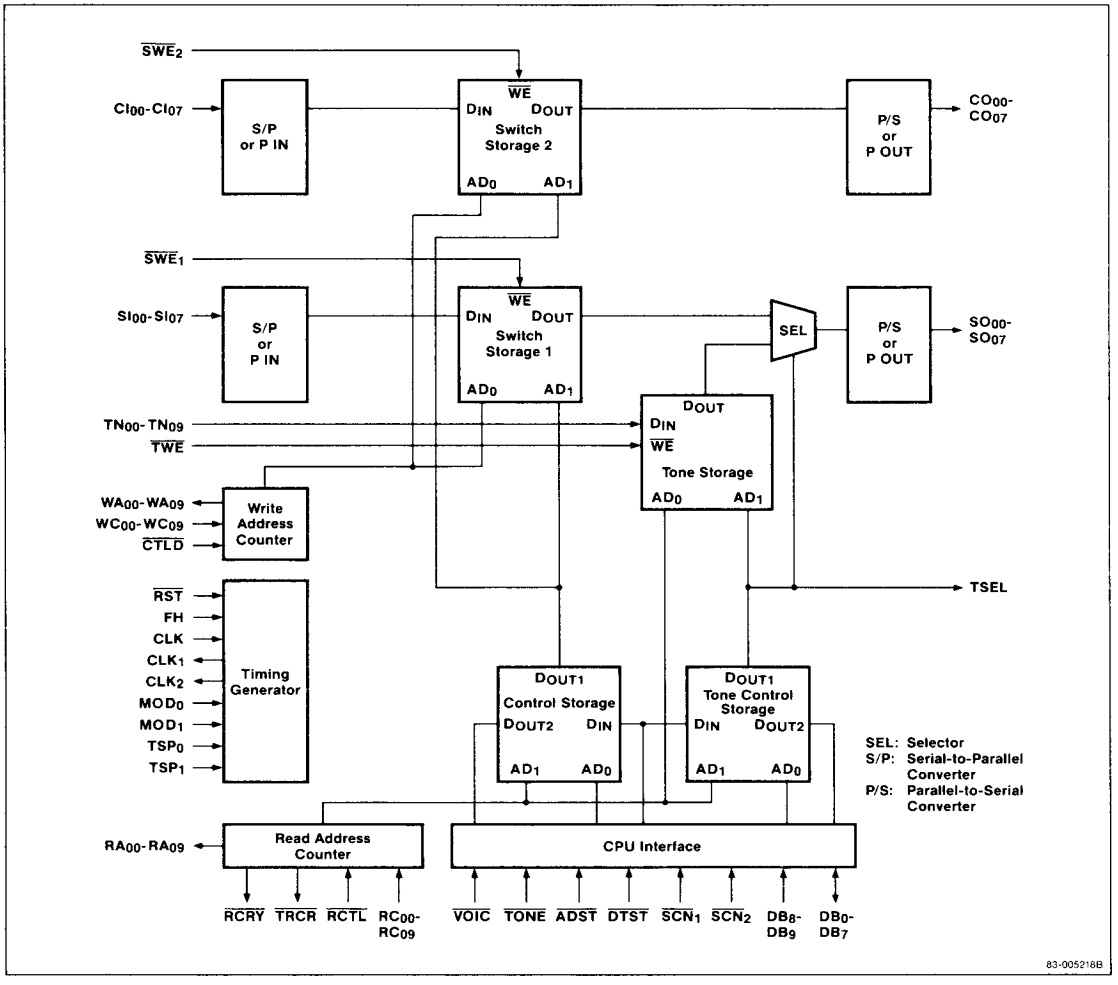
Contact your NEC sales representative for a copy of the complete data sheet.

Block Diagram



Switching Functions

Mode 0

In this mode, the μPD43501 inputs eight 128-channel multiplexed lines from ports SI_{00} through SI_{07} (or from CI_{00} through CI_{07}) and outputs eight 128-channel multiplexed lines to ports SO_{00} through SO_{07} (or CO_{00} through CO_{07}). Refer to figure 1 for a functional pin diagram.

Serial input data from the input ports first is converted to parallel data by the serial-to-parallel converters in the receive section, and then multiplexed and sent to the input section of the switch storage area. Since the write address counter is synchronized with input data, the write address of the switch storage area corresponds to the time slot number of the input signal. Writing multiplexed data to the switch address specified by the write address counter causes input data in the time slot corresponding to the switch address always to be stored at that address (figure 2).

Conversely, a control storage address corresponds to an output-side time slot number, and the data in control storage indicates the switch storage address, i.e., the input-side time slot number is stored at the control storage address corresponding to the output-side time slot to which the input-side is transferred.

The address signal is sent from the read address counter to control storage in synchronization with each output-side time slot. Data read out by this operation is then sent to the switch storage area as the address signal, and the data in the specified address (input-side time slot) is then read out on the output side and switched. Switched data is sent to the parallel-to-serial converters in the transmission section, where it is converted to serial data and then output to the appropriate output ports.

With this switching function, the data in an arbitrary time slot on the input side can be output as data in an arbitrary time slot on the output side. Furthermore, in addition to the time division switch function, a space switch function enables switching time slots on any of the eight input ports to be output on any of the eight output ports. This means that a nonblocking 8 x 8 space switch for 128-channel multiplexed lines can be realized.

Mode 1

Mode 1 makes it possible for the μPD43501 to input 512-channel multiplexed lines (4.096 Mbps by 8 bits), 8 bits in parallel, and output 512-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are then performed.

Mode 2

In Mode 2, the μPD43501 inputs 1,024-channel multiplexed lines (8.192 Mbps by 8 bits), 8 bits in parallel, and outputs 1,024-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are performed.

Figure 1. Functional Pin Diagram

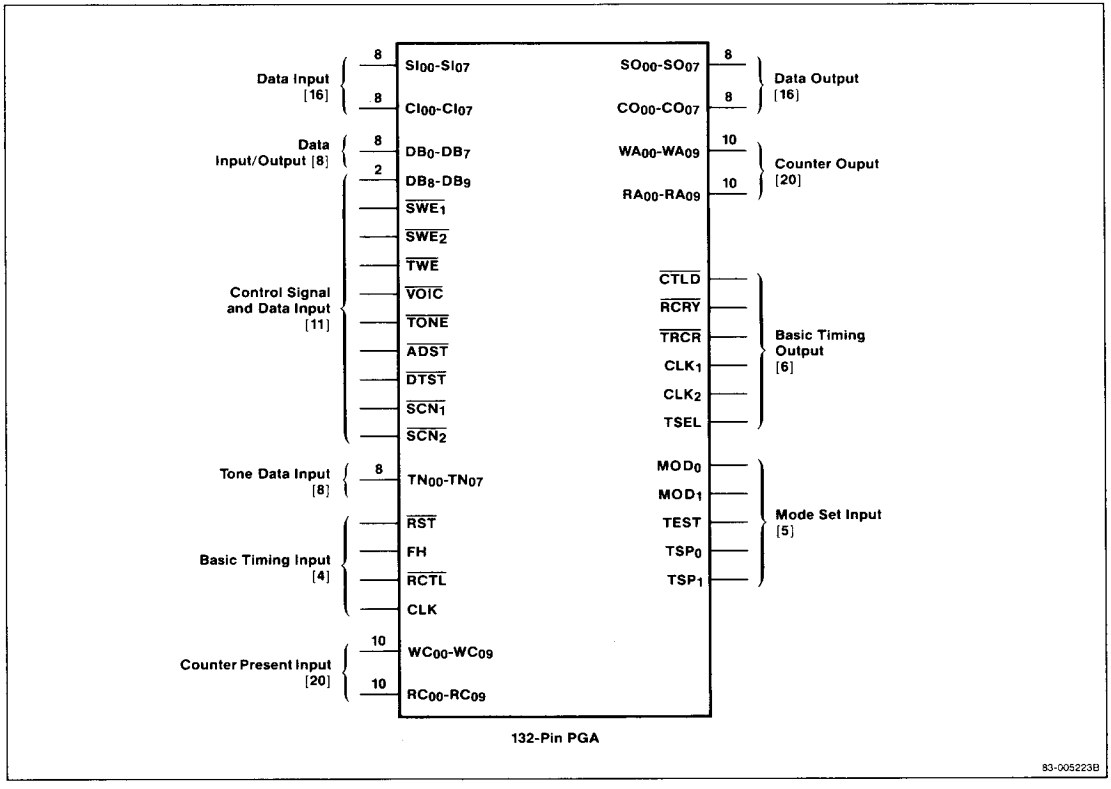


Figure 2. Time Slot Versus Frame Configuration