
HB56A272E Series

2,097,152-word $\times$ 72-bit High Density Dynamic RAM Module

HITACHI

ADE-203-291

Description

The HB56A272E belongs to 8 byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56A272E is a 2 M $\times$ 72 dynamic RAM module, mounted 9 pieces of 16-Mbit DRAM (HM5117800BTT) sealed in TSOP package and 2 pieces of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package. An outline of the HB56A272E is 168-pin socket type package (dual lead out). Therefore, the HB56A272E makes high density mounting possible without surface mount technology. The HB56A272E provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

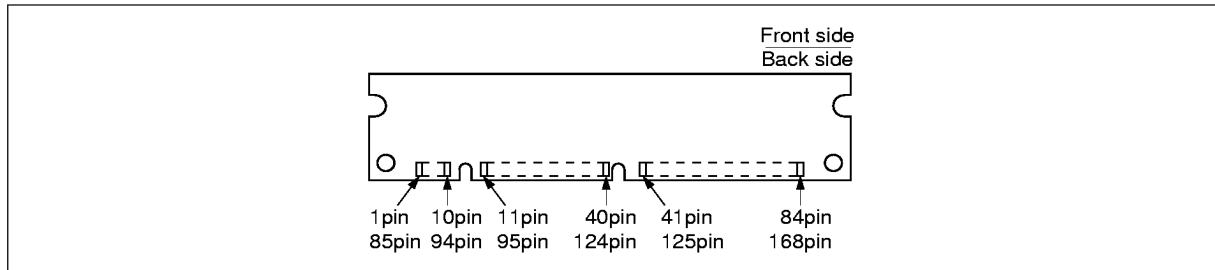
- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{\text{RAC}} = 60/70/80$ ns (max)
 - Access time: $t_{\text{CAC}} = 20/23/25$ ns (max)
- Low power dissipation
 - Active mode: 6.01/5.53/5.06 W (max)
 - Standby mode (TTL): 431 mW (max)
- Buffered input except $\overline{\text{RAS}}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 2,048 refresh cycle: 32 ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

HB56A272E Series

Ordering Information

Type No.	Access time	Package	Contact pad
HB56A272E-6B	60 ns	168-pin dual lead out socket type	Gold
HB56A272E-7B	70 ns		
HB56A272E-8B	80 ns		

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{ss}	16	DQ12	31	$\overline{OE0}$	46	$\overline{CE4}$
2	DQ0	17	DQ13	32	V _{ss}	47	NC
3	DQ1	18	V _{cc}	33	A0	48	$\overline{WE2}$
4	DQ2	19	DQ14	34	A2	49	V _{cc}
5	DQ3	20	DQ15	35	A4	50	NC
6	V _{cc}	21	DQ16	36	A6	51	NC
7	DQ4	22	DQ17	37	A8	52	DQ18
8	DQ5	23	V _{ss}	38	A10	53	DQ19
9	DQ6	24	NC	39	NC	54	V _{ss}
10	DQ7	25	NC	40	V _{cc}	55	DQ20
11	DQ8	26	V _{cc}	41	NC	56	DQ21
12	V _{ss}	27	$\overline{WE0}$	42	NC	57	DQ22
13	DQ9	28	$\overline{CE0}$	43	V _{ss}	58	DQ23
14	DQ10	29	NC	44	$\overline{OE2}$	59	V _{cc}
15	DQ11	30	$\overline{RE0}$	45	$\overline{RE2}$	60	DQ24

Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
61	NC	88	DQ38	115	NC	142	DQ59
62	NC	89	DQ39	116	V _{SS}	143	V _{CC}
63	NC	90	V _{CC}	117	A1	144	DQ60
64	NC	91	DQ40	118	A3	145	NC
65	DQ25	92	DQ41	119	A5	146	NC
66	DQ26	93	DQ42	120	A7	147	NC
67	DQ27	94	DQ43	121	A9	148	NC
68	V _{SS}	95	DQ44	122	NC	149	DQ61
69	DQ28	96	V _{SS}	123	NC	150	DQ62
70	DQ29	97	DQ45	124	V _{CC}	151	DQ63
71	DQ30	98	DQ46	125	NC	152	V _{SS}
72	DQ31	99	DQ47	126	B0	153	DQ64
73	V _{CC}	100	DQ48	127	V _{SS}	154	DQ65
74	DQ32	101	DQ49	128	NC	155	DQ66
75	DQ33	102	V _{CC}	129	NC	156	DQ67
76	DQ34	103	DQ50	130	NC	157	V _{CC}
77	DQ35	104	DQ51	131	NC	158	DQ68
78	V _{SS}	105	DQ52	132	P $\overline{\text{DE}}$	159	DQ69
79	PD1	106	DQ53	133	V _{CC}	160	DQ70
80	PD3	107	V _{SS}	134	NC	161	DQ71
81	PD5	108	NC	135	NC	162	V _{SS}
82	PD7	109	NC	136	DQ54	163	PD2
83	ID0 (V _{SS})	110	V _{CC}	137	DQ55	164	PD4
84	V _{CC}	111	NC	138	V _{SS}	165	PD6
85	V _{SS}	112	NC	139	DQ56	166	PD8
86	DQ36	113	NC	140	DQ57	167	ID1 (V _{SS})
87	DQ37	114	NC	141	DQ58	168	V _{CC}

HB56A272E Series

Pin Description

Pin Name	Function
A0 to A11, B0	Address Input (D0 to D8) : A0 to A10, B0 Row Address (D0 to D8) : A0 to A10, B0 Column Address (D0 to D8) : A0 to A9, B0 Refresh Address (D0 to D8) : A0 to A10, B0
DQ0 to DQ71	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row Address Strobe ($\overline{RAS}$)
$\overline{CE0}$, $\overline{CE4}$	Column Address Strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
PD1 to PD8	Presence Detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence Detect Enable
NC	No Connection

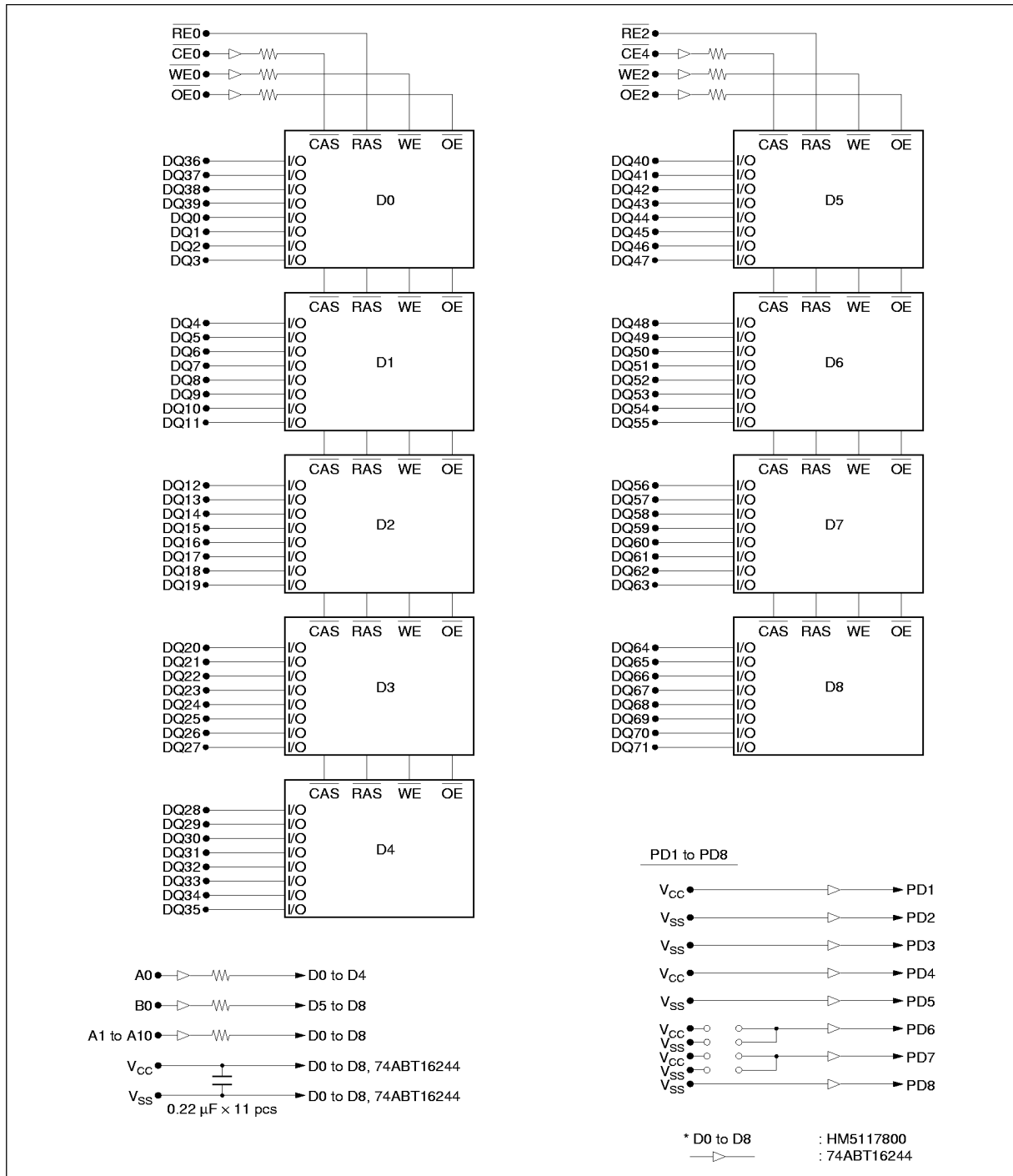
Presence Detect Pin Assignment

Pin Name	Pin No.	$\overline{PDE}$ = Low			$\overline{PDE}$ = High
		60 ns	70 ns	80 ns	All
PD1	79	1	1	1	High-Z
PD2	163	0	0	0	High-Z
PD3	80	0	0	0	High-Z
PD4	164	1	1	1	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	0	0	0	High-Z

1: High-Level (Driver Output)

0: Low Level (Driver Output)

Block Diagram



HB56A272E Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	10	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−0.5	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

HB56A272E Series

DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)

		HB56A272E								
		60 ns		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions	Notes
Operating current	I_{CC1}	—	1144	—	1054	—	964	mA	$t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	82	—	82	—	82	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z	
		—	73	—	73	—	73	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
$\overline{\text{RAS}}$ -only refresh current	I_{CC3}	—	1144	—	1054	—	964	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	109	—	109	—	109	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I_{CC6}	—	1144	—	1054	—	964	mA	$t_{RC} = \text{min}$	
Fast page mode current	I_{CC7}	—	874	—	784	—	739	mA	$t_{PC} = \text{min}$	1, 3
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 5.5\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 5.5\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.

3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{\text{CAS}}, \overline{\text{WE}}, \overline{\text{OE}}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{\text{RAS}}$)	C_{I3}	—	78	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

HB56A272E Series

AC characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)^{*1, *2, *18}

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HB56A272E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	18	10000	20	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	47	20	55	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	20	—	23	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	20	—	23	—	25	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	32	—	32	—	32	ms	19

HB56A272E Series

Read Cycle

		HB56A272E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	23	—	25	ns	9, 10, 17
Access time from address	t_{AA}	—	35	—	40	—	45	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	20	—	23	—	25	ns	9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	30	—	35	—	45	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	2	—	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	—	20	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	20	—	20	—	20	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	20	—	23	—	25	—	ns	5

Write Cycle

		HB56A272E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20	—	23	—	25	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15	—	18	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	15	—	20	—	20	—	ns	15

HB56A272E Series

Read-Modify-Write Cycle

		HB56A272E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	155	—	181	—	205	—	ns	
RAS to $\overline{WE}$ delay time	t _{RWD}	90	—	103	—	115	—	ns	14
CAS to $\overline{WE}$ delay time	t _{CWD}	40	—	46	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t _{AWD}	55	—	63	—	70	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t _{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

		HB56A272E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t _{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t _{WRP}	5	—	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t _{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t _{RPC}	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

		HB56A272E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t _{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	40	—	45	—	50	ns	9, 17
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HB56A272E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t _{PRWC}	85	—	96	—	105	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t _{CPW}	60	—	68	—	75	—	ns	14

- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh cycle or $\overline{CAS}$ -before- $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
 11. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 13. t_{OFF} (max) and t_{OEZ} (max) is defined the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{CPW} \geq t_{CPW}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OE} \geq t_{CWL}$, the I/O pins will remain open circuit (high impedance); if $t_{OE} \leq t_{CWL}$, invalid data will be out at each I/O.
 19. t_{REF} is determined by 2,048 refresh cycles.

