Brushless DC motor and VCM drive circuit with speed control

TDA5341

FEATURES

- Full-wave commutation (using push-pull output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull MOS outputs:
  - 1 A output current
  - Low voltage drop
  - Built-in current limiter
- Thermal protection
- General purpose operational amplifier
- Reset generator
- Motor brake facility
- Actuator driver (H-bridge current-controlled)
- Power-down detector
- Automatic park and brake procedure
- Adjustable park voltage
- Sleep mode
- Speed control with Frequency-Locked Loop (FLL)
- Serial port
- Friction reduction prior to spin-up.

APPLICATIONS

- Hard Disk Drive (HDD).

GENERAL DESCRIPTION

The TDA5341 is a BiCMOS integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

The TDA5341 also includes a Voice Coil Motor driver (VCM), reset and park facilities and an accurate speed regulator. In addition, a serial port facilitates the control of the device.

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	general supply voltage for logic and power	4.5	5.0	5.25	V
I_{oMOT}	motor output current	1.3	1.6	1.9	A
$R_{DS(MOT)}$	motor output resistance	–	1.1	1.56	Ω
I_{oACT}	actuator output current	0.7	1.1	1.4	A
$R_{DS(ACT)}$	actuator output resistance	–	2.0	2.5	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5341G	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM

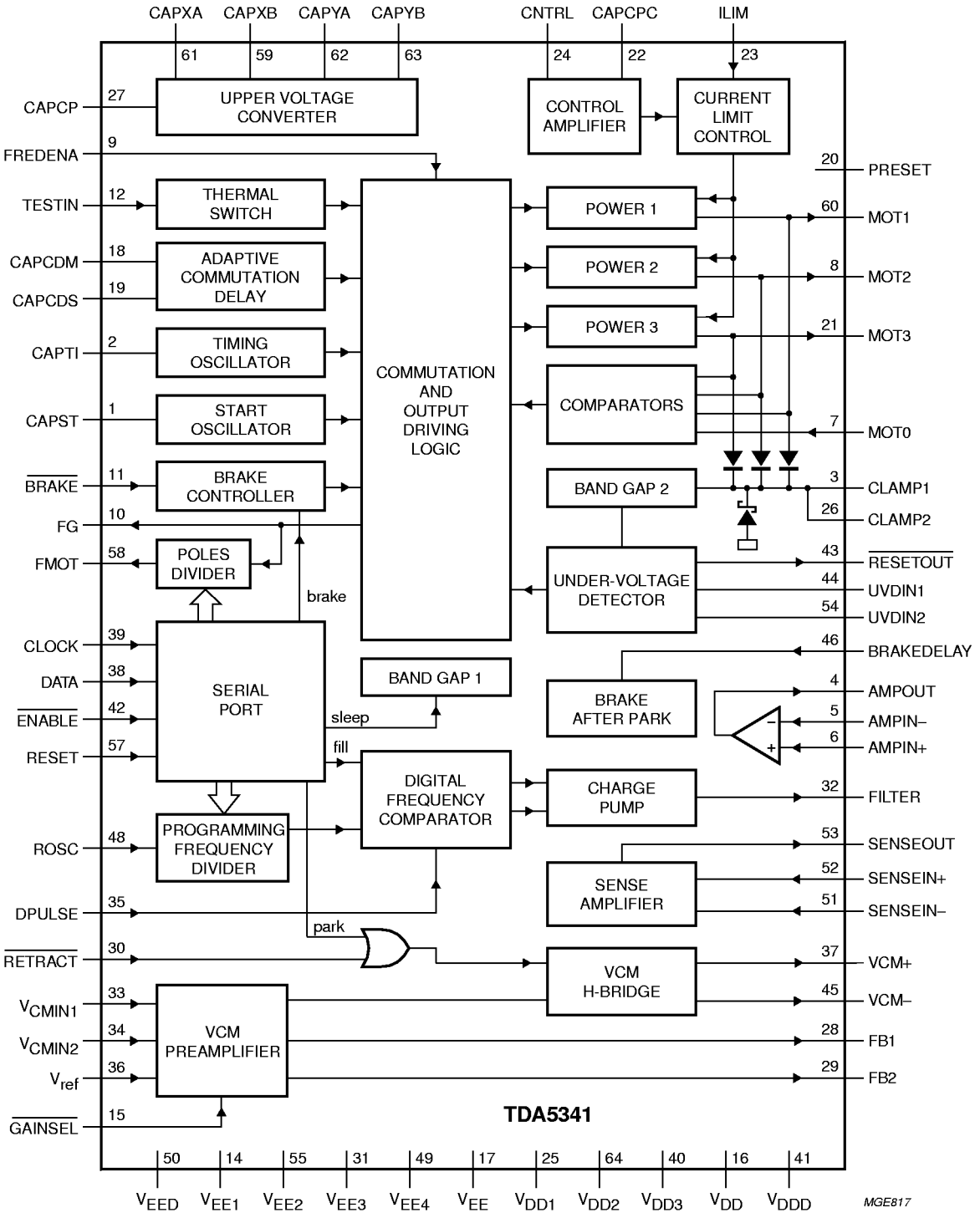


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CAPST	1	external capacitor for starting oscillator
CAPTI	2	external capacitor for timer circuit
CLAMP1	3	external capacitor used to park the heads; must be externally connected to CLAMP2
AMPOUT	4	uncommitted operational amplifier output
AMPIN−	5	uncommitted operational amplifier invert input
AMPIN+	6	uncommitted operational amplifier direct input
MOT0	7	motor centre tap input
MOT2	8	motor driver output 2
FREDENA	9	friction reduction mode enable input (active HIGH)
FG	10	frequency generator (tacho) output
$\overline{\text{BRAKE}}$	11	brake input command (active LOW)
TESTIN	12	test input for power output switch-off (active HIGH)
TP1	13	test purpose 1 (should be left open-circuit)
V_{EE1}	14	ground for the spindle motor drivers
$\overline{\text{GAINSEL}}$	15	VCM gain adjustment input (switch ON when $\overline{\text{GAINSEL}}$ is LOW)
V_{DD}	16	general power supply
V_{EE}	17	general ground
CAPCDM	18	external capacitor for adaptive commutation delay (master)
CAPCDS	19	external capacitor for adaptive commutation delay (slave)
PRESET	20	set the motor drivers into a fixed state: MOT1 = F (floating), MOT2 = L, MOT3 = H
MOT3	21	motor driver output 3
CAPCPC	22	frequency compensation of the current control
ILIM	23	current limit control input
CNTRL	24	motor control
V_{DD1}	25	power supply 1 for the spindle motor drivers
CLAMP2	26	external capacitor used to park the heads; must be externally connected to CLAMP1
CAPCP	27	external capacitor for the charge pump output
FB1	28	output of the VCM preamplifiers
FB2	29	switchable output of the VCM preamplifier
$\overline{\text{RETRACT}}$	30	park input command (active LOW)
V_{EE3}	31	ground 3 for the actuator driver
FILTER	32	charge pump output to be connected to an external filter
V_{CMIN1}	33	VCM voltage control input
V_{CMIN2}	34	switchable VCM voltage control input
DPULSE	35	data pulse input of the frequency comparator of the speed control
V_{ref}	36	voltage reference input
VCM+	37	positive output of the VCM amplifier
DATA	38	input data of the serial port (active HIGH)
CLOCK	39	clock input signal to shift DATA into SERIALIN register (active HIGH)
V_{DD3}	40	power supply 3 for the actuator driver

SYMBOL	PIN	DESCRIPTION
V_{DDD}	41	digital power supply
$\overline{ENABLE}$	42	enable input; enables the serial port, i.e. allows DATA to be shifted in (active LOW)
$\overline{RESETOUT}$	43	under-voltage detector output flag (active LOW)
UVDIN1	44	external capacitor for the $\overline{RESETOUT}$ duration
VCM−	45	negative output of the VCM amplifier
BRAKEDELAY	46	delay control input for brake after park
TP2	47	test purpose 2 (should be left open-circuit)
ROSC	48	reference oscillator input for motor speed control
V_{EE4}	49	ground 4 for the actuator driver
V_{EED}	50	digital ground
SENSEIN−	51	inverting input of the VCM sense amplifier
SENSEN+	52	non-inverting input of the VCM sense amplifier
SENSEOUT	53	output of the VCM sense amplifier
UVDIN2	54	external voltage reference for the under-voltage detector
V_{EE2}	55	ground 2 for the spindle motor drivers
TP3	56	test purpose 3 (should be left open-circuit)
RESET	57	reset input; forces all bits of the SERIALIN register to 0 (active HIGH)
FMOT	58	tachometer output (one pulse per mechanical revolution)
CAPXB	59	external capacitor for the charge pump output
MOT1	60	motor driver output 1
CAPXA	61	external capacitor for the charge pump output
CAPYA	62	external capacitor for the charge pump output
CAPYB	63	external capacitor for the charge pump output
V_{DD2}	64	power supply for the spindle motor drivers

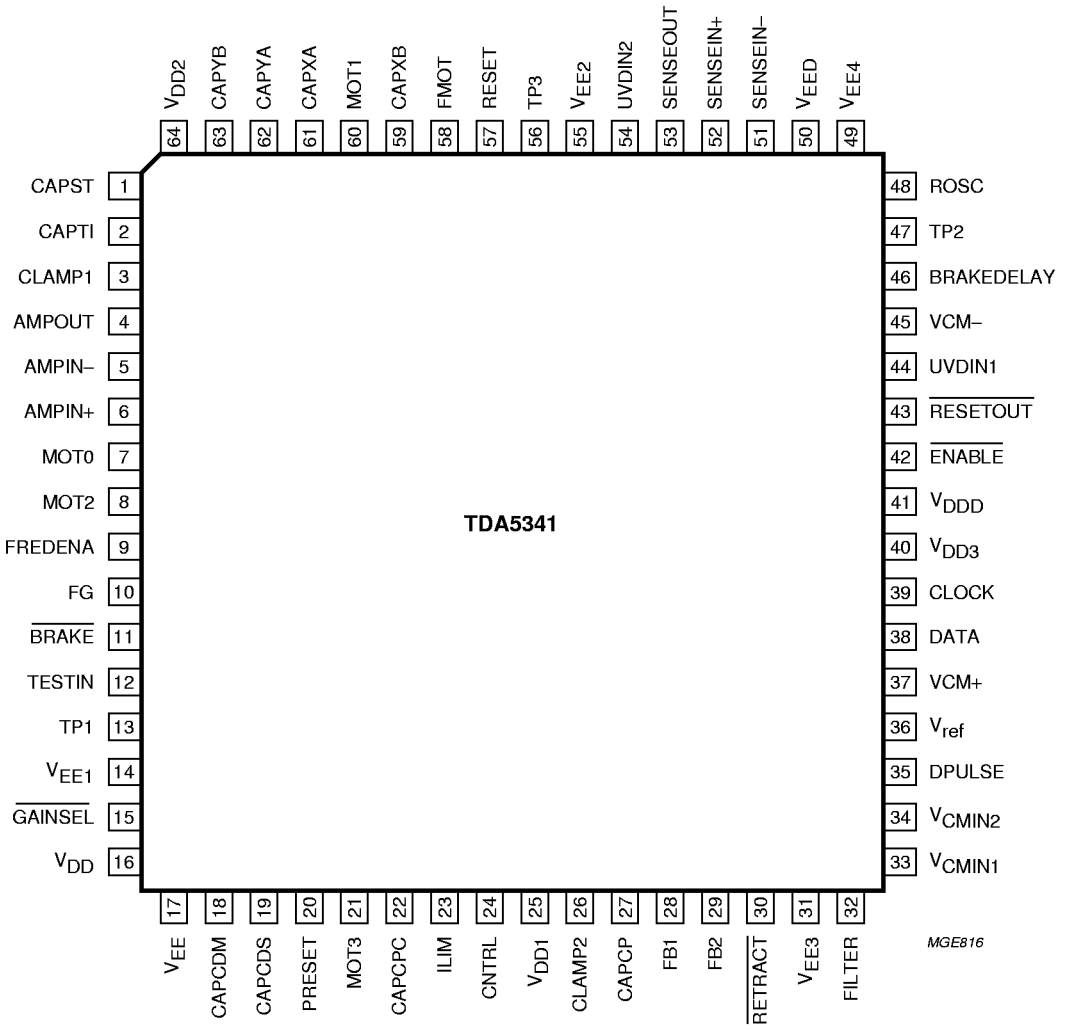


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TDA5341 offers a sensorless three-phase motor full-wave drive function. The device also offers protected outputs capable of handling high currents and can be used with star or delta connected motors.

The TDA5341 can easily be adapted for different motors and applications.

The TDA5341 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three-phase full-wave drive
- High output current (1.3 A)
- Low MOS R_{DSon} (1 Ω)
- Outputs protected by current limitation and thermal protection of each output transistor
- Low current consumption
- Additional uncommitted operational amplifier
- H-bridge actuator driver current controlled with an external series sense resistor
- Automatic retract procedure
- Adjustable park voltage
- Sleep mode
- Automatic brake (after park) procedure
- Speed control based on FLL technique
- Serial port DATAIN (24 bits)
- Friction reduction prior to spin-up.

TDA5341 modes description

The TDA5341 can be used in two main modes, depending on whether they are controlled or not.

The 'controlled modes' (user commands) are executed by the TDA5341 without delay or priority treatment, either by software via the serial port or by hardware. BRAKE is a hardware command whereas RETRACT can be controlled in both ways. If it is preferable to control the heads parking via the serial bus, the equivalent pin can be left open-circuit.

The sleep mode is controlled by software only; it results from the combination of the spindle and actuator being disabled. The spindle is turned off by bit SPINDLE DISABLE, whereas the actuator is disabled towards bit VCM DISABLE of the serial port (see Section "Serial port"). In addition, a special spin-up mode can be activated in the event of high head stiction

The 'uncontrolled modes' only result from different failures caused by either a too high internal temperature or an abnormally low power voltage, which will cause the actuator to retract and, after the spindle, to brake. The output signals mainly affected by those failures are $\overline{\text{RESETOUT}}$, MOT1, 2 and 3, VCM+ and VCM–. This is summarised in Tables 1 and 2.

Table 1 Summary of controlled modes

HARDWARE/ SOFTWARE	MODE	MOT1, 2 AND 3	VCM+ AND VCM–	$\overline{\text{RESETOUT}}$	EFFECT
Software	spindle disable	high impedance	high impedance	HIGH	spindle off
Software	VCM disable	not affected	high impedance	HIGH	spindle on; VCM off
Hardware	brake	LOW	not affected	HIGH	spindle coils ground
Software/ hardware	retract	not affected	VCM– = 0.65 V; VCM+ = 0 V	HIGH	heads parked
Hardware	friction reduction	–	not affected	HIGH	heads in vibration

Table 2 Summary of uncontrolled modes

FAILURE	MOT1, 2 AND 3	VCM+ AND VCM–	$\overline{\text{RESETOUT}}$	EFFECT
Thermal shut-down	high impedance → LOW	VCM– = 0.65 V; VCM+ = 0 V	LOW	automatic park and brake
Voltage shut-down	high impedance → LOW	VCM– = 0.65 V; VCM+ = 0 V	LOW	automatic park and brake

Controlled modes

SPINDLE DISABLE

The spindle circuitry is switched off when bit 23 (SPINDLE DISABLE) of the serial port is pulled HIGH. In that mode, the reference band gap generator is cut off so that all internal current sources are disabled. Both the spindle and actuator outputs will be set to the high impedance state because the upper converter is also turned off.

It should be noted that the uncommitted operational amplifier is also disabled in that mode.

VCM DISABLE

The actuator will be disabled when bit 22 (VCM DISABLE) is set to logic 1; the spindle circuitry is not affected in that mode. The retract circuitry also remains active, so that the heads can be parked although the VCM is disabled. In that mode, the current consumption can be reduced by ±4 mA.

SLEEP MODE

The sleep mode is obtained by pulling both the SPINDLE and VCM DISABLE bits of the serial port HIGH. The power monitor circuitry only remains active in sleep mode.

RETRACT

Retract is activated by pulling either bit 21 (PARK) HIGH or $\overline{\text{RETRACT}}$ (pin 30) LOW. When $\overline{\text{RETRACT}}$ is set LOW, a voltage of 0.65 V is applied to pin VCM– for parking.

It should be noted that the park voltage can be made adjustable by changing one of the interconnect masks. Accordingly, some different voltages, varying from 0.2 to 1.2 V, can quickly be obtained on customer demand. This mode does not affect the control of the spindle rotation.

BRAKE MODE

The brake mode is activated by pulling $\overline{\text{BRAKE}}$ (pin 11) LOW. When a voltage of less than 0.8 V is applied to pin $\overline{\text{BRAKE}}$, the 3 motor outputs are short-circuited to ground, which results in a quick reduction of the speed until the motor stops completely.

FRICTION REDUCTION

Pulling FREDENA HIGH activates the friction reduction mode of the TDA5341. In that mode, a clock signal fed via pin TESTIN will cause the MOT outputs to sequentially switch-on and switch-off at the same frequency and, as a result, generate an AC spindle torque high enough to overcome the head stiction.

Before start-up, the head stiction might be higher than normal due to condensation between the head(s) and the disk(s). Normal spin-up is not possible when this friction torque is higher than the start-up torque of the spindle motor. Spin-up is then only possible after friction has been reduced by breaking the head(s) free. Bringing a static friction system into mechanical resonance is an effective method to break static friction head(s) free.

The resonance frequency is:

$$f_{res} = \left(\frac{1}{2\pi}\right) \times 0.5\left(\frac{C}{J}\right)$$

Where:

C = Stiffness of the head-spring(s) in direction of disk(s) rotation, (N/m)

J = Inertia of the disk(s), (kg/m^2).

The external clock input frequency must be:

$$f_{clk} = \left(\frac{6}{2\pi}\right) \times 0.5\left(\frac{C}{J}\right)$$

A burst of n × 6 clock pulse will bring the system into resonance and break the heads free (n > 2). Once the heads have been broken free, the normal spin-up procedure can be applied.

It should be noted that the clock frequency must be smaller than 40000/CAPCDM (nF).

Uncontrolled modes

POWER SHUT-DOWN

If the power supply decreases to less than the voltage threshold determined by the ratio between R1 and R2 connected to UVDIN2 (see Fig.8) (for more than 1 μs), the TDA5341 will issue a reset ($\overline{\text{RESETOUT}}$ goes LOW) and the following operation will start:

- Firstly, the MOT outputs are switched to the high impedance state so as to get back the rectified EMF issued from the motor itself. At the same time, the voltage upper converter is cut off in order to preserve the voltage on the charge pump capacitance at CAPCP. The energy supplied in that way is then used to park the heads in a safe position
- Secondly, after a certain period of time, depending on the RC constant of the device connected to BRAKEDELAY, the lower MOS drivers will be turned on in order to stop the motor completely.

THERMAL SHUT-DOWN

Should the temperature of the chip exceed +140 ±10 °C, a shut-down operation will also be processed. The actions described for power shut-down will be sequenced in the same manner.

SPINDLE SECTION (see Fig.1)

Full-wave driving of a three-phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing current and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, i.e. the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal (FG).

The system will only function when the EMF voltage from the motor is present. Consequently, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5341 also contains a control amplifier, directly driving output amplifiers.

The TDA5341 also provides access to the user of some of its internal test modes. Firstly, a PRESET mode can be used for prepositioning the three motor output drivers into a fixed state. By pulling pin PRESET to 0.75 V above V_{DD}, MOT3 goes HIGH, MOT2 goes LOW and MOT1 goes to the high impedance state.

In addition, when TESTIN is pulled HIGH (provided that FREDENA is LOW), the 3 motor output drivers are switched off. It should be noted that $\overline{\text{RESETOUT}}$ goes LOW in that particular event.

Adjustments

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals.

The start capacitor (CAPST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 5.5 μA, from 0.05 to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$t_{start} = (0.78 \times C)$; where C is given in μF.

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5341 will run the motor.

If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = \frac{0.5}{\Pi} \times \left(K_t \times I \times \frac{P}{J} \right)^{\frac{1}{2}}$$

Where:

K_t = torque constant (N.m/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J (kg/m^2).

Example: J = 6.34×10^{-7} kg/m^2, K = 4.5×10^{-3} N.m/A, p = 6 and I = 0.48 A; thus f_{osc} = 22.7 Hz. Without damping, a start frequency of 48.4 Hz can be chosen or t = 24 ms, thus C = 0.024/0.78 = 0.031 μF, (choose 33 nF).

The Adaptive Commutation Delay (CAPCDM and CAPCDS)

In this circuit capacitor CAPCDM is charged during one commutation period, with an interruption of the charging current during the diode pulse.

During the next commutation period this capacitor (CAPCDM) is discharged at twice the charging current. The charging current is 10 μA and the discharging current 20 μA; the voltage range is from 0.87 to 2.28 V.
The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = \frac{10 \times 10^{-6}}{f \times 1.41} = \frac{7092}{f_{C1}}$$

Where C is in nF.

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.28 to 0.87 V at 20 μA.

Maximum delay = (0.070 × C) ms: Where C is in nF.

Example: nominal commutation frequency is 3240 Hz and the lowest usable frequency is 1600 Hz, thus CAPCDM = 7092/1600 = 4.43 (choose 4.7 nF)

The other capacitor, CAPCDS, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAPCDM. Figure 3 illustrates typical voltage waveforms.

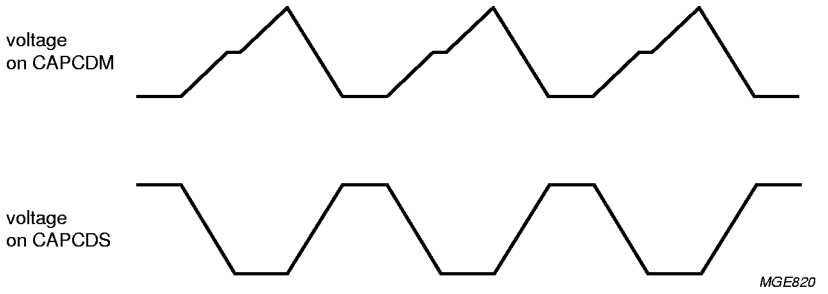


Fig.3 CAPCDM and CAPCDS voltage waveforms in normal running mode.

The Timing Capacitor (CAPTI)

Capacitor CAPTI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode pulse back to a positive EMF voltage (or vice-versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).

A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding. However, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 60 μA, from 0.03 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 30 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V. The value of CAPTI is given by:

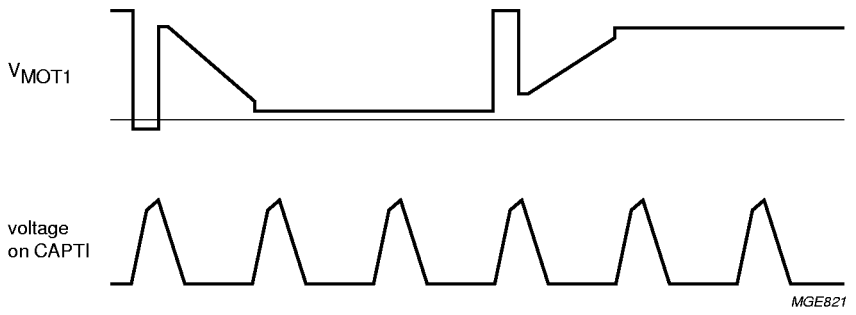
$$C = 5 \times 10^{-6} \times \frac{t_m}{1.9} = 2.63 t_m$$

Where: C is in nF and t is in ms.

Example: If, after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 10 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$C = 2.63 \times 3.5 = 9.2$ (choose 10 nF)

Typical voltage waveforms are illustrated by Fig.4.



If the chosen value of CAPTI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.4 Typical CAPTI and V_{MOT1} voltage waveforms in normal running mode.

Other design aspects

There are other design aspects concerning the application of the TDA5341 besides the commutation function. They are as follows:

- Generation of the tacho signal FG
- Motor control
- Current limiting
- Thermal protection.

FG signal

The FG signal is generated in the TDA5341 by using the zero-crossing of the motor EMF from the three motor windings and the commutation signal.

Output FG switches from HIGH-to-LOW on all zero-crossings and LOW-to-HIGH on all commutations and can source more than 40 μA and sink more than 1.6 mA.

Example: A three-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of $25 \times 6 \times 6 = 900$ Hz and generates a tacho signal of 900 Hz.

Motor control

Figure 5 shows the spindle transconductance by giving the relative output current as a function of the voltage applied to pin CNTRL.

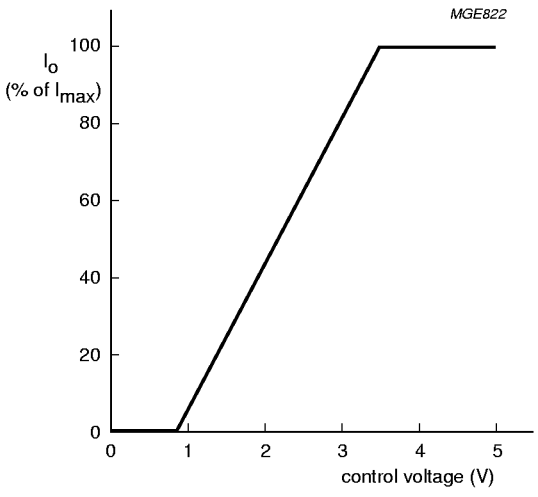


Fig.5 Output current control.

Current limiting

Outputs MOT1 to MOT3 are protected against high currents in two ways; current limiting of the 'lower' output transistor and current limiting of the 'upper' one. This means that the current from and to the output stages is limited.

It is possible to adjust the limiting current externally by using an external resistor connected between pin ILIM and ground, the value is determined by the formula:

$$I_{ILIM} = 10020 \times \frac{2.54}{R}$$

Where R = R (min.) = 19.5 kΩ and I_{ILIM} = 1.3 A.

If R < 19.5 kΩ, then I_{ILIM} is internally limited for device protection purposes.

Thermal protection

Thermal protection of the six output transistors of the spindle section is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high. In that event, a RESET is automatically generated to the external world by pulling $\overline{\text{RESETOUT}}$ LOW.

Reset section

This circuit provides the following:

- An external signal that sends a $\overline{\text{RESETOUT}}$ (active LOW) to the disk drive circuitry at power-up and power-down
- Causes actuator to retract (PARK).

The power-up reset signal ($\overline{\text{RESETOUT}}$) applied to external circuits as a digital output is typically 150 ms after power-up. In the same way, as soon as V_{DD} goes below a threshold that is externally set (UVDIN2), $\overline{\text{RESETOUT}}$ goes LOW. The under voltage detection threshold is adjustable with external resistors (see Fig.8).

The reset circuitry has a minimum output pulse (100 ms) even for brief power interruptions (higher than 1 ms). The pulse duration can be adjusted with an external capacitor (UVDIN1).

The power for retraction is received from the rectification of the EMF of the spindle before it is spun down. After retraction, a brake procedure is automatically settled. The time needed for retraction, prior to braking, can be precisely adjusted with the external RC device connected to pin BRAKEDELAY. The discharge of the capacitance across the resistance from V_{DD} – 0.7 V down to 1 V will provide the desired time constant.

Actuator section

The actuator driver has a control input voltage that is proportional to the actuator current which is capable of a closed-loop band-pass frequency higher than 10 kHz.

An operational amplifier input allows passive external components for compensation and gain setting. The compensation amplifier is able to be pulled out of a saturation state within 5 μs and its output swing is V_{DD} – 1.5 V.

An actuator current-sense amplifier is provided for use by the disc drive controller. The gain from current-sense resistor to sense the amplifier output is typically 10 (±3%) and the output voltage swing is ±1.25 V. An input common mode range insures operation through all normal coil voltage excursions. Maximum recovery time from saturation is 20 μs (typ.).

TRANSFER FUNCTION

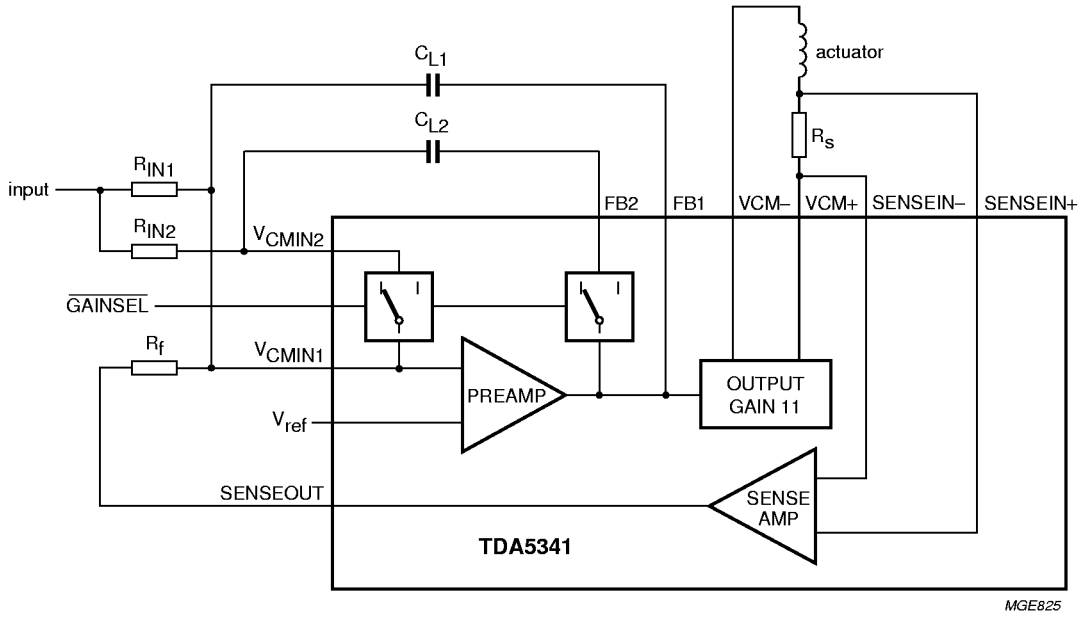


Fig.6 VCM section application diagram.

$$T = -11 \times R_f \times Z_L \times \left(\frac{1}{R_{IN} \times (R_f \times R_s + R_f \times Z_{VCM} + 110 \times R_s \times Z_L)} \right)$$

With $\overline{GAINSEL}$ = HIGH; $R_{IN} = R_{IN1}$

With $\overline{GAINSEL}$ = LOW; $R_{IN} = \frac{R_{IN1} \times R_{IN2}}{R_{IN1} + R_{IN2}}$

Speed control function

Speed control is efficiently achieved by the frequency-locked loop circuitry which is enabled by bit D20 of the CONTROL register.

Its aim is to keep the tachometer signal set to a reference programmed by the user via the serial port (see Section "Serial port").

The FLL operates as follows:

When power is first applied to the circuit, the FILTER pin is pulled HIGH so that maximum output current can be sourced for optimum torque.

FG pulses will appear rapidly so as to provide a 'clean' clock signal (FMOT) that will issue one pulse per mechanical revolution. This may be used for speed regulation, by re-entering the signal through the DPULSE pin. Then, after it has been synchronised to the ROSC clock, it is compared to an accurate reference derived from the ROSC clock and programmed by the user via the serial port. The resulting variation in frequency generates a speed error term that will switch a charge-pump up or down in order to charge or discharge an external RC filter (FILTER). The voltage at the FILTER pin is then used as an input to the current control amplifier that regulates the current in both upper and lower NMOS transistors.

A velocity regulation based upon (maximum) one corrective action per mechanical revolution may be considered insufficient in some applications. That is the reason why the second input of the FLL circuitry was intentionally left open-circuit and directly accessible to the external world via pin DPULSE. In that way, total freedom is given to the user to use any signal coming out of the microcontroller in order to regulate the motor velocity with a finer accuracy.

Moreover, a mixed regulation is also possible: firstly, the FMOT signal is fed via DPULSE into the FLL circuitry and then once data is read out off the disc, it is switched to another clock signal with a higher frequency than FMOT. Simultaneously, a new division factor is programmed via the serial port.

It should be noted that there is no need for external synchronization. However, it is recommended to change the division factor and the DPULSE clock rate during the period when FMOT is HIGH.

Serial port

The serial port operates as follows:

When $\overline{\text{ENABLE}}$ is HIGH, the serial port is disabled, which means the TDA5341 functions regardless of any change at pins DATA and CLOCK.

When $\overline{\text{ENABLE}}$ is set LOW some set-up time before the falling edge of CLOCK, the serial port is enabled, i. e. data is serially shifted into the 24-bit shift register on the falling edge of the CLOCK signal. The least significant bit (LSB = DATA 0) is the first in, DATA(23) the MSB is the last in.

When $\overline{\text{ENABLE}}$ goes HIGH, the contents of the shift register are loaded into the internal fixed register (CONTROL register), it will not change until the next rising edge of $\overline{\text{ENABLE}}$.

It should be noted that when RESET goes HIGH it will force all bits of the shift register and the control register to logic 0. However, there is no reset effect on both power-up and power-down i.e there is no correlation between RESET and $\overline{\text{RESETOUT}}$.

CLOCK can be stopped (either in the HIGH or LOW state) once RESET or $\overline{\text{ENABLE}}$ have been asserted.

The 24-bit control register is organized as follows:

- D23: SPINDLE DISABLE
  - When LOW, the spindle circuitry is enabled
- D22: VCM DISABLE
  - When LOW, the actuator circuitry is enabled
- D21: PARK
  - When HIGH, it enables the head retraction. This has the same effect as pin $\overline{\text{RETRACT}}$ pulled LOW
- D20: FLL ENABLE
  - When HIGH, it closes the complete speed regulation loop
  - When LOW, it will set the output of the charge pump (FILTER) to the high impedance state
- D19 and D18
  - The combination of these bits fixes the division factor to apply on the FG signal with respect to the number of poles.

Table 3 Division factor

D19	D18	POLE PAIRS
0	0	4
0	1	6
1	0	8
1	1	12

- D17 to D0

  These bits program the division factor to apply to the ROSC signal so as to generate a reference that will precisely control the spindle rotation;

  – The division factor can range from 8 (DIV = 1) to $8 \times [2^{18} - 1] = 2097144$ (DIV = 3FFFF)

  – The relationship between this division factor, ROSC and the motor frequency is as follows:

  DIVISION FACTOR = 7.5 × ROSC/MOTOR speed where the MOTOR speed is given in rpm and ROSC in Hz.

Example: for a motor speed of 3600 rpm and a reference oscillation ROSC of 16 MHz, the division factor that has to be programmed via the bus, will be:

$$DIV = 7.5 \times \frac{16 \times 10^{-6}}{3600} = 33333$$

The resulting error will be less than 0.04 rpm.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

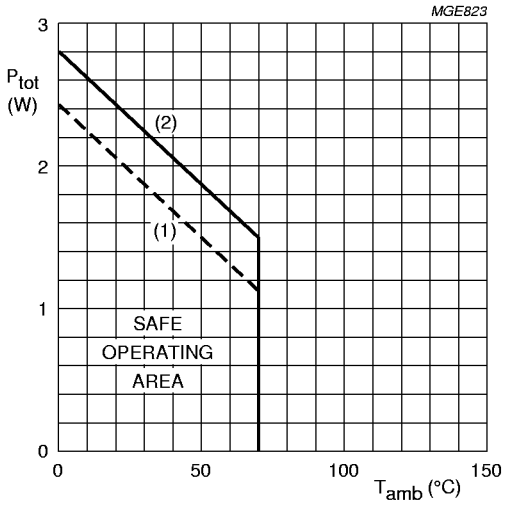
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	5.5	V
V_i	input voltage (all pins)	–0.3	V_{DD} + 0.3	V
$V_{60,8,21}$	output voltage pins MOT1, MOT2 and MOT3	–0.25	+5.5	V
$V_{45,37,53}$	output voltage pins VCM–, VCM+ and SENSEOUT	0.7	V_{DD} + 0.7	V
$V_{1,2,18,19}$	input voltage pins CAPST, CAPTI, CAPCDM and CAPCDS	–	2.5	V
T_{stg}	IC storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
P_{tot}	total power dissipation	see Fig.7		

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C. Method 3015 (HBM 1900 Ω, 100 pF) 3 pulses positive and 3 pulses negative on each pin with reference to ground. Class 1 : 0 to 1999 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	54	K/W



(1) $T_{j(max)}$ = 130 °C.
(2) $T_{j(max)}$ = 150 °C.

Fig.7 Power derating curve.

CHARACTERISTICS (SPINDLE FUNCTION)

V_{DD} = 5 V; V_{DD1} and V_{DD2} > V_{DD} is not allowed; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	general supply voltage		4.5	5.0	5.25	V
V_{DD1}	supply voltage 1 for the spindle motor drivers		4.5	5.0	5.25	V
V_{DD2}	supply voltage 2 for the spindle motor drivers		4.5	5.0	5.25	V
V_{DD3}	supply voltage for the actuator driver		4.5	5.0	5.25	V
I_{DD}	general supply current		–	11	15	mA
$I_{q(sm)}$	quiescent current in sleep mode		–	1.4	2	mA
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	°C
V_{so}	test pin switch-off voltage		2.5	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MOT0						
V_i	input voltage level		–0.3	–	V_{DD} – 1.7	V
I_{bias}	input bias current		–1	–	0	µA
V_{CSW}	comparator switching voltage level	note 1	±6.8	±9.2	±11.6	mV
ΔV_{CWS}	variation in comparator switching voltage levels within one IC		–3.4	–	+3.4	mV
MOT1, MOT2 and MOT3; pins 60, 8 and 21						
V_{DO}	drop-out voltage	I_o = 250 mA	–	–	0.34	V
		I_o = 250 mA; T_{amb} = 70 °C	–	–	0.39	V
t_r	output rise time	from 0.2 to 0.8V_{DD}	10	25	35	µs
t_f	output fall time	from 0.8 to 0.2V_{DD}	10	25	35	µs
Output current limiting circuit; V_{ILIM} = 5 V; pin 23						
I_{ILIM}	limiting current (estimation)	R_{ILIM} = 20 kΩ	1.15	1.25	1.35	A
V_{ILIM}	input voltage	I_{ILIM} = 100 µA	2.43	2.51	2.60	V
$I_{ILIM(CR)}$	limiting current control range (estimation)	$I_{ILIM} = \frac{I_o}{10000}$	0.01	–	1.3	A
Output current control circuit; pin 24						
V_{CNTRL}	input voltage level		0	–	V_{DD}	V
C_{CPC}	control loop stability capacitor		–	100	–	nF
CAPCPC; pin 22						
$I_{o(sink)}$	output sink current		30	40	50	µA
$I_{o(source)}$	output source current		–5.5	–3.5	–1.5	µA
CAPCP; pin 27						
C_{extCP}	external output capacitor for the charge pump	note 2	22	–	–	nF
$I_{o(sink)}$	output sink current	V_{DD} = 0 V; V_{clamp} = 1.2 V	–	1	2.5	µA
V_{CP}	charge pump voltage		9.0	9.9	10.8	V
CAPST; pin 1						
$I_{o(sink)}$	output sink current		4.5	6.0	7.5	µA
$I_{o(source)}$	output source current		–7.0	–5.5	–4.0	µA
$V_{SW(L)}$	lower switching level		–	0.20	–	V
$V_{SW(M)}$	middle switching level		–	0.30	–	V
$V_{SW(H)}$	upper switching level		–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAPTI; pin 2						
$I_{o(sink)}$	output sink current		25	35	45	µA
$I_{oH(source)}$	HIGH level output source current		–85	–70	–55	µA
$I_{oL(source)}$	LOW level lower source current		–7.5	–5.0	–2.5	µA
$V_{SW(L)}$	lower switching level		–	30	–	mV
$V_{SW(M)}$	middle switching level		–	0.3	–	V
$V_{SW(H)}$	upper switching level		–	2.2	–	V
CAPCDM; pin 18						
$I_{o(sink)}$	output sink current		13	20	27	µA
$I_{o(source)}$	output source current		–13.5	–10	–6.5	µA
I_{sink}/I_{source}	ratio of sink-to-source current		–2.2	–2.0	–1.8	
V_{IL}	LOW level input voltage		0.82	0.87	0.92	V
V_{IH}	HIGH level input voltage		2.20	2.28	2.37	V
CAPCDS; pin 19						
$I_{o(sink)}$	output sink current		13	20	27	µA
$I_{o(source)}$	output source current		–27	–20	–13	µA
I_{sink}/I_{source}	ratio of sink-to-source current		–1.1	–1.0	–0.9	µA
V_{IL}	LOW level input voltage		0.82	0.87	0.92	V
V_{IH}	HIGH level input voltage		2.20	2.28	2.37	V
FG; pin 10						
V_{OL}	LOW level output voltage	I_o = 0 µA	–	–	0.5	V
I_{OL}	LOW level output current	V_{OL} = 1 V	3.3	5.3	–	mA
I_{OH}	HIGH level output current	V_{OH} = 4.5 V	–	–83	–40	mA
R_F	ratio of FG frequency and commutation frequency		–	1	–	
δ	duty factor		–	50	–	%
$\overline{\text{BRAKE}}$; pin 11						
I_{NM}	normal mode current	V_{NM} = 2.8 V	–40	–27	–	µA
V_{NM}	normal mode voltage		2.65	–	V_{DD}	V
V_{BM}	brake mode voltage		–	–	2.35	V
I_{BM}	brake mode current		–40	–24	–	µA
Upper converter; pins 61 and 62						
C_{XA}	external pump capacitor pin 61		–	10	–	nF
C_{YA}	external pump capacitor pin 62		–	10	–	nF

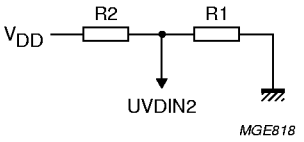
Notes

1. Switching levels with respect to MOT1, MOT2 and MOT3.
2. CAPCP value is dependant of the powerless park and brake operations.

CHARACTERISTICS (RESET FUNCTION)

V_{DD} = 5 V; V_{DD1} and V_{DD2} > V_{DD} is not allowed; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
UVDIN1; pin 44						
I_{UVDIN1}	load capacitance current to control the reset pulse width		–2.3	–1.7	–1.3	µA
V_{UVDIN1}	input voltage threshold to activate the reset output		2.4	2.55	2.75	V
UVDIN2; pin 54						
V_{UVDIN2}	comparator voltage for power-up and power-down detection	see Fig.8	1.280	1.315	1.340	V
I_{UVDIN2}	input current	V_{UVDIN2} = 1.6 V	–0.5	–	+0.5	µA
$\overline{\text{RESETOUT}}$; pin 43						
V_{PTH}	power threshold voltage	see Fig.9	–	4.25	–	V
t_{dPU}	power-up reset delay	C = 0.1 µF; see Fig.9	100	150	200	ms
t_{dPD}	power-down reset delay	see Fig.9	–	–	4	µs
t_{PDW}	power-down reset pulse width	see Fig.9	1.0	–	4	µs
$t_{W(min)}$	minimum output pulse width	C = 0.1 µF	100	–	–	ms
R_{pu}	pull-up resistance		6	10	14	kΩ
V_{OL}	LOW level output voltage	I_{OL} = 8.5 mA	–	–	0.5	V



$$\text{under-voltage threshold} = 1.32 \times \frac{(R2 + R1)}{R1}$$

Fig.8 Reset mode threshold.

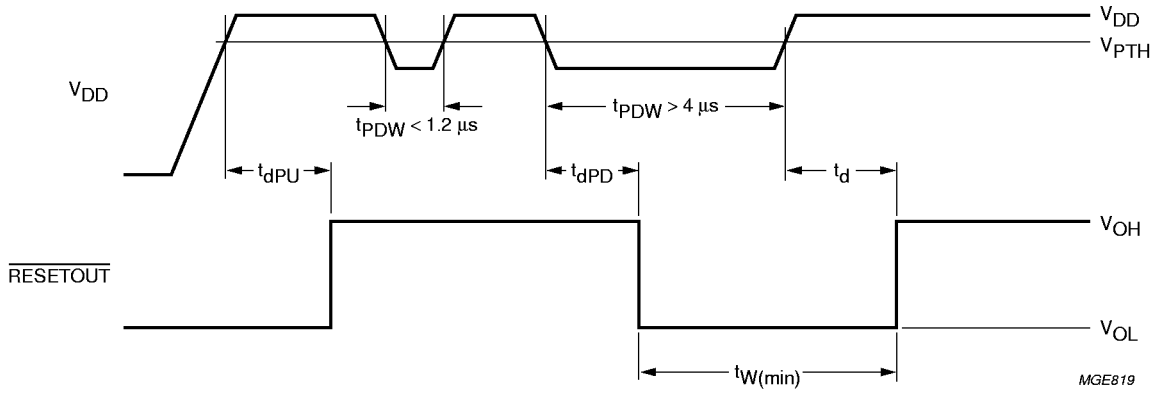


Fig.9 Reset mode timing.

CHARACTERISTICS (VCM FUNCTION)

V_{DD} = 5 V; V_{DD1} and V_{DD2} > V_{DD} is not allowed; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SENSEIN− and SENSEIN+; pins 51 and 52						
V_{CS}	common input sense voltage		0	–	V_{DD}	V
I_{iSENSE}	input sense current		−250	–	+250	µA
SENSEOUT; pin 53						
ΔV_{SENSE}	differential output voltage	V_{ref} = 1.9 to 2.6 V	0.5	V_{ref} ±1.25	4.0	V
I_{oSENSE}	output sense current		−250	–	+250	µA
G_{SENSE}	sense amplifier gain		9.9	10.2	10.5	
f_{co}	cross-over frequency		–	40	–	MHz
$V_{o(os)}$	output offset voltage	$I_{SENSEIN}$ = 0	−66	–	+66	mV
t_{RSA}	recovery time from saturation		–	20	–	µs
V_{ref}; pin 36						
V_{ref}	reference input voltage		1.9	–	2.6	V
I_{ref}	reference input current		−5	–	+5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCM+ and VCM–; pins 37 and 45						
V_{CMdo}	drop-out voltage	I_o = 400 mA	–	0.8	1.0	V
I_{oLIM}	output current limiting		0.7	1.15	1.5	A
G_v	power amplifier voltage gain		9	–	12	
V_{oPARK}	output park voltage	R_L = 40 Ω; note 1	–	0.75	–	V
VCMIN1 and VCMIN2						
V_i	input voltage level		1.9	–	2.6	V
I_{ibias}	input bias current		–	–	0.25	µA
$I_{i(os)}$	input offset current		–	25	–	nA
$\overline{\text{GAINSEL}}$; pin 15						
V_{IH}	HIGH level input voltage		2	–	–	V
V_{IL}	LOW level input voltage		–	–	0.8	V
I_{IH}	HIGH level input current		–10	–	+10	µA
I_{IL}	LOW level input current		–20	–	+10	µA
R_{SW}	switch resistance	$\overline{\text{GAINSEL}}$ = LOW	–	–	40	Ω
		$\overline{\text{GAINSEL}}$ = HIGH	10	–	–	MΩ
FB1 and FB2; pins 28 and 29						
$V_{i(os)}$	input offset voltage		–5	–	+5	mV
ΔV_{FB}	feed-back differential output voltage	V_{DD} = 5.25 V	±0.4	–	$\pm V_{DD}$ – 0.45	V
f_{co}	cross-over frequency		–	10	–	MHz
I_{oFB}	feed-back output current		–250		+250	µA
t_{RSB}	recovery time from saturation		–	5	–	µs
R_{SW}	switch resistance	$\overline{\text{GAINSEL}}$ = LOW	–	–	40	Ω
		$\overline{\text{GAINSEL}}$ = HIGH	10	–	–	MΩ
$\overline{\text{RETRACT}}$; pin 30						
V_{IH}	HIGH level input voltage		2	–	–	V
V_{IL}	LOW level input voltage		–	–	0.8	V
I_{IH}	HIGH level input current		–10	–	+10	µA
I_{IL}	LOW level input current		–20	–	+10	µA
BRAKEDELAY; pin 46						
V_{BM}	brake mode threshold voltage		–	0.75	1.0	V
V_{NM}	normal mode voltage		V_{DD} – 0.85	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Uncommitted operational amplifier; pins 4 to 6						
$V_{i(os)}$	input offset voltage		–3.5	–	+3.5	mV
$I_{i(bias)}$	input bias current		–250	–	+250	nA
$I_{i(os)}$	input offset current		–	25	–	nA
V_{CM}	common mode voltage		1.7	–	2.6	V
G_{OL}	open loop gain		–	68	–	dB
f_{co}	cross-over frequency		–	10	–	MHz
V_{OL}	LOW level output voltage	I_{OL} = 250 μA	–	–	0.7	V
V_{OH}	HIGH level output voltage	I_{OH} = –250 μA	4.3	–	–	V

Note

1. This is the PARK default value. Other values can be obtained with a metal mask change.

CHARACTERISTICS (SPEED CONTROL FUNCTION)

V_{DD} = 5 V; V_{DD1} and V_{DD2} > V_{DD} is not allowed; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FILTER; pin 32						
$I_{o(sink)}$	output sink current		80	100	120	μA
$I_{o(source)}$	output source current		–110	–90	–70	μA
I_{sink}/I_{source}	ratio of sink-to-source current		0.9	1.1	1.2	
$\lvert I_{LO} \rvert$	charge pump leakage current		–5	–	+5	nA
DATA, RESET and $\overline{\text{ENABLE}}$; pins 38, 57 and 42						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.4	–	–	V
I_i	input current		–	0	–	μA
CLOCK; pin 39						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.4	–	–	V
f_{clk}	clock frequency		–	–	18	MHz
ROSC; pin 48						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.4	–	–	V
f_{refOSC}	reference oscillator frequency		1	–	20	MHz
DPULSE; pin 35						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.4	–	–	V
f_{DPULSE}	data pulse frequency		–	–	10	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FMOT; pin 58						
V_{OL}	LOW level output voltage	I_{OL} = 500 μA	–	–	0.1	V
δ	duty factor		–	50	–	%
Timing; see Fig.10						
t_{su1}	$\overline{\text{ENABLE}}$ set-up time		8	–	–	ns
t_{su2}	DATA set-up time		6	–	–	ns
t_h	DATA hold time		10	–	–	ns

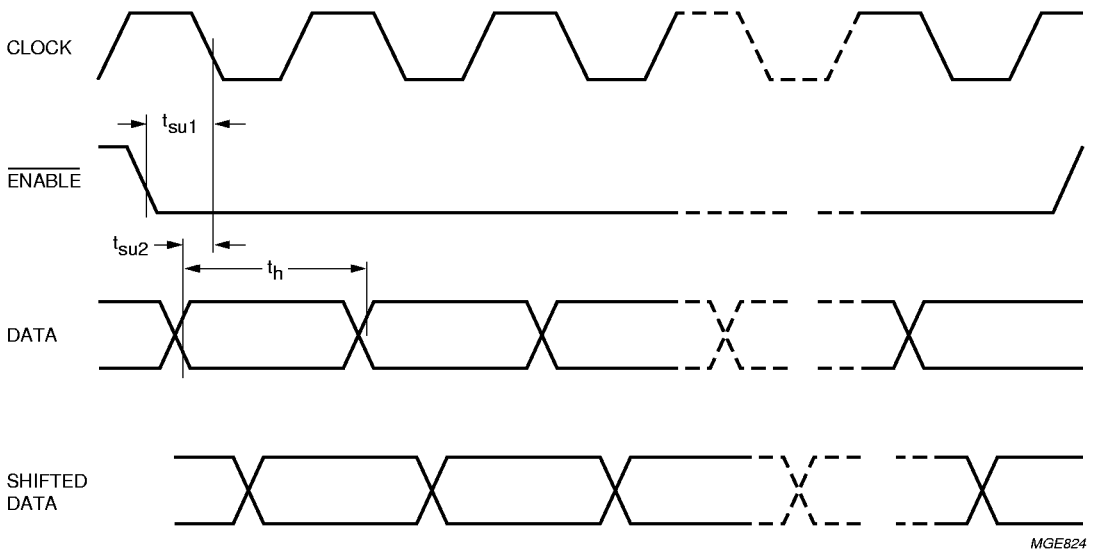


Fig.10 Timing diagram.

APPLICATION INFORMATION

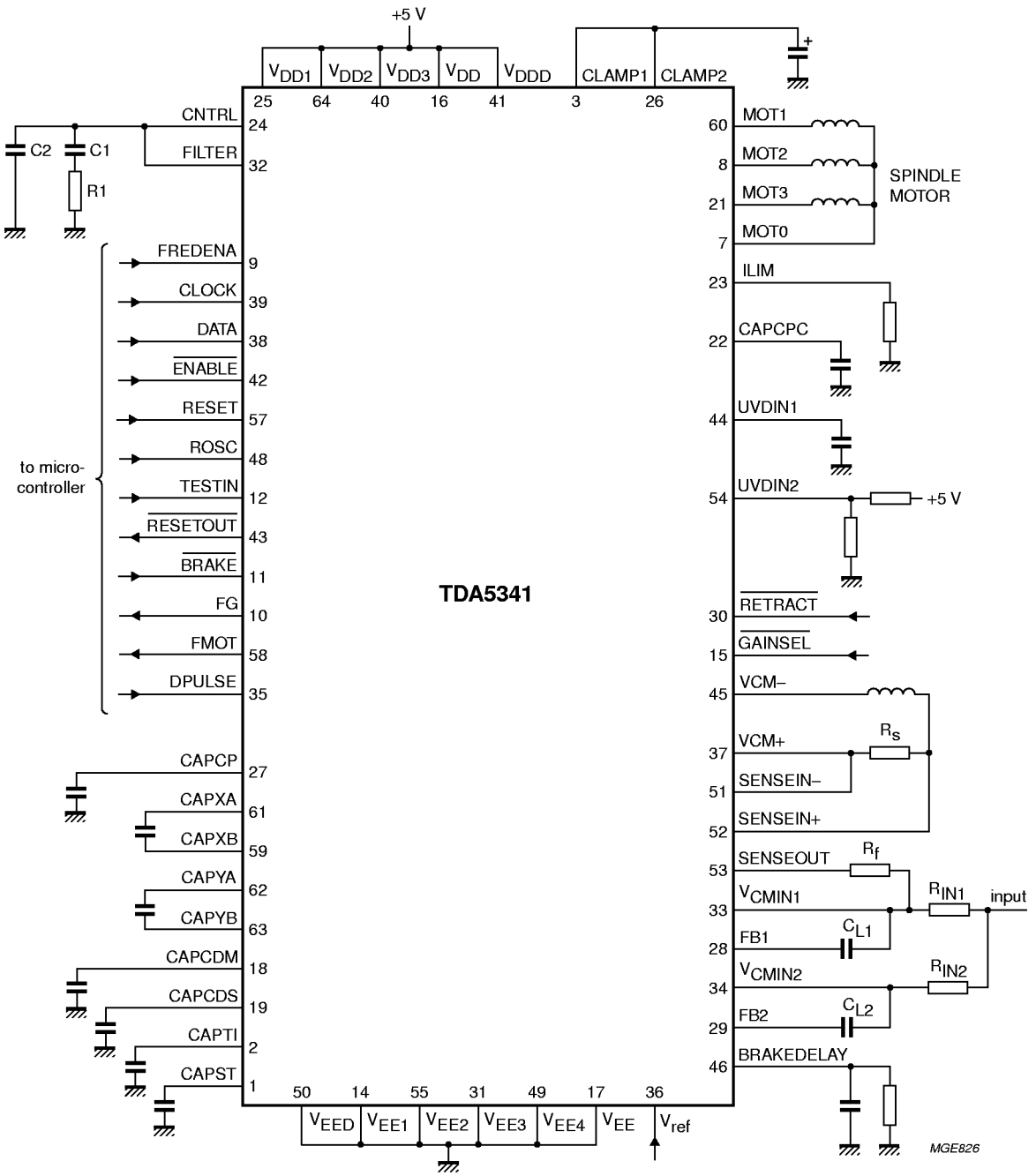
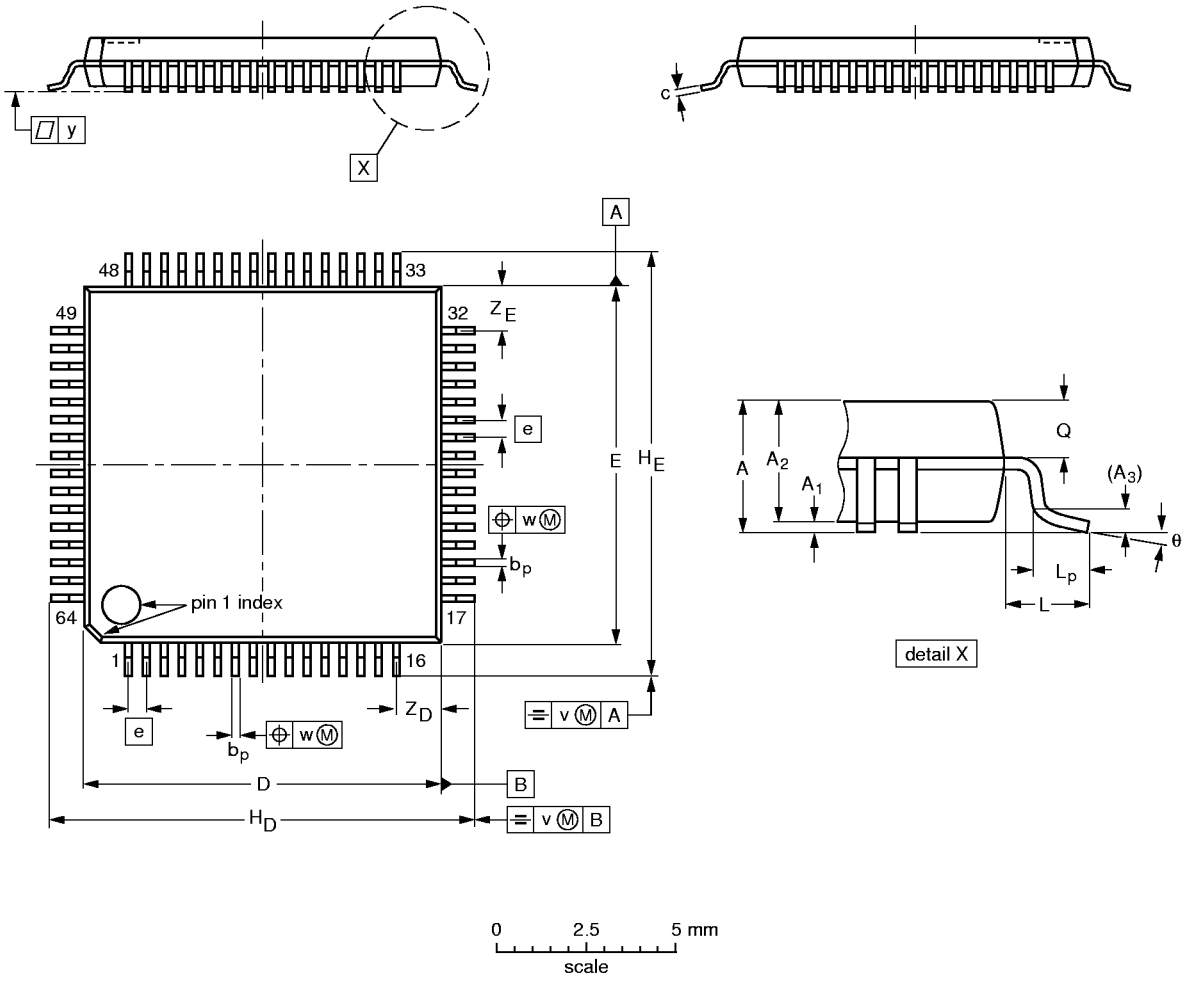


Fig.11 Application diagram of the TDA5341 in a hard disk drive.

PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.