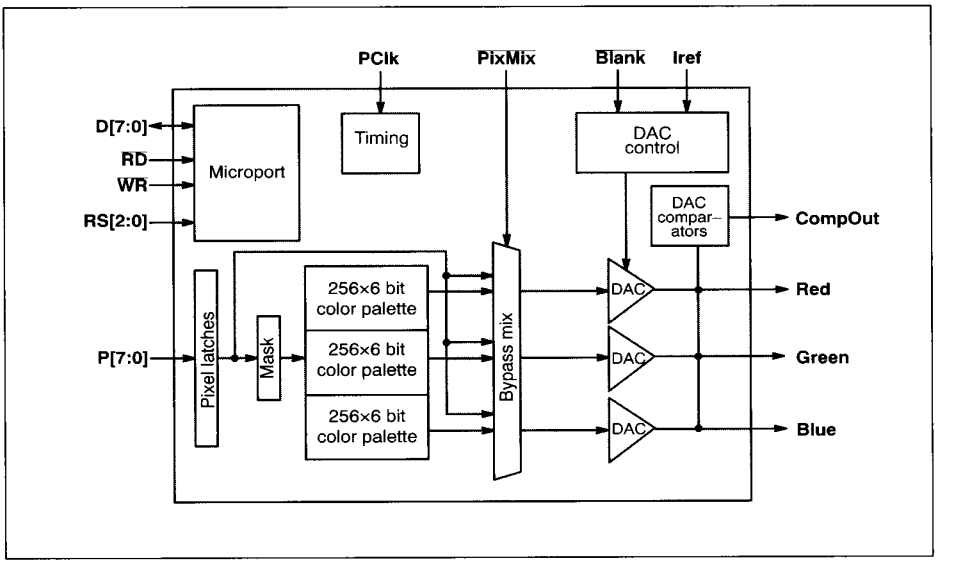
IMS G173

HIGH COLOR PALETTE-DAC WITH PixMix™

PRELIMINARY INFORMATION



FEATURES

- Compatible with VGA standard IMS G171/176
- Compatible with Sierra SC1148x family
- Pixel rates up to 80MHz
- Single or double edge latching high color modes
- 16-bit 5:5:5, 5:6:5, 6:6:4 and Select:5:5:5 formats supported
- Synchronous PixMix in software (pseudo/true color switching on pixel boundaries)
- Asynchronous PixMix switching by hardware
- DAC gain under register control
- DAC requires external current reference (**Iref**). For Advance Information on Iref/Vref version refer to page 57.

FEATURES

- Triple 6-bit DACs with output comparators
- 256×18 palette RAM with anti-sparkle
- Upgrade path to IMS G174 for enhanced functionality
- 44-pin PLCC and 28-pin DIP packages

APPLICATIONS

- Leading edge VGA with high color
- TARGA format add-in boards
- Low-cost multimedia systems
- Low-cost true color solutions

TABLE OF CONTENTS

4.1	Description	31
4.2	Pin function reference guide	32
4.3	Internal register description	35
4.4	Pixel interface operation	40
4.5	Timing reference guide	43
4.6	Electrical specifications	48
4.7	Package specifications	52
4.8	Ordering information	56

4.1 Description

The IMS G173 is a backwards compatible superset of the IMS G171/176 series of SGS-THOMSON palette-DACs. It provides a number of additional features to enable support of enhanced VGA, true color, and multimedia applications.

A standard VGA pseudo color mode is supported, offering simultaneous display of 256 colors from a choice of 256K using the 6-bit DACs.

The IMS G173 also supports16-bit high color modes with an extensive range of pixel formats to generate true color displays. This is achieved in a low pin-count device by assembling successive bytes on the pixel port into larger pixel words. Pixel formats supported include 5:5:5 TARGA format, 5:6:5 XGA format, and 6:6:4 i860 format. These modes and formats can be controlled asynchronously in software through control registers.

Also supported is a Select:5:5:5 mixed file format which allows the synchronous switching of pixel formats by software on pixel-by-pixel basis. This PixMix feature also allows mixed pseudo and true color images to be displayed on the same screen, offering the "picture-in-picture" capability required by many multimedia and windowing applications.

Additionally the high color modes can be enabled and disabled asynchronously by hardware using the **$\overline{\text{PixMix}}$** pin. (Note: The IMS G174 true color palette-DAC is a functional upgrade to the IMS G173. It allows synchronous hardware PixMix as well as a number of other functional enhancements, including support for 24-bit pixels.)

The IMS G173 is fully compatible with existing high color features available on some graphics system controllers. **It is also pin and software compatible** with the Sierra SC1148x family of high color palette-DACs, though offering significant extra functionality.

Circuitry has been added to the DACs to provide controllable gain and automatic fading, enabling smooth fading of the display under register control without changing the display memory contents. On-chip comparators provide additional information for software interaction and board level debugging.

The IMS G173 is available in two packages; 44 pin PLCC and 28 pin DIP. Due to pin limitations the following features are only available in the 44 pin PLCC:

- Access to non-VGA registers using **RS[2]**
- Hardware PixMix using the **$\overline{\text{PixMix}}$** pin
- The comparator output pin **CompOut**

4.2 Pin function reference guide

4.2.1 Pixel interface

Signal	I/O	44-pin PLCC pin(s)	28-pin DIP pin(s)	Signal name	Description
PClk	I	40	13	Pixel Clock	The rising edge of the Pixel Clock controls the sampling of values on the synchronous interface (the Pixel Data, VSync and Blank inputs). (NB: High Color Mode 1 references to both edges of the pixel clock, see Section 4.4.3.)
P[7:0]	I	39, 38, 37, 36, 35, 34, 33, 32	12,11, 10,9,8, 7,6,5	Pixel port	In pseudo color mode the values latched at this port are used as addresses to point to an entry in the Color Palette. The data at this port may, for example, be supplied by an existing VGA display controller. The data at the pixel port is also affected by the Pixel Select Function, enabled whenever the **PixMix** pin is latched Low or the Pixel Select Bit is set to a logical "1". In such a case, the value of the Pixel Command register may allow the pixel data to form a true color pixel which then bypasses the palette and is applied directly to the DACs. (The control of this data and its use is described in Section 4.4, *Pixel Interface Operation.*)
PixMix	I	20		Pixel Mixing	This pin is inverted and logical ORed with the Pixel Select Bit (bit 7 of the Pixel Command Register) to enable the high color modes. When the high color modes are inactive, **P[7:0]** is used as an address to the Color Palette. When the high color modes are enabled, data other than straight VGA data from input pins **P[7:0]** is used to generate a display pixel. The high color mode used and pixel format enabled are determined by the contents of the pixel command register. (Refer to Section 4.4, *Pixel Interface Operation* for a full explanation.)
Blank	I	7	16	Blank	A latched low value causes a color value of zero to be applied to the DACs' input regardless of the present pixel color.

4.2.2 Micro port

Signal	I/O	44-pin PLCC pin(s)	28-pin DIP pin(s)	Signal name	Description
RD	I	6	15	Read Enable	Read Enable controls the timing of the asynchronous microprocessor interface during a read operation. The Read Enable pin latches **RS[2:0]** on its falling edge and immediately accesses the selected register. The selected data is driven out from Program Data pins **D[7:0]** before a maximum specified time has elapsed. When the Read Enable pin has been taken high again the data on **D[7:0]** is held for a specified time before the pins are tri-stated.
WR	I	16	25	Write Enable	Write Enable controls the timing of the asynchronous microprocessor interface during a write operation. The Write Enable pin latches **RS[2:0]** on its falling edge and writes the data present on the Program Data Bus sampled by the rising edge of the Write Enable signal to the specified register.
RS[2:0]	I	19,18, 17	27,26	Register Select	The values on these inputs are sampled on the falling edge of Read and Write Enable and are used to specify the register to be accessed. (Refer to Section 4.3, *Internal Register Description* for a full description of the function of these registers.) Note, only **RS[1:0]** are available in PDIP package.
D[7:0]	I/O	15, 14, 13, 12, 11, 10, 9, 8	24,23, 22,21, 20,19, 18,17	Program Data	Data is transferred between the 8-bit wide bidirectional Program Data bus and the registers within the IMS G173 under control of the active enable signals.

4.2.3 Analogue interface

Signal	I/O	44-pin PLCC pin(s)	28-pin DIP pin(s)	Signal name	Description
Red, Green, Blue	O	25, 26, 27	1,2,3	Red, Green, Blue	6-bit DAC video outputs (drive into a doubly terminated 75Ω load).
Iref	I	28	4	Current Reference	The reference current drawn from **AVdd** via the **Iref** pin determines the current sourced by each DAC. See Chapter 10 for details on the design of an external current reference circuit.
Comp-Out	O	1		Comparator Output	An analogue pin which provides the result of the on-chip DAC comparators. **CompOut** is a logical zero if one or more of the DAC outputs exceeds the internal reference (typically 335mV at 5V supply voltage, independent of **Iref** current).

4.2.4 Power supply

Signal	Signal name	44-pin PLCC pin(s)	28-pin DIP pin	Description
Vdd	Digital Supply	4	28	Digital logic is supplied via **Vdd**
AVdd	Analogue Supply	22		Analogue circuitry, including DACs and reference circuitry, is supplied through the **AVdd** pin. Digital and Analogue power to the 44-pin IMS G173 is supplied on separate pins to provide maximum noise immunity. **These two pins should both be connected to the same power supply immediately outside the IMS G173.**
Gnd	Ground	3, 24	14	All ground pins must be connected.
NC		23, 29, 30, 31		These pins are not used by the current IMS G173/4. Links that are required for other manufacturer's devices will not affect the operation of the IMS G173/4.
NC or **hold to Gnd**		2, 5, 41, 42, 43, 44		If future upgrade to IMS G174 is intended, these pins should not be connected directly to the power planes. Connection via tracks or jumpers will ease modification when/if G174 features are used.
NC or **hold to Vdd**		21		

4.3 Internal register description

The IMS G173 internal registers are addressed in the same way as a standard VGA palette-DAC, such as the IMS G176, via Register select pins **RS[1:0]**.

To obtain access to the new features, it is recommended that the extra **RS[2]** signal is used. However, to maintain hardware compatibility, where the additional **RS[2]** signal is not available, high color modes can be selected in software by specific read sequences to the Pixel Mask Register (see the Pixel Command Register description). Note also that the **RS[2]** pin is not available on the 28-pin DIP package.

All bits of all registers (with the exception of the Color Value Register) can be read and written, and will return the last written data when read. All Reserved register bits must be written as "0" and will be read back as "0". The two most significant bits of the Color Value Register are ignored on write and return "00" on read.

4.3.1 Microprocessor Interface Registers

The direct access registers of the IMS G173 are divided into two main groups:

1 **Standard VGA registers.** Four registers which can be used to program the IMS G173 in exactly the same way as the industry standard IMS G171 and G176.

2 **Hardware control registers.** Three registers which are responsible for the configuration of the IMS G173. These control such features as the pixel format, the DAC gain and fade control, high color modes, etc.

The **RS** address map for the IMS G173 is shown in Table 4.1.

Hex Address	RS[2:0]	Register description	Register Type	See page
0	000	Address (write mode)	VGA	35
1	001	Color Value	VGA	36
2	010	Pixel Mask	VGA	36
3	011	Address (read mode)	VGA	35
4	100	DAC Fade	Hardware	36
5	101	DAC Gain	Hardware	37
6	110	Pixel Command	Hardware	38
7	111	Reserved	Hardware	-

Table 4.1 RS Address Map

Address Registers (#X0 and #X3)

These registers are identical to those in a standard IMS G171 or G176 device. Loading a value into the Address Register (write mode) points to a palette location which is written to when additional writes to the Color Value Register are performed. Similarly, when a value is written to the Address Register (read mode), a read from the palette is performed which makes the palette data for that specified address available to be read through the Color Value Register. Block accesses are allowed to the color palette by the Address Register incrementing to point to the next location after three consecutive writes to the Color Value Register on write cycles. On read cycles the Address Register is automatically incremented **before** every block of three reads from the Color Value Register.

Bit	R/W	Function
7:0	R/W	Palette Address

Color Value Register (#X1)

Data may be transferred to and from the color palette via successive accesses to the Color Value Register.

Only the 6 least significant bits of this register are used to update the color palette, maintaining compatibility with the VGA standard. When writing to the Color Value register, **D[7:6]** are ignored. During read cycles they return values of "0".

Bit	R/W	Function
7:6	R	Ignored on write, 00 on read.
5:0	R/W	Palette Data

Pixel Mask Register (#X2)

The Palette Mask provides a bitwise AND function of the Palette Address entered through the synchronous VGA pixel port. True color pixels compiled from multiple bytes of VGA data are not interpreted as palette addresses and therefore are not affected by the Pixel Mask Register. Accesses through the micro port are not affected by the Pixel Mask.

Multiple reads of the Pixel Mask register may be used to gain access to the Pixel Command register for use in systems which cannot exercise the **RS[2]** pin (see Pixel Command register descriptions).

Bit	R/W	Function
7:0	R/W	Palette Address Mask

DAC Fade Register (#X4)

A manual DAC gain feature has been provided on the IMS G173 which is a subset of the automatic fading provided on the IMS G174. The use of a palette-DAC in a graphics system normally provides the useful feature of being able to dim the screen by rewriting the palette without modifying the framestore. With a high color palette-DAC however, the palette is not used for displaying true color. A DAC gain feature can therefore provide the same easy-dim feature without rewriting the true color framestore.

Bit	R/W	Value	Function
7:6	R/W	00	Normal DAC operation
		01	Normal DAC operation
		10	Reserved
		11	Manual DAC gain control
5:0	R		Reserved

Table 4.2 DAC Fade Register (#X4)

DAC Gain Register (#X5)

This register specifies the relative DAC intensity when DAC Gain Control has been enabled.

Because of the non-linear nature of perceived intensity on a display screen, levels of fractional DAC intensity have been provided which give a *perceived* linear result. This will vary only slightly from one monitor to another due to common gamma values found in most monitors. Sixteen intensity levels have been provided including a zero level, approximating a square law behavior. The values of DAC Gain are guaranteed to be monotonic, although the absolute values may vary from device to device.

All display pixels are scaled by the specified factor to give a fraction of their normally specified intensity.

Bit	R/W	Value	DAC Gain Value
3:0	R/W	0000	DACs blanked
		0001	DACs 0.005 normal intensity, 1/15th perceived intensity
		0010	DACs 0.02 normal intensity, 2/15th perceived intensity
		0011	DACs 0.04 normal intensity, 3/15th perceived intensity
		0100	DACs 0.07 normal intensity, 4/15th perceived intensity
		0101	DACs 0.11 normal intensity, 5/15th perceived intensity
		0110	DACs 0.17 normal intensity, 6/15th perceived intensity
		0111	DACs 0.22 normal intensity, 7/15th perceived intensity
		1000	DACs 0.30 normal intensity, 8/15th perceived intensity
		1001	DACs 0.36 normal intensity, 9/15th perceived intensity
		1010	DACs 0.44 normal intensity, 10/15th perceived intensity
		1011	DACs 0.57 normal intensity, 11/15th perceived intensity
		1100	DACs 0.67 normal intensity, 12/15th perceived intensity
		1101	DACs 0.75 normal intensity, 13/15th perceived intensity
		1110	DACs 0.87 normal intensity, 14/15th perceived intensity
		1111	DACs at normal intensity
7:4	R/W		Reserved

Table 4.3 DAC Gain Register (#X5)

Pixel Command Register (#X6)

The Pixel Command Register configures the Pixel Interface of the IMS G173, controlling the interpretation of Pixel Data supplied to the pixel port **P[7:0]**.

The **PixMix** pin is inverted and logical ORed with the Pixel Select bit to enable the high color modes asynchronously.

When the high color modes are disabled, pixel data **P[7:0]** is used unconditionally as an address to the color palette. When the high color modes are enabled successive values applied to **P[7:0]** can be used to assemble larger pixel words which bypass the palette with the options described below. Color integrity of the palette is maintained during high color mode operations, so no re-writing of palette locations is required when switching between pseudo and true color operation.

To enable the features of the Pixel Command Register to be accessed by existing VGA hardware designs where the **RS[2]** signal is not provided, four successive reads of the Pixel Mask Register will set an internal flag which will allow the next read or write access to the Pixel Mask to be directed to the Pixel Command Register. Any other access at any time will reset this flag operation. Where possible it is recommended that the additional **RS[2]** input be exercised to access this register in the normal way.

True color formats

Once a pixel word has been assembled it may be interpreted as one of three true color RGB formats or a mixed file format. The true color format at any one time is determined by bits 3, 6 and 4 of the Pixel Command Register.

The Mixed File format enables VGA pseudo color and 15-bit true color data to be mixed in the same file and thus in the same datastream. The IMS G173 can interpret this datastream and display pseudo or true color conditionally on the status of bit [15] of the pixel word. This gives a PixMix capability where areas of different pixel formats can be displayed on the same screen simultaneously.

The specification of this register is backwards compatible with that provided on other high color devices which only specify register bits [7:5] in the command register, with all other bits reserved. In such a case, where bits [4:3] are written as zero, bit [6] (Pixel Format bit 1) becomes a selector bit between 5:6:5 and 5:5:5 true color formats.

High color modes

High color modes allow the creation of greater pixel depth by allowing multiple byte pixels to be constructed from successive bytes latched onto the pixel port pins **P[7:0]**. A full description of the two modes available on the IMS G173 and their operation is given in Section 4.4.3.

Bit	R/W	Value	Function
0	R/W		Reserved, write as "0"
1	R/W		Reserved, write as "0"
2	R/W		Reserved, write as "0"
3	R/W	0	Pixel Format bit 2 (see Table 4.5)
4	R/W		Pixel Format bit 0 (see Table 4.5)
5	R/W	0	High Color Mode 1
		1	High Color Mode 2
6	R/W		Pixel Format bit 1 (see Table 4.5)
7	R/W		Pixel Select Bit
		0	If the **PixMix** pin is a logical "1", high color modes are disabled. If the **PixMix** pin is a logical "0", they are enabled.
		1	Enable high color modes irrespective of the **PixMix** pin.

Table 4.4 Pixel Command Register (#X6)

Pixel Format bits [2:0]	Function
000	True color data is 5R 5G 5B
001	Reserved
010	True color data is 5R 6G 5B
011	True color data is 6R 6G 4B
100	Mixed File Format for software PixMix (Select, 5R 5G 5B)
101	Reserved
110	Reserved
111	Reserved

Table 4.5 Interpretation of Pixel Format bits

4.4 Pixel interface operation

Most pixel interface inputs are latched on the rising edge of the **PClk** input. Inputs are also latched on the falling edge of the **PClk** input if requested by enabling High Color Mode 1 in the Pixel Command Register.

Three 16-bit true color formats and a mixed file format are supported.

4.4.1 The Blank function

As with any industry standard IMS G176 device, a **$\overline{\text{Blank}}$** input pin is provided which can be used to blank the analogue outputs when this pin is low. A value of zero is applied to the inputs of the DACs regardless of the color value of the current pixel.

An example of such operation can be found in the timing diagram for video operation, Figure 4.5, page 47. The value of **$\overline{\text{Blank}}$** latched at the input pin is always delayed by the same number of PClks as the pixel input data **P[7:0]**. The timing requirements on the **$\overline{\text{Blank}}$** pin are also changed when in High Color Mode 1 to match the different timing constraints on pins **P[7:0]**.

4.4.2 "PixMix™" pixel mixing function

On the IMS G173 the PixMix function is achieved by enabling the high color modes and using the mixed file format. This format can be enabled by the Pixel Format bits [2:0] being set to 100 in the Pixel Command register. Using this method of software switching, picture in picture displays can be generated from existing hardware designs. With the IMS G174 true color palette-DAC this function can be achieved more flexibly in hardware since the **$\overline{\text{PixMix}}$** pin can enable high color modes synchronously on a pixel by pixel basis.

On the IMS G173 the **$\overline{\text{PixMix}}$** pin is inverted and logical ORed with the Pixel Select bit (bit [7] in the Pixel Command Register #X6) to enable the high color modes asynchronously. The choice of high color mode 1 or 2 is determined by bit [5] of the Pixel Command Register (#X6).

4.4.3 High color modes

There are two high color modes which allow multiple byte pixels to be constructed from successive bytes latched on the pixel port pins **P[7:0]**. The resulting pixel data then bypasses the palette and is applied directly to the DACs. These modes enable the user to achieve a greater color resolution (up to 65,536 colors on a single display screen for the IMS G173) while still only using an 8-bit pixel interface.

The integrity of the palette contents is always maintained in high color modes, so no rewriting of the palette is required when switching back to pseudo-color VGA operation.

High Color Mode 1

High Color Mode 1 latches data from **P[7:0]** on both the rising and falling edges of **PClk**. The rising edge latches byte[0] and the falling edge latches byte[1].

The Pixel Command Register bits 3, 4 and 6 specify the format of the resulting 16-bit true color pixel.

The pixel set-up and hold times on all pixel inputs are different when in High Color Mode 1 (see Figure 4.6). This also includes the control input **$\overline{\text{Blank}}$**. Note that High Color Mode 1 is only available at a reduced **PClk** rate. Note that this mode allows a new displayed pixel on the rising edge of every **PClk** and so preserves square pixels in both the VGA and the true color format.

High Color Mode 2

High Color Mode 2 latches data from **P[7:0]** on just the rising edges of **PClk** until the full pixel depth has accumulated. Normal pixel timings are adhered to, with the advantage that a high speed **PClk** input is allowed. This in turn means that an existing system does not have to undergo redesigned pixel timing to benefit from the greater color resolution.

Because Mode 2 inherently uses subsampling, a 16-bit display is produced at one half the full rate **PClk** input frequency. Also, since extra cycles are needed to latch pixel data, the resulting true color pixel will be displayed for two full rate **PClk** periods.

Because the input **PClk** is still operating at the full rate, the high color mode can be disabled revealing a VGA image that is still operating at the full pixel rate. This provides a VGA image and a reduced resolution 16-bit true color image on the same screen.

The above descriptions are summarized in Table 4.6.

Pixel Format bits[1] [2:0]	Pixel Command Register bit 5	High color modes enabled?	Function
XXX	X	N	**P[7:0]** used as VGA palette address
000	X	Y	True color data is [xRRRRRGG.GGGBBBBB]
001	0	Y	Reserved
001	1	Y	Reserved
010	X	Y	True color data is [RRRRRGGG.GGGBBBBB]
011	X	Y	True color data is [RRRRRRGG.GGGGBBBB]
100	X	Y	True color data, software PixMix if bit15=0 is [0xxxxxxx.–VGA–] if bit15= 1 is [1RRRRRGG.GGGBBBBB]
101	X	Y	Reserved
110	X	Y	Reserved
111	X	Y	Reserved
1. Pixel Format bits are bits 3, 6 and 4 of the Pixel Command Register			

Table 4.6 Pixel interface modes

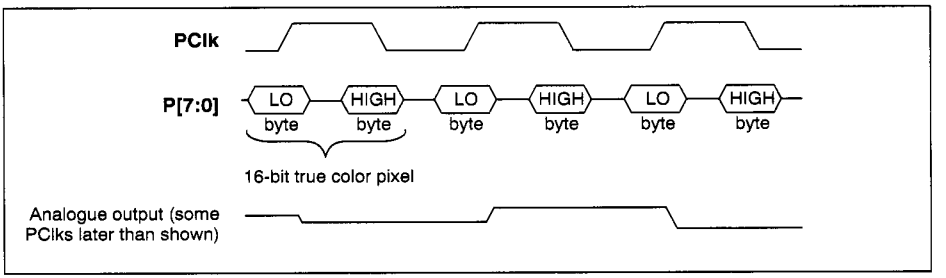


Figure 4.1 High Color Mode 1 operation

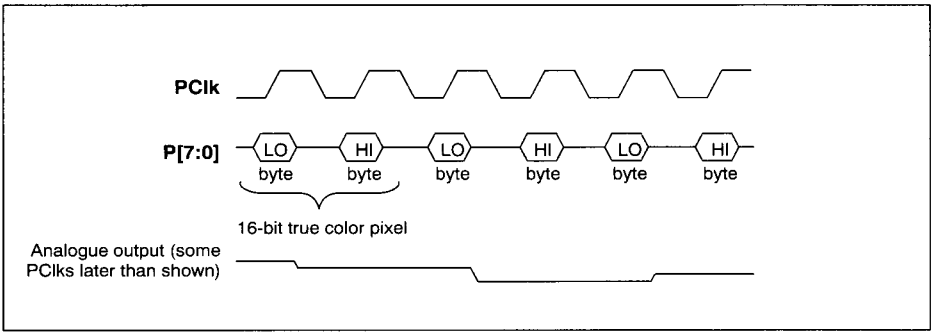


Figure 4.2 High Color Mode 2 operation

4.5 Timing reference guide

4.5.1 Micro port timing

Symbol	Parameter	Min.	Max.	Units	Notes
tWLWH	**WR** pulse width low	50		ns	
tRLRH	**RD** pulse width low	50		ns	
tWHWL	**WR** pulse width high	6×tCHCH +40ns		ns	
tRHWL	**RD** pulse width high	6×tCHCH +40ns		ns	
tSVWL	**RS** setup time	10		ns	
tSVRL	**RS** setup time	10		ns	
tWLSX	**RS** hold time	10		ns	
tRLSX	**RS** hold time	10		ns	
tDVWH	Write data setup time	10		ns	
tWHDX	Write data hold time	10		ns	
tRLQX	Output turn–on delay	5		ns	
tRLQV	Read enable access time		40	ns	
tRHQX	Output hold time	5		ns	
tRHQZ	Output turn–off delay		20	ns	1
tWHWL1	Successive write interval				
tWHRL1	Write followed by read interval				
tRHRL1	Successive read interval				
tRHWL1	Read followed by write interval	4×tCHCH +30ns		ns	2
tWHWL2	Write after color write				
tWHRL2	Read after color write				
tRHWL2	Write after color read				
tRHRL2	Read after color read	6×tCHCH +40ns		ns	2
tWHRL3	Read after read address write				
tCYC	Write/Read cycle time	6×tCHCH +40ns		ns	2,3
	Write/Read enable transition time		50	ns	

Table 4.7 Micro port timing parameters

Notes

1 Measured ±200mV from steady output voltage.

2 These parameters allow for synchronization between operations on the micro port and the pixel stream being processed by the color look–up table.

3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the micro port are internally synchronized to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the micro port being specified in terms of pixel clock periods.

The minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is 6×tCHCH +40ns.

For example, in the case of a 25MHz system the pixel clock period (tCHCH) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

6×40ns + 40ns = 280ns

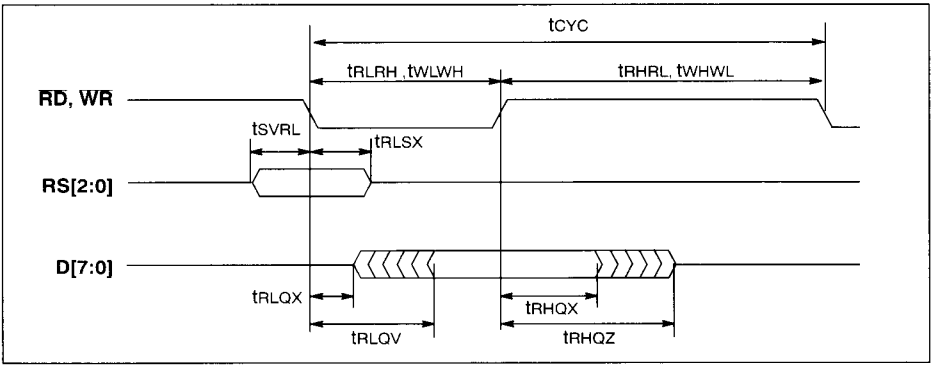


Figure 4.3 Basic read/write cycle

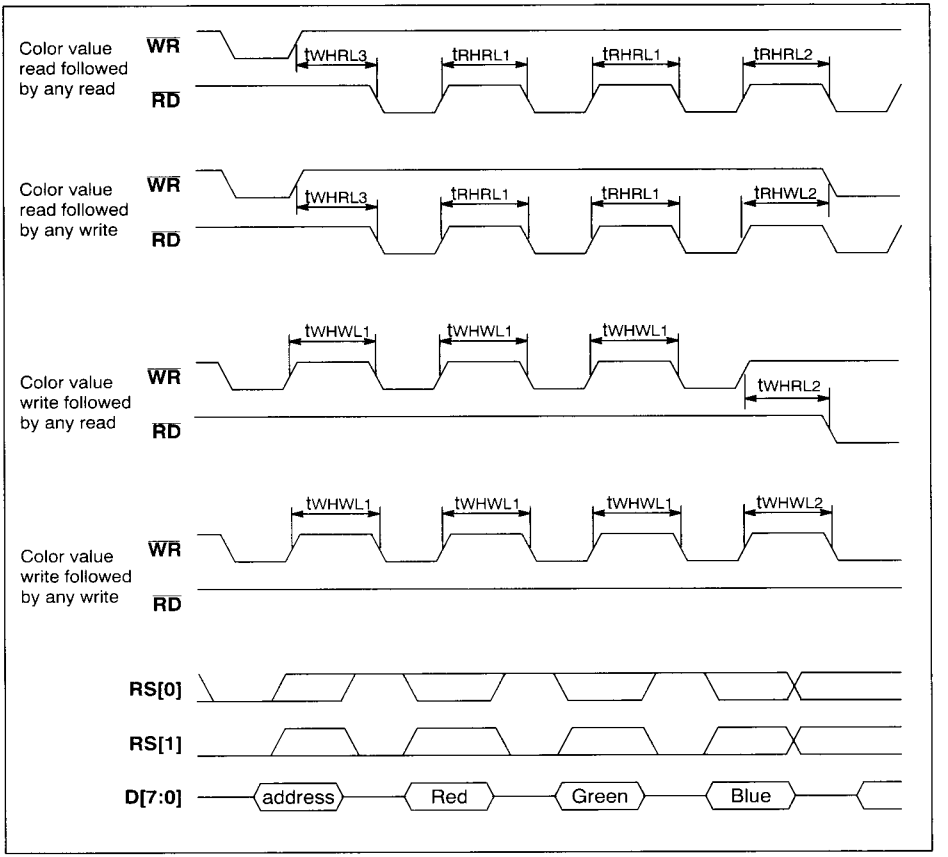


Figure 4.4 Color value read and write accesses

4.5.2 Video operation

Symbol	Parameter	66MHz Min.	80MHz Min.	All Max.	Units	Notes
tCHCH	**PClk** period	15.1	12.5	10000	ns	
ΔtCHCH	**PClk** jitter			± 2.5	%	1
tCLCH	**PClk** width low	5	5	10000	ns	
tCHCL	**PClk** width high	5	5	10000	ns	
tPVCH	Pixel interface set–up time	3	3		ns	2, 3
tCHPX	Pixel interface hold time	3	3		ns	2, 3
tCHAV	**PClk** to valid DAC output	5	5	30	ns	4
ΔtCHAV	Differential output delay			2	ns	5
	Pixel clock transition time			50	ns	
tCHCH(D)	**PClk** period	20	20	10000	ns	6
tCLCH(D)	**PClk** width low	8	8		ns	6
tCHCL(D)	**PClk** width high	8	8		ns	6
tPVCH(D)	Pixel Interface set-up time	–1	–1		ns	2, 3, 6
tCHPX(D)	Pixel Interface hold time	7	7		ns	2, 3, 6

Table 4.8 Video operation timing parameters

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.

2 These parameters apply to the **$\overline{\text{Blank}}$** and **P[7:0]** pins.

3 The Pixel Address input to the color look–up table must be set up as a valid logic level with the appropriate setup and hold times to each rising edge of **PClk** (this requirement must be met during the blanking period).

4 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

5 Between different analogue outputs on the same device.

6 (D) indicates the changed value of a parameter when the IMS G173 is in High Color Mode 1 and is using both edges of **PClk** to latch data.

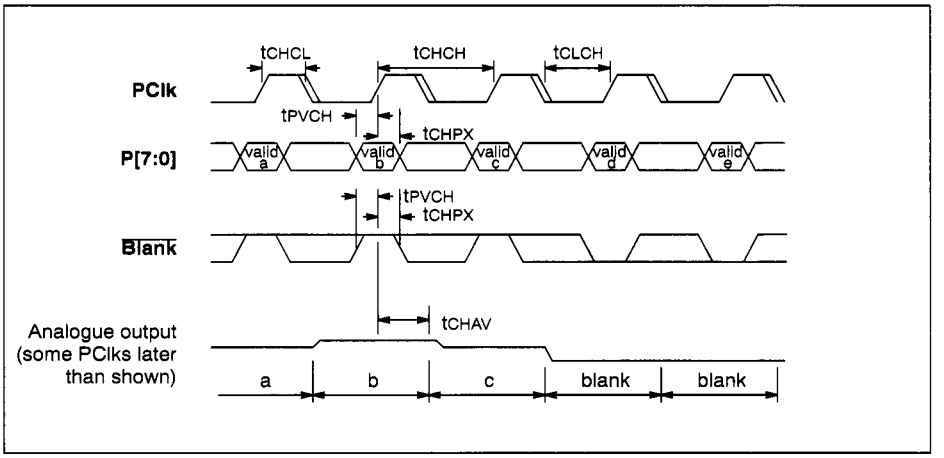


Figure 4.5 Video operation

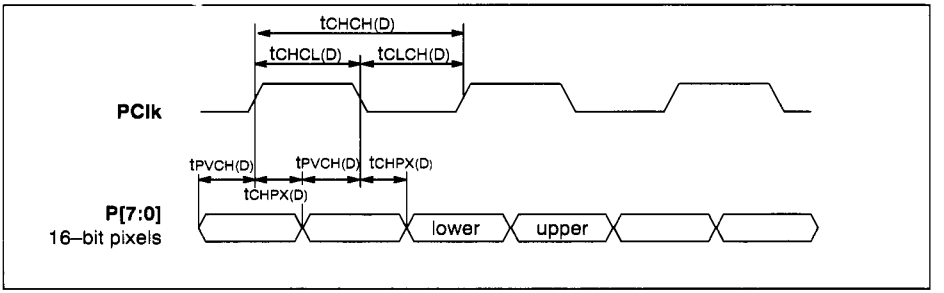


Figure 4.6 Pixel Interface (High Color Mode 1)

4.6 Electrical specifications

4.6.1 Absolute maximum ratings*

Symbol	Parameter	Min.	Max.	Units	Notes
Vdd/AVdd	DC supply voltage		7.0	V	
	Voltage on input and output pins	Gnd–1.0	Vdd+0.5	V	
TS	Storage temperature (ambient)	–55	125	°C	
TA	Temperature under bias	–40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	–15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.6.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Vdd	Positive supply voltage	4.75	5.0	5.25	V	1, 2, 3
Gnd	Ground		0		V	1
VIH	Input logic '1' voltage	2.0		Vdd+0.5	V	1, 3
VIL	Input logic '0' voltage	–0.5		0.8	V	1, 4
TC	Case temperature	0		70	°C	1
Iref	Reference current	–6.0		–10	mA	1, 5

Notes

1 All voltages are with respect to Gnd unless specified otherwise.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 These voltage ranges apply equally for AVdd and Vdd.

4 VIL(min) = –1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

5 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

4.6.3 DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes
Idd	Average power supply current		250	mA	4
Vref	Voltage at **Iref** pin	Vdd–3	Vdd	volts	5
IIN	Digital input current		±10	µA	6,7
IINR	Digital input current		±100	µA	6,8
IOZ	Off state digital output current		±50	µA	6,9
VOH	Output logic '1'	2.4		V	IO = 5mA
VOL	Output logic '0'		0.4	V	IO = –5mA

Notes (Notes 1–3 apply to all parameters)

1 All voltages are with respect to Gnd unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). Idd is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 These voltages apply equally for AVdd and Vdd.

6 Vdd = max, Gnd ≤ VIN ≤ Vdd.

7 On digital inputs (**P[7:0]**, **PCIk**, **RD**, **$\overline{\text{Blank}}$**, **$\overline{\text{WR}}$**, **$\overline{\text{PixMix}}$** and **RS[1:0]**).

8 On digital inputs (**$\overline{\text{VSync}}$**, **RS[2]**)

9 On digital input/output (**D[7:0]**).

4.6.4 DAC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
	Resolution			6	bits	
VO(max)	Output voltage			1.5	V	IO≤10mA
IO(max)	Maximum output current			–21	mA	VO≤1V
IO	Full scale output current	–16.74	–17.62	–18.50	mA	4
IO	Full scale output current	–17.72	–18.65	–19.58	mA	5
K	DAC gain constant		2.10			6
	Full scale error		±2.5	±5	%	7
	DAC to DAC correlation error		±1	±2.5	%	8
	Rise time (10% to 90%)		2	5	ns	9
	Full scale settling time		12.5		ns	9,11,12
	Integral linearity (6-bit)		±0.25	±0.5	LSB	10
	Differential linearity (6-bit)		±0.25	±0.5	LSB	10
	Monotonicity	guaranteed				
	Glitch energy		120		pVsec	9,12

Table 4.9 DAC Characteristics

Notes (Notes 1–3 apply to all parameters)

1 All voltages are with respect to Gnd unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with Iref = –8.88mA.

4 Using Iref = –8.39mA

5 Using Iref = –8.88mA

6 IO = K × Iref

7 Full scale error from the value predicted by the DAC gain constant, K.

8 About the mid point of the distribution of the three DACs measured at full scale deflection.

9 Load = 37.5Ω + 30pF with **Iref** = –8.88mA.

10 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

11 From a 2% change in the output voltage until settling to within 2% of the final value.

12 This parameter is sampled, not 100% tested.

4.6.5 AC test conditions

Parameter	
Input pulse levels	Gnd to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see Figure 4.7

Table 4.10 AC test conditions

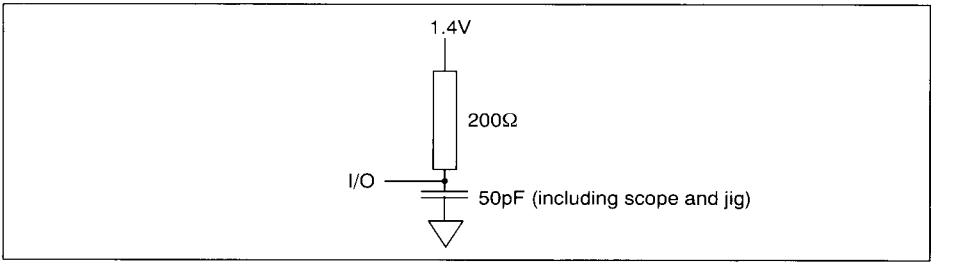


Figure 4.7 Digital output load

4.6.6 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes
CI	Digital input		7	pF	1, 2
CO	Digital output		7	pF	1, 2, 3
COA	Analogue output		10	pF	1, 2 ,4

Table 4.11 Capacitance values

Notes

1 These parameters are sampled, not 100% tested.

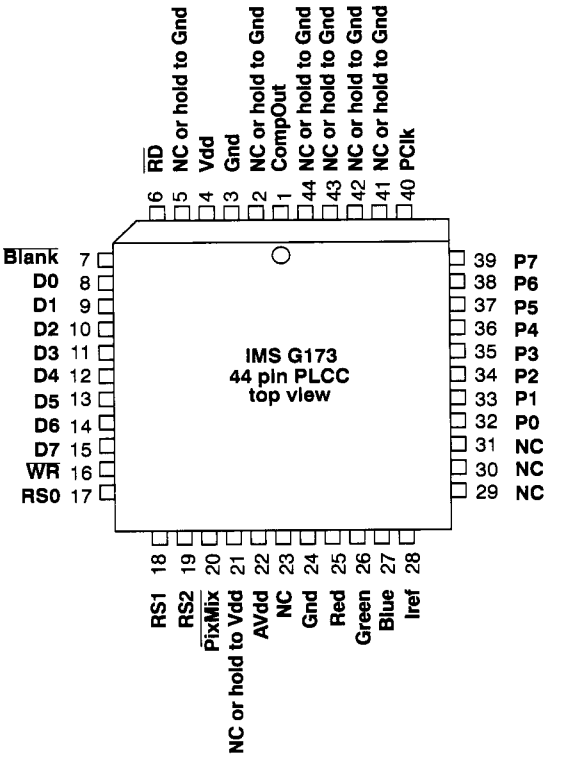
2 Measured on a Boonton meter.

3 $\overline{\textbf{RD}}$ ≥ VIH(min) to disable **D[7:0]**

4 $\overline{\textbf{Blank}}$ ≤ VIL(max) to disable **Red**, **Green** and **Blue**.

4.7 Package specifications

4.7.1 44 pin plastic leaded–chip–carrier package

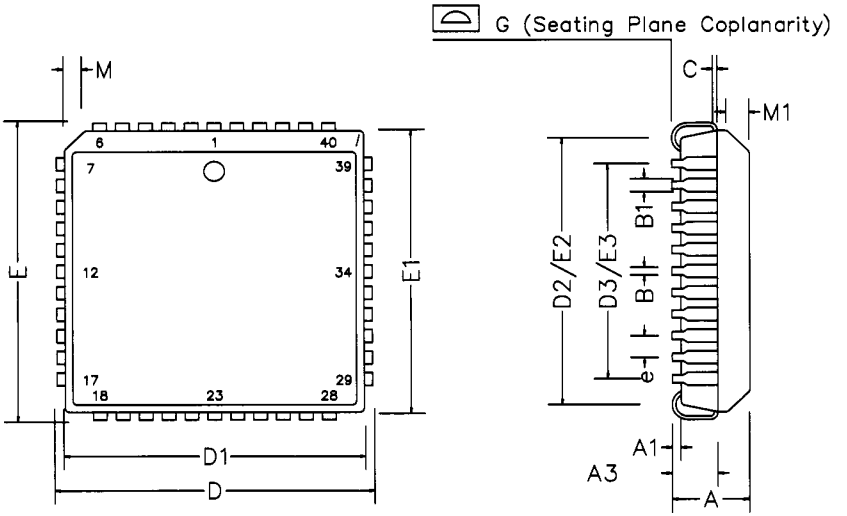


Note

All **Vdd** pins **must** be connected to the 5 Volt power supply.
All **Gnd** pins **must** be connected to ground.

Figure 4.8 IMS G173 44 pin PLCC J-bend package pinout

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.165	0.170	0.180	4.191	4.318	4.572
A1	0.020	–	–	0.508	–	–
A3	0.095	–	0.110	2.413	–	2.794
B	0.013	–	0.023	0.330	–	0.584
B1	0.025	–	0.035	0.635	–	0.889
C	0.0095	0.010	0.0105	0.241	0.254	0.267
D	0.685	0.690	0.695	17.399	17.526	17.653
D1	0.650	0.655	0.660	16.510	16.637	16.764
D2	0.590	0.610	0.630	14.986	15.494	16.002
D3	–	0.500REF	–	–	12.700REF	–
E	0.685	0.690	0.695	17.399	17.526	17.653
E1	0.650	0.655	0.660	16.510	16.637	16.764
E2	0.590	0.610	0.630	14.986	15.494	16.002
E3	–	0.500REF	–	–	12.700REF	–
e	–	0.050BSC	–	–	1.270BSC	–
G	–	–	0.004	–	–	0.102
L	–	N/A	–	–	N/A	–
L1	–	N/A	–	–	N/A	–
M	0.042	–	0.048	1.067	–	1.219
M1	0.042	–	0.056	1.067	–	1.422



Notes;

1. Maximum lead displacement from notional centre line = ±0.007".

Figure 4.9 44 pin PLCC J-bend package dimensions

4.7.2 28 pin plastic dual-in-line (DIL) package

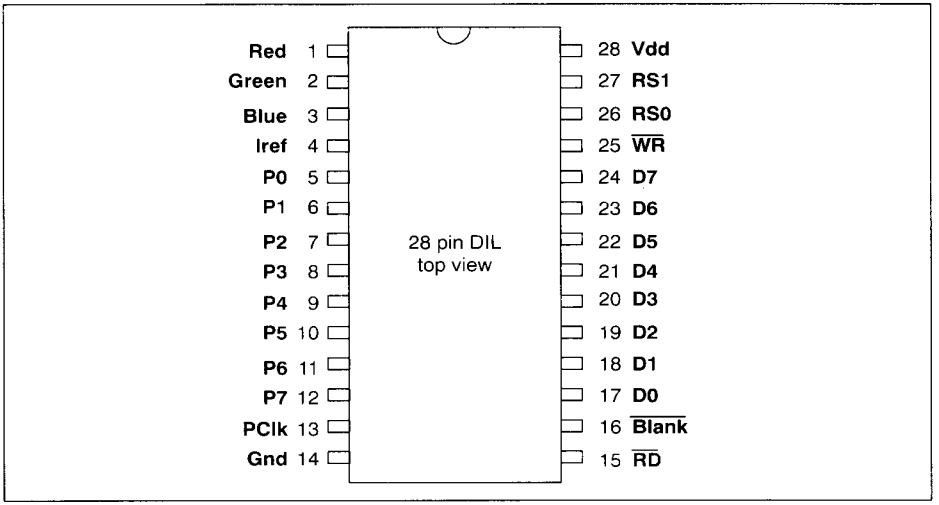


Figure 4.10 IMS G173 28 pin plastic dual-in-line package pinout

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	0.195	–	–	4.953
A1	0.015	–	–	0.381	–	–
A2	0.120	–	0.180	3.048	–	4.572
B	0.014	0.018	0.022	0.356	0.457	0.559
B1	0.045	0.055	0.065	1.143	1.397	1.651
C	0.008	0.010	0.012	0.203	0.254	0.305
D	1.366	1.450	1.470	34.696	36.830	37.338
E	0.583	–	0.625	14.808	–	15.875
E1	0.492	0.550	0.560	12.496	13.970	14.224
e	–	0.100BSC	–	–	2.540BSC	–
eA	–	0.600TYP	–	–	15.240TYP	–
e3	–	1.300BSC	–	–	33.020BSC	–
L	0.125	0.130	0.135	3.175	3.302	3.429
M	0 DEG	–	15 DEG	0 RAD	–	0.26 RAD
S	0.033	0.075	0.080	0.838	1.905	2.032

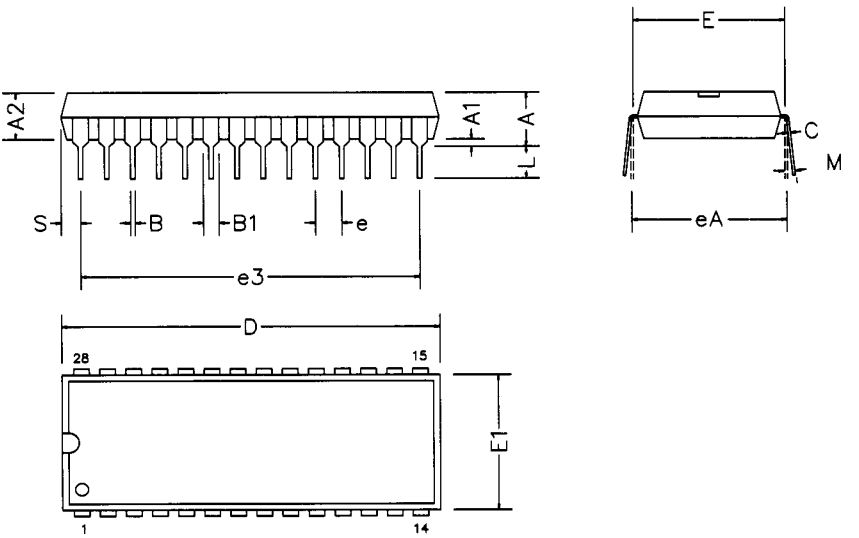


Figure 4.11 28 pin plastic dual-in-line package dimensions

4.8 Ordering information

Device	Clock rate	Package	Part number
IMS G173	66MHz	44 pin plastic LCC	IMS G173JI66Z
IMS G173	80MHz	44 pin plastic LCC	IMS G173JI80Z
IMS G173	66MHz	28 pin plastic DIP	IMS G173PI66S
IMS G173	80MHz	28 pin plastic DIP	IMS G173PI80S