CS4236B

CrystalClear™ Single Chip Audio System

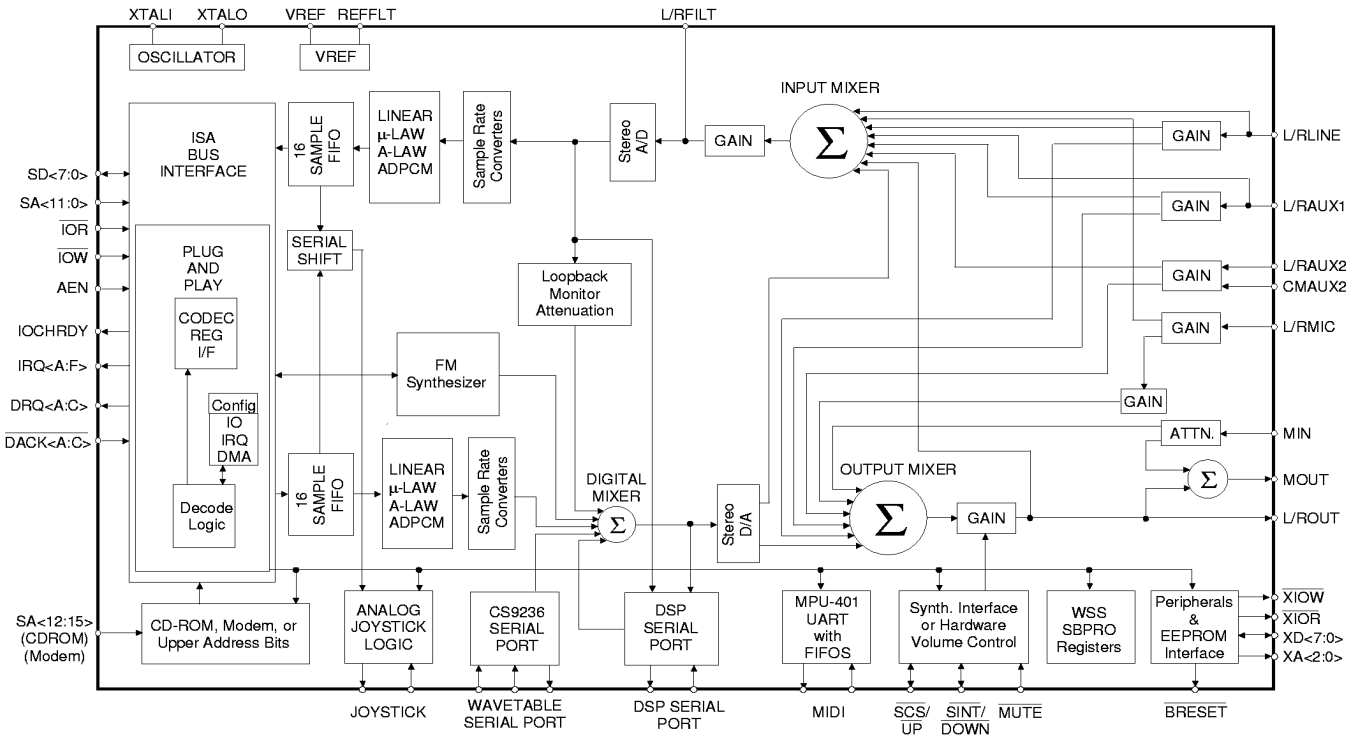
- Compatible with Sound Blaster™, Sound Blaster Pro™, and Windows Sound System™
- Advanced MPC3-Compliant Input and Output Mixer
- Enhanced Stereo Full Duplex Operation
- Dual Type-F DMA Support
- Industry Leading Delta-Sigma Data Converters
- Fully Plug-and-Play ISA Compatible
- 3.3 V or 5 V ISA Bus Operation
- Programmable Power Management
- Hardware Master Volume Control
- Joystick Port and MPU-401 Compatible MIDI Interface
- Optional Enhanced IDE CD-ROM Interface
- CS9236 Wavetable Digital Audio Interface
- 16-Bit Address Decode Support
- CS4236/CS4232/CS4231 Register Compatible

General Description

The CS4236B is a single chip multimedia audio system that is a pin-compatible upgrade to the CS4236. The CS4236B adds an input mixer and a wavetable-synthesis interface to the industry standard CS4236. The CS4236B is compatible with the Microsoft Windows Sound System standard and will run software written to the Sound Blaster and Sound Blaster Pro interfaces. The CS4236B is fully compliant with Microsoft's PC '97 and WHQL audio requirements. In addition, the CS4236B includes hardware master volume control pins as well as extensive power management control over each internal logical section.

ORDERING INFORMATION:

CS4236B-JQ	100 pin TQFP, 14x14x1.4mm
CS4236B-KQ	100 pin TQFP, 14x14x1.4mm



Advanced Product Information | This document contains information for a new product. Cirrus Logic, Inc. reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS

T_A = 25 °C; VA, VD1, VDF1-VDF4 = +5V
Input Levels: Logic 0 = 0V, Logic 1 = VD1; 1 kHz Input Sine wave; Sample Frequency, Fs = 44.1 kHz;
Measurement Bandwidth is 20 Hz to 20 kHz - unweighted, 16-bit linear coding.)

Parameter*	Symbol	CS4236B-JQ Min	CS4236B-JQ Typ	CS4236B-JQ Max	CS4236B-KQ Min	CS4236B-KQ Typ	CS4236B-KQ Max	Units
Analog Input Characteristics - Minimum Gain Setting (0dB); unless otherwise specified.								
ADC Resolution (Note 1)		16	-	-	16	-	-	Bits
ADC Differential Nonlinearity (Note 1)		-	-	±0.5	-	-	±0.5	LSB
Instantaneous Dynamic Range Line Inputs	IDR	-	80	-	80	85	-	dB
(Note 2) Mic Inputs		-	75	-	72	79	-	dB
Total Harmonic Distortion Line Inputs	THD	-	0.05	-	-	0.006	0.02	%
Mic Inputs		-	0.05	-	-	0.01	0.025	%
Interchannel Isolation Line to Line Inputs		-	80	-	-	80	-	dB
Line to Mic Inputs		-	80	-	-	80	-	dB
Line-to-AUX1		-	90	-	-	90	-	dB
Line-to-AUX2		-	90	-	-	90	-	dB
Interchannel Gain Mismatch Line Inputs		-	-	±0.5	-	-	±0.5	dB
Mic Inputs		-	-	±0.5	-	-	±0.5	dB
Programmable Input Gain Span Line Inputs		21.5	22.5	-	21.5	22.5	-	dB
Gain Step Size		1.3	1.5	1.7	1.3	1.5	1.7	dB
ADC Offset Error 0 dB Gain		-	-	-	-	±10	±100	LSB
Full Scale Input Voltage: (MGE=1) MIC Inputs		0.26	0.28	-	0.26	0.28	-	V_{pp}
(MGE=0) MIC Inputs		2.6	2.8	-	2.6	2.8	-	V_{pp}
LINE, AUX1, AUX2, MIN Inputs		2.6	2.8	-	2.6	2.8	-	V_{pp}
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Input Resistance (Note 1) Mic Inputs		8	11	-	8	11	-	kΩ
Other Inputs		20	23	-	20	23	-	kΩ
Input Capacitance (Note 1)		-	-	15	-	-	15	pF

Notes: 1. This specification is guaranteed by characterization, no production testing.
2. MGE = 1 (see WSS Indirect Reg I0, I1).

*Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*	Symbol	CS4236B-JQ Min	CS4236B-JQ Typ	CS4236B-JQ Max	CS4236B-KQ Min	CS4236B-KQ Typ	CS4236B-KQ Max	Units
Analog Output Characteristics - Minimum Attenuation (0dB); unless otherwise specified.								
DAC Resolution (Note 1)		16	-	-	16	-	-	Bits
DAC Differential Nonlinearity (Note 1)		-	-	±0.5	-	-	±0.5	LSB
Dynamic Range -Total All Outputs -Instantaneous	TDR IDR	- -	- 85	- -	- 80	95 85	- -	dB
Total Harmonic Distortion (Note 3)	THD	-	0.01	-	-	0.01	0.02	%
Interchannel Isolation Line Out (Note 3)		-	95	-	-	95	-	dB
Interchannel Gain Mismatch Line Out		-	±0.1	±0.5	-	±0.1	±0.5	dB
Voltage Reference Output - VREF		2.0	2.2	2.5	2.0	2.2	2.5	V
Voltage Reference Output Current - VREF (Notes 1,4)		-	100	400	-	100	400	µA
DAC Programmable Attenuation Span		100	106.5	-	100	106.5	-	dB
DAC Attenuation Step Size +12 dB to -81 dB -82.5 dB to -94.5 dB		1.3 1.0	1.5 1.5	1.7 2	1.3 1.0	1.5 1.5	1.7 2	dB dB
DAC Offset Voltage		-	-	-	-	±1	±10	mV
Full Scale Output Voltage: OUT, MOUT (Note 3)		2.6	2.8	3.2	2.6	2.8	3.2	Vpp
Gain Drift		-	100	-	-	100	-	ppm/°C
Deviation from Linear Phase (Passband) (Note 1)		-	-	1	-	-	1	Degree
External Load Impedance (Note 1)		10	-	-	10	-	-	kΩ
Mute Attenuation		80	-	-	80	-	-	dB
Total Out-of-Band Energy 0.6xFs to 100 kHz (Note 1)		-	-	-	-	-	-45	dB
Audible Out-of-Band Energy 0.6xFs to 22 kHz (Fs=8kHz) (Note 1)		-	-	-	-	-	-70	dB
Power Supply								
Power Supply Current Digital, Operating Analog, Operating Total Operating Total Power Down		- - - -	80 25 105 100	- - - -	- - - -	80 25 105 100	91 31 122 400	mA mA mA µA
Power Supply Rejection 1 kHz (Note 1)		40	-	-	40	-	-	dB

Notes: 3. 10 kΩ, 100 pF load.
4. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.

MIXERS (T_A = 25 °C; VA, VD1, VDF1-VDF4 = +5V; Input Levels: Logic 0 = 0V, Logic 1 = VD1; 1 kHz Input Sine wave, Measurement Bandwidth is 20 Hz to 20 kHz - unweighted.)

Parameter*		CS4236B-JQ Min	CS4236B-JQ Typ	CS4236B-JQ Max	CS4236B-KQ Min	CS4236B-KQ Typ	CS4236B-KQ Max	Units
Mixer Gain Range Span	LINE, AUX1, AUX2	-	-	-	45	46.5	-	dB
	MIC, MIN	-	-	-	42	45	-	dB
	Hardware Master	-	-	-	44	48	-	dB
(Digital)	Wavetable, Monitor, PC Wave, DSP, FM	-	-	-	90	94.4	-	dB
Step Size	MIC, LINE, AUX1, AUX2	-	-	-	1.3	1.5	1.7	dB
	MIN	-	-	-	2.3	3.0	3.7	dB
	Hardware Master	-	-	-	1.6	2.0	2.4	dB
(Digital)	Wavetable, Monitor, PC Wave, DSP, FM	-	-	-	0.9	1.5	2.0	dB
Dynamic Range	-Total	-	-	-	-	94.5	-	dB
(Analog Mixers)	-Instantaneous	-	88	-	-	91	-	dB
Total Harmonic Distortion (Analog Mixers)	(Note 3)	-	0.005	-	-	0.002	-	dB

ABSOLUTE MAXIMUM RATINGS (AGND, DGND, SGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital	VD1	-0.3	6.0	V
		VDF1-VDF4	-0.3	6.0	V
	Analog	VA	-0.3	6.0	V
Total Power Dissipation	(Supplies, Inputs, Outputs)		-	1	W
Input Current per Pin	(Except Supply Pins)		-10.0	+10.0	mA
Output Current per Pin	(Except Supply Pins)		-50	+50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input Voltage:	SA<11:0>, IOR, IOW, AEN SD<7:0>, DACK<A:C>		-0.3	VD1+0.3	V
	All other digital inputs		-0.3	VDF+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND, SGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD1	4.75	5.0	5.25	V
	(Note 5)		3.0	3.3	3.6	V
	Digital Filtered	VDF1-VDF4	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
Operating Ambient Temperature		T_A	0	25	70	°C

Note 5. When VD1 is powered from 3.3 Volts, all ISA bus input pins, except DRQA, must also be 3.3 Volts. DRQA is internally powered from the VDF supply and must have a 5 Volt interface. To use DRQA in a 3.3 Volt application, a level translator is needed.

DIGITAL FILTER CHARACTERISTICS (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
Passband			0	-	0.40xFs	Hz
Frequency Response			-1.0	-	+0.5	dB
Passband Ripple	(0-0.40xFs)		-	-	±0.1	dB
Transition Band			0.40xFs	-	0.60xFs	Hz
Stop Band			0.60xFs	-	-	Hz
Stop Band Rejection			74	-	-	dB
Group Delay	8- and 16-bit formats		-	-	10/Fs	s
	Stereo ADPCM format		-	-	14/Fs	s
	Mono ADPCM format		-	-	18/Fs	s
Group Delay Variation vs. Frequency	ADCs		-	-	0.0	µs
	DACs		-	-	0.1/Fs	µs

DIGITAL CHARACTERISTICS (T_A = 25°C; VA, VDF1-VDF4 = 5V, VD1 = 5V/3V; AGND, DGND1, SGND1-SGND4 = 0V.)

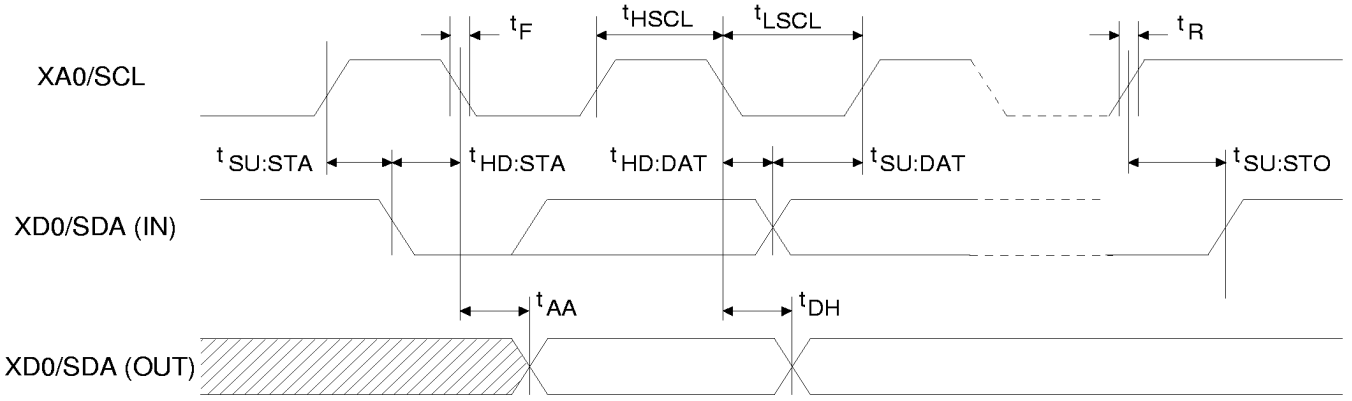
Parameter			Symbol	Min	Max	Units
High-level Input Voltage	Digital Inputs		V_{IH}	2.0	-	V
	XTALI			VD-1.0	-	V
Low-level Input Voltage			V_{IL}	-	0.8	V
High-level Output Voltage:			V_{OH}			
ISA Bus Pins (except DRQA)		I_0 = -24.0 mA		2.4	VD1	V
DRQA		I_0 = -24.0 mA		2.4	VDF	V
IOCHRDY, SDA/XD0 (Note 6)				2.4	VDF	V
All Others		I_0 = -1.0 mA		2.4	VDF	V
Low-level Output Voltage:	ISA Bus Pins	I_0 = 24.0 mA	V_{OL}	-	0.55	V
		I_0 = 18.0 mA		-	0.4	V
	IOCHRDY	I_0 = 8.0 mA		-	0.4	V
	All Others	I_0 = 4.0 mA		-	0.4	V
Input Leakage Current	(Digital Inputs)			-10	10	µA
Output Leakage Current	(High-Z Digital Outputs)			-10	10	µA

Note 6. Open Collector pins. High level output voltage dependent on external pull up (required) used and number of peripherals (gates) attached.

TIMING PARAMETERS (T_A = 25 °C; VA, VD1, VDF1-VDF4 = +5V; outputs loaded with 30pF Input Levels: Logic 0 = 0V, Logic 1 = VD1)

Parameter	Symbol	Min	Max	Units
E^2PROM Timing (Note 1)				
SCL Low to SDA Data Out Valid	t_{AA}	0	3.5	µs
Start Condition Hold Time	$t_{HD:STA}$	4.0	-	µs
Clock Low Period	t_{LSCL}	4.7	-	µs
Clock High Period	t_{HSCL}	4.0	-	µs
Start Condition Setup Time (for a Repeated Start Condition)	$t_{SU:STA}$	4.7	-	µs
Data In Hold Time	$t_{HD:DAT}$	0	-	µs
Data In Setup Time	$t_{SU:DAT}$	250	-	ns
SDA and SCL Rise Time (Note 7)	t_R	-	1	µs
SDA and SCL Fall Time	t_F	-	300	ns
Stop Condition Setup Time	$t_{SU:STO}$	4.7	-	µs
Data Out Hold Time	t_{DH}	0	-	ns

Notes 7. Rise time on SDA is determined by the capacitance of the SDA line with all connected gates and the external pullup resistor required.

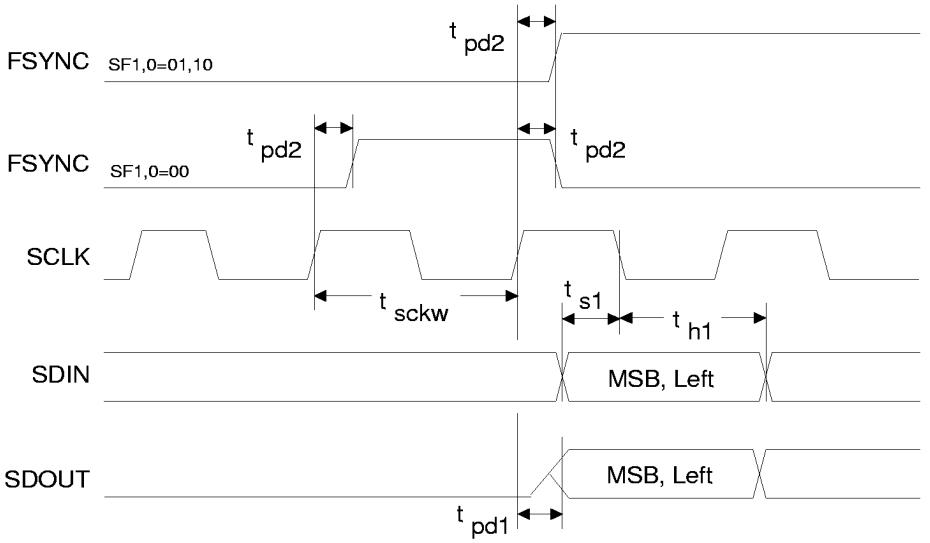


E^2PROM 2-Wire Interface Timing

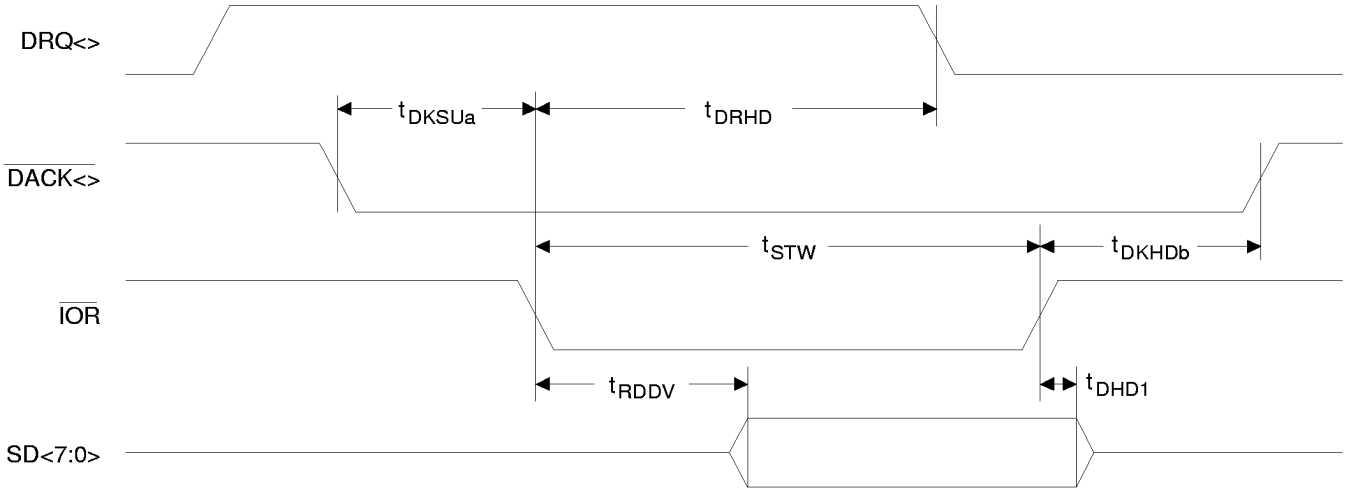
TIMING PARAMETERS (Continued)

Parameter	Symbol	Min	Max	Units
Parallel Bus Timing				
IOW or IOR strobe width	t_{STW}	90	-	ns
Data valid to IOW rising edge (write cycle)	t_{WDSU}	22	-	ns
IOR falling edge to data valid (read cycle)	t_{RDDV}	-	60	ns
SA <> and AEN setup to IOR or IOW falling edge	t_{ADSU}	22	-	ns
SA <> and AEN hold from IOW or IOR rising edge	t_{ADHD}	10	-	ns
DACK<> inactive to IOW or IOR falling edge (DMA cycle immediately followed by a non-DMA cycle) (Note 8)	t_{SUDK1}	60	-	ns
DACK<> active from IOW or IOR rising edge (non-DMA cycle completion followed by DMA cycle) (Note 8)	t_{SUDK2}	0	-	ns
DACK<> setup to IOR falling edge (DMA cycles) DACK<> setup to IOW falling edge (Note 8)	t_{DKSUa} t_{DKSUb}	25 25	- -	ns ns
Data hold from IOW rising edge	t_{DHD2}	15	-	ns
DRQ<> hold from IOW or IOR falling edge DTM(I10) = 0 (assumes no more DMA cycles needed) DTM(I10) = 1	t_{DRHD}	- -25	45 -	ns
Time between rising edge of IOW or IOR to next falling edge of IOW or IOR	t_{BWDN}	80	-	ns
Data hold from IOR rising edge	t_{DHD1}	0	25	ns
DACK<> hold from IOW rising edge DACK<> hold from IOR rising edge	t_{DKHDa} t_{DKHDb}	25 25	- -	ns ns
RESDRV pulse width high (Note 1)	t_{RESDRV}	1	-	ms
Initialization Time (Note 1, 9)	t_{INIT}	130	1200	ms
EEPROM Read Time (Note 1, 10)	t_{EEPROM}	1	420	ms
XTAL, 16.9344 MHz, frequency (Notes 1, 11)		16.92	16.95	MHz
XTALI high time (Notes 1, 11)		24	-	ns
XTALI low time (Notes 1, 11)		24	-	ns
Sample Frequency (Note 1)	Fs	3.918	50	kHz
Serial Port Timing				
SCLK rising to SDOUT valid (Note 1)	t_{PD1}	-	60	ns
SCLK rising to FSYNC transition (Note 1)	t_{PD2}	-20	20	ns
SDIN valid to SCLK falling (Note 1)	t_{S1}	30	-	ns
SDIN hold after SCLK falling (Note 1)	t_{H1}	30	-	ns

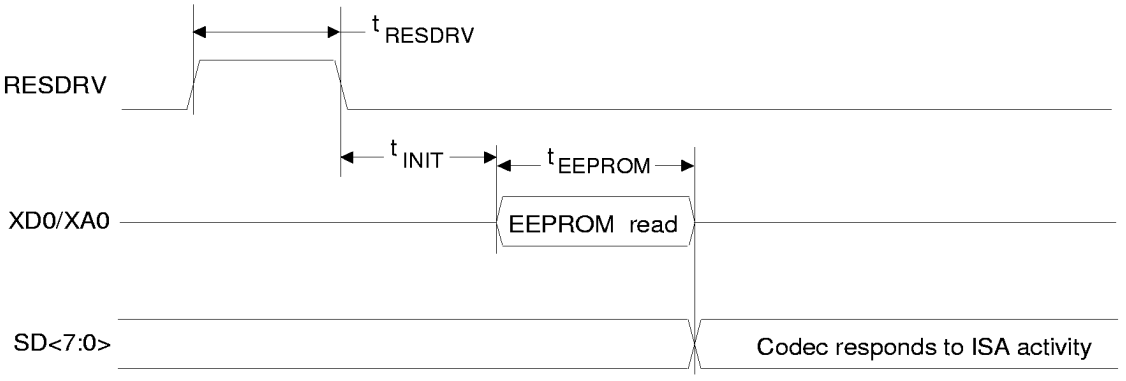
Notes: 8. AEN must be high during DMA cycles.
9. Initialization time depends on the power supply circuitry, as well as the the type of clock used.
10. EEPROM read time is dependent on amount of data in EEPROM. Minimum time relates to no EEPROM present. Maximum time relates to EEPROM data size of 2k bytes.
11. The Sample frequency specification must not be exceeded.



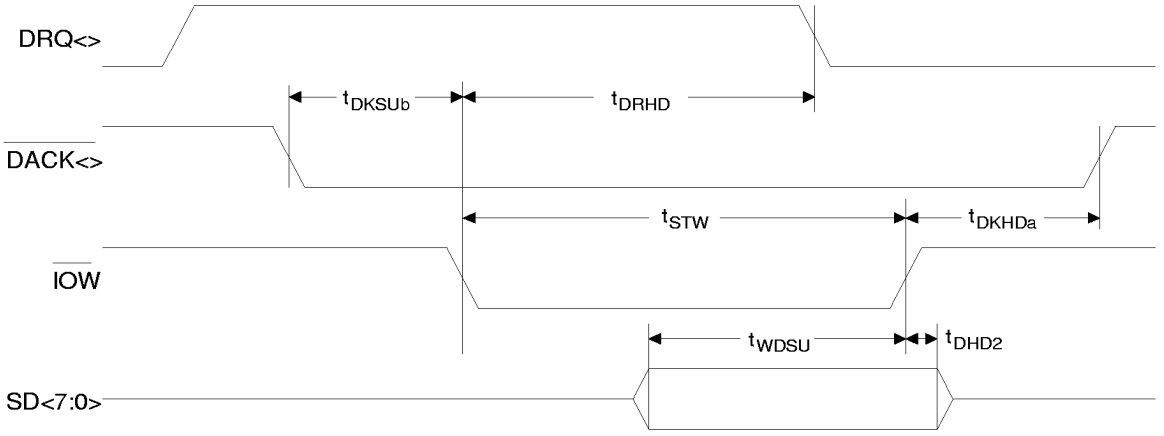
DSP Serial Port Timing



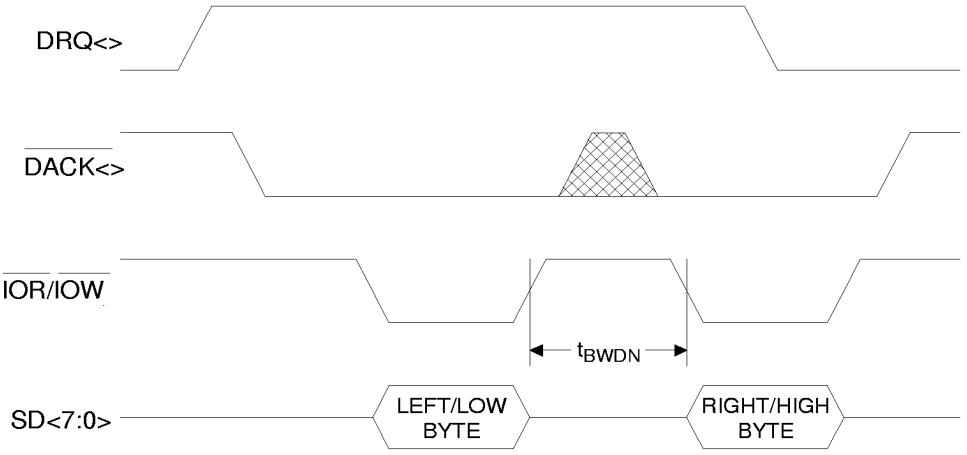
8-Bit Mono DMA Read/Capture Cycle



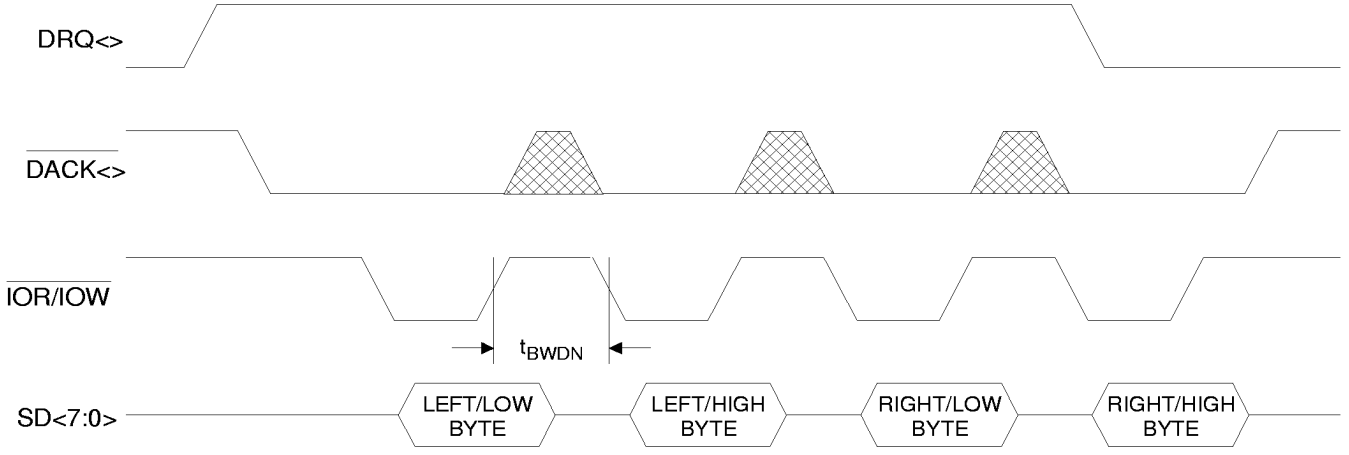
Reset Timing



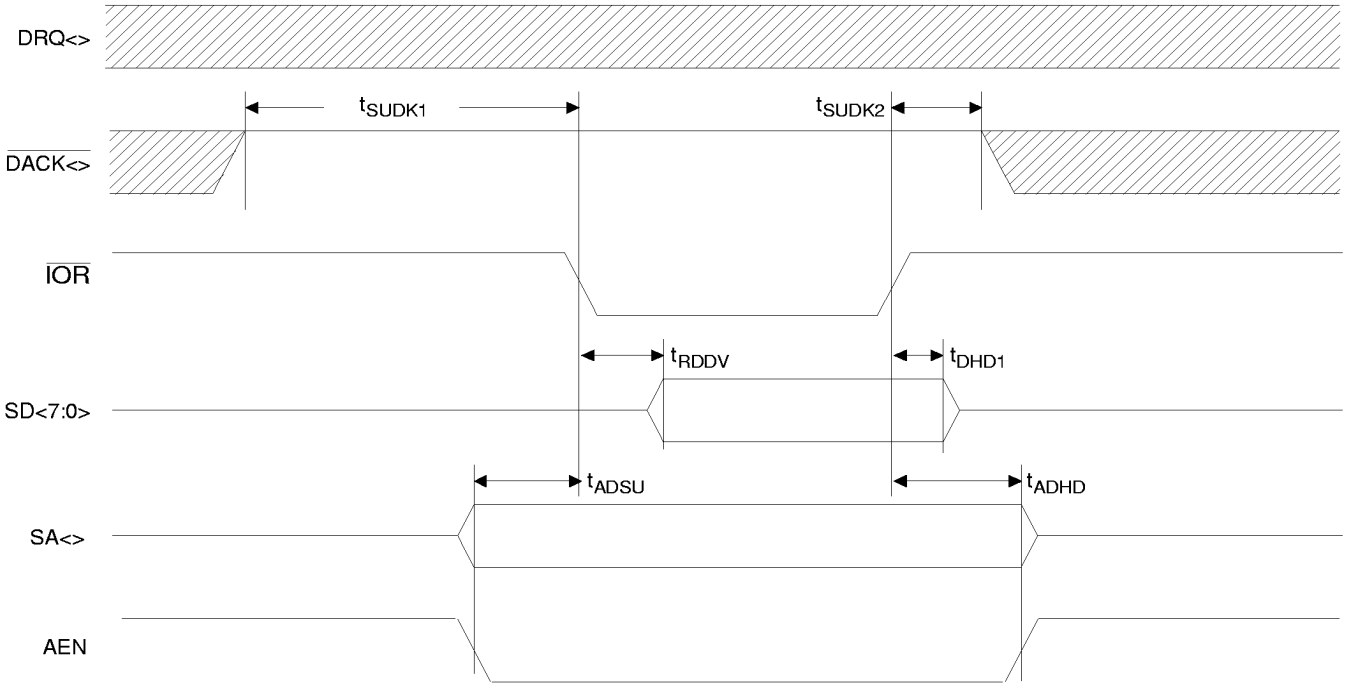
8-Bit Mono DMA Write/Playback Cycle



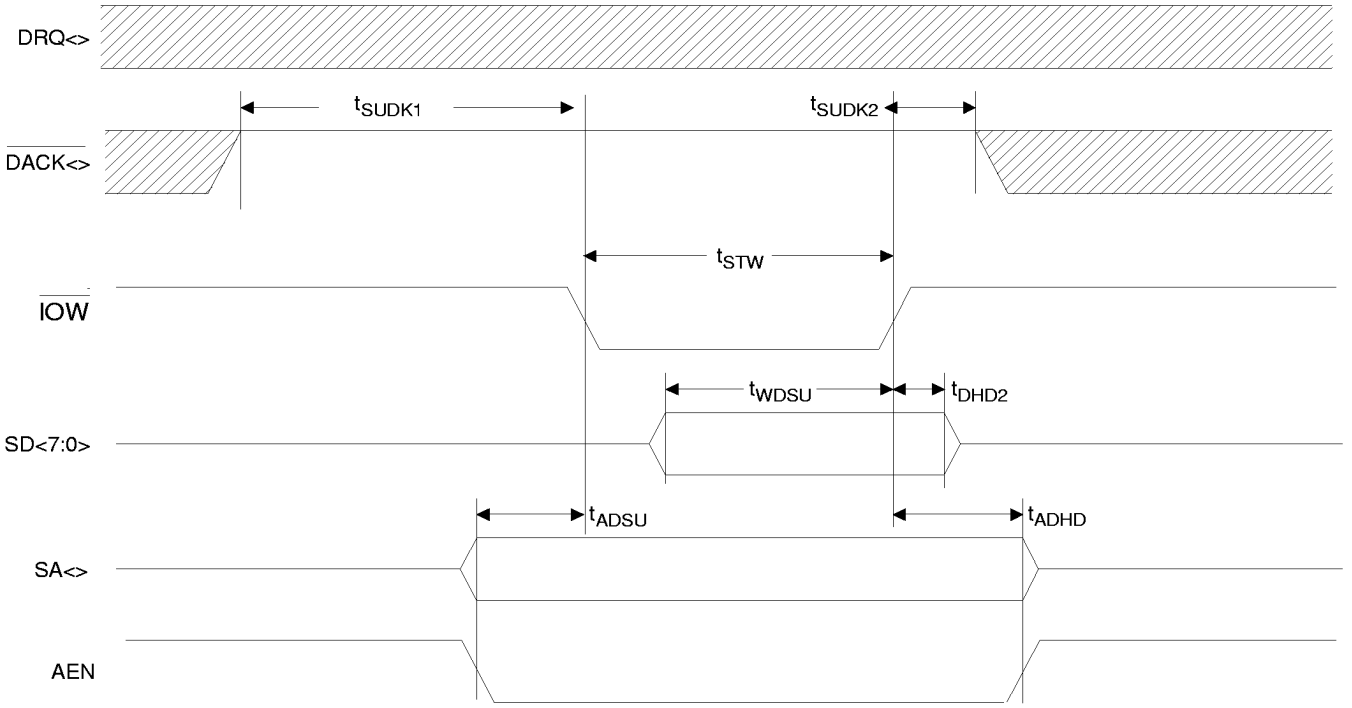
8-Bit Stereo or 16-Bit Mono DMA Cycle



16-Bit Stereo or ADPCM DMA Cycle



I/O Read Cycle



I/O Write Cycle

GENERAL DESCRIPTION

This device is comprised of six physical devices along with Plug-and-Play support for two additional external devices. The internal devices are:

Windows Sound System Codec
Sound Blaster Pro Compatible Interface
Game Port (Joystick)
Control
MPU-401
FM Synthesizer

The two external devices are:

IDE CDROM
Modem

A full ISA interface with Plug and Play compatibility and an External Peripheral Port for interfacing to external devices (i.e. Wave-Table Synthesizer, CDROM, and Modem) is included. Since the Wave-Table Synthesizer and CDROM analog inputs are external, mapping as shown in Figure 5, on page 58, must be used to maintain Sound Blaster compatibility, i.e. CDROM analog must be connected to the AUX2 analog inputs of the mixer.

On power up, this part requires a RESDRV signal to initialize the internal configuration. When initially powered up, the part is isolated from the bus, and each device supported by the part must be activated via software. Once activated, each device responds to the resources given (Address, IRQ, and DMA channels). The eight devices listed above are grouped into six logical devices, as shown in Figure 1 (bracketed features are supported, but typically not used). The six logical devices are:

LOGICAL DEVICE 0:
Windows Sound System Codec (WSS Codec)
Adlib/Sound Blaster-compatible Synthesizer
Sound Blaster Pro Compatible Interface

LOGICAL DEVICE 1: Game Port

LOGICAL DEVICE 2: Control

LOGICAL DEVICE 3: MPU401

LOGICAL DEVICE 4: CDROM

LOGICAL DEVICE 5: Modem

Logical Device 0 consists of three physical devices. The WSS Codec and the Synthesizer are grouped together since the original Windows Sound System board expected an FM synthesizer if the codec was present. The Sound Blaster Pro Compatible interface, SBPro, is also grouped to allow the WSS Codec and the SBPro to share Interrupts and DMA channels. The Synthesizer device could be the internal FM synthesizer, or a synthesizer externally located on the Peripheral Port. The external synthesizer interface supports both FM and wavetable synthesizers such as the CS9233. The WSS Codec, FM synthesizer, and the SBPro compatible devices are internal to the part.

Logical Device 1 is the Game Port that supports up to two joystick devices.

Logical Device 2 is the Control device that supports global features of the part. This device uses I/O locations to control power management, joystick rate, and PnP resource data loading.

Logical Device 3 is the MPU-401 interface. The MPU-401 MIDI interface includes a 16-byte FIFO for data transmitted out the MIDOUT pin and a 16-byte FIFO for data received from the MIDIN pin.

Logical Device 4 supports an IDE CDROM connected to the peripheral port. This interface, on the external peripheral port, can support CDROMs with up to 8 I/O locations and supports both the base address and the alternate base address, an interrupt, and a DMA channel. Although this logical device is listed as a CDROM, any external device that fits within the resources listed above may be substituted.

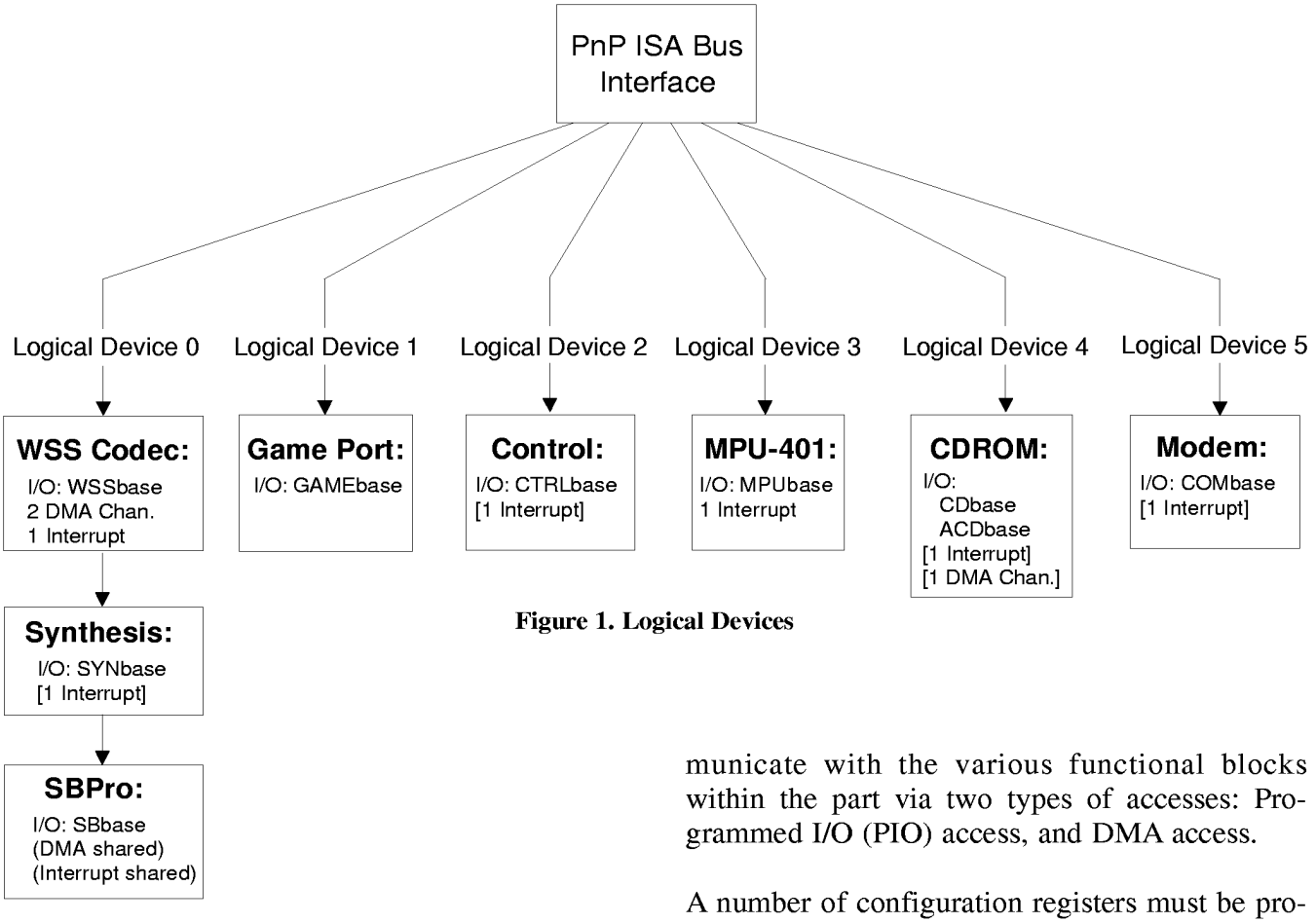


Figure 1. Logical Devices

Logical Device 5 supports a modem connected to the peripheral port. This interface, on the external peripheral port, supports modems with 2 to 256 I/O locations (only SA2-SA0 are buffered through the part) and supports a base address and an interrupt. Although this logical device is listed as a modem, any external device that fits within the resources listed above may be substituted.

ISA Bus Interface

The 8-bit parallel I/O and 8-bit parallel DMA ports provide an interface which is compatible with the Industry Standard Architecture (ISA) bus. The ISA Interface enables the host to communicate with the various functional blocks within the part via two types of accesses: Programmed I/O (PIO) access, and DMA access.

A number of configuration registers must be programmed prior to any accesses by the host computer. The configuration registers are programmed via a Plug-and-Play configuration sequence or via configuration software provided by Crystal Semiconductor.

I/O CYCLES

Every device that is enabled, requires I/O space. An I/O cycle begins when the part decodes a valid address on the bus while the DMA acknowledge signals are inactive and AEN is low. The $\overline{IOR}$ and $\overline{IOW}$ signals determine the direction of the data transfer. For read cycles, the part will drive data on the SD<7:0> lines while the host asserts the $\overline{IOR}$ strobe. Write cycles require the host to assert data on the SD<7:0> lines and strobe the $\overline{IOW}$ signal. Data is latched on the rising edge of the $\overline{IOW}$ strobe.

I/O ADDRESS DECODING

The logical devices use 10-bit or 12-bit address decoding. The Synthesizer, Sound Blaster, Game Port, MPU-401, CDROM, and Modem devices support 10-bit address decoding, while the Windows Sound System and Control devices support 12-bit address decoding. Devices that support 10-bit address decoding, require A10 and A11 be zero for proper decode; therefore, no aliasing occurs through the 12-bit address space.

To prevent aliasing into the upper address space, a "16-bit decode" option may be used, where the upper address bits SA12 through SA15 are connected to the part. SA12-SA15 are then decoded to be 0,0,0,0 for all logical device address decoding. When the upper address bits are used, the CDROM and Modem interfaces are no longer available since the upper address pins are multiplexed with the CDROM and Modem interfaces (See *Reset and Power Down* section). If the CDROM or Modem is needed, the circuit shown in Figure 2 can replace the SA12 through SA15 pins and provide the same functionality. Four cascaded OR gates, using a 74ALS32, can replace the ALS138 in Figure 2, but causes a greater delay in address decoding.

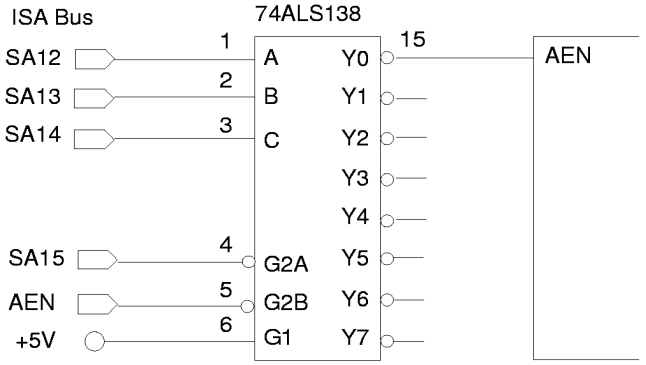


Figure 2. 16-bit Decode Circuit

DMA CYCLES

The part supports up to three 8-bit ISA-compatible DMA channels. The default hardware connections, which can be changed through the hardware configuration data, are:

DMA A = ISA DMA channel 0
DMA B = ISA DMA channel 1
DMA C = ISA DMA channel 3

The typical configuration would require two DMA channels. One for the WSS Codec and Sound Blaster playback, and the other for WSS Codec capture (to support full-duplex). The CDROM, if used, can also support a DMA channel, although this is not typical.

DMA cycles are distinguished from control register cycles by the generation of a DRQ (DMA Request). The host acknowledges the request by generating a $\overline{\text{DACK}}$ (DMA Acknowledge) signal. The transfer of audio data occurs during the $\overline{\text{DACK}}$ cycle. During the $\overline{\text{DACK}}$ cycle the address lines are ignored.

The digital audio data interface uses DMA request/grant pins to transfer the digital audio data between the part and the ISA bus. Upon receipt of a DMA request, the host processor responds with an acknowledge signal and a command strobe which transfers data to and from the part, eight bits at a time. The request pin stays active until the appropriate number of 8-bit cycles have occurred. The number of 8-bit transfers will vary depending on the digital audio data format, bit resolution, and operation mode.

The DMA request signal can be asserted at any time. Once asserted, the DMA request will remain asserted until a complete DMA cycle occurs. A complete DMA cycle consists of one or more bytes depending on which device internal to the part is generating the request.

INTERRUPTS

For Plug-and-Play flexibility, six interrupt pins are supported, although only one or two are typically used. The default hardware connections, which can be modified through the hardware configuration data, are:

IRQ A = ISA Interrupt 5
IRQ B = ISA Interrupt 7
IRQ C = ISA Interrupt 9
IRQ D = ISA Interrupt 11
IRQ E = ISA Interrupt 12
IRQ F = ISA Interrupt 15

The typical configuration would support two interrupt sources: one shared between the WSS Codec and the Sound Blaster Pro compatible devices, and the other for the MPU401 device. Interrupts are also supported for the Synthesizer, Control, CDROM devices, but are typically not used. If the modem logical device (LD5) is used, it would typically support an interrupt.

PLUG AND PLAY

The Plug-and-Play (PnP) interface logic is compatible with the Intel/Microsoft Plug-and-Play specification, version 1.0a, for an ISA-bus device. Since the part is an ISA-bus device, it only supports ISA-compatible IRQs and DMA channels. Plug and Play compatibility allows the PC to automatically configure the part into the system upon power up. Plug and Play capability optimally resolves conflicts between Plug and Play and non-Plug and Play devices within the system. Alternatively, the PnP feature can be bypassed. See the *Bypassing PnP* section for more information. For a detailed Plug-and-Play protocol description, please refer to the *Plug and Play ISA Specification.*

To support Plug-and-Play in ISA systems that do not have a PnP BIOS or a PnP-aware operating system, the Configuration Manager (CM) TSR and an ISA Configuration Utility (ICU) from Intel Corp. are used to provide these functions. The CM isolates the cards, assigns Card Select Numbers, reads PnP card resource requirements, and allocates resources to the cards based on system resource availability. The ICU is used to keep the BIOS and the CM informed of the current system configuration. It also aids users in determining configurations for non-PnP ISA cards. A more thorough discussion of the Configuration Manager and the ISA Configuration Utility can be found in the *Product Development Information* document of the Plug and Play Kit by Intel Corp. In a PnP BIOS system, the BIOS is responsible for configuring at least all system board PnP devices. Some systems require additional software to aid the BIOS in configuring PnP ISA cards. The PnP BIOS can execute all PnP functions independently of the type of operating system. However, if a PnP aware operating system is present, the PnP responsibilities are shared between the BIOS and the operating system. For more information regarding PnP BIOS, please refer to the latest revision of the *Plug and Play BIOS Specification* published by Compaq Computer, Phoenix Technologies, and Intel.

The Plug and Play configuration sequence maps the various functional blocks of the part (logical devices) into the host system address space and configures both the DMA and interrupt channels. The host has access to the part via three 8-bit auto-configuration ports: Address port (0279h), Write Data port (0A79h), and relocatable Read Data port (020Bh - 03FFh). The read data port is relocated automatically by PnP software when a conflict occurs.

The configuration sequence is as follows:

1. Host sends a software key which places all PnP cards in the sleep state (or Plug-and-Play mode).

2. The Crystal part is isolated from the system using an isolation sequence.

3. A unique identifier (handle) is assigned to the part and the resource data is read.

4. After all cards' resource requirements are determined, the host uses the handle to assign conflict-free resources

5. After the configuration registers have been programmed, each configured logical device is activated.

6. The part is then removed from Plug-and-Play mode.

Upon power-up, the chip is inactive and must be enabled via software. The Crystal part monitors writes to the PnP Auto-Configuration Address port (0279h). If the host sends a PnP initiation key, consisting of a series of 32 predefined byte writes, the hardware will detect the key and place the part into the Plug-and-Play (PnP) mode. Another method to program the part is to use a special Crystal initiation key which functions like the PnP initiation key, but can be invoked by the user at any time. However, the Crystal Key only supports one Crystal part per system. The Crystal key and special commands are detailed in the *Crystal Key* and *Bypassing PnP* sections.

The isolation sequence uses a unique 72-bit serial identifier. The host performs 72 pairs of I/O read accesses to the Read Data port. The identifier determines what data is put on the data bus in response to those read accesses. When the isolation sequence is complete, the CM assigns a Card Select Number (CSN) to the part. This number distinguishes the Crystal part from the other PnP devices in the system. The Configuration Manager (CM) then reads the resource data from the Crystal part. The 72-bit identifier and the resource data is either stored in an external user-programmable E^2PROM, or loaded via a "hostload" procedure from BIOS before PnP software is initiated.

The CM determines the necessary resource requirements for the system and then programs the part through the configuration registers. The configuration register data is written one logical device at a time. After all logical devices have been configured, CM activates each device individually. Each logical device is now available on the ISA bus and responds to the programmed address range, DMA channels, and interrupts that have been allocated to that logical device.

PnP Data

Hardware Configuration and Plug-and-Play resource data must be loaded into the part's RAM. The data may be stored in an external E^2PROM or may be downloaded from the host.

To load the data, refer to the *Loading Resource Data* section. The following is the Plug-and-Play resource data:

The first nine bytes of the PnP resource data are the Plug-and-Play ID, which uniquely identifies the Crystal part from other PnP devices. The Crystal default is broken down as follows:

0Eh, 63h - Crystal ID - 'CSC' in compressed ASCII. (See the PnP Spec for more information)

42h - Oem ID. A unique Oem ID must be obtained from Crystal for each unique Crystal product used.

35h - Crystal product ID for the CS4236B

FFh, FFh, FFh, FFh - Serial number. This can be modified by each OEM to uniquely identify their card.

??h - Checksum.

Of the 9-byte serial number listed above, Crystal software uses the first two bytes to indicate the presence of a Crystal part, and the fourth byte, 0x35, to indicate the CS4236B; therefore, these three bytes must not be altered.

The next 3 bytes are the PnP version number. The default is version 1.0a: 0Ah, 10h, 01h.

The next sequence of bytes are the ANSI identifier string. The default is: 82h, 0Eh, 00h, 'Crystal Codec', 00h.

The logical device data must be entered using the PnP ISA Specification format. Typical logical device values are found in Table 1. The E^2PROM version for this data is found in Appendix A.

Loading Resource Data

A serial E^2PROM interface allows user-programmable serial number and resource data to be stored in an external E^2PROM. The interface is compatible with devices from a number of vendors and the size may vary according to specific customer requirements. The maximum size for resource data supported by the part's internal RAM is 384 bytes of combined Hardware Configuration and PnP resource data. With the addition of the 4-byte header, the maximum amount of E^2PROM space used would be 388 bytes. However, the part also supports firmware upgrades via the E^2PROM. The maximum size E^2PROM supported is 2k bytes. After power-up, the existence of an E^2PROM is checked by reading the first two bytes from the E^2PROM interface. If the data from the E^2PROM port reads 55h and BBh, then the rest of the E^2PROM data is loaded into the internal RAM. If the first two bytes aren't correct, the E^2PROM is assumed not to exist and a "hostload" procedure must be used to load the internal RAM. The Hostload procedure can be found in the *Hostload* section. For motherboard designs, an E^2PROM should still be included, to allow faster integrating of resource and firmware patch data. This allows updates without respiring BIOS code. If the part is installed on a plug-in card, then an external E^2PROM is required to ensure that the proper PnP resource data is loaded into the internal RAM prior to a PnP sequence. See the *External E^2PROM* section for more information on the serial E^2PROM interface and E^2PROM programming.

The format for the data stored in the E^2PROM is as follows:

(Hardware Configuration Data:)
2 bytes E^2PROM validation: 55h, BBh

2 bytes length of resource data in E^2PROM

19 bytes Hardware Configuration

(Plug and Play Resource Data:)
9 bytes Plug and Play ID

3 bytes Plug and Play version number

Variable number of bytes of user defined ASCII ID string

Logical Device 0 (Windows Sound System, FM Synthesizer, Sound Blaster Pro) data

Logical Device 1 (Game Port) data

Logical Device 2 (Control) data

Logical Device 3 (MPU-401) data

Logical Device 4 (CD-ROM) data

Logical Device 5 (Modem) data

End of Resource byte & checksum byte

Firmware patch code.

A typical E^2PROM data load, in assembly format, can be found in Appendix A.

Loading Firmware Patch Data

An external E^2PROM is read during the power-up sequence that stores Hardware Configuration and PnP data, and firmware patch data. The part contains RAM and ROM to run the core proces-

sor. The RAM allows updates to the core processor functionality. Placing the firmware patches in E^2PROM, gives the maximum functionality at power-up without the need for a software driver.

The firmware patch data is typically included at the end of the PnP resource data. Crystal provides a utility that will read in patch data from a file, and append it to the PnP resource data. The patch file must be obtained from Crystal.

The Crystal Key

NOTE: The Crystal Key cannot differentiate between multiple Crystal Codecs in a system; therefore, ONLY ONE Crystal part is allowed in systems using the Crystal Key. To allow multiple parts in a system, the Plug-and-Play isolation sequence must be used since it supports multiple parts via the serial identifier used in the isolation sequence.

Physical Device	Logical Device	Best Choice	Acceptable Choice 1	Sub optimal Choice 1	Sub optimal Choice 2
WSS	**0**			ANSI ID = WSS/SB	
16-bit address decode	WSSbase Length/Alignment	534h-534h 4/4	534-608h 4/D4h	534-FFCh 4/4	
high true edge sensitive	IRQ	5 (SB share)	5,7,9,11,12,15 (SB share)	5, 7, 9, 11, 12, 15 (SB share)	
8-bit, count by byte, type A	DMA	1 (SB share)	0, 3 (SB share)	0, 1, 3 (SB share)	
same	DMA	0, 3	0, 1, 3	----	
Synthesis	**0**				
16-bit address decode	SYNbase Length/Alignment	388h 4/8	388h 4/8	388-3F8h 4/8	
	IRQ	----	----	----	
SB Pro	**0**				
16-bit address decode	SBbase Length/Alignment	220h 16/16	220-260h 16/32	220-300h 16/32	
Game Port	**1**			ANSI ID = GAME	
16-bit address decode	GAMEbase Length/Alignment	200h 8/8	208h 8/8		
Control	**2**			ANSI ID = CTRL	
16-bit address decode	CTRLbase Length/Alignment	120-3F8h 8/8			
	IRQ	----			
MPU401	**3**			ANSI ID = MPU	
16-bit address decode	MPUbase Length/Alignment	330h 2/8	330-360h 2/8	330-3E0h 2/8	
	IRQ	9	9,11,12,15	----	

---- Feature not supported in the listed configuration, but is supported through customization.

Table 1. Typical Motherboard Plug-and-Play Resource Data

The Crystal key places the part in the configuration mode. Once the Crystal key has been initiated, new PnP resource data can be downloaded by a hostload sequence, or an alternate method of programming the configuration registers may be used. This alternate method is referred to as the "SLAM" method. The SLAM method allows the user to directly access the configuration registers, configure, and activate the chip, and then, optionally, disable the PnP and/or Crystal key feature. The SLAM method uses commands that are similar to the PnP commands; however, they are different since the user has direct access to the configuration registers. To use the SLAM method, see the *Bypassing PnP* section.

The following 32 bytes, in hex, are the Crystal key:

96, 35, 9A, CD, E6, F3, 79, BC,

5E, AF, 57, 2B, 15, 8A, C5, E2

F1, F8, 7C, 3E, 9F, 4F, 27, 13,

09, 84, 42, A1, D0, 68, 34, 1A

Bypassing Plug and Play

The SLAM method allows the user to bypass the Plug and Play features and, as an option, allows the part to act like a non-Plug and Play or legacy device; however, the SLAM method only supports one Crystal IC per system. The user directly programs the resources into the part, and then optionally disables the PnP and/or the Crystal Key, which forces the part to disregard any future PnP or Crystal initiation key sequences (All activated logical devices appear as legacy devices to PnP). The Crystal and PnP keys can also be disabled through the E^2PROM.

To use the SLAM method, the following sequence must be followed:

1. Host sends 32-byte Crystal key to I/O 0279h, chip enters configuration mode.

2. Host programs CSN (Card Select Number) by writing a 06h and 00h to I/O 0279h.

3. Host programs the configuration registers of each logical device by writing to I/O 0279h. The following data is the maximum amount of information per device. All current devices only need a subset of this data:
   Logical Device ID (15h, xxh)
   xxh is logical device number: 0-5

   I/O Port Base Address 0 (47h, xxh, xxh)
   high byte , low byte

   I/O Port Base Address 1 (48h, xxh, xxh)
   high byte , low byte

   I/O Port Base Address 2 (42h, xxh, xxh)
   high byte , low byte

   Interrupt Select 0 (22h, xxh)

   Interrupt Select 1 (27h, xxh)

   DMA Select 0 (2Ah, xxh)

   DMA Select 1 (25h, xxh)

   Activate Device (33h, 01h)
   (33h, 00h deactivates a device)

4. Repeat #3 for each logical device to be enabled. (Not all devices need be enabled.)

5. Host activates chip by writing a 79h to 279h.

6. (Optional) Host disables PnP Key by writing a 55h to CTRLbase+5. The part will not participate in any future PnP cycles. The Crystal Key can also be disabled by writing a 56h to CTRLbase+5.

NOTE: To enable the PnP/Crystal Keys after they have been disabled by the SLAM method, bring the RESDRV pin to a logic high or remove power from the device.

The following illustrates typical data sent using the SLAM method.

```
006h, 001h          ; CSN=1

015h, 000h          ; LOGICAL DEVICE 0
047h, 005h, 034h    ; WSSbase = 0x534
048h, 003h, 088h    ; SYNbase = 0x388
042h, 002h, 020h    ; SBbase = 0x220
022h, 005h          ; WSS & SB IRQ = 5
02Ah, 001h          ; WSS & SB DMA0 = 1
025h, 003h          ; WSS capture DMA1 = 3
033h, 001h          ; activate logical device 0

015h, 001h          ; LOGICAL DEVICE 1
047h, 002h, 000h    ; GAMEbase = 0x200
033h, 001h          ; activate logical device 1

015h, 002h          ; LOGICAL DEVICE 2
047h, 001h, 020h    ; CTRLbase = 0x120
033h, 001h          ; activate logical device 2

015h, 003h          ; LOGICAL DEVICE 3
047h, 003h, 030h    ; MPUbase=0x330

022h, 009h          ; MPU IRQ = 9
033h, 001h          ; activate logical device 3

079h                ; activate Crystal device
```

If all the above data is sent, after the Crystal key, all devices except the CDROM and Modem will respond to the appropriate resources given.

Hardware Configuration Data

The Hardware Configuration data contains mapping information that links interrupt and DMA pins with actual interrupt numbers used by PnP and SLAM procedures. This data also controls the XCTL0/XA2 pin functionality. The Hardware Configuration data precedes the PnP Resource data.

The Hardware Configuration data is either 19 or 23 bytes long and contains the data necessary to configure the part. If an E^2PROM is not used (Hostload), the first four bytes are not needed, which means the configuration data is only 19 bytes long. The configuration data maps the many functions of the logical devices to the physical pins of the chip. Table 2 lists the Hardware Configuration bytes. The detailed bit descriptions for each byte follows below.

HW Config. Byte 5: ACDbase Address Length Mask, Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	CM2	CM1	CM0

CM2-CM0 — Address bit masks for the Alternate CDROM address decode, ACDbase. See the *CDROM Interface* section for more details on ACDbase

000 - $\overline{\text{ACDCS}}$ low for 1 byte
001 - $\overline{\text{ACDCS}}$ low for 2 bytes
011 - $\overline{\text{ACDCS}}$ low for 4 bytes
111 - ACDCS low for 8 bytes
xxx - all others, RESERVED

BYTE	Default	Description
1	55h	E^2PROM validation byte 1. The first two bytes tell the Crystal Codec that the E^2PROM exists.
2	BBh	E^2PROM validation byte 2
3	00h	High byte for length of resource data in E^2PROM
4	DDh	Low byte for length of resource data in E^2PROM
5	00h	Alternate CDROM (Logical Device 4), ACDbase, Address length mask
6	03h	Modem (Logical Device 5), COMbase, Address length mask
7	80h	Misc. Configuration Bits: Interrupt Pin Polarities, Key Disables, VCEN, & LD4 features
8	00h	Global Configuration Bits: IFM, VCF1 and VCF0, WTEN, SPS
9	0Bh	Code Base Byte - Must be 0x0B
10*	20h	RESERVED - Must be 0x20
11*	04h	RESERVED - Must be 0x04
12*	08h	RESERVED - Must be 0x08
13*	10h	RESERVED - Must be 0x10
14*	80h	RESERVED - Must be 0x80
15*	00h	RESERVED - Must be 0x00
16*	00h	RESERVED - Must be 0x00
17	00h	External Peripheral Port I/O Decode Address Length 00 = 4 bytes, 08 = 8 bytes 08h causes XCTL0/XA2 pin to change to peripheral port address bit XA2.
18*	48h	RESERVED - Must be 0x48
19	75h	IRQ A/B Selection: Lower nibble = A, Upper nibble = B. Along with next two bytes - specify hardware interrupts tied to IRQA-IRQF pins
20	B9h	IRQ C/D Selection: Lower nibble = C, Upper nibble = D.
21	FCh	IRQ E/F Selection: Lower nibble = E, Upper nibble = F.
22	10h	DMA A/B Selection: Lower nibble = A, Upper nibble = B. This byte and the next byte - specify hardware DRQ/DACKs tied to the DMAA-DMAC pins
23	03h	DMA C Selection: Lower nibble = C, Upper nibble = reserved (must be 0).

NOTE:The first four bytes are exclusive to the E^2PROM and are not used in the Hostload mode.
* Currently not supported. Must be set to default values given in the table.

Table 2. Hardware Configuration Data

HW Config. Byte 6: COMbase Address Length Mask, Default = 00000011

D7	D6	D5	D4	D3	D2	D1	D0
MM7	MM6	MM5	MM4	MM3	MM2	MM1	MM0

MM7-MM0 Address bit masks for Logical Device 5, typically a modem address, COMbase. See the *Modem Interface* Section for more details on COMbase.

00000000 - $\overline{\text{MCS}}$ low for 1 byte
00000001 - $\overline{\text{MCS}}$ low for 2 bytes
00000011 - $\overline{\text{MCS}}$ low for 4 bytes
00000111 - $\overline{\text{MCS}}$ low for 8 bytes
00001111 - $\overline{\text{MCS}}$ low for 16 bytes
00011111 - $\overline{\text{MCS}}$ low for 32 bytes
00111111 - $\overline{\text{MCS}}$ low for 64 bytes
01111111 - $\overline{\text{MCS}}$ low for 128 bytes
11111111 - MCS low for 256 bytes
xxxxxxxx - all others, RESERVED

NOTE: The part only buffers the lower three address bits onto the peripheral port. When setting the address decode greater than 8 bytes, the upper address bits should be buffered externally.

HW Config. Byte 7: Misc. Configuration Bits, Default = 10000000

D7	D6	D5	D4	D3	D2	D1	D0
IHCD	IHS	PKD	CKD	IHM	VCEN	SDD	ACDB7D

ACDB7D Alternate CDROM, data Bit 7 Disable. When set, SD7 is held in a high impedance state when reading from ACDbase+1 (only this one address). This bit provides support for IDE alternate base address sharing with the floppy disk controller.

SDD SD Disable. When set, SD<7:0> are high impedance on reads from any peripheral port address: External synthesis, CDROM or Modem devices. Allows external buffers to bypass the part while still allowing PnP address support. This bit is also internally forced on whenever WTEN or SPS in HW Config. byte 8, or C8, is set.

VCEN Volume Control Enable. When set, the $\overline{\text{UP}}$, $\overline{\text{DOWN}}$, and $\overline{\text{MUTE}}$ pins become active and provide a hardware master volume control.

IHM Interrupt High - Modem (LD5). When set, MINT is active high. When clear, MINT is active low.

CKD Crystal Key disable. When set, blocks the part from receiving the Crystal key. Note that if both CKD and PKD are set, software will be unable to reconfigure the part.

PKD PnP Key disable. When set, blocks the part from receiving the Plug-and-Play key. Note that if both CKD and PKD are set, software will be unable to reconfigure the part.

IHS Interrupt High - Synthesizer. When set, SINT is active high. When clear, SINT is active low.

IHCD Interrupt High - CDROM. When set, CDINT is active high. When clear, CDINT is active low.

HW Config. Byte 8: Global Configuration Bits, Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
IFM	VCF1	VCF0	SLAD	WTEN	SPS	res	res

res — Must be set to zero to allow compatibility with future upgrades.

SPS — DSP Serial Port Switch. When set, switches the DSP serial port pins from the second joystick to the XD4-XD1 pins. Then, when SPE in I16 is set, the XD4-XD1 pins convert to the DSP serial port pins. Once this bit is enabled, the SD bus will not be driven when accesses occur to peripheral port devices. This function is also available in C8.

WTEN — WaveTable Serial Port Enable. When set, forces XD7-XD5 pins to convert to the CS9236 Single-Chip Wavetable Music Synthesizer serial port pins. Once this bit is enabled, the SD bus will not be driven when accesses occur to peripheral port devices. This function is also available in C8.

SLAD — Soundblaster Alternate Line Disable. When clear, Sound Blaster (SB) Synthesizer Volume changes affect the LINE Alternate (X0/X1) volume. When set, SB Synthesizer Volume changes do not affect X0/X1 registers.

VCF1,0 — Hardware Volume Control Format. These bits control the format of the hardware volume control pins UP, DOWN, and MUTE. The volume control is enabled by setting VCEN in the previous Hardware Configuration byte.

00 - $\overline{\text{MUTE}}$ is a toggle switch. When $\overline{\text{MUTE}}$ is low, the volume is muted.
01 - $\overline{\text{MUTE}}$ is a momentary switch. $\overline{\text{MUTE}}$ toggles between mute and un-mute. Pressing the up or down switch always un-mutes.
10 - $\overline{\text{MUTE}}$ is not used. Two button volume control. Pressing the up and down buttons simultaneously causes the volume to mute. Pressing up or down un-mutes.
11 - $\overline{\text{UP}}$ pin is not used. The $\overline{\text{MUTE}}$ pin functions as the Up function. With this exception, this mode functions similarly to the pervious two-button mode. This mode provides backwards compatibility with the CS4236.

IFM — Internal FM. When set, the internal FM synthesizer is enabled. When clear, FM must be provided on the external LINE analog inputs.

HW Config. Byte 9: Code Base Byte, Default = 00001011

D7	D6	D5	D4	D3	D2	D1	D0
CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0

CB7-CB0 — Code Base Byte. Determines the code base located in the E^2PROM. If not correct, the Firmware code after the PnP resource data is not loaded.

0x0B - CS4236B
0x43 - CS4236

The next 7 bytes are reserved for future expansion and must be set to their default values as listed in Table 2

The next byte of hardware configuration data is byte 17 in Table 2. This byte determines the function of the XCTL0/XA2 pin. The default of 0, forces the pin to the control function XCTL0, and the external peripheral port supports only 4 I/O locations through XA0-XA1. If this byte is set to 08h, the pin switches to the XA2 function and the peripheral port supports 8 I/O locations through XA2-XA0.

The next byte, listed as byte 18, is reserved for future expansion and must be set to 0x48.

Bytes 19 through 21 map the interrupt number to the actual interrupt pins A - F. As shown in the table, the byte 20 default is 0xB9; therefore, IRQC, which is the lower nibble, maps to the ISA interrupt 9. Likewise IRQD, which is the upper nibble, maps to the ISA interrupt 11 (0Bh).

Bytes 22 and 23 map the DMA channel number to the actual DMA pins A-C. As shown in the table, the byte 22 default is 0x10; therefore, DRQA/$\overline{\text{DACKA}}$ is the lower nibble which maps to the ISA DMA channel 0. Likewise DRQB/$\overline{\text{DACKB}}$ is the upper nibble which maps to the ISA DMA channel 1.

Hostload Procedure

This procedure is provided for backwards compatibility with the CS4236. Since the E^2PROM allows all resource and firmware patch data to be loaded at power-up, this procedure is typically not used. To download PnP resource data from the host to the part's internal RAM, use the following sequence:

1. Configure Control I/O base address, CTRLbase, by one of two methods: regular PnP cycle or Crystal Key method.

   a. The host can use the regular PnP cycle to program the CTRLbase, and then place the chip in the wait_for_key_state

   b. If the Crystal Key method is used:

      First, send the 32-byte Crystal key to I/O address 0279h. (The Crystal Key only supports one Crystal part per system.)

      Second, configure logical device 2 base address, CTRLbase, by writing to I/O 0279h (15h, 02h, 47h, xxh, xxh, 33h, 01h, 79h).
      Note: The two xxh represent the base_address_high and base_address_low respectively. The default is: 01h, 20h.

2. Write 57h (Jump to ROM) command to CTRLbase+5.

3. Download the PnP resource data.

   a. Send download command by writing AAh to CTRLbase+5.

   b. Send starting download address (4000h) by writing low byte (00h) first, and then high byte (40h) to CTRLbase+5.

   c. Send the Hardware Configuration and resource data in successive bytes to CTRLbase+5. This includes the Hardware Configuration and the PnP resource data. The PnP resource format is described in the *PnP Data* section. The resource header should not contain the first four bytes which are only used for E^2PROM loads.

4. End download by writing 00h to CTRLbase+6.

5. If any of the Hardware Configuration Data (first 19 bytes) has changed, 5Ah must be written to CTRLbase+5 to force the part to internally update this information.

The new PnP data is loaded and the part is ready for the next PnP cycle.

External E^2PROM

The Plug and Play specification defines 32 bits of the 72-bit Serial Identifier as being a user defined serial number. The E^2PROM is used to change the user section of the identifier, store default resource data for PnP, Hardware Configuration data specific to the Crystal part, and firmware patches to upgrade the core processor functionality.

The E^2PROM interface uses an industry standard 2-wire interface consisting of a bi-directional data line and a clock line driven from the part. After power-on the part looks for the existence of an E^2PROM device and loads the user defined data. The existence is determined by the first two bytes read (0x55 followed by 0xBB). If the first two bytes are correct, the part reads the next two bytes to determine the length of data in the E^2PROM. The length bytes indicate the number of bytes left to be read (not including the two validation bytes or two length bytes). As shown in Figure 3, the E^2PROM is read using a start bit followed by a dummy write, to initialize the address to zero. Then another start bit and device address, followed by all the data. Since the part uses the sequential read properties of the E^2PROM, only one E^2PROM, is supported (ganged E^2PROMs are not supported).

Some E^2PROMs that are compatible with this interface are:

Atmel	AT24Cxx series
MicroChip	24LCxxB series
National	NM24CxxL series
Ramtron	FM24Cxx series
SGS Thompson	ST24Cxx series
Xicor	X24Cxx series

where the xx is replaced by 02, 04, 08, or 16 based on the size of the E^2PROM desired. The size of 16 (2k bytes) is preferred since it allows the maximum flexibility for upgrading firmware patches. Other E^2PROMs compatible with Figure 3 and the timing parameters listed in the front of the data sheet may also be used.

The maximum Hardware Configuration and PnP resource RAM data supported is 384 bytes, and a four byte header; therefore, the maximum amount of data storage, without firmware patches, in E^2PROM would be 388 bytes. The maximum size E^2PROM supported is 2k bytes. This allows the inclusion of firmware patches after the PnP resource data.

If an external E^2PROM exists, it is accessed by the serial interface and is connected to the XD0 and XA0 pins. The two-wire interface is controlled by three bits in the Control logical device, Hardware Control Register (CTRLbase+1). The serial data can be written to or read from the E^2PROM by sequentially writing or reading that register. The three register bits, D0, D1, D2 are labeled CLK, DOUT, and DIN/EEN respectively. The DIN/EEN bit, when written to a one, enables the E^2PROM serial interface. When the DIN/EEN bit is written to a zero, the serial interface is disabled. The DIN/EEN bit is also the Data In (DIN) signal to read back data from the E^2PROM. The XD0 pin is a bi-directional open-drain data line supporting DIN and DOUT; therefore, to read the correct data, the DOUT bit must be set to a one prior to performing a read of the register. Otherwise, the data read back from DIN/EEN will be all zeros. The E^2PROM data can then be read from the DIN/EEN bit. The CLK bit timing is controlled by the host software. This is the serial clock for the E^2PROM. The DOUT bit is used to write/program the data out to the E^2PROM. An external pull-up resistor is required on XD0 because it is an open-drain output. Use the guidelines in the

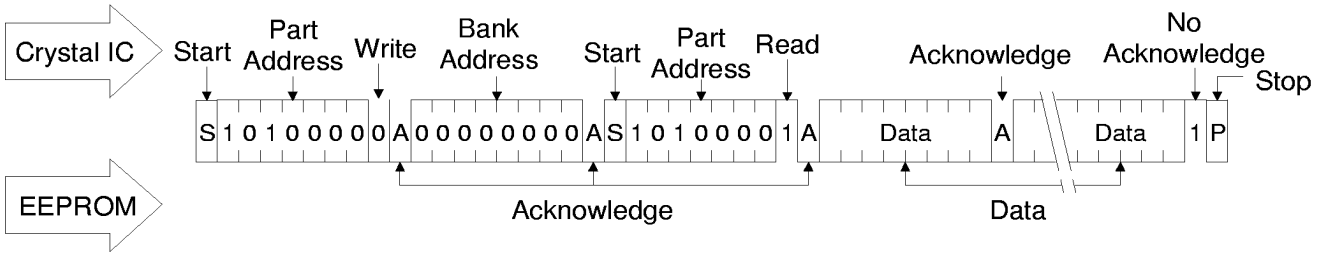


Figure 3. EEPROM Format

specific E^2PROM data sheet to select the value of the pull-up resistor (a typical value would be 3.3kΩ).

Programming the E^2PROM:

1. Configure Control I/O base address by one of two methods: regular PnP cycle or Crystal Key method.

   a. The host can use the regular PnP cycle to program the logical device 2 I/O base address, and then place the chip in the wait_for_key_state

   b. If the Crystal Key method is used:

      First, write to I/O 0279h, send the 32-byte Crystal key. (The Crystal Key only supports one Crystal part per system.)

      Second, configure the Control I/O base address by writing 15h, 02h, 47h, 01h, 20h, 33h, 01h, 79h to 0279h.

2. Refer to the specific data sheet for the E^2PROM you are using for timing requirements and data format. Also, refer to the *Loading Resource Data* section of this data sheet for the E^2PROM resource data format.

3. Send the E^2PROM data in successive bits to CTRLbase+1 (Hardware Control Register) while following the E^2PROM data sheet format.

The E^2PROM now contains the PnP resource data. For this new data to take effect, the part must be reset, causing the part to read the E^2PROM during initialization. Crystal can provide a utility, RESOURCE.EXE, to program E^2PROMs through the Control logical device interface.

WINDOWS SOUND SYSTEM CODEC

The WSS Codec software interface consists of 4 I/O locations starting at the Plug and Play address 'WSSbase', and supports 12-bit address decoding. If the upper address bits, SA12-SA15 are used, they must be 0 to decode a valid address. The WSS Codec also requires one interrupt and one or preferably two DMA channels, one for playback and one for capture. Since the WSS Codec and Sound Blaster device are mutually exclusive, the two devices share the same interrupt and DMA playback channel.

The WSS Codec/Mixer is register compatible with the Microsoft Windows Sound System. Functions include stereo Analog-to-Digital and Digital-to-Analog converters (ADCs and DACs), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, optional A-Law/μ-Law coding, simultaneous capture and playback (at independent sample frequencies) and a parallel bus interface. Five analog inputs are provided and four can be mixed to the ADC mixer. All five can be mixed with the output of the DAC with full volume control. Several data modes are supported including 8- and 16-bit linear as well as 8-bit companded, 4-bit ADPCM compressed, and 16-bit big Endian.

Enhanced Functions (MODEs)

The initial state is labeled MODE 1 and forces the part to appear as a CS4248. The more popular second mode, MODE 2, forces the part to appear as a CS4231 super set and is compatible with the CS4232. To switch from MODE 1 to MODE 2, the CMS1,0 bits, in the MODE and ID register (I12), should be set to 10 respectively. When MODE 2 is selected, the bit IA4 in the Index Address register (R0) will be decoded as a valid index pointer providing 16 additional registers and increased functionality over the CS4248.

To reverse the procedure, set the CMS1,0 bits to 00 and the part will resume operation in

MODE 1. Except for the Capture Data Format (I28), Capture Base Count (I30/31), and Alternate Feature Status (I24) registers, all other Mode 2 functions retain their values when returning to Mode 1. The WSS Codec is backwards compatible with the CS4236, CS4232, CS4231 and CS4248.

The additional MODE 2 functions are: full-duplex support, a programmable timer, Mono In and Mono Out support.

MODE 3 is selected by setting CMS1,0 to 11. MODE 3 allows access to new bits in the indirect registers I0-I31, and allows access to a third set of "extended registers" which are designated X0-X17+X25. The extended registers are accessed through I23. The additional MODE 3 functions are:

1. A full symmetrical mixer. This changes the input multiplexer to a input mixer.

2. Independent sample frequency control on the ADCs and DACs.

3. Programmable Gain and Attenuation on the Microphone inputs.

4. Independent control over the volume of internal FM synthesis and external wavetable.

5. Volume control on the DSP serial port input data.

6. Stereo volume on the monitor feedback path.

FIFOs

The WSS Codec contains 16-sample FIFOs in both the playback and capture digital audio data paths. The FIFOs are transparent and have no programming associated with them.

When playback is enabled, the playback FIFO continually requests data until the FIFO is full, and then makes requests as positions inside the FIFO are emptied, thereby keeping the playback FIFO as full as possible. Thus when the system cannot respond within a sample period, the FIFO starts to empty, avoiding a momentary loss of audio data. If the FIFO runs out of data, the last valid sample can be continuously output to the DACs (if DACZ in I16 is set) which will eliminate pops from occurring.

When capture is enabled, the capture FIFO tries to continually stay empty by making requests every sample period. Thus when the system cannot respond within a sample period, the capture FIFO starts filling, thereby avoiding a loss of data in the audio data stream.

WSS Codec PIO Register Interface

Four I/O mapped locations are available for accessing the Codec functions and mixer. The control registers allow access to status, audio data, and all indirect registers via the index registers. The $\overline{IOR}$ and $\overline{IOW}$ signals are used to define the read and write cycles respectively. A PIO access to the Codec begins when the host puts an address on to the ISA bus which matches WSSbase and drives AEN low. WSSbase is programmed during a Plug and Play configuration sequence. Once a valid base address has been decoded then the assertion of $\overline{IOR}$ will cause the WSS Codec to drive data on the ISA data bus lines. Write cycles require the host to assert data on the ISA data bus lines and strobe the $\overline{IOW}$ signal. The WSS Codec will latch data into the PIO register on the rising edge of the $\overline{IOW}$ strobe.

The audio data interface typically uses DMA request/grant pins to transfer the digital audio data between the WSS Codec and the bus. The WSS Codec is responsible for asserting a request signal whenever the Codec's internal buffers need updating. The bus responds with an acknowledge signal and strobes data to and from the Codec, 8 bits at a time. The WSS Codec keeps the request

pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Note that different audio data types will require a different number of 8-bit transfers.

DMA Interface

The second type of parallel bus cycle from the WSS Codec is a DMA transfer. DMA cycles are distinguished from PIO register cycles by the assertion of a DRQ followed by an acknowledgment by the host by the assertion of $\overline{\text{DACK}}$ (with AEN high). While the acknowledgment is received from the host, the WSS Codec assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines.

The WSS Codec may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a complete DMA cycle occurs to the part. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration register (I9), depending on the DMA that is in progress (playback, capture, or both). Termination of DMA transfers may only happen between sample transfers on the bus. If DRQ goes active while resetting PEN and/or CEN, the request must be acknowledged with $\overline{\text{DACK}}$ and a final sample transfer completed.

DMA CHANNEL MAPPING

Mapping of the WSS Codec's DRQ and $\overline{\text{DACK}}$ onto the ISA bus is accomplished by the Plug and Play configuration registers. If the Plug and Play resource data specifies only one DMA channel for the Codec (or the codec is placed in SDC mode) then both the playback and capture DMA requests should be routed to the same DRQ/$\overline{\text{DACK}}$ pair (DMA Channel Select 0). If the Plug and Play resource data specifies two DMA channels for the Codec, then the playback DMA request will be routed to the DMA pair specified by the DMA Channel Select 0 resource data, and the capture DMA requests will be routed to the DMA pair specified by the DMA Channel Select 1 resource data.

DUAL DMA CHANNEL MODE

The WSS Codec supports a single and a dual DMA channel mode. In dual DMA channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In dual DMA mode, SDC should be set to 0. The Playback- and Capture-Enables (PEN, CEN, I9) can be changed without a Mode Change Enable (MCE, R0). This allows for proper full duplex control where applications are independently using playback and capture.

SINGLE DMA CHANNEL (SDC) MODE

When two DMA channels are not available, the SDC mode forces all DMA transfers (capture or playback) to occur on a single DMA channel (playback channel). The trade-off is that the WSS Codec will no longer be able to perform simultaneous DMA capture and playback.

To enable the SDC mode, set the SDC bit in the Interface Configuration register (I9). With the SDC bit asserted, the internal workings of the WSS Codec remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation; however, the capture audio channel is now diverted to the playback channel. Alternatively stated, the capture DMA request occurs on DMA channel select 0 for the WSS Codec. (In MODEs 2 and 3, the capture data format is always set in register I28.) If both playback and capture are enabled, the default will be playback. SDC does not have any affect when using PIO accesses.

Sound System Codec Register Interface

The Windows Sound System codec is mapped via four locations. The I/O base address, WSSbase, is determined by the Plug and Play configuration. The WSSbase supports four direct registers, shown in Table 3. The first two direct registers are used to access 32 indirect registers shown in Table 4. The Index Address register (WSSbase+0) points to the indirect register that is accessed through the Indexed Data register (WSSbase+1).

This section describes all the direct and indirect registers for the WSS Codec. Table 5 details a summary of each bit in each register with Tables 6 through 15 illustrating the majority of decoding needed when programming the WSS logical device, and are included for reference. When enabled, the WSS Codec default state is defined as MODE 1. MODE 1 is backwards compatible with the CS4248 and only allows access to the first 16 indirect registers. Putting the part in MODE 2 or MODE 3, using CMS1,0 bits in the MODE and ID register (I12), allows access to indirect registers 16 through 31. Putting the part in MODE 3 also allows access to the extended registers through I23 and other extended features in the indirect registers.

DIRECT MAPPED REGISTERS

The first two WSS Codec registers provide indirect accessing to more codec registers via an index register. The other two registers provide status information and allow audio data to be transferred to and from the WSS Codec without using DMA cycles or indexing.

Note that register defaults are listed in binary form with reserved bits marked with 'x' to indicate unknown. To maintain compatibility with future parts, these reserved bits must be written as 0, and must be masked off when the register is read. The current value read for reserved bits is not guaranteed on future revisions.

Direct Registers: (R0-R3)

Address	Reg.	Register Name
WSSbase+0	R0	Index Address register
WSSbase+1	R1	Indexed Data register
WSSbase+2	R2	Status register
WSSbase+3	R3	PIO Data register

Table 3. WSS Codec Direct Register

Index	Register Name
I0	Left ADC Input Control
I1	Right ADC Input Control
I2	Left Aux #1 Volume
I3	Right Aux #1Volume
I4	Left Aux #2 Volume
I5	Right Aux #2 Volume
I6	Left DAC (PC Wave) Volume
I7	Right DAC (PC Wave) Volume
I8	Fs & Playback Data Format
I9	Interface Configuration
I10	Pin Control
I11	Error Status and Initialization
I12	MODE and ID
I13	Monitor Loopback Volume
I14	Playback Upper Base Count
I15	Playback Lower Base Count
I16	Alternate Feature Enable I
I17	Alternate Feature Enable II
I18	Left Line (Synthesizer) Volume
I19	Right Line (Synthesizer) Volume
I20	Timer Low Byte
I21	Timer High Byte
I22	Alternate Sample Frequency
I23	Extended Register Access (X regs)
I24	Alternate Feature Status
I25	Compatibility ID
I26	Mono Input & Output Control
I27	Reserved
I28	Capture Data Format
I29	Reserved
I30	Capture Upper Base Count
I31	Capture Lower Base Count

Table 4. WSS Codec Indirect Registers

Direct Registers: WSSbase (R0-R3)

ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
WSSbase+0	R0	INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0
WSSbase+1	R1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
WSSbase+2	R2	CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT
WSSbase+3	R3	CD7/PD7	CD6/PD6	CD5/PD5	CD4/PD4	CD3/PD3	CD2/PD2	CD1/PD1	CD0/PD0

Indirect Registers: (I0-I31)

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LAG3	LAG2	LAG1	LAG0
1	RSS1	RSS0	RMGE	-	RAG3	RAG2	RAG1	RAG0
2	LX1OM	LX1IM	LX1BM	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1OM	RX1IM	RX1BM	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2OM	LX2IM	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2OM	RX2IM	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LDOM LPM	LDG6 res	LDG5 LPA5	LDG4 LPA4	LDG3 LPA3	LDG2 LPA2	LDG1 LPA1	LDG0 LPA0
7	RDOM RPM	RDG6 res	RDG5 RPA5	RDG4 RPA4	RDG3 RPA3	RDG2 RPA2	RDG1 RPA1	RDG0 RPA0
8 §	FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	CFS2	CFS1	CFS0	C2SL
9 §	CPIO	PPIO	-	CAL1	CAL0	SDC	CEN	PEN
10	XCTL1	XCTL0	OSM1	OSM0	DEN	DTM	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	CMS1	CMS0	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
16	OLB	TE	CMCE	PMCE	SF1	SF0	SPE	DACZ
17	TEST	TEST	TEST	TEST	APAR	-	XTALE	HPF
18	LLOM LR7	LLIM LR6	LLBM LR5	LLG4 LR4	LLG3 LR3	LLG2 LR2	LLG1 LR1	LLG0 LR0
19	RLOM RR7	RLIM RR6	RLBM RR5	RLG4 RR4	RLG3 RR3	RLG2 RR2	RLG1 RR1	RLG0 RR0
20	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
21	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
22	SRE	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	CS2
23	XA3	XA2	XA1	XA0	XRAE	XA4	-	ACF
24	-	TI	CI	PI	CU	CO	PO	PU
25	0	0	0	0	0	0	1	1
26	MIM	MOM	MBY	-	MIA3	MIA2	MIA1	MIA0
27	-	-	-	-	-	-	-	-
28	FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	-	-	-	-
29	-	-	-	-	-	-	-	-
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

Table 5. WSS Codec Direct & Indirect Register Bits

	bit5	bit4	bit3	bit2	bit1	bit0	WG5-0 (X16,17)	LBA5-0, PA5-0, SPA5-0, FMA5-0
0	0	0	0	0	0	0	12.0 dB	0.0 dB
1	0	0	0	0	0	1	10.5 dB	-1.5 dB
2	0	0	0	0	1	0	9.0 dB	-3.0 dB
3	0	0	0	0	1	1	7.5 dB	-4.5 dB
.	.	.	.	.	.	.	-	.
8	0	0	1	0	0	0	0 dB	-12.0 dB
.	.	.	.	.	.	.	-	.
.	.	.	.	.	.	.	-	.
60	1	1	1	1	0	0	-78.0 dB	-90.0 dB
61	1	1	1	1	0	1	-79.5 dB	-91.5 dB
62	1	1	1	1	1	0	-81.0 dB	-93.0 dB
63	1	1	1	1	1	1	-82.5 dB	-94.5 dB

Table 6. Wavetable, Loopback, PC Wave, DSP Serial, & FM

	bit3	bit2	bit1	bit0	Input Gain (I0,I1)	Mono In (I26)
0	0	0	0	0	0.0 dB	0.0 dB
1	0	0	0	1	1.5 dB	-3.0 dB
2	0	0	1	0	3.0 dB	-6.0 dB
3	0	0	1	1	4.5 dB	-9.0 dB
.	.	.	.	.	-	.
.	.	.	.	.	-	.
.	.	.	.	.	-	.
12	1	1	0	0	18.0 dB	-36.0 dB
13	1	1	0	1	19.5 dB	-39.0 dB
14	1	1	1	0	21.0 dB	-42.0 dB
15	1	1	1	1	22.5 dB	-45.0 dB

Table 7. Input ADC Gain and Mono In Levels

LIS1 RIS1	LIS0 RIS0	LEVEL
0	0	0 dB
0	1	-6 dB
1	0	-12 dB
1	1	-18 dB

Table 8. Input Mixer Attenuation

CFS				
2	1	0	C2SL = 0	C2SL=1
0	0	0	8.0 kHz	5.51 kHz
0	0	1	16.0 kHz	11.025 kHz
0	1	0	27.42 kHz	18.9 kHz
0	1	1	32.0 kHz	22.05 kHz
1	0	0	N/A	37.8 kHz
1	0	1	N/A	44.1 kHz
1	1	0	48.0 kHz	33.075 kHz
1	1	1	9.6 kHz	6.62 kHz

Table 9. Sample Frequencies

	G4	G3	G2	G1	G0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	**0**	**1**	**0**	**0**	**0**	**0.0 dB**
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	-34.5 dB

Table 10. AUX1, AUX2, LINE

FMT1	FMT0	C/$\overline{L}$	Data Format
0	0	0	Linear, 8-bit unsigned
0	0	1	µ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian

Table 11. WSS Codec Data Format

Decimal Value	Hex Value	Digital Atten.	Analog Atten.	LEVEL
64	40	0 dB	12.0 dB	12.0 dB
65	41	0 dB	10.5 dB	10.5 dB
66	42	0 dB	9.0 dB	9.0 dB
67	43	0 dB	7.5 dB	7.5 dB
68	44	0 dB	6.0 dB	6.0 dB
69	45	0 dB	4.5 dB	4.5 dB
70	46	0 dB	3.0 dB	3.0 dB
71	47	0 dB	1.5 dB	1.5 dB
72	48	res	res	res
-	-	-	-	-
127	7F	res	res	res
0	**0**	**0 dB**	**0.0 dB**	**0.0 dB**
1	1	0 dB	-1.5 dB	-1.5 dB
2	2	0 dB	-3.0 dB	-3.0 dB
3	3	0 dB	-4.5 dB	-4.5 dB
4	4	0 dB	-6.0 dB	-6.0 dB
5	5	0 dB	-7.5 dB	-7.5 dB
6	6	0 dB	-9.0 dB	-9.0 dB
-	-	-	-	-
23	17	0 dB	-34.5 dB	-34.5 dB
24	18	-6 dB	-30.0 dB	-36.0 dB
25	19	-6 dB	-31.5 dB	-37.5 dB
26	1A	-6 dB	-33.0 dB	-39.0 dB
27	1B	-6 dB	-34.5 dB	-40.5 dB
28	1C	-12 dB	-30.0 dB	-42.0 dB
29	1D	-12 dB	-31.5 dB	-43.5 dB
30	1E	-12 dB	-33.0 dB	-45.0 dB
31	1F	-12 dB	-34.5 dB	-46.5 dB
32	20	-18dB	-30.0 dB	-48.0 dB
-	-	-	-	-
62	3E	-60 dB	-33.0 dB	-93.0 dB
63	3F	-60 dB	-34.5 dB	-94.5 dB

Table 12. Master Digital Gain

	MG4	MG3	MG2	MG1	MG0	LEVEL
0	0	0	0	0	0	22.5 dB
1	0	0	0	0	1	21.0 dB
2	0	0	0	1	0	19.5 dB
3	0	0	0	1	1	18.0 dB
-	-	-	-	-	-	-
11	0	1	0	1	1	6.0 dB
12	0	1	1	0	0	4.5 dB
13	0	1	1	0	1	3.0 dB
14	0	1	1	1	0	1.5 dB
15	**0**	**1**	**1**	**1**	**1**	**0 dB**
-	-	-	-	-	-	-
28	1	1	1	0	0	-19.5 dB
29	1	1	1	0	1	-21.0 dB
30	1	1	1	1	0	-22.5 dB
31	1	1	1	1	1	-24.0 dB

Table 13. Microphone Gain

Decimal Value	Sample Rate	Divider
0	50.40 KHz	16 X 21
1	48.00 KHz	353
2	32.00 KHz	529
3	27.42 KHz	617
4	16.00 KHz	1058
5	9.600 KHz	1764
6	8.000 KHz	2117
7	6.620 KHz	2558
8	50.40 KHz	16 X 21
-	-	-
21	50.40 KHz	16 X 21
22	48.10 KHz	16 X 22
23	46.01 KHz	16 X 23
24	44.10 KHz	16 X 24
25	42.36 KHz	16 X 25
26	40.70KHz	16 X 26
-	-	-
189	5600 KHz	16 X 189
190	5570.5 KHz	16 X 190
191	5541.4 KHz	16 X 191
192	5512.5 KHz	16 X 192
-	-	-
255	5512.5 KHz	16 X 192

Table 14. A/D Sample Rate (SRAD7-SRAD0)

Decimal Value	Sample Rate	Divider
0	50.40 KHz	16 X 21
1	48.00 KHz	353
2	32.00 KHz	529
3	27.42 KHz	617
4	16.00 KHz	1058
5	9.600 KHz	1764
6	8.000 KHz	2117
7	6.620 KHz	2558
8	50.40 KHz	16 X 21
-	-	-
21	50.40 KHz	16 X 21
22	48.10 KHz	16 X 22
23	46.01 KHz	16 X 23
24	44.10 KHz	16 X 24
25	42.36 KHz	16 X 25
26	40.70 KHz	16 X 26
27	39.20 KHz	16 X 27
28	37.80 KHz	16 X 28
-	-	-
255	4.150 KHz	16 X 255

Table 15. D/A Sample Rate (SRDA7-SRDA0)

Index Address Register

(WSSbase+0, R0)

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0

IA3-IA0 — Index Address: These bits define the address of the indirect register accessed by the Indexed Data register (R1). These bits are read/write.

IA4 — Allows access to indirect registers 16 - 31. In MODE 1, this bit is reserved and must be written as zero.

TRD — Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the Status Register (R2) is set. Independent for playback and capture interrupts.

0 - Transfers Enabled (playback and capture DRQs occur uninhibited)
1 - Transfers Disabled (playback and capture DRQ only occur if INT bit is 0)

MCE — Mode Change Enable: This bit must be set whenever the current mode of the WSS Codec is changed. The Data Format (I8, I28) and Interface Configuration (I9) registers CANNOT be changed unless this bit is set. The exceptions are CEN and PEN which can be changed "on-the-fly". The DAC output is muted when MCE is set.

INIT — WSS Codec Initialization: This bit is read as 1 when the Codec is in a state in which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the WSS Codec has left the INIT state), the state of this register is: 010x0000 (binary - where 'x' indicates unknown).

During initialization and software power down (PM1,0 = 01), this register CANNOT be written and always reads 10000000 (80h)

Indexed Data Register

(WSSbase+1, R1)

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0 — Indexed Data register: These bits are the indirect register referenced by the Indexed Address register (R0).

During initialization and software power down of the WSS Codec, this register can NOT be written and is always read 10000000 (80h)

Status Register

(WSSbase+2, R2, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT

INT — Interrupt Status: This indicates the status of the internal interrupt logic of the WSS Codec. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register (I10) determines whether the state of this bit is reflected on the IRQ pin assigned to the WSS Codec.

Read States

0 - Interrupt inactive
1 - Interrupt active

PRDY — Playback Data Ready. The Playback Data register (R3) is ready for more data. This bit would be used when direct programmed I/O data transfers are desired.

0 - Data still valid. Do not overwrite.
1 - Data stale. Ready for next host data write value.

PL/$\overline{R}$ — Playback Left/Right Sample: This bit indicates whether data needed is for the Left channel or Right channel in all data formats except ADPCM. In ADPCM it indicates whether the first two or last two bytes of a 4-byte set (8 ADPCM samples) are needed.

0 - Right or 3/4 ADPCM byte needed
1 - Left, Mono, or 1/2 ADPCM byte needed

PU/$\overline{L}$ — Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel. In ADPCM it indicates, along with PL/$\overline{R}$, which one of the four ADPCM bytes is needed.

0 - Lower or 1/3 ADPCM byte needed
1 - Upper, any 8-bit format, or 2/4 ADPCM byte needed.

SER — Sample Error: This bit indicates that a sample was not serviced in time and an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. However, the Alternate Feature Status register (I24) can indicate the exact source of the error.

CRDY — Capture Data Ready. The Capture Data register (R3) contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers.

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/$\overline{R}$ — Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Left channel or Right channel in all audio data formats except ADPCM. In ADPCM it indicates whether the first two or last two bytes of a 4-byte set (8 ADPCM samples) are waiting.

0 - Right or 3/4 ADPCM byte available
1 - Left, Mono, or 1/2 ADPCM byte available

CU/$\overline{L}$ — Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel. In ADPCM it indicates, along with CL/$\overline{R}$, which one of four ADPCM bytes is available.

0 - Lower or 1/3 ADPCM byte available
1 - Upper, any 8-bit format, or 2/4 ADPCM byte available

Note on PRDY/CRDY: These two bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one, the device is ready for more data; or when the CRDY is set to one, data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

I/O DATA REGISTERS

The PIO Data register is two registers mapped to the same address. Writes to this register sends data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

During initialization and software power down of the WSS Codec, this register CANNOT be written and is always read 10000000 (80h)

Capture I/O Data Register

(WSSbase+3, R3, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 — Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register (R2). Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. Once the Status register (R2) is read and a new sample is received from the FIFO, the state machine and Status register (R2) will point to the first byte of the new sample.

During initialization and software power down of the WSS Codec, this register can NOT be written and is always read 10000000 (80h)

Playback I/O Data Register

WSSbase+3, R3, Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0 — Playback Data Port. This is the control register where playback data is written during programmed IO data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset after the Status register (R2) is read, and the current sample is sent to the DACs via the FIFOs.

INDIRECT MAPPED REGISTERS

These registers are accessed by placing the appropriate index in the Index Address register (R0) and then accessing the Indexed Data register (R1). A detailed description of each indirect register is given below. All reserved bits should be written zero and may be 0 or 1 when read. Note that indirect registers 16-31 are not available when in MODE 1 (CMS1,0 in MODE and ID register I12 are both zero).

Left ADC Input Control (I0)

Default = 000x0000

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LAG3	LAG2	LAG1	LAG0

LAG3-LAG0 — Left ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 7.

res — Reserved. Must write 0. Could read as 0 or 1.

LMGE — This bit has no function in MODE 3. In MODEs 1 & 2 it controls the 20 dB gain boost for the left MIC input to the ADC.

LSS1-LSS0 — Left output loopback. In MODE 3, setting these bits to 11 enables the left output loopback into the input mixer. Bit combinations of 01, 10, and 00 disable the loopback.
In MODEs 1 & 2, the input mixer is used as a multiplexer where these bits select the left ADC input source.
00 - LLINE
01 - LAUX1
10 - LMIC
11 - Left Output Mixer Loopback

Right ADC Input Control (I1)

Default = 000x0000

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RAG3	RAG2	RAG1	RAG0

RAG3-RAG0 Right ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 7.

res Reserved. Must write 0. Could read as 0 or 1.

RMGE This bit has no function in MODE 3. In MODEs 1 & 2 it controls the 20 dB gain boost for the right MIC input to the ADCs.

RSS1-RSS0 Right output loopback. In MODE 3 setting these bits to 11 enables the right output loopback into the input mixer. Other bit combinations disable the loopback.
In MODEs 1 & 2, the input mixer is used as a mux. where these bits select the right ADC input source.
00 - RLINE
01 - RAUX1
10 - RMIC
11 - Right Output Mixer Loopback

Left Auxiliary #1 Volume (I2)

Default = 11101000

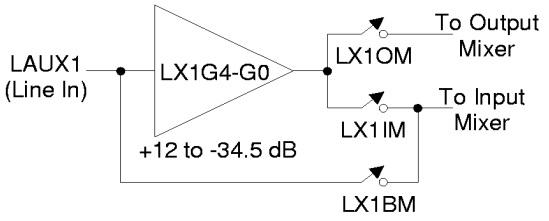
D7	D6	D5	D4	D3	D2	D1	D0
LX1OM	LX1IM	LX1BM	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4-LX1G0 Left Auxiliary #1, LAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

LX1BM Left Auxiliary #1 Bypass Mute. In MODE 3, when set, the left Auxiliary #1 input, LAUX1, (bypassing the gain) to the input mixer, is muted. In MODEs 1 & 2, this bit is not available and is internally controlled by LSS1,0 in I0.

LX1IM Left Auxiliary #1 Mute. In MODE 3, when set, the left Auxiliary #1 input, LAUX1, to the input mixer through the gain stage, is muted.
In MODEs 1 & 2, this bit is not available and internally forced on (muted).

LX1OM Left Auxiliary #1 Mute. When set to 1, the left Auxiliary #1 input, LAUX1, to the output mixer through the gain stage, is muted.



Right Auxiliary #1 Volume (I3)

Default = 11101000

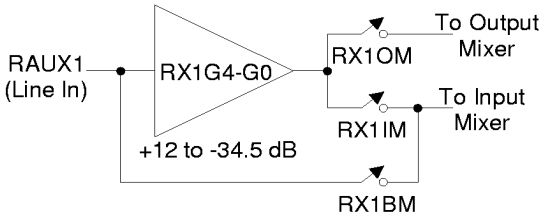
D7	D6	D5	D4	D3	D2	D1	D0
RX1OM	RX1IM	RX1BM	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4-RX1G0 Right Auxiliary #1, RAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

RX1BM Right Auxiliary #1 Bypass Mute. In MODE 3, when set, the right Auxiliary #1 input, RAUX1, (bypassing the gain) to the input mixer is muted. In MODEs 1 & 2, this bit is not available and is internally controlled by RSS1,0 in I1.

RX1IM Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the input mixer through the gain stage, is muted.
In MODEs 1 & 2, this bit is not available and internally forced on (muted).

RX1OM Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the output mixer through the gain stage, is muted.



Left Auxiliary #2 Volume (I4)

Default = 11x01000

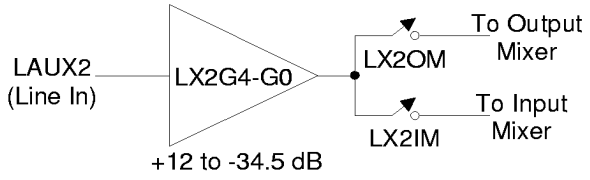
D7	D6	D5	D4	D3	D2	D1	D0
LX2OM	LX2IM	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0 Left Auxiliary #2, LAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

res Reserved. Must write 0.

LX2IM Left Auxiliary #2 Mute. In MODE 3, when set to 1, the left Auxiliary #2 input, LAUX2, to the input mixer through the gain stage, is muted. In MODEs 1 & 2, this bit is not available and internally forced on (muted).

LX2OM Left Auxiliary #2 Mute. When set to 1, the left Auxiliary #2 input, LAUX2, to the output mixer through the gain stage, is muted.



Right Auxiliary #2 Volume (I5)

Default = 11x01000

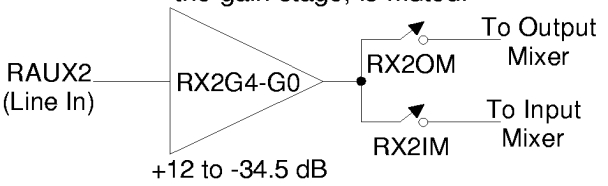
D7	D6	D5	D4	D3	D2	D1	D0
RX2OM	RX2IM	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0 Right Auxiliary #2, RAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

res Reserved. Must write 0. Could read as 0 or 1.

RX2IM Right Auxiliary #2 Mute. In MODE 3, when set, the right Auxiliary #2 input, RAUX2, to the input mixer through the gain stage, is muted. In MODEs 1 & 2, this bit is not available and internally forced on (muted).

RX2OM Right Auxiliary #2 Mute. When set to 1, the right Auxiliary #2 input, RAUX2, to the output mixer through the gain stage, is muted.



Left DAC (PC Wave) Volume (I6)

Default = 10000000

D7	D6	D5	D4	D3	D2	D1	D0
LDOM	LDG6	LDG5	LDG4	LDG3	LDG2	LDG1	LDG0
LPM	res	LPA5	LPA4	LPA3	LPA2	LPA1	LPA0

If both IFM (X4 or Global Config. byte) and WTEN (C8 or Global Config. byte) are cleared, this register is the master digital audio volume for the left channel with the following bit definitions:

LDG6-LDG0 Left DAC Master Volume. The least significant bit represents 1.5 dB, with 0000000 = 0 dB. The total range is +12 to -94.5 dB. See Table 12.

LDOM Left DAC Master Mute. When set, the left DAC to the output mixer is muted.

If IFM or WTEN is set, this register controls the left channel volume for data coming from the ISA bus only (and X14 is the left channel digital audio master volume) with the following bit descriptions.

LPA5-LPA0 Left PC Wave Attenuation. The least significant bit represents -1.5 dB, with 000000 = 0 dB. The total range is 0 to -94.5 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

LPM Left PC Wave Mute. When set, the left PCM input to the digital mixer summer will be muted.

Right DAC (PC Wave) Volume (I7)

Default = 10000000

D7	D6	D5	D4	D3	D2	D1	D0
RDOM	RDG6	RDG5	RDG4	RDG3	RDG2	RDG1	RDG0
RPM	res	RPA5	RPA4	RPA3	RPA2	RPA1	RPA0

If both IFM (X4 or Global Config. byte) and WTEN (C8 or Global Config. byte) are cleared, this register is the master digital audio volume for the right channel with the following bit definitions:

RDG6-RDG0 Right DAC Master Volume. The least significant bit represents 1.5 dB, with 0000000 = 0 dB. The total range is +12 to -94.5 dB. See Table 12.

RDOM Right DAC Master Mute. When set, the right DAC to the output mixer is muted.

If IFM or WTEN is set, this register controls the right channel volume for data coming from the ISA bus only (and X15 is the right channel digital audio master volume) with the following bit descriptions.

RPA5-RPA0 Right PC Wave Attenuation. The least significant bit represents -1.5 dB, with 000000 = 0 dB. The total range is 0 to -94.5 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

RPM Right PC Wave Mute. When set, the right PCM input to the digital mixer summer will be muted.

Fs and Playback Data Format (I8)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	CFS2	CFS1	CFS0	C2SL

C2SL Clock 2 Source Select: This bit selects the clock base used for the audio sample rates for both capture and playback. Note that this bit can be disabled by setting SRE in I22 or by setting IFSE in X11.
CAUTION: C2SL can only be changed while MCE (R0) is set.

See Table below.

CFS2-CFS0 Clock Frequency Divide Select: These bits select the audio sample frequency for both capture and playback. The actual audio sample frequency depends on which clock base (C2SL) is selected. Note that these bits can be disabled by setting SRE in I22 or IFSE in X11.
CAUTION: CFS2-CFS0 can only be changed while MCE (R0) is set.

DIVIDE	C2SL = 0	C2SL = 1
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result in alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left channel. In MODE 1, this bit is used for both playback and capture. In MODEs 2 and 3, this bit is only used for playback, and the capture format is independently selected via I28. MCE (R0) or PMCE (I16) must be set to modify S/$\overline{M}$. See *Changing Audio Data Formats* section for more details.

0 - Mono
1 - Stereo

C/$\overline{L}$, FMT1, and FMT0 bits set the audio data format as shown below. In MODE 1, FMT1, which is forced low, FMT0, and C/$\overline{L}$ are used for both playback and capture. In MODEs 2 and 3, these bits are only used for playback, and the capture format is independently selected via register I28. MCE (R0) or PMCE (I16) must be set to modify the upper four bits of this register. See *Changing Audio Data Formats* section for more details.

FMT1† D7	FMT0 D6	C/$\overline{L}$ D5	Audio Data Format
0	0	0	Linear, 8-bit unsigned
0	0	1	μ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	RESERVED
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian
1	1	1	RESERVED

† FMT1 is not available in MODE 1 (forced to 0).

Interface Configuration (I9)

Default = 00x01000

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	CAL1	CAL0	SDC	CEN	PEN

PEN — Playback Enable. This bit enables playback. The WSS Codec will generate a DRQ and respond to DACK signal when this bit is enabled and PPIO=0. If PPIO=1, PEN enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 - Playback Disabled (playback DRQ and PIO inactive)
1 - Playback Enabled

CEN — Capture Enabled. This bit enables the capture of data. The WSS Codec will generate a DRQ and respond to DACK signal when CEN is enabled and CPIO=0. If CPIO=1, CEN enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 - Capture Disabled (capture DRQ and PIO inactive)
1 - Capture Enabled

SDC — Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. This bit forces the WSS Codec to use one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the *DMA Interface* section for further explanation.

0 - Dual DMA channel mode
1 - Single DMA channel mode

CAL1,0 — Calibration: These bits determine which type of calibration the WSS Codec performs whenever the Mode Change Enable (MCE) bit, R0, changes from 1 to 0. The number of sample periods required for calibration is listed in parenthesis.

0 - No calibration (0)
1 - Converter calibration (321)
2 - DAC calibration (120)
3 - Full calibration (450)

PPIO — Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

CPIO — Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

Caution: This register, except bits CEN and PEN, can only be written while in Mode Change Enable (either MCE or PMCE). See the *Changing Sampling Rate* section for more details.

Pin Control (I10)

Default = 0000000x

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	OSM1	OSM0	DEN	DTM	IEN	res

res — Reserved. Must write 0. Could read as 0 or 1.

IEN — Interrupt Enable: This bit enables the interrupt pin. The Interrupt pin will reflect the value of the INT bit of the Status register (R2). The interrupt pin is active high.

0 - Interrupt disabled
1 - Interrupt enabled

DTM — DMA Timing Mode. MODE 2 & 3 only. When set, causes the current DMA request signal to be deasserted on the rising edge of the IOW or IOR strobe during the next to last byte of a DMA transfer. When DTM = 0 the DMA request is released on the falling edge of the IOW or IOR during the last byte of a DMA transfer.

DEN — Dither Enable: When set, triangular pdf dither is added before truncating the ADC 16-bit value to 8-bit, unsigned data. Dither is only active in the 8-bit unsigned data mode.

0 - Dither enabled
1 - Dither disabled

OSM1-OSM0 — These bits are enabled by setting SRE = 1 in I22. These bits in combination with DIV5-DIV0 and CS2 (I22) determine the current sample rate of the WSS Codec when SRE = 1. Note that these bits can be disabled by setting IFSE in X11.

00 - 12kHz < Fs ≤ 24kHz
01 - Fs > 24kHz
10 - Fs ≤ 12kHz
11 - reserved

XCTL1-XCTL0 — XCTL Control: These bits are reflected on the XCTL1,0 pins of the part. NOTE: These pins are multiplexed with other functions; therefore, they may not be available on a particular design.

0 - TTL logic low on XCTL1,0 pins
1 - TTL logic high on XCTL1,0 pins

Error Status and Initialization (I11, Read Only)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0 — Overrange Left Detect: These bits determine the overrange on the left ADC channel. These bits are updated on a sample by sample basis.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

ORR1-ORR0 — Overrange Right Detect: These bits determine the overrange on the Right ADC channel.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

DRS — DRQ Status: This bit indicates the current status of the DRQs assigned to the WSS Codec.

0 - Capture AND Playback DRQs are presently inactive
1 - Capture OR Playback DRQs are presently active

ACI — Auto-calibrate In-Progress: This bit indicates the state of calibration.

0 - Calibration not in progress
1 - Calibration is in progress

PUR — Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result, if DACZ = 0, the last valid sample will be sent to the DACs. This bit is set when an error occurs and will not clear until the Status register (R2) is read.

COR — Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The old sample will not be overwritten and the new sample will be ignored. This bit is set when an error condition occurs and will not clear until the Status register (R2) is read.

The SER bit in the Status register (R2) is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

MODE and ID (I12)

Default = 100x1010

D7	D6	D5	D4	D3	D2	D1	D0
1	CMS1	CMS0	res	ID3	ID2	ID1	ID0

ID3-ID0 — Codec ID: These four bits indicate the ID and initial revisions of the codec. Further revisions are expanded in indirect register I25 through the CS4236 and C1 for newer chips. These bits are read only.

0001 - Rev B CS4248/CS4231
1010 - All other revisions and parts. See Registers X25 or C1.

res — Reserved. Must write 0. Could read as 0 or 1.

CMS1,0 — Codec Mode Select bits: Enables the Extended registers and functions of the part.

00 - MODE 1
01 - Reserved
10 - MODE 2
11 - MODE 3

Monitor Loopback Volume (I13)

Default = 000000x0

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

LBE — Loopback Enable: When set to 1, the ADC data is digitally mixed with data sent to the DACs. This bit controls the loopback enable for both channels regardless of how SLBE in X10 is set.

0 - Loopback disabled
1 - Loopback enabled

res — Reserved. Must write 0. Could read as 0 or 1.

LBA5-LBA0 — Loopback Attenuation: These bits determine the attenuation of the loopback from ADC to DAC. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

LBA5-LBA0 control left and right channels when SLBE in X10 is clear. When SLBE = 1, these bits only control the left channel and RLBA5- RLBA0 in X10 control the right.

Playback Upper Base (I14)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

PUB7-PUB0 — Playback Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Playback Base register. Reads from this register return the same value

which was written. The Current Count registers cannot be read. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

Playback Lower Base (I15)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

PLB7-PLB0 — Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

Alternate Feature Enable I (I16)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
OLB	TE	CMCE	PMCE	SF1	SF0	SPE	DACZ

DACZ — DAC Zero: This bit will force the output of the playback channel to AC zero when an underrun error occurs

1 - Go to center scale
0 - Hold previous valid sample

SPE — DSP Serial Port Enable. When set, audio data from the ADCs is sent out SDOUT and audio data from SDIN is sent to the DACs. MCE in R0 must be set to change this bit.

1 - Enable serial port
0 - Disable serial port. ISA Bus used for audio data.

SF1,SF0 — Serial Format. Selects the format of the serial port when enabled by SPE. MCE in R0 must be set to change these bits.

0 - 64-bit enhanced. Figure 7.
1 - 64-bit. Figure 8.
2 - 32-bit. Figure 9.
3 - ADC/DAC. Figure 10.

PMCE — Playback Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the playback channel, I8. MCE in R0 must be used to change the sample frequency.

CMCE — Capture Mode Change Enable. When set, it allows modification of the stereo/mono and audio data format bits (D7-D4) for the capture channel, I28. MCE in R0 must be used to change the sample frequency in I8.

TE — Timer Enable: This bit, when set, will enable the timer to run and interrupt the host at the specified frequency in the timer registers.

OLB — Output Level Bit: Provided for backwards compatibility with the CS4236. This bit does nothing on this chip.

Alternate Feature Enable II (I17)

Default = 0000x000

D7	D6	D5	D4	D3	D2	D1	D0
TEST	TEST	TEST	TEST	APAR	res	XTALE	HPF

HPF — High Pass Filter: This bit enables a DC-blocking high-pass filter in the digital filter of the ADC. This filter forces the ADC offset to 0.

0 - disabled
1 - enabled

XTALE — Crystal Enable. Provided for backwards compatibility with the CS4231A. This bit does nothing on the this part.

res — Reserved. Must write 0. Could read as 0 or 1.

APAR — ADPCM Playback Accumulator Reset. While set, the Playback ADPCM accumulator is held at zero. Used when pausing a playback stream.

TEST — Factory Test. These bits are used for factory testing and must remain at 0 for normal operation.

Left Line (Synthesizer) Volume (I18)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
LLOM	LLIM	LLBM	LLG4	LLG3	LLG2	LLG1	LLG0
LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0

This register controls either the left LINE input or is remapped to control the internal FM (X6) or external CS9236 Wavetable synthesizer (X16), or both. When no remapping occurs, the bit definitions are:

LLG4-LLG0 — Left LINE Volume. This register is used to control the LLINE analog input volume to the mixers. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

LLBM — Left LINE Bypass Mute. In MODE 3, when set to 1, the analog Left Line Input, LLINE, (bypassing the gain block) to the input mixer is muted. In MODEs 1 & 2, this bit is not available and is internally controlled by LSS1,0 in I0.

LLIM — Left LINE Input Mute. In MODE 3, when set to 1, the Left Line Input, LLINE, from the volume control to the input mixer is muted. In MODEs 1 & 2, this bit is not available and internally forced on (muted).

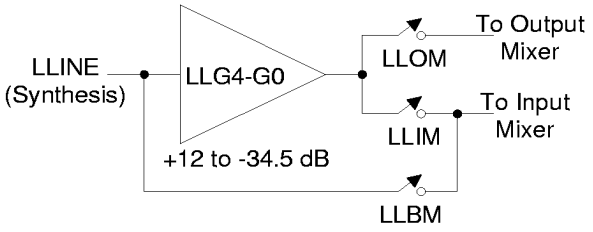
LLOM — Left LINE Output Mute. When set to 1, the Left Line Input, LLINE, from the volume control to the output mixer is muted.

When IFM=1 (X4 or Global Config. byte) and FMRM=1 (X4), FM remapping is enabled. When WTEN=1 (C8 or Global Config. byte) and WTRMD=0 (X4), Wavetable remapping is enabled. If either synthesizer remap is enabled, left LINE analog volume is controlled through X0. With remapping the bit definitions are:

LR7-LR0 — Left Remapped Register.

When IFM=1 and FMRM=1, writes to I18 will write the Internal FM register X6.

When WTEN=1 and WTRMD=0, writes to I18 will write the Wavetable synthesis register X16.



Right Line (Synthesizer) Volume (I19)

Default = xxxxxxxx

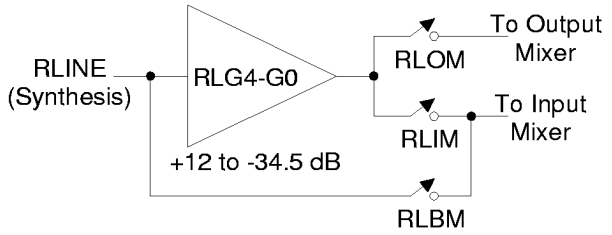
D7	D6	D5	D4	D3	D2	D1	D0
RLOM	RLIM	RLBM	RLG4	RLG3	RLG2	RLG1	RLG0
RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0

This register controls either the right LINE input or is remapped to control the internal FM (X7) or external CS9236 Wavetable synthesizer (X17), or both. When no remapping occurs, the bit definitions are:

RLG4-RLG0 — Right LINE Volume. This register is used to control the RLINE analog input volume to the mixers. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

RLBM — Right LINE Bypass Mute. In MODE 3, when set to 1, the analog Right Line Input, RLINE, (bypassing the gain block) to the input mixer is muted. In MODEs 1 & 2, this bit is not available and is internally controlled by RSS1,0 in I1.

RLIM — Right LINE Input Mute. In MODE 3, when set to 1, the Right Line Input, RLINE, from the volume control to



the input mixer is muted. In MODEs 1 & 2, this bit is not available and internally forced on (muted).

RLOM — Right LINE Output Mute. When set to 1, the Right Line Input, RLINE, from the volume control to the output mixer is muted.

When IFM=1 and FMRM=1, FM remapping is enabled. When WTEN=1 and WTRMD=0, Wavetable remapping is enabled. If either synthesizer remap is enabled, right LINE analog volume is controlled through X1. With remapping the bit definitions are:

RR7-RR0 — Right Remapped Register.

When IFM=1 and FMRM=1, writes to I19 will write the Internal FM register X7.

When WTEN=1 and WTRMD=0, writes to I19 will write the Wavetable synthesis register X17.

Timer Lower Base (I20)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0

TL7-TL0 — Lower Timer Bits: This is the low order byte of the 16-bit timer base register. Writes to this register cause both timer base registers to be loaded into the internal timer; therefore, the upper timer register should be loaded before the lower. Once the count reaches zero, an interrupt is generated, if enabled, and the timer is automatically reloaded with these base registers.

Timer Upper Base (I21)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0

TU7-TU0 — Upper Timer Bits: This is the high order byte of the 16-bit timer. The time base is determined by the frequency base selected from either C2SL in I8 or CS2 in I22.

C2SL = 0 - 24.576MHz / 245 (9.969 µs)

C2SL = 1 - 16.9344MHz / 168 (9.92 µs)

Alternate Sample Frequency Select (I22)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
SRE	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	CS2

CS2 — Clock 2 Base Select. This bit selects the base clock frequency used for generating the audio sample rate. Note that the part uses only one crystal to generate both clock base frequencies. This bit can be disabled by setting IFSE in X11.

0 - 24.576 MHz base
1 - 16.9344 MHz base

DIV5 - DIV0 — Clock Divider. These bits select the audio sample frequency for both capture and playback. These bits can be overridden by IFSE in X11.

Fs = (2*XT)/(M*N)

XT = 24.576 MHz CS2 = 0
XT = 16.9344 MHz CS2 = 1

N = DIV5-DIV0
16 ≤ N ≤ 49 for XT = 24.576 MHz
12 ≤ N ≤ 33 for XT = 16.9344 MHz

(M set by OSM1,0 in I10)
M = 64 for Fs > 24 kHz
M = 128 for 12 kHz < Fs ≤ 24 kHz
M = 256 for Fs ≤ 12 kHz

SRE — Alternate Sample Rate Enable. When this bit is set to a one, bits 0-3 of I8 will be ignored, and the sample frequency is then determined by CS2, DIV5-DIV0, and the oversampling mode bits OSM1, OSM0 in I10. Note that this register can be overridden (disabled) by IFSE in X11.

Extended Register Access (I23)

Default = 00000xx0

D7	D6	D5	D4	D3	D2	D1	D0
XA3	XA2	XA1	XA0	XRAE	XA4	res	ACF

ACF — ADPCM Capture Freeze. When set, the capture ADPCM accumulator and step size are frozen. This bit must be set to zero for adaptation to continue. This bit is used when pausing a ADPCM capture stream.

res — Reserved. Must write 0. Could read as 0 or 1.

XA4 — Extended Register Address bit 4. Along with XA3-XA0, enables access to extended registers X16, X17, and X25. MODE 3 only.

XRAE — Extended Register Access Enable. Setting this bit converts this register from the extended address register to the extended data register. To convert back to an address register, R0 must be written. MODE 3 only.

XA3-XA0 — Extended Register Address. Along with XA4, sets the register number (X0-X17+X25) accessed when XRAE is set. MODE 3 only. See the *WSS Extended Register* section for more details.

Alternate Feature Status (I24)

Default = x0000000

D7	D6	D5	D4	D3	D2	D1	D0
res	TI	CI	PI	CU	CO	PO	PU

PU — Playback Underrun: When set, indicates the DAC has run out of data and a sample has been missed.

PO — Playback Overrun: When set, indicates that the host attempted to write data into a full FIFO and the data was discarded.

CO — Capture Overrun: When set, indicates that the ADC had a sample to load into the FIFO but the FIFO was full. In this case, this bit is set and the new sample is discarded.

CU — Capture Underrun: Indicates the host has read more data out of the FIFO than it contained. In this condition, the bit is set and the last valid byte is read by the host.

PI — Playback Interrupt: Indicates an interrupt is pending from the playback DMA count registers.

CI — Capture Interrupt: Indicates an interrupt is pending from the capture DMA count registers.

TI — Timer Interrupt: Indicates an interrupt is pending from the timer registers

res — Reserved. Must write 0. Could read as 0 or 1.

The PI, CI, and TI bits are reset by writing a "0" to the particular interrupt bit or by writing any value to the Status register (R2).

Compatibility ID (I25)

Default = 00000011

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	CID4	CID3	CID2	CID1	CID0

CID4-CID0 — Chip Identification. Distinguishes between this chip and previous codec chips that support this register set. This register is fixed to indicate code compatibility with the CS4236. X25 or C1 should be used to further differentiate between parts that are compatible with the CS4236.

All Chips:
00011 - CS4236, CS4236B
00010 - CS4232/CS4232A
00000 - CS4231/CS4231A

V2-V0 — Version number. As enhancements are made to the part, the version number is changed so software can distinguish between the different versions.

000 - Compatible with the CS4236

These bits are fixed for compatibility with the CS4236. Register X25 or C1 may be used to differentiate between the CS4236 and newer chips.

Mono Input and Output Control (I26)

Default = 101x0000

D7	D6	D5	D4	D3	D2	D1	D0
MIM	MOM	MBY	res	MIA3	MIA2	MIA1	MIA0

MIA3-MIA0 — Mono Input Attenuation. When MIM is 0, these bits set the level of MIN summed into the mixer. MIA0 is the least significant bit and represents 3 dB attenuation, with 0000 = 0 dB. See Table 7.

res — Reserved. Must write 0. Could read as 0 or 1.

MBY — Mono Bypass. MBY connects MIN directly to MOUT with an attenuation of 9 dB. When MBY = 1, MIM should be set to 1.

0 - MIN not connected directly to MOUT.
1 - MIN connected directly to MOUT.

MOM — Mono Output Mute. In MODE 3, MOM will mute the left Line Out to the mono mix output, MOUT. The right Line Out mute, MOMR, is in X5. In MODE 2, MOM mutes left and right Line Out to MOUT. This mute is independent of the line output mute.

0 - no mute
1 - mute

MIM — Mono Input Mute. In MODE 3, MIM mutes the MIN analog input to the left output mixer channel. MIMR in X4 mutes MIN analog input to the right output mixer channel. In MODE 2, MIM mutes both left and

right channels. The mono input provides mix for the "beeper" function in most personal computers.

0 - no mute
1 - muted

Reserved (I27)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Capture Data Format (I28)

Default = 0000xxxx

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

S/$\overline{M}$ — Stereo/Mono Select: This bit determines how the capture audio data stream is formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Selecting mono only captures data from the left audio channel. MCE (R0) or C$\overline{M}$CE (I16) must be set to modify S/$\overline{M}$. See *Changing Audio Data Formats* section for more details.

0 - Mono
1 - Stereo

C/L, FMT1, FMT0 set the capture data format in MODEs 2 and 3. See Table 11 or register I8 for the bit settings and data formats. The capture data format can be different than the playback data format; however, the sample frequency must be the same and is set in I8. MCE (R0) or CMCE (I16) must be set to modify this register. See *Changing Audio Data Formats* section for more details.

Reserved (I29)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Capture Upper Base (I30)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

CUB7-CUB0 — Capture Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Capture Base register. Reads from this this register returns the same value that was written.

Capture Lower Base (I31)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

CLB7-CLB0 — Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Capture Base register. Reads from this register returns the same value which was written.

WSS EXTENDED REGISTERS

The Windows Sound System codec contains three sets of registers: R0-R3, I0-I31, and X0-X25. R0-R3 are directly mapped to the ISA bus through WSSbase+0 through WSSbase+3 respectively. R0 and R1 provide access to the indirect registers I0-I31. The third set of registers are extended registers X0-X25 that are indirectly mapped through the WSS register I23. I23 acts as both the extended address and extended data register. These extended registers are only available when in MODE 3.

Accessing the X registers requires writing the register address to I23 with XRAE set. When XRAE is set, I23 changes from an address register to a data register. Subsequent accesses to I23 access the extended data register. To convert I23 back to the extended address register, R0 must be written which internally clears XRAE. Assuming the part is in MODE 3, the following steps access the X registers:

1. Write 17h to R0 (to access I23).
   R1 is now the extended **address register**.
2. Write the desired X register address to R1 with XRAE = 1.
   R1 is now the extended **data register**.
3. Write/Read X register data from R1.

To read/write a different X register:

4. Write 17h to R0 again. (resets XRAE)
   R1 is now the extended **address register**.
5. Write the new X register address to R1 with XRAE = 1.
   R1 is now the new extended **data register**.
6. Read/Write new X register data from R1.

Address	Reg.	Register Name
WSSbase+0	R0	Reset Address
WSSbase+1	R1	Address/Data access
	I23	Indexed Address/Data

Extended Register Access (I23)

D7	D6	D5	D4	D3	D2	D1	D0
XA3	XA2	XA1	XA0	XRAE	XA4	res	ACF

Table 16. WSS Extended Register Control

Index	Register Name
X0	Left LINE Alternate Volume
X1	Right LINE Alternate Volume
X2	Left MIC Volume
X3	Right MIC Volume
X4	Synthesis and Input Mixer Control
X5	Right Input Mixer Control
X6	Left FM Synthesis Volume
X7	Right FM Synthesis Volume
X8	Left DSP Serial Port Volume
X9	Right DSP Serial Port Volume
X10	Right Loopback Monitor Volume
X11	DAC Mute and IFSE Enable
X12	Independent ADC Sample Freq.
X13	Independent DAC Sample Freq.
X14	Left Master Digital Audio Volume
X15	Right Master Digital Audio Volume
X16	Left Wavetable Serial Port Volume
X17	Right Wavetable Serial Port Volume
X18-X24	Reserved
X25	Chip Version and ID

Table 17. WSS Extended Registers

Control Registers for the Extended Registers

ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
WSSbase+0	R0	INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0
WSSbase+1	R1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	I23	XA3	XA2	XA1	XA0	XRAE	XA4	-	ACF

Extended Registers: (X0-X17, X25)

XA4 - XA0	D7	D6	D5	D4	D3	D2	D1	D0
X0	LLAOM	LLAIM	LLABM	LLAG4	LLAG3	LLAG2	LLAG1	LLAG0
X1	RLAOM	RLAIM	RLABM	RLAG4	RLAG3	RLAG2	RLAG1	RLAG0
X2	LMIM	LMOM	LMBST	LMG4	LMG3	LMG2	LMG1	LMG0
X3	RMIM	RMOM	RMBST	RMG4	RMG3	RMG2	RMG1	RMG0
X4	MIMR	LIS1	LIS0	IFM	WTRMD	FMRM	-	-
X5	MOMR	RIS1	RIS0	-	-	-	-	-
X6	LFMM	-	LFMA5	LFMA4	LFMA3	LFMA2	LFMA1	LFMA0
X7	RFMM	-	RFMA5	RFMA4	RFMA3	RFMA2	RFMA1	RFMA0
X8	LSPM	-	LSPA5	LSPA4	LSPA3	LSPA2	LSPA1	LSPA0
X9	RSPM	-	RSPA5	RSPA4	RSPA3	RSPA2	RSPA1	RSPA0
X10	SLBE	-	RLBA5	RLBA4	RLBA3	RLBA2	RLBA1	RLBA0
X11	LDMIM	RDMIM	IFSE	-	-	-	-	-
X12	SRAD7	SRAD6	SRAD5	SRAD4	SRAD3	SRAD2	SRAD1	SRAD0
X13	SRDA7	SRDA6	SRDA5	SRDA4	SRDA3	SRDA2	SRDA1	SRDA0
X14	LDMOM	LDMG6	LDMG5	LDMG4	LDMG3	LDMG2	LDMG1	LDMG0
X15	RDMOM	RDMG6	RDMG5	RDMG4	RDMG3	RDMG2	RDMG1	RDMG0
X16	LWM	-	LWG5	LWG4	LWG3	LWG2	LWG1	LWG0
X17	RWM	-	RWG5	RWG4	RWG3	RWG2	RWG1	RWG0
X25	V2	V1	V0	CID4	CID3	CID2	CID1	CID0

Table 18. Extended Register Bit Summary

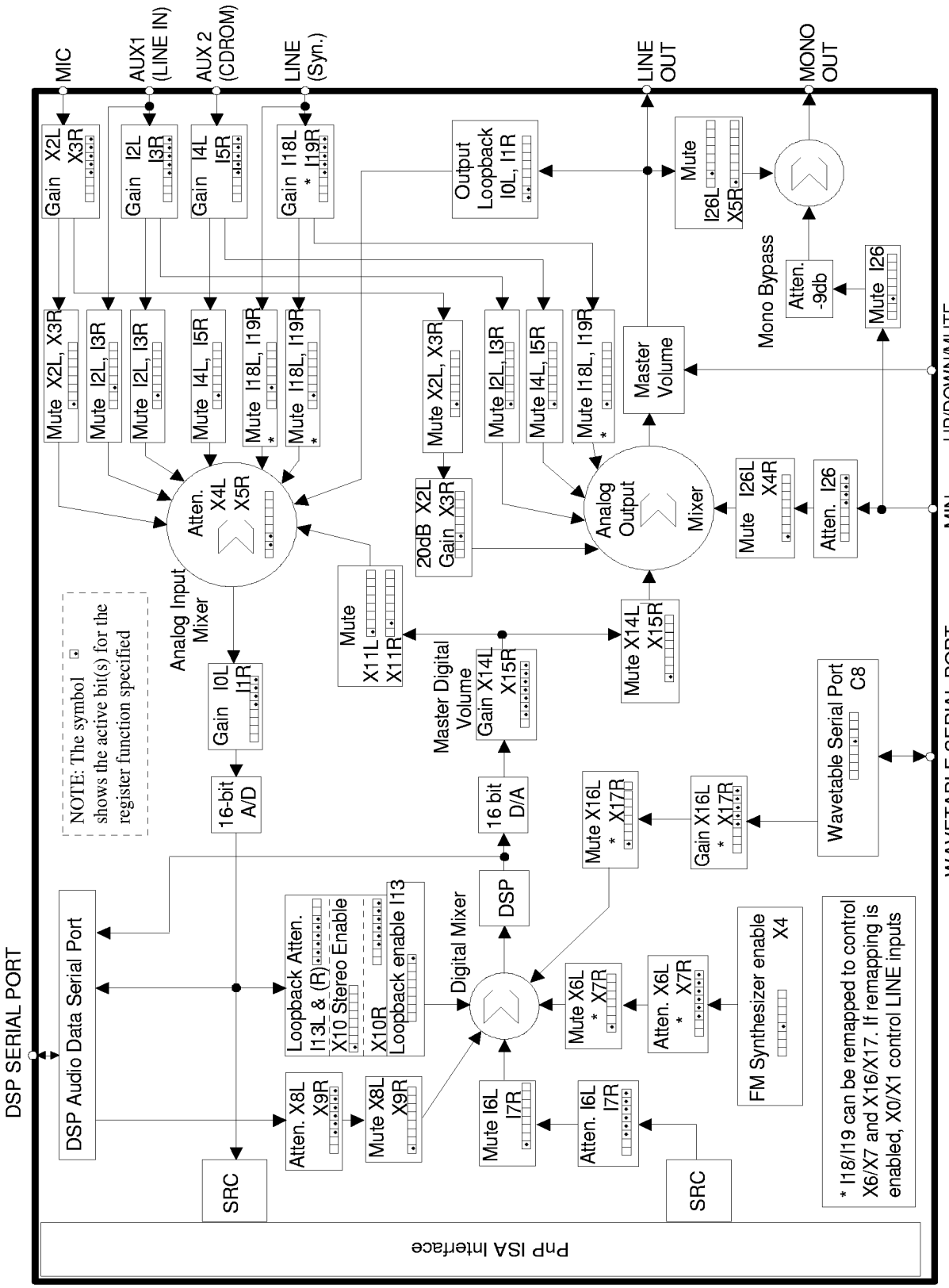


Figure 4. MODE 3 Mixer (assumes IFM or WTEN is set)

Left LINE Alternate Volume (X0)

Default = 11101000

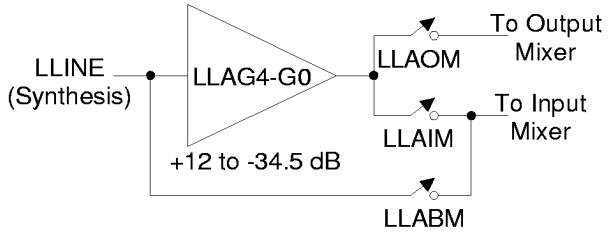
D7	D6	D5	D4	D3	D2	D1	D0
LLAOM	LLAIM	LLBAM	LLAG4	LLAG3	LLAG2	LLAG1	LLAG0

LLAG4-LLAG0 Left LINE Alternate Volume. This register is used to control the LLINE analog input volume to the mixers when I18 is remapped to control FM and/or Wavetable Serial Port volume. The remapping bits are FMRM and WTRMD (X4). The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

LLABM Left LINE Alternate Bypass Mute. When set to 1, the analog Left Line Input, LLINE, (bypassing the gain block) to the input mixer is muted.

LLAIM Left LINE Alternate Input Mute. When set to 1, the Left Line Input, LLINE, from the volume control to the input mixer is muted.

LAOM Left LINE Alternate Output Mute. When set to 1, the Left Line Input, LLINE, from the volume control to the output mixer is muted.



Right LINE Alternate Volume (X1)

Default = 11101000

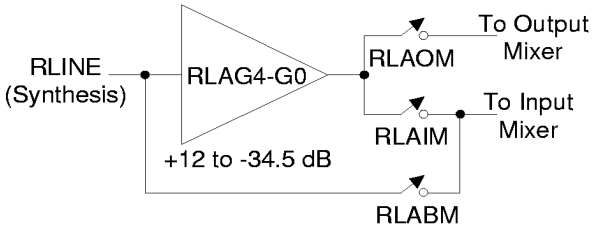
D7	D6	D5	D4	D3	D2	D1	D0
RLAOM	RLAIM	RLABM	RLAG4	RLAG3	RLAG2	RLAG1	RLAG0

RLAG4-RLAG0 Right LINE Alternate Volume. This register is used to control the RLINE analog input volume to the mixers when I19 is remapped to control FM and/or Wavetable Serial Port volume. The remapping bits are FMRM and WTRMD in X4. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 10.

RLABM Right LINE Alternate Bypass Mute. When set to 1, the analog Right Line Input, RLINE, (bypassing the gain block) to the input mixer is muted.

RLAIM Right LINE Alternate Input Mute. When set to 1, the Right Line Input, RLINE, from the volume control to the input mixer is muted.

RLAOM Right LINE Alternate Output Mute. When set to 1, the Right Line Input, RLINE, from the volume control to the output mixer is muted.



Left MIC Volume (X2)

Default = 11001111

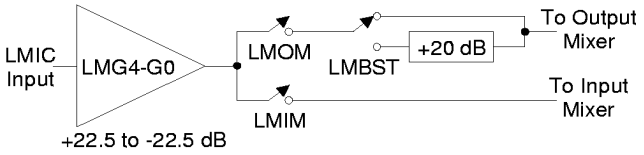
D7	D6	D5	D4	D3	D2	D1	D0
LMIM	LMOM	LMBST	LMG4	LMG3	LMG2	LMG1	LMG0

LMG4-LMG0 Left Microphone Gain. The least significant bit represents 1.5 dB, with 01111 = 0 dB. See Table 13.

LMBST Left Microphone 20 dB boost. When set to 1, the signal to the output mixer is given a 20 dB boost.

LMOM Left Microphone Output Mixer Mute. When set to 1, the signal to the output mixer is muted.

LMIM Left Microphone Input Mixer Mute. When set to 1, the signal to the input mixer is muted.



Right MIC Volume (X3)

Default = 11001111

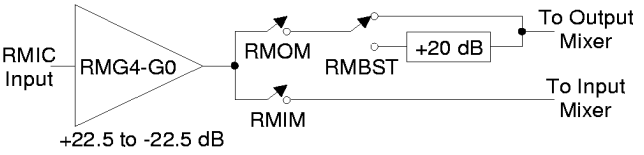
D7	D6	D5	D4	D3	D2	D1	D0
RMIM	RMOM	RMBST	RMG4	RMG3	RMG2	RMG1	RMG0

RMG4-RMG0 Right Microphone gain. The least significant bit represents 1.5 dB, with 01111 = 0 dB. See Table 13.

RMBST Right Microphone 20 dB boost. When set to 1, the signal to the output mixer is given a 20 dB boost.

RMOM Right Microphone Output Mixer Mute. When set to 1, the signal to the output mixer is muted.

RMIM Right Microphone Input Mixer Mute. When set to 1, the signal to the input mixer is muted.



Synthesis and Input Mixer Control (X4)

Default = 100001xx

D7	D6	D5	D4	D3	D2	D1	D0
MIMR	LIS1	LIS0	IFM	WTRMD	FMRM	res	res

res Reserved. Must write 0. Could be read as 0 or 1.

FMRM FM Volume Control Remap. This bit only functions when IFM = 1.

If FMRM = 1, internal FM Synthesis volume is controlled by I18/I19 (writes to I18/I19 get remapped to X6/X7). Analog LINE volume is controlled by X0/X1.

If FMRM = 0, internal FM synthesis volume is controlled by X6/X7 only.

WTRMD WaveTable Volume Remap Disable. This bit only functions when WTEN = 1 (C8/Global Config. byte).

If WTRMD = 0, the Wavetable Serial Port volume is controlled by I18/I19 (writes to I18/I19 get remapped to X16/X17). Analog LINE volume is controlled by X0/X1.

If WTRMD = 1, the Wavetable Serial Port volume is controlled by X16/X17 only.

NOTE: If FMRM = 1, and WTRMD = 0, I18/I19 control both internal FM and Wavetable Serial Port volume.

IFM Internal FM enable. When set to 1, the internal FM synthesis engine is enabled. Setting this bit also changes I6/7 from the master digital audio volume to the ISA bus wave volume control. X14/15 becomes the

master digital audio volume. This bit can be set through the Hardware Configuration data in the EEPROM.

LIS1-LIS0 Left Input Mixer Summer Attenuator. This attenuates the inputs to the left input mixer to enable overload protection when multiple input sources are utilized. The least significant bit represents 6 dB of attenuation, where 00 yields 0 dB of attenuation. See Table 8.

MIMR Mono Input Mute to the Right Output mixer. When set to 1, the MIN signal to the right output mixer is muted.

Right Input Mixer Control (X5)

Default = 000xxxxx

D7	D6	D5	D4	D3	D2	D1	D0
MOMR	RIS1	RIS0	res	res	res	res	res

res Reserved. Must write 0. Could be read as 0 or 1.

RIS1-RIS0 Right Input Mixer Summer Attenuator. This attenuates the inputs to the right input mixer to enable overload protection when multiple input sources are utilized. The least significant bit represents 6 dB of attenuation, where 00 yields 0 dB of attenuation. See Table 8.

MOMR Mono Output Mute from the Right Line Out, ROUT, to the mono output mixer. When set to 1, the signal to the mono output mixer from the Right Line Out is muted.

Left FM Synthesis Volume (X6)

Default = 1x000000

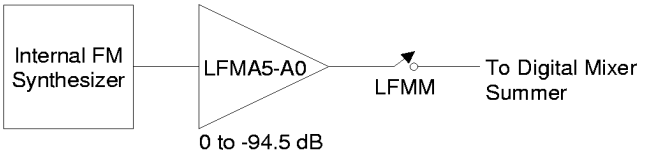
D7	D6	D5	D4	D3	D2	D1	D0
LFMM	res	LFMA5	LFMA4	LFMA3	LFMA2	LFMA1	LFMA0

NOTE: This FM volume register can also be controlled through I18 when IFM = 1 and FMRM = 1.

LFMA5-LFMA0 Left Internal FM Synthesis Volume. The least significant bit represents 1.5 dB, with 000000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

LFMM Left FM mute. When set to 1, the left internal FM input to the digital mixer is muted.



Right FM Synthesis Volume (X7)

Default = 1x000000

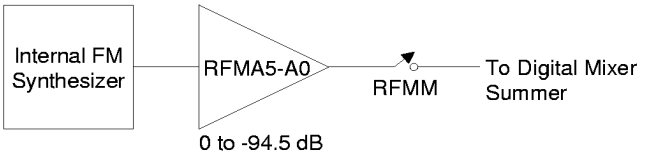
D7	D6	D5	D4	D3	D2	D1	D0
RFMM	res	RFMA5	RFMA4	RFMA3	RFMA2	RFMA1	RFMA0

NOTE: This FM volume register can also be controlled through I19 when IFM = 1 and FMRM = 1.

RFMA5-RFMA0 Right Internal FM Synthesis Volume. The least significant bit represents 1.5 dB, with 000000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

RFMM Right FM mute. When set to 1, the right internal FM input to the digital mixer is muted.



Left DSP Serial Port Volume (X8)

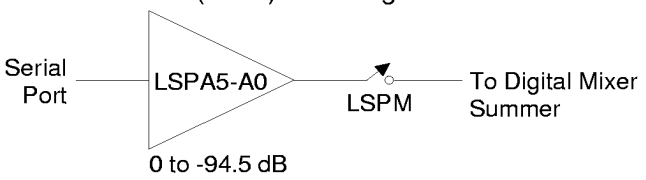
Default = 0x000000

D7	D6	D5	D4	D3	D2	D1	D0
LSPM	res	LSPA5	LSPA4	LSPA3	LSPA2	LSPA1	LSPA0

LSPA4-LSPA0 Left DSP Serial Port Attenuation. The least significant bit represents 1.5 dB, with 000000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

LSPM Left DSP Serial Port Mute. When set to 1, the Left DSP Serial Port input (SDIN) to the digital mixer is muted.



Right DSP Serial Port Volume (X9)

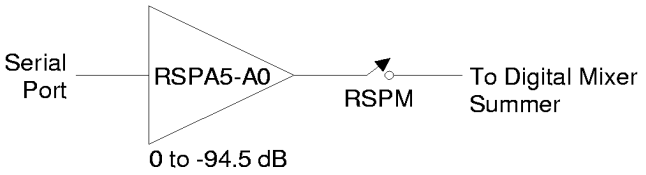
Default = 0x000000

D7	D6	D5	D4	D3	D2	D1	D0
RSPM	res	RSPA5	RSPA4	RSPA3	RSPA2	RSPA1	RSPA0

RSPA4-RSPA0 Right DSP Serial Port Attenuation. The least significant bit represents 1.5 dB, with 000000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

RSPM Right DSP Serial Port Mute. When set to 1, the Right DSP Serial Port input (SDIN) to the digital mixer is muted.



Right Loopback Monitor Volume (X10)

Default = 0x111111

D7	D6	D5	D4	D3	D2	D1	D0
SLBE	res	RLBA5	RLBA4	RLBA3	RLBA2	RLBA1	RLBA0

RLBA5-RLBA0 Right Channel Loopback Attenuation. These bits determine the attenuation of the loopback from the right ADC to the right digital mixer. LBE in I13 must be set to enable loopback. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

SLBE Stereo LoopBack Enable. When set to 1, control over the Left and Right loopback volume is separated. RLBA5-RLBA0 (X10) control the Right channel, and LBA5-LBA0 (I13) control the Left channel. When set to 0, LBA5-LBA0 (I13) control both channels.

DAC Mute and IFSE Enable (X11)

Default = 110xxxxx

D7	D6	D5	D4	D3	D2	D1	D0
LDMIM	RDMIM	IFSE	res	res	res	res	res

res Reserved. Must write 0. Could read as 0 or 1.

IFSE Independent Sample Freq. Enable. When set to 1, the extended registers X12 and X13 are used to set the sample rate, and registers I8, I10 (OSM1,0), and I22 are ignored. X12 and X13 cannot be modified unless this bit is set to 1.

RDMIM Right Digital Master Input Mixer Mute. When set to 1, the output from the Right DAC is Muted to the Right input mixer. See Figure 4.

LDMIM Left Digital Master Input Mixer Mute. When set to 1, the output from the Left DAC is Muted to the Left input mixer. See Figure 4.

Independent ADC Fs (X12)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
SRAD7	SRAD6	SRAD5	SRAD4	SRAD3	SRAD2	SRAD1	SRAD0

SRAD7-SRAD0 Sample Rate frequency select for the A/D converter. This register is only in effect (and can only be written) while IFSE=1 in X11. See Table 14.

Independent DAC Fs (X13)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
SRDA7	SRDA6	SRDA5	SRDA4	SRDA3	SRDA2	SRDA1	SRDA0

SRDA7-SRDA0 Sample Rate frequency select for the D/A converter. This register is only in effect (and can only be written) while IFSE=1 in X11. See Table 15.

Left Master Digital Audio Volume (X14)

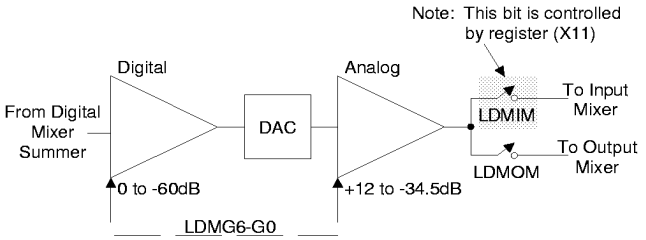
Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
LDMOM	LDMG6	LDMG5	LDMG4	LDMG3	LDMG2	LDMG1	LDMG0

This register becomes the master digital audio volume control for the left channel when either IFM or WTEN is set to one.

LDMG6-LDMG0 Left Digital Master Mixer Attenuation. The least significant bit represents 1.5 dB, with 000000 = 0 dB. See Table 12.

LDMOM Left Digital Master Output Mixer Mute. When set to 1, the output of the Left DAC is muted to the Left output mixer.



Right Master Digital Audio Volume (X15)

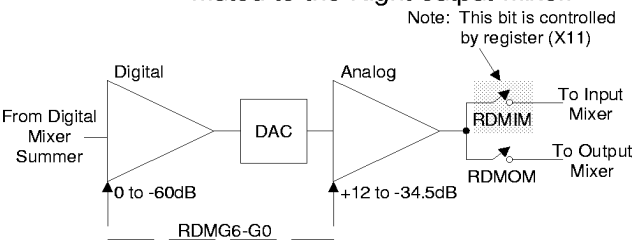
Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
RDMOM	RDMG6	RDMG5	RDMG4	RDMG3	RDMG2	RDMG1	RDMG0

This register becomes the master digital audio volume control for the left channel when either IFM or WTEN is set to one.

RDMG6-RDMG0 Right Digital Master Mixer Attenuation. The least significant bit represents 1.5 dB, with 000000 = 0 dB. See Table 12.

RDMOM Right Digital Master Output Mixer Mute. When set, the Right DAC output is muted to the Right output mixer.



Left Wavetable Serial Port Volume (X16)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
LWM	res	LWG5	LWG4	LWG3	LWG2	LWG1	LWG0

This Wavetable volume register can also be controlled through I18 when WTEN=1 (C8 or Global Config. byte) & WTRMD=0 (X4).

LWG5-LWG0 Left Wavetable Serial Port Gain. Least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

LWM Left Wavetable Serial Port Mute. When set, the Left Wavetable Serial Input to the digital mixer is muted.

Right Wavetable Serial Port Volume (X17)

Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
RWM	res	RWG5	RWG4	RWG3	RWG2	RWG1	RWG0

This Wavetable volume register can also be controlled through I19 when WTEN=1 (C8 or Global Config. byte) & WTRMD=0 (X4).

RWG5-RWG0 Right Wavetable Serial Port Gain. Least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 6.

res Reserved. Must write 0. Could read as 0 or 1.

RWM Right Wavetable Serial Port Mute. When set, the Right Wavetable Serial Input to the digital mixer is muted.

Chip Version and ID (X25)

Default = 11001011

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	CID4	CID3	CID2	CID1	CID0

This register was added to Revision C silicon. In revision B, this register read 0x00.

CID5-CID0 Chip Identification. Distinguishes between this chip and other codec chips that support this register set. This register is identical to C1 and replaces the ID register in I25.

00000 - CS4236B, Revision B
01011 - CS4236B

V2-V0 Version Number. As enhancements are made, the version number is changed so software can distinguish between the different versions of the same chip.

000 - Revision B
110 - Revision C/D
111 - Revision E

SOUND BLASTER INTERFACE

The Sound Blaster Pro compatible interface is the third physical device in logical device 0. Since the WSS Codec and the Sound Blaster are mutually exclusive, the WSS Codec interrupt and playback DMA channel are shared with the Sound Blaster interface. To map volume controls properly, the external devices: synthesizer (when used), CDROM, etc., must be connected to the proper analog inputs as illustrated in Figure 5.

Mode Switching

To facilitate switching between different functional modes (i.e. Sound Blaster and Windows Sound System), logic is included to handle the switch transparently to the host. No special software is required on the host side to perform the mode switch.

Sound Blaster Direct Register Interface

The Sound Blaster software interface utilizes 10-bit address decoding and is compatible with Sound Blaster and Sound Blaster Pro interfaces. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. This device requires 16 I/O locations located at the PnP address 'SBbase'. The following registers, shown in Table 19, are provided for Sound Blaster compatibility.

Left/Right FM Registers,
SBbase+0 - SBbase+3
These registers are mapped directly to the appropriate FM synthesizer registers.

Mixer Address Register,
SBbase+4, write only
This register is used to specify the index address for the mixer. This register must be written before any data is accessed from the mixer registers. The mixer indirect register map is shown in Table 20.

Address	Description	Type
SBbase+0	Left FM Status Port	Read
SBbase+0	Left FM Register Status Port	Write
SBbase+1	Left FM Data Port	Write Only
SBbase+2	Right FM Status Port	Read
SBbase+2	Right FM Register Status Port	Write
SBbase+3	Right FM Status Port	Write Only
SBbase+4	Mixer Register Address	Write Only
SBbase+5	Mixer Data Port	Read/Write
SBbase+6	Reset	Write Only
SBbase+8	FM Status Port	Read Only
SBbase+8	FM Register port	Write
SBbase+9	FM Data Port	Write Only
SBbase+A	Read Data Port	Read Only
SBbase+C	Command/Write Data	Write
SBbase+C	Write Buffer Status (Bit 7)	Read
SBbase+E	Data Available Status (Bit 7)	Read

Table 19. Sound Blaster Pro Compatible I/O Interface

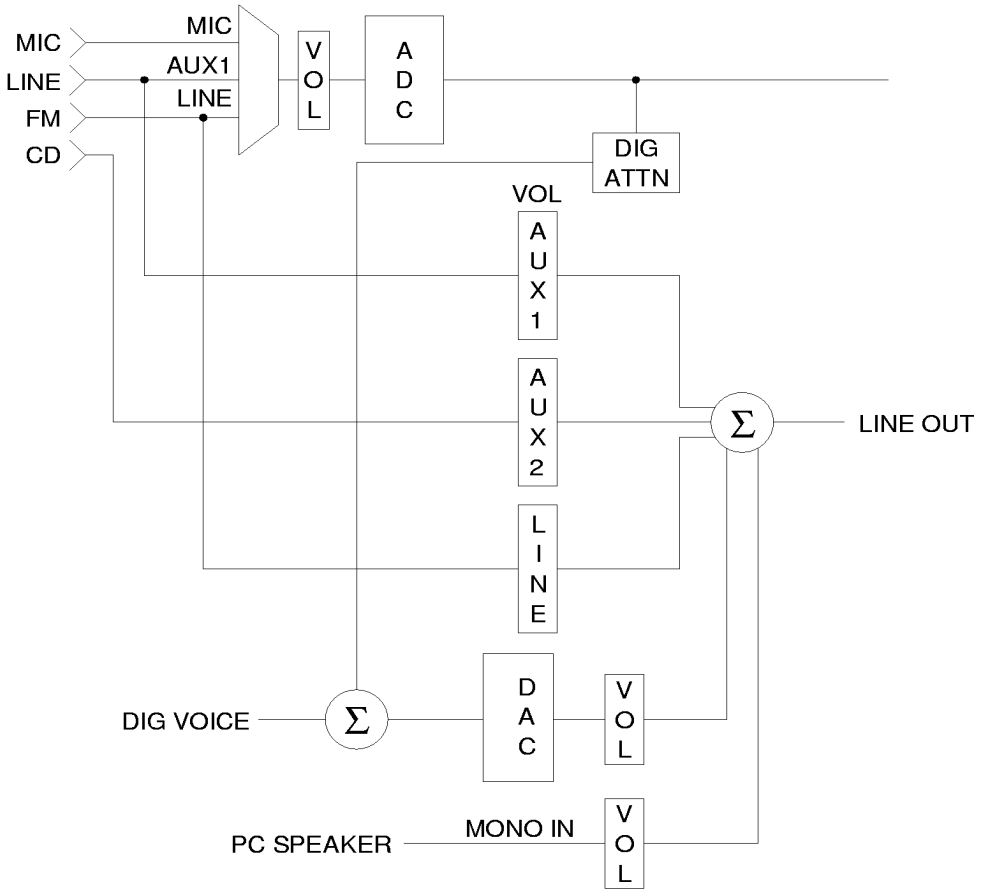


Figure 5. SBPro Mixer Mapping

Register	D7	D6	D5	D4	D3	D2	D1	D0
00H	DATA RESET							
02H	RESERVED							
04H	VOICE VOLUME LEFT				VOICE VOLUME RIGHT			
06H	RESERVED							
08H	RESERVED							
0AH	X	X	X	X	X	MIC MIXING		
0CH	X	X	X			INPUT SELECT		X
0EH	X	X	X	X	X	X	VSTC	X
20H	RESERVED							
22H	MASTER VOLUME LEFT				MASTER VOLUME RIGHT			
24H	RESERVED							
26H	FM VOLUME LEFT				FM VOLUME RIGHT			
28H	CD VOLUME LEFT				CD VOLUME RIGHT			
2AH	RESERVED							
2CH	RESERVED							
2EH	LINE VOLUME LEFT				LINE VOLUME RIGHT			

Table 20. SBPro Compatible Mixer Interface

Mixer Data Register,
SBbase+5
This register provides read/write access to a particular mixer register depending on the index address specified in the Mixer Address Register.

Reset
SBbase+6, write only
When bit D[0] of this register is set to a one and then set to a zero, a reset of the Sound Blaster interface will occur.

Read Data Port
SBbase+A, read only
When bit D[7] of the Data Available Register, SBbase+E, is set =1 then valid data is available in this register. The data may be the result of a Command that was previously written to the Command/Write Data Register or digital audio data.

Command/Write Data
SBbase+C, write only
The Command/Write Data register is used to send Sound Blaster Pro commands.

Write Buffer Status,
SBbase+C, read only
The Write Buffer Status register bit D[7] indicates when the SBPro interface is ready to accept another command to the Command/Write Data register. D[7]=1 indicates ready. D[7]=0 indicates not ready.

Sound Blaster Mixer Registers

The Sound Blaster mixer registers are shown in Table 20. The Sound Blaster mixer to WSS Codec mixer mapping is shown in Figure 5.

Reset Register,
Mixer Index 00H
Writing any value to this register will reset the mixer to default values.

Voice Volume Register,
Mixer Index 04H, Default = 99H
This register provides 8 steps of voice volume control each for the right and left channels.

Microphone Mixing Register,
Mixer Index 0AH, Default = 01H
This register provides 4 steps of microphone volume control.

Input Control Register,
Mixer Index 0CH
This register selects the input source to the ADC.

D2,D1 - 00 - Microphone
01 - CD Audio
10 - Microphone
11 - Line In

Output Control Register,
Mixer Index 0EH

VSTC - 0 - Mono Mode
1 - Stereo Mode

Master Volume Register,
Mixer Index 22H, Default = 99H
This register provides 8 steps of master volume control each for the right and left channels.

FM Volume Register,
Mixer Index 26H, Default = 99H
This register provides 8 steps of FM volume control each for the right and left channels.

CD Volume Register,
Mixer Index 28H, Default = 01H
This register provides 8 steps of CD volume control each for the right and left channels.

Line-In Volume Register,
Mixer Index 2EH, Default = 01H
This register provides 8 steps of line-in volume control each for the right and left channels.

GAME PORT INTERFACE

The Game Port logical device software interface utilizes 10-bit address decoding and is located at PnP address 'GAMEbase'. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. For backwards compatibility, the Game Port consists of 8 I/O locations where the lower 6 alias to the same location, which consists of one read and one write register.

Plug and Play configuration capability will allow the joystick I/O base address, GAMEbase, to be located anywhere within the host I/O address space. Currently most games software assume that the joystick I/O port is located at 200h.

A write to the GAMEbase register triggers four timers. A read from the same register returns four status bits corresponding to the joystick fire buttons and four bits that correspond to the output from the four timers.

A button value of 0 indicates the button is pressed or active. The button default state is 1. When GAMEbase is written, the X/Y timer bits go high. Once GAMEbase is written, each timer output remains high for a period of time determined by the current joystick position. The number in parenthesis below is the joystick connector pin number.

GAMEbase+0 - GAMEbase+5

D7	D6	D5	D4	D3	D2	D1	D0
JBB2	JBB1	JAB2	JAB1	JBCY	JBCX	JACY	JACX

JACX Joystick A, Coordinate X (pin 3)

JACY Joystick A, Coordinate Y (pin 6)

JBCX Joystick B, Coordinate X (pin 11)

JBCY Joystick B, Coordinate Y (pin 13)

JAB1 Joystick A, Button 1 (pin 2)

JAB2 Joystick A, Button 2 (pin 7)

JBB1 Joystick B, Button 1 (pin 10)

JBB2 Joystick B, Button 2 (pin 14)

Two bits, JR1 and JR0, are located in the Control register space (CTRLbase+0) for defining the speed of the Game Port Interface. Four different rates are software selectable for use with various joysticks and to support older software timing loops with aliasing (roll-over) problems.

GAMEbase+6

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res Must not write any value to this register. May read any value.

GAMEbase+7

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res Must not write any value to this register. May read any value.

The Game Port hardware interface consists of 8 pins that connect directly to the standard game port connector. Buttons must have a 4.7 kΩ pullup resistor and a 1000 pF capacitor to ground. X/Y coordinates must have a 5.6 nF capacitor to ground and a 2.2 kΩ series resistor to the appropriate joystick connector pin. For a detailed hardware description, see the *Reference Design* Data Sheet.

CONTROL INTERFACE

The Control logical device includes registers for controlling various functions of the part that are not included in the other logical device blocks. These functions include game port rate control and programmable power management, as well as extra mixing functions.

Control Register Interface

The Control logical device software interface occupies 8 I/O locations, utilizes 12-bit address decoding, and is located at PnP address 'CTRLbase'. If the upper address bits, SA12-SA15 are used, they must be 0 to decode a valid address. This device can also support an interrupt. Table 21 lists the eight Control registers.

Address	Register
CTRLbase+0	Joystick & Power Control
CTRLbase+1	E^2PROM Interface
CTRLbase+2	Block Power Down
CTRLbase+3	Control Indirect Address Reg.
CTRLbase+4	Control Indirect Data Register
CTRLbase+5	Control/RAM Access
CTRLbase+6	RAM Access End
CTRLbase+7	Global Status

Table 21. Control Logical Device Registers

Joystick and Power Control
CTRLbase + 0, Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PM1	PM0	CONSW	PDC	PDP	PDM	JR1	JR0

JR1,0 — Joystick rate control. Selects operating speed of the joystick (changes the trigger threshold for the X/Y coordinates).

00 - slowest speed
01 - medium slow speed
10 - medium fast speed
11 - fastest speed

PDM — Power Down Mixer. When set, the analog mixer is powered down and all mixer control registers (in WSSbase space) are reset to default values.

PDP* — Power Down Processor. When set, places the internal processor in an idle state. This effects the PnP interface, MPU-401, and SBPro devices.

PDC* — Power Down Codec. When set, ADCs and DACs are powered down.

CONSW — controls host interrupt generation when a context switch occurs

0 - no interrupt on context switch
1 - Control interrupt generated on context switch

PM1,0 — Power Management. These bits are provided for backwards compatibility. For new designs, the bits in CTRLbase+2 should be used.

00 - All functions active.
01 - A/D and D/A powered down. Mixer still active, but volume registers are frozen. Disables PDC and PDM bits.
10 - Full part power down. All functions are disabled except reads and writes to this register. All internal logic, including PnP config. registers are reset. To exit this power-down mode, PM1/0 must be reset, through CTRLbase+0, and then the entire chip must be reinitialized.
11* - WSS Codec, SBPro, MPU-401, and PnP interfaces, and the analog mixer are powered down.

* NOTE: The SBPro, PnP, and MPU-401 interfaces are linked together. Setting PM1,0 or PDP will power all three interfaces down; however, if any one of the interfaces is written to, they will all power back up automatically. PM1,0 and PDP always reflects the value written, not whether the three devices are powered up or not.

E^2PROM Interface
CTRLbase+1, Default = 10000000

D7	D6	D5	D4	D3	D2	D1	D0
ICH	ISH	ADC1	ADC0	IMH	DIN/ EEN	DOUT	CLK

CLK — This bit is used to generate the clock for the Plug and Play E^2PROM. EEN must be set to 1 to make this bit operational.

DOUT — This bit is used to output serial data to the Plug and Play E^2PROM. EEN must be set to 1 to make this bit operational.

DIN/EEN — When read (DIN), this bit reflects the XD0 pin, which should be serial data output from the Plug and Play E^2PROM. EEN and DOUT must be 1 for this bit to function.

When written (EEN), enables the E^2PROM interface: CLK and DOUT onto the peripheral port pins. Writing:

0 - E^2PROM interface disabled
1 - E^2PROM interface enabled

IMH* — Interrupt polarity - Modem. When set, the MINT pin is an active high signal. When low, MINT is an active low signal.

ADC1,0 — These two bits are used to control an additional A/D mux and enable for an analog loopback path. These two mixing paths provide Karaoke support. These bits are provided for backwards compatibility. New software should use the MIC volume control in MODE 3 registers X2/X3 to support MIC mix to the output mixer. See Figure 6.

00 - Normal. A/D input from the input mux.
01 - Codec Input mux is mixed into output mixer. A/D input is from the input mux. This facilitates the Mic mixed to output, but only Mic recorded.
10 - Codec Input mux is mixed into output mixer. A/D input is from line outputs. This facilitates the Mic mixed to output, and the output recorded by the ADCs.
11 - reserved.

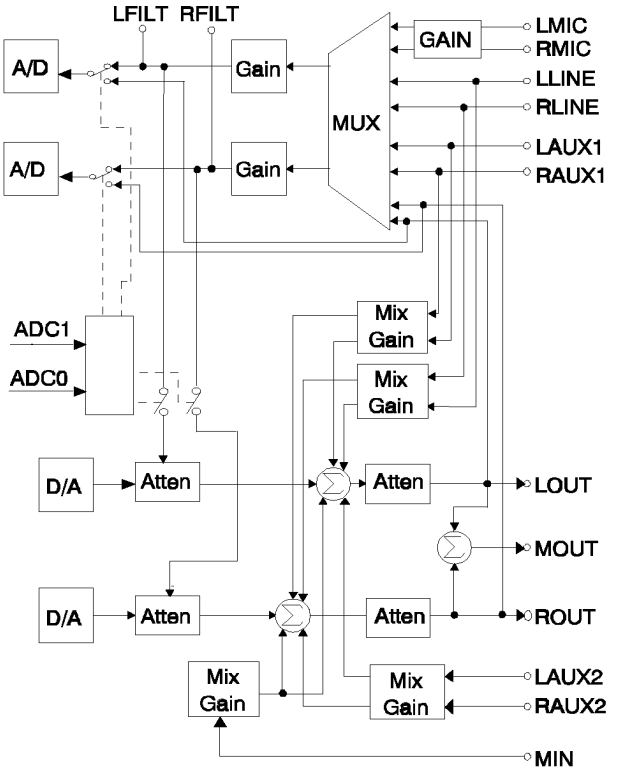


Figure 6. MODE 2 Mixer Addition

ISH* — Interrupt polarity - External Synthesizer. When set, the $\overline{\text{SINT}}$ pin is an active high signal. When low, $\overline{\text{SINT}}$ is an active low signal.

ICH* — Interrupt polarity - CDROM. When set, the CDINT pin is an active high signal. When low, CDINT is an active low signal.

* Note: These bits can be initialized through the Hardware Configuration data.

Block Power Down

CTRLbase+2, Default = 00000000

D7	D6	D5	D4	D3	D2	D1	D0
PDWN	SRC	VREF	MIX	ADC	DAC	PROC	FM

FM — Internal FM synthesizer powered down when set.

PROC — Processor set to idle mode. When set, places the internal processor in an idle state. This effects the PnP interface, MPU401, and SBPro devices. Any command to any one of these interfaces will cause the processor to go active.

DAC — DAC power down. When set, powers down the D/A converters, serial ports, and internal FM synthesizer. The DACs should be muted prior to setting this bit to prevent audible pops.

ADC — ADC power down. When set, powers down the A/D Converters.

MIX — Mixer power down. All analog input and output channels are powered down, except MIN and MOUT (assuming VREF is not powered down). If MIX is 1 and VREF is 0, the MBY bit in the WSS I26 register is forced on. The outputs should be muted prior to setting this bit to prevent audible pops.

VREF — VREF power down. When set, powers down the entire mixer. Since powering down VREF, powers down the entire analog section, some audible pops can occur.

SRC — Internal Sample-Rate Converters are powered down. Only 44.1 kHz sample frequency is allowed when this bit is set.

PDWN — Global Power Down. When set, the entire chip is powered down, except reads and writes to this register. When this bit is cleared, a full calibration is initiated. All registers retain their values; therefore, normal operation can resume after calibration is completed. When clearing this bit, the internal processor stays in power-down until accesses occur to processor interface (Sound Blaster, MPU, or PnP accesses). If hardware volume control is enabled, this bit should be written to 0 twice causing the processor to go active (which reenables the hardware volume).

NOTE: Software should mute the DACs and Mixers and FM volume when asserting any power down modes to prevent clicks and pops.

Control Indirect Address Register

CTRLbase+3

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	CA3	CA2	CA1	CA0

CA3-CA0 — Address bits to access the Control Indirect registers C0-C8 through CTRLbase+4

res — Reserved. Could read as 0 or 1. Must write as 0.

Control Indirect Data Register

CTRLbase+4

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 — Control Indirect Data register. This register provides access to the indirect registers C0-C8, where CTRLbase+3 selects the actual register. See the *Control Indirect Register* section for more details.

Control/RAM Access

CTRLbase+5, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

CR7-CR0 This register controls the loading of the part's internal RAM. RAM support includes hardware configuration and PnP default resource data, as well as program memory. See the *Hostload Procedure* section for more information. Commands are followed by address and data information.

Commands:
- 0x55 - Disable PnP Key
- 0x56 - Disable Crystal Key
- 0x57 - Jump to ROM
- 0x5A - Update Hardware Configuration Data.
- 0xAA - Download RAM. Address followed by data. (Stopped by writing 0 to CTRLbase+6)

RAM Access End

CTRLbase+6, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

RE7-RE0 A 0 written to this location resets the previous location, CTRLbase+5, from data download mode to command mode.

Global Status

CTRLbase+7, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
CWSS	ICTRL	ISB	IWSS	IMPU	res	res	res

res Reserved. Could read as 0 or 1.

IMPU MPU-401 Interrupt status.

0 - no interrupt pending
1 - an interrupt is pending

IWSS Windows Sound System Interrupt status.

0 - no interrupt pending
1 - an interrupt is pending

ISB Sound Blaster Interrupt status.

0 - no interrupt pending
1 - an interrupt is pending

ICTRL Control Logical Device 2 Interrupt status. Interrupts are generated on a context switch between WSS and SBPro modes.

0 - no interrupt pending
1 - an interrupt is pending

CWSS Context - WSS. Indicates the current context.

0 - Sound Blaster Emulation
1 - Windows Sound System

Control Indirect Registers

The Control Indirect registers are accessed through CTRLbase+3 and CTRLbase+4. CTRLbase+3 is the address register and CTRLbase+4 is the data register used to access C0 through C8 indirect registers. Currently, only C0, C1, and C8 are defined.

Address	Register Name
CTRLbase+3	Control Indirect Address
CTRLbase+4	Control Indirect Data

Table 22. Control Indirect Access Registers

Index	Register Name
C0	WSS Master Control
C1	Version / Chip ID
C2	Reserved
C3	Reserved
C4	Reserved
C5	Reserved
C6	Reserved
C7	Reserved
C8	CS9236 Wavetable Control

Table 23. Control Indirect Registers

WSS Master Control (C0)

Default = 0xxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RWSS	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

RWSS — Reset WSS registers. Setting this bit forces the WSS registers to zero, then clearing this bit forces the WSS registers to their default state.

Version / Chip ID (C1)

Default = 11001011

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	CID4	CID3	CID2	CID1	CID0

CID4-CID0 — Chip Identification. Distinguishes between this chip and other codec chips that support this register set. This register is identical to the WSS X25 register.

01011 - CS4236B

V2-V0 — Version number. As enhancements are made, the version number is changed so software can distinguish between the different versions of the same chip.

101 - Revision B
110 - Revision C/D
111 - Revision E

Reserved (C2)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Reserved (C3)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Reserved (C4)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Reserved (C5)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Reserved (C6)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

Reserved (C7)

Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

res — Reserved. Must write 0. Could read as 0 or 1.

CS9236 Wavetable Control (C8)

Default = xxxx0000

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	WTEN	SPS	DMCLK	BRES

BRES — Force $\overline{\text{BRESET}}$ low. When set, the $\overline{\text{BRESET}}$ pin is forced low. Typically used for power management of peripheral devices.

DMCLK — Disable MCLK. When set, the MCLK pin of the CS9236 Wavetable Synthesizer serial interface is forced low providing a power savings mode.

SPS — DSP Serial Port Switch. When set, switches the DSP serial port pins from the 2nd joystick to the XD4-XD1 pins. When SPE in I16 is set, XD4-XD1 convert to the DSP serial port pins. Once SPS is enabled, the SD<7:0> bus will not be driven when accesses occur to peripheral port devices. SPS can also be set in the E^2PROM Hardware Configuration data, Global Configuration byte.

WTEN — WaveTable Serial Port Enable. When, set, forces XD7-XD5 pins to convert to the CS9236 Single-Chip Wavetable Music Synthesizer serial port pins. Once WTEN is enabled, the SD<7:0> bus will not be driven when accesses occur to peripheral port devices. WTEN can also be set in the E^2PROM Hardware Configuration data, Global Configuration byte. Setting this bit also changes I6/I7 from the master digital audio volume to the ISA bus wave volume control. X14/15 becomes the master digital audio volume.

res — Reserved. Must write 0. Could read as 0 or 1.

MPU-401 INTERFACE

The MPU-401 is an intelligent MIDI interface that was introduced by Roland in 1984. Voyetra Technologies subsequently introduced an IBM-PC plug in card that incorporated the MPU-401 functionality. The MPU-401 has become the de-facto standard for controlling MIDI devices via IBM-PC compatible personal computers.

Although the MPU-401 does have some intelligence, a non-intelligent mode is available in which the MPU-401 operates as a basic UART.

By incorporating hardware to emulate the MPU-401 in UART mode, MIDI capability is supported.

MPU-401 Register Interface

The MPU401 logical device software interface occupies 2 I/O locations, utilizes 10-bit address decoding, and is located at PnP address 'MPUbase'. 10-bit addressing requires that the upper address bits be 0 to decode a valid address, i.e. no aliasing occurs. The standard base address is 330h. This device also uses an interrupt, typically 9. The PnP alignment for the MPU-401 must be a multiple of 8.

MPUbase+0 is the MIDI Transmit/Receive port and MPUbase+1 is the Command/Status port. In addition to I/O decodes the only additional functionality required from an ISA bus viewpoint is the generation of a hardware interrupt whenever data has been received into the receive buffer.

MIDI Transmit/Receive Port,
MPUbase+0, default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0

TR7-TR0 — The MIDI Transmit/Receive Port is used to send and receive MIDI data as well as status information that was returned from a previously sent command.

All MIDI transmit data is transferred through a 16-byte FIFO and receive data through a 16-byte FIFO. The FIFO gives the ISA interface time to respond to the asynchronous MIDI transfer rate of 31.25K baud.

The Command/Status Registers occupy the same address and are used to send instructions to and receive status information from the MPU-401.

Command Register, write only
MPUbase+1

D7	D6	D5	D4	D3	D2	D1	D0
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

CS7-CS0 — Each write to the Command/Status Register must be monitored and the appropriate acknowledge generated.

Status Register, read only
MPUbase+1, Default = xxxxxxxx

D7	D6	D5	D4	D3	D2	D1	D0
RXS	TXS	CS5	CS4	CS3	CS2	CS1	CS0

CS5-CS1 — D0-D5 are the 6 LSBs of the last command written to this port.

TXS — Transmit Buffer Status Flag.

0 - Transmit buffer not full
1 - Transmit buffer full

RXS — Receive Buffer Status Flag

0 - Data in Receive buffer
1 - Receive buffer empty

When in "UART" mode, data is received into the receive buffer FIFO and a hardware interrupt is generated. Data can be received from two sources: MIDI data via the UART serial input or acknowledge data that is the result of a write to the Command Register (MPUbase+1). The interrupt is cleared by a read of the MIDI Receive Port (MPUbase+0).

MIDI UART

The UART is used to convert parallel data to the serial data required by MIDI. The serial data rate is fixed at 31.25K baud (±1%). The serial data format is RS-232 like: 1 start bit, 8 data bits, and 1 stop bit.

In multimedia systems, the MIDI pins are typically connected to the joystick connector. See the *Reference Design* Data Sheet for detailed information.

MPU-401 "UART" Mode Operation

After power-up reset, the interface is in "non-UART" mode. Non-UART mode operation is defined as follows:

1. All writes to the Transmit Port, MPUbase+0, are ignored.

2. All reads of the Receive Port, MPUbase+0, return the last received buffer data.

3. All writes to the Command Port, MPUbase+1, are monitored and acknowledged as follows:
   a. A write of 3Fh sets the interface into UART operating mode. An acknowledge is generated by putting an FEh into the receive buffer FIFO which generates an interrupt.
   b. A write of A0-A7, ABh, ACh, ADh, AFh places an FEh into the receive buffer FIFO (which generates an interrupt) followed by a one byte write to the receive buffer FIFO of 00h for A0-A7, and ABh commands, 15h for ACh, 01h for ADh, and 64h for AFh commands.
   c. All other writes to the Command Port are ignored and an acknowledge is generated by putting an FEh into the receive buffer FIFO which generates an interrupt.

UART mode operation is defined as follows:

1. All writes to the Transmit Port, MPUbase+0, are placed in the transmit buffer FIFO. Whenever the transmit buffer FIFO is not empty, the next byte is read from the buffer and sent out the MIDOUT pin. The Status Register, MPUbase+1, bit 6, TXS is updated to reflect the transmit buffer FIFO status.

2. All reads of the Receive Port, MPUbase+0, return the next byte in the receive buffer FIFO. When serial data is received from the MIDIN pin, it is placed in the next receive buffer FIFO location. If the buffer is full, the last location is overwritten with the new data. The Status Register, MPUbase+1, bit 7, RXS is updated to reflect the new receive buffer FIFO state.

3. A write to the Command Register, MPUbase+1, of FFh will return the interface to non-UART mode.

4. All other writes to the Command Register, MPUbase+1, are ignored.

FM SYNTHESIZER (Internal)

This part contains a games-compatible internal FM synthesizer. When enabled, this internal FM synthesis engine responds to both the SBPro FM synthesis addresses as well as the SYNbase addresses.

To enable the internal FM synthesis engine, the IFM bit in the Hardware Configuration data, byte 8 (Global Configuration Byte) must be set. This bit is also available in WSS register X4.

Volume control for the internal FM synthesizer is supported through X6 and X7 in the WSS extended register space. The volume range is 0 dB to -94.4 dB with 000000 equal to 0 dB. After

volume is applied to the PCM FM data, it is summed into the digital mixer which is then summed into the analog output mixer.

For backwards compatibility with analog-mixed external FM devices, I18 and I19 in the WSS logical device can be remapped to control the volume of internal FM. Remapping is controlled through the FMRM bit in X4 register. When IFM = 1, and FMRM = 1, writes to I18 and I19 are remapped to X6 and X7 respectively. When remapping is enabled, the LINE analog input volume is controlled through X0/1. When FMRM = 0, internal FM volume is only controlled through X6/7.

The synthesizer interface is compatible with the Adlib and Sound Blaster standards. The typical Adlib I/O address is SYNbase = 388h.

Standard Adlib Synthesizer I/O Map

Address	Name	Type
SYNbase+0	FM Status	Read Only
SYNbase+0	FM Address 0	Write Only
SYNbase+1	FM Data 0	Write Only
SYNbase+2	FM Address 1	Write Only
SYNbase+3	FM Data 1	Read Only

EXTERNAL PERIPHERAL PORT

An external peripheral port is provided for interfacing devices external to the part. These may include the CS9233 Wavetable synthesizer, CDROM interface, modem interface, and Plug and Play E^2PROM.

The External Peripheral Port consists of the following signals: 8-bit data bus, 2 or 3 address lines, read strobe, write strobe, and reset signal.

External Synthesizer Interface

This part contains an internal FM synthesis engine. For backwards compatibility the default is to use an external FM-type synthesizer chip such as the Yamaha OPL3LS, or the Crystal Semiconductor CS9233 wave-table synthesizer chip. This interface consists of:

$\overline{SCS}$ - chip select
$\overline{SINT}$ - Synthesizer Interrupt

The other signals such as address bits, data strobes, data, and reset are provided by the External Peripheral Port. The interface allows the host computer to access up to eight I/O mapped locations. When using an external FM synthesizer, $\overline{SCS}$ will respond to the SYNbase decode addresses as well as the SBPro mapped FM synthesizer addresses. The PnP synthesizer alignment must be a multiple of 8.

The polarity of $\overline{SINT}$ is programmable via Hardware Configuration data, IHS in byte 7, or through CTRLbase+1. The default is active low (IHS = 0).

Since the typical FM interface only requires four I/O address and does not use an interrupt, the XA2 address and the $\overline{SINT}$ pins are multifunction pins that default to XCTL0 and XCTL1. To use XCTL0/XA2 as an address pin, the hardware resource data must be changed. See the *Hardware Configuration Data* section for more information. To use XCTL1/$\overline{SINT}$/$\overline{ACDCS}$/$\overline{DOWN}$ as an interrupt for the synthesizer, VCEN (in the Hardware Configuration data) must be zero, a pulldown resistor must be placed on the $\overline{XIOW}$ pin. Since XCTL1 and $\overline{SINT}$ are rarely used the pin has a third multiplexed function, $\overline{ACDCS}$, which is described in the CDROM section below. The fourth multiplexed function is the hardware volume control pin $\overline{DOWN}$ which is controlled through the VCEN bit. See the *Volume Control Interface* section for more details. Note that $\overline{ACDCS}$ takes precedence over XCTL1/$\overline{SINT}$. Also $\overline{DOWN}$, when VCEN is set, takes precedence over all other functions.

CDROM Interface

An IDE CDROM controller interface is provided that supports Enhanced as well as Legacy IDE CDROM drives. This interface includes two programmable chip selects and on-chip hardware to map DMA and interrupt signals to the ISA bus.

There are five pins that make up the CDROM interface which consist of:

CDCS - chip select, COMbase address
CDINT - interrupt, COMint
CDRQ - DMA request, COMdma
CDACK - DMA acknowledge, COMdma
ACDCS - alternate chip select, ACDbase

The four basic CDROM interface pins are multifunction pins that default to the upper address bits SA12 - SA15. To use the pins as a CDROM interface, a pulldown resistor must be placed on XIOR (XIOR must be buffered if driving TTL logic). Once the CDROM interface is selected, the CDROM DMA pins are further multiplexed with the Modem pins. Therefore, a fifth logical device, typically a modem, can be used if the CDROM doesn't support DMA. See the *Modem Interface* section for more details.

The fifth CDROM pin ACDCS is multiplexed with XCTL1/SINT/DOWN. This chip select supports the alternate CDROM chip select used for status in legacy IDE drives. The volume control pin DOWN has the highest precedence; therefore, the VCEN bit must be zero to use this pin for the CDROM interface. Given that VCEN is zero, if the base address for ACDCS, which is ACDbase, is programmed to a non-zero value, this pin converts to ACDCS. ACDbase, base address 1 in LD4, is programmed via PnP or via the SLAM method. Once this pin is set to ACDCS, the only way to revert to XCTL1 or SINT is to reset the part. The range of addresses that ACDCS will respond to is programmable via the Hardware Configuration data, byte 5, from one to eight bytes. The default is 1 byte. In legacy IDE CDROM drives, the alternate CDROM address plus 1, ACDbase+1, is typically shared with the floppy controller, which only drives data bit 7. Therefore, a bit in the Hardware Configuration data keeps the SD7 pin from driving data bit 7 when that address is decoded. This bit is labeled ACDB7D and is located in the Hardware Configuration data, byte 7. When using ACDCS, the SINT function should be selected and a pullup placed on this line, which will allow this pin to powerup inactive. If XCTL1 is selected, it will powerup low; therefore, ACDCS will be low until ACDbase is programmed to a non-zero value.

The default address space for the peripheral port is 4 I/O locations where XCTL0/XA2 defaults to the control pin XCTL0. To use XCTL0/XA2 as the XA2 address pin, thereby increasing the address range of the peripheral port to 8 locations, the hardware resource data must be changed. See the *Hardware Configuration Data* section. Even though the default address space is only 4 locations, the alignment for CDbase must be a division of 8.

To make the CDROM interface more flexible, two global bits, located in the Hardware Configuration data section - byte 7, allow control over the polarity of the CDROM interrupt pin CDINT, and whether the SD<7-0> pins drive the ISA bus or not. The first bit is IHC which defaults to 1 indicating that CDINT is an active high interrupt. IHC is also controllable through CTRLbase+1. The second bit is SDD - SD<7:0> bus Disable. When this bit is set, the part will not drive the ISA Data bus SD<7:0> pins, on reads from either CDbase or ACDbase addresses. This bit allows external data buffers to be used for a CDROM that bypasses the XD<7:0> bus and connects directly to the ISA bus. Note that SDD affects any peripheral port device which includes the external FM and modem interfaces.

Modem Interface

The modem interface, Logical Device 5 (LD5) consist of:

$\overline{\text{MCS}}$ - Modem Chip Select
MINT - Modem Interrupt

The other signals such as address bits, data strobes, data, and reset are provided by the External Peripheral Port. The interface allows the host computer to access up to eight I/O mapped locations.

The Modem signals are multiplexed with both the upper ISA address pins, and the CDROM DMA pins. To enable the Modem, first a pull-down resistor must be placed on $\overline{\text{XIOR}}$ which disables the upper ISA address pins. Second, the Modem base address, COMbase, must be programmed to a non-zero value which will convert the SA13/$\overline{\text{CDACK}}$/$\overline{\text{MCS}}$ pin to the modem chip select $\overline{\text{MCS}}$, and the SA15/CDRQ/MINT pin to the modem interrupt pin MINT. Once these two pins switch to modem pins, they can only be changed by resetting the part. COMbase, Logical Device 5 base address 0, is programmed via PnP or the SLAM method.

The polarity of MINT is programmable via Hardware Configuration data, IHM in byte 7, or through CTRLbase+1. The default is active low (IHM = 0).

DSP SERIAL AUDIO DATA PORT

The WSS Codec includes a DSP serial audio interface for transferring digital audio data between the part and an external serial device such as a DSP processor. The DSP serial port pins are multiplexed with either the #2 joystick inputs of the Game Port interface or a portion of the XD peripheral bus. The selection is made via the SPS bit located in Control register C8, or the Global Config. byte in the Hardware Configuration data. If SPS is 0, the joystick B pins convert to the DSP serial port when SPE is set (MCE must be 1 to change SPE). If SPS is 1, XD<4:1> convert to the DSP serial port when SPE is set. In this case, SD<7:0> is disabled on reads of peripheral port addresses (CDROM, modem, etc.) since XD<7:0> is no longer available.

The DSP audio serial port is software enabled via the SPE bit in the WSS Codec indirect register I16. The ISA interface is fully active in this mode. While the serial port is enabled, audio data may still be read from the ADCs over the ISA bus, and the DACs will sum data from the SDIN pin, the parallel ISA bus data, and the internal FM synthesizer engine. The serial port sample frequency is always 44.1 kHz regardless of the ISA bus sample frequency, and the data format is always two's complement 16-bit linear.

FSYNC and SCLK are always output from the part when the serial port is enabled. The serial port can be configured in one of four serial port formats, shown in Figures 7-10. SF1 and SF0 in I16 select the particular format. MCE in R0 must be set to change SF1/0. Both left and right audio words are always 16 bit two's complement. When the mono audio format is selected, the right channel output is set to zero and the left channel input is summed to both DAC channels.

The first format - SPF0, shown in Figure 7, is called 64-bit enhanced. This format has 64 SCLKs per frame with a one bit period wide FSYNC that precedes the frame. The first 16 bits occupy the left word and the second 16 bits occupy the right word. The last 32 bits contain four status bits and 28 zeros. This is the only mode that contains status information.

The second serial format - SPF1, shown in Figure 8, is called 64-bit mode. This format has 64 SCLKs per frame, with FSYNC high transitions at the start of the left data word and low transitions at the start of the right data word. Both the left and right data words are followed by 16 zeros.

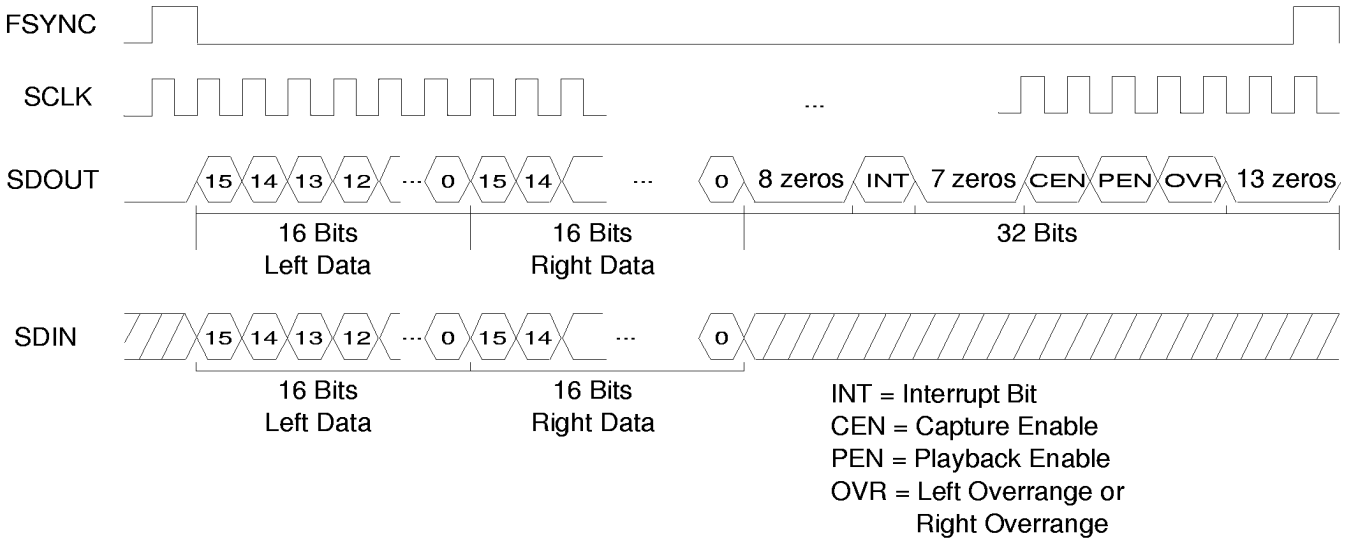


Figure 7. 64-bit Enhanced Mode (SF1,0 = 00)

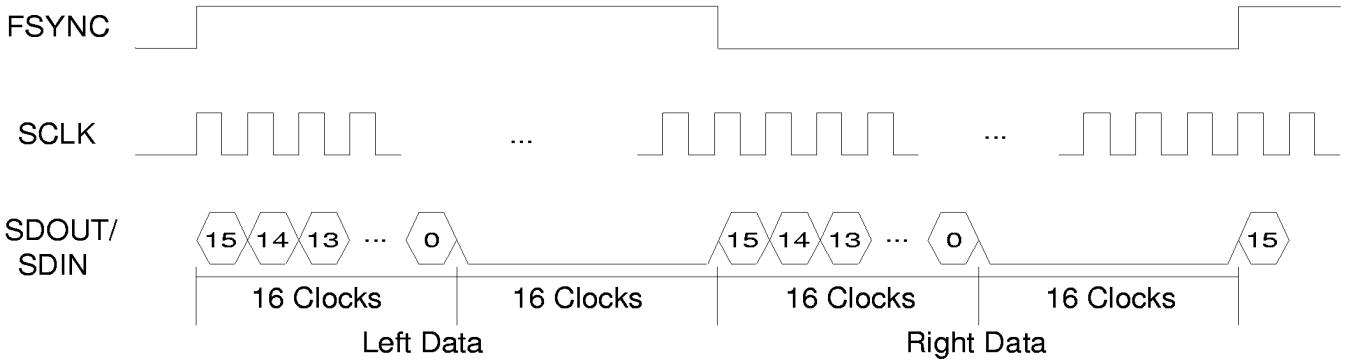


Figure 8. 64-bit Mode (SF1,0 = 01)

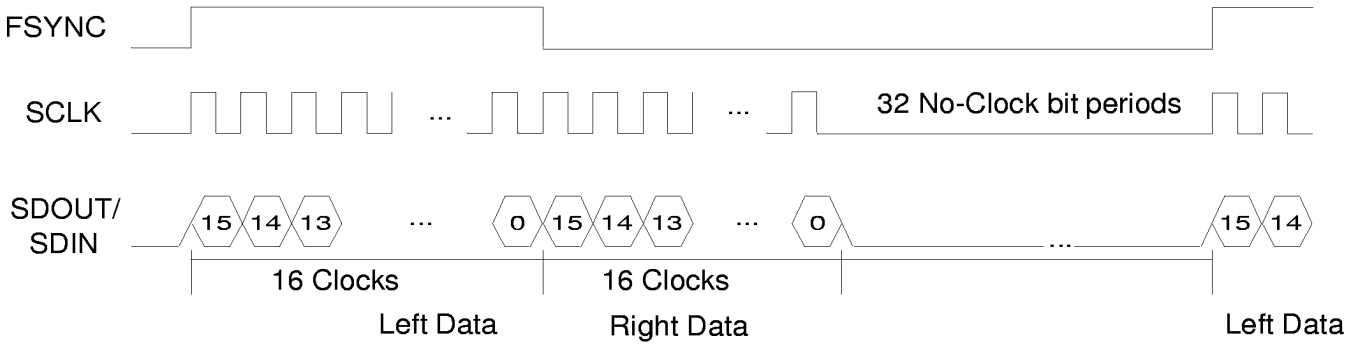


Figure 9. 32-bit Mode (SF1,0 = 10)

The third serial format - SPF2, shown in Figure 9, is called 32-bit mode. This format has 32 SCLKs per frame and FSYNC is high for the left channel and low for the right channel. The absolute time is similar to the other two modes but SCLK is stopped after the right channel is finished. SCLK is held stopped until the start of the next frame (stopped for 32 bit period times). This mode is useful for DSPs that do not want the interrupt overhead of the 32 unused bit periods. As an example, if a DSP serial word length is 16 bits, then four interrupts will occur in SPF0 and SPF1 modes. In mode SPF2 the DSP will only be interrupted twice.

The fourth serial format - SPF3, shown in Figure 10, is called ADC/DAC mode. This format has 64 SCLKs per frame, with FSYNC high transitions at the start of the left ADC data word and low transitions at the start of the right ADC data word. For serial data in, SDIN, both the left and right 16-bit DAC data word should be followed by zeros. For serial data out, SDOUT, both the left and right ADC data words are followed by 16 bits of the DAC data words. The DAC data words are tapped off the data stream right before the data enters the Codec DACs (after all digital summing is done). Having the ADC and DAC data on the SDOUT allows external modem DSPs to cancel the local audio source from the local microphone signal.

CS9236 WAVETABLE SERIAL PORT

A digital interface to the Crystal CS9236 Single-Chip Wavetable Music Synthesizer is provided that allows the CS9236 PCM audio data to be summed digitally into the output digital mixer. The Wavetable Serial port pins are multiplexed with the XD7-XD5 external bus pins; therefore, when this serial interface is enabled, any external peripheral (CDROM, modem, etc.) will need an external buffer to the ISA bus. This serial port is enabled via the WTEN bit located in Control register C8 or in the Global Configuration byte in the Hardware Configuration data. The hardware connections to the CS9236 are illustrated in Figure 11.

Volume control for the serial port is supported through X16 and X17 in the WSS extended register space. The volume range is +12 dB to -82.5 dB with 001000 equal to 0 dB. After volume is applied to the PCM data, it is summed into the digital mixer which is then summed into the analog output mixer.

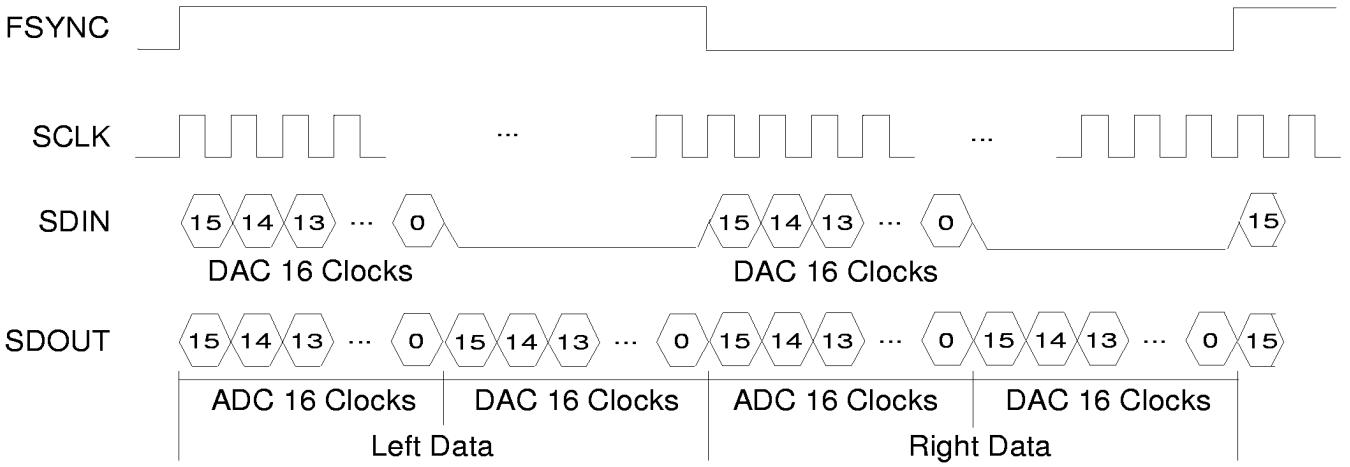


Figure 10. ADC/DAC Mode (SF1,0 = 11)

For backwards compatibility with analog-mixed wavetable devices, I18 and I19 in the WSS logical device can be remapped to control the volume of the Wavetable serial port. Remapping is controlled through the WTRMD bit in X4 register. When WTEN = 1, and WTRMD = 0, writes to I18 and I19 are remapped to X16 and X17 respectively. When remapping is enabled, the LINE analog input volume is controlled through X0/1. When WTRMD = 1, the Wavetable Serial Port volume is only controlled through X16/17.

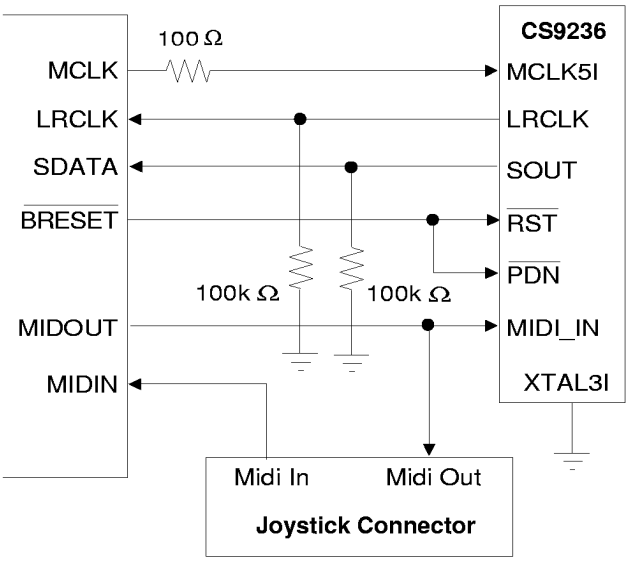


Figure 11. CS9236 Wavetable Serial Port Interface

WSS CODEC SOFTWARE DESCRIPTION

The WSS Codec must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register (I9) or the Sample Frequency (lower four bits) in the Fs & Playback Data Format registers (I8) are allowed. The actual audio data formats, which are the upper four bits of I8 for playback and I28 for capture, can be changed by setting MCE (R0) or PMCE/CMCE (I16) high. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

Calibration

The WSS Codec has four different calibration modes. The selected calibration occurs whenever the Mode Change Enable (MCE, R0) bit goes form 1 to 0.

The completion of calibration can be determined by polling the Auto-Calibrate In-Progress bit in the Error Status and Initialization register (ACI, I11). This bit will be high while the calibration is in progress and low once completed. Transfers enabled during calibration will not begin until the calibration cycle has completed. Since the part always operates at 44.1 kHz internally, all calibration times are based on 44.1 kHz sample periods.

The Calibration procedure is as follows:

1) Place the WSS Codec in Mode Change Enable using the MCE bit of the Index Address register (R0).

2) Set the CAL1,0 bits in the Interface Configuration register (I9).

3) Return from Mode Change Enable by resetting the MCE bit of the Index Address register (R0).

4) Wait until 80h NOT returned

5) Wait until ACI (I11) cleared to proceed

NO CALIBRATION (CAL1,0 = 00)

This is the fastest mode since no calibration is performed. This mode is useful for games which require the sample frequency be changed quickly. This mode is also useful when the codec is operating full-duplex and an ADC data format change is desired. This is the only calibration mode that does not affect the DACs (i.e. mute the DACs). The No Calibration mode takes zero sample periods.

CONVERTER CALIBRATION (CAL1,0 = 01)

This calibration mode calibrates the ADCs and the DACs, but does not calibrate any of the analog mixing channels. This is the second longest calibration mode, taking 321 sample periods at 44.1 kHz. Because the analog mixer is not calibrated in this mode, any signals fed through the mixer will be unaffected. The calibration sequence is as follows:

The DACs are muted
The ADCs are calibrated
The DACs are calibrated
The DACs are unmuted

DAC CALIBRATION (CAL1,0 = 10)

This calibration mode only clears the DACs (playback) interpolation filters leaving the ADC unaffected. This is the second fastest calibration mode (no cal. is the fastest) taking 120 sample periods at 44.1 kHz to complete. The calibration sequence is as follows:

The DACs are muted
The DAC filters are cleared
The DACs are unmuted

FULL CALIBRATION (CAL1, 0 = 11)

This calibration mode calibrates all offsets, ADCs, DACs, and analog mixers. Full calibration will automatically be initiated on power up or anytime the WSS Codec exits from a full power down state. This is the longest calibration mode and takes 450 sample periods at 44.1 kHz to complete. The calibration sequence is as follows:

All outputs are muted (DACs and mixer)
The mixer is calibrated
The ADCs are calibrated
The DACs are calibrated
All outputs are unmuted

Changing Sampling Rate

The internal states of the WSS Codec are synchronized by the selected sampling frequency. The sample frequency can be set in one of three fashions. The standard WSS Codec method uses the Fs & Playback Data Format register (I8) to set the sample frequency. The changing of either the clock source or the clock frequency divide requires a special sequence for proper WSS Codec operation:

1) Place the WSS Codec in Mode Change Enable using the MCE bit of the Index Address register (R0).

2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock 2 Base Select (C2SL) bits of the Fs & Playback Data Format register (I8) to the desired value. (The data format may also be changed.)

3) The WSS Codec resynchronizes its internal states to the new frequency. During this time the WSS Codec will be unable to respond. Writes to the WSS Codec will not be recognized and reads will always return the value 80 hex.

4) The host now polls the WSS Codec's Index Address register (R0) until the value 80 hex is no longer returned. On slow processor systems, 80h may occur to fast; therefore, it may never be seen by software.

5) Once the WSS Codec is no longer responding to reads with a value of 80 hex, normal operation can resume and the WSS Codec can be removed from MCE.

A second method of changing the sample frequency is to disable the sample frequency bits in I8 (lower four bits) by setting SRE in I22. When this bit is set, OSM1 and OSM0 in I10, along

with the rest of the bits in I22, are used to set the sample frequency. Once enabled, these bits can be changed without doing an MCE cycle.

The third method supports independent sample frequencies (Fs) for capture and playback. The independent sample frequency mode is enabled by setting IFSE in X11. Once enabled, the other two methods for setting Fs (I8, I10, and I22) are disabled. The capture (ADC) Fs is set in X12 and the playback (DAC) Fs is set in X13.

Changing Audio Data Formats

In MODE 1, MCE must be used to select the audio data format in I8. Since MCE causes a calibration cycle, it is not ideal for full-duplex operation. In MODE 2 and 3, individual Mode Change Enable bits for capture and playback are provided in register I16. MCE (R0) must still be used to select the sample frequency, but PMCE (playback) and CMCE (capture) allow changing the respective data formats without causing a calibration to occur. Setting PMCE (I16) clears the playback FIFO and allows the upper four bits of I8 to be changed. Setting CMCE (I16) clears the capture FIFO and allows the upper four bits of I28 to be changed.

Audio Data Formats

In MODE 1 operation, all data formats of the WSS Codec are in "little endian" format. This format defines the byte ordering of a multibyte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The sample frequency is always selected in the Fs & Playback Data Format register (I8). In MODE 1 the same register, I8, determines the audio data format for both playback and capture; however, in MODE 2 and 3, I8 only selects the playback data format and the capture data format is independently selectable in the Capture Data Format register (I28).

The WSS Codec always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, 8-bit linear data streams look exactly like 8-bit companded data streams. Also, the left sample always comes first in the data stream regardless of whether the sample is 16-bit or 8-bit in size.

There are four data formats supported by the WSS Codec during MODE 1 operation: 16-bit signed (little endian), 8-bit unsigned, 8-bit companded μ-Law, and 8-bit companded A-Law. See Figures 12-15.

Additional data formats are supported in MODE 2 and 3: 4-bit ADPCM, and 16-bit signed Big Endian. See Figures 16 through 19. With the addition of the Big Endian and ADPCM audio data formats, the WSS Codec is compliant with the IMA recommendations for digital audio data formats (and sample frequencies).

16-BIT SIGNED

The 16-bit signed format (also called 16-bit 2's complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent maximum negative analog amplitude, 0 for center scale, and 32767 (7FFFh) to represent maximum positive analog amplitude.

8-BIT UNSIGNED

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent maximum negative analog amplitude, 128 for center scale, and 255 (FFh) to represent maximum positive analog amplitude. The 16-bit signed and 8-bit unsigned transfer functions are shown in Figure 20.

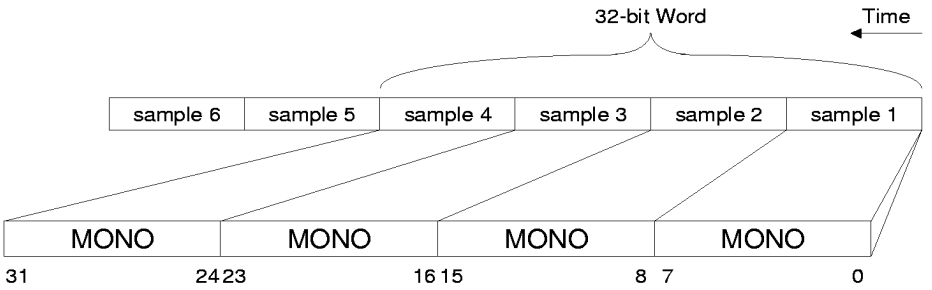


Figure 12. 8-bit Mono, Unsigned Audio Data

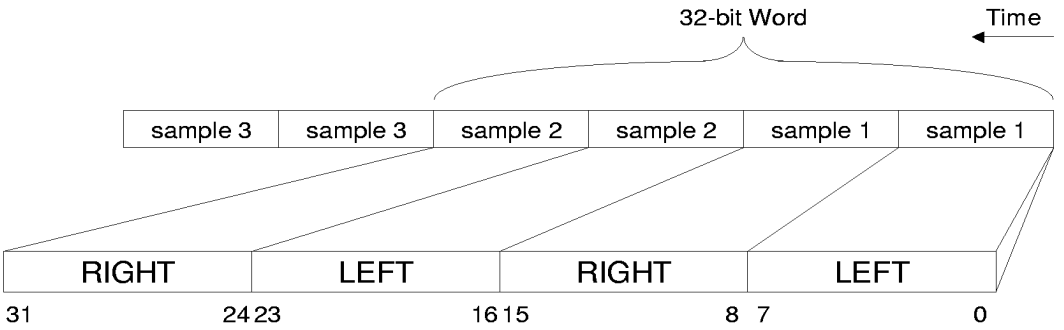


Figure 13. 8-bit Stereo, Unsigned Audio Data

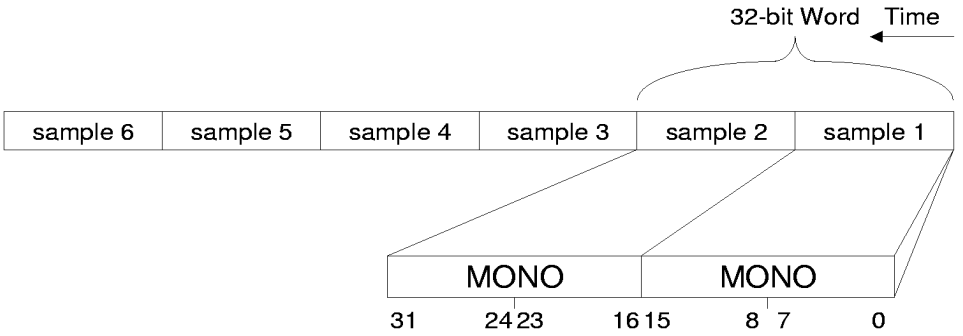


Figure 14. 16-bit Mono, Signed Little Endian Audio Data

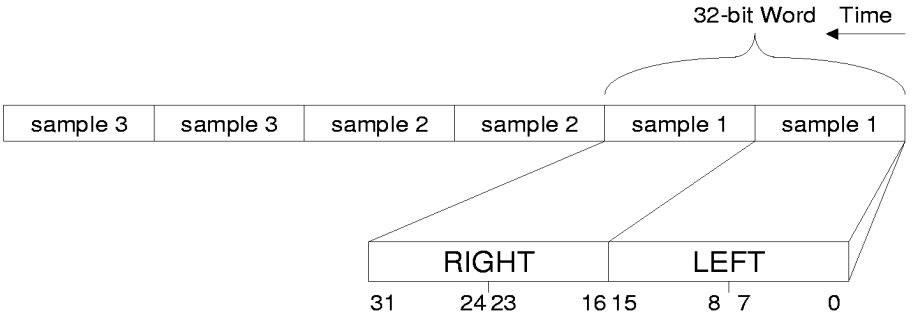


Figure 15. 16-bit Stereo, Signed Little Endian Audio Data

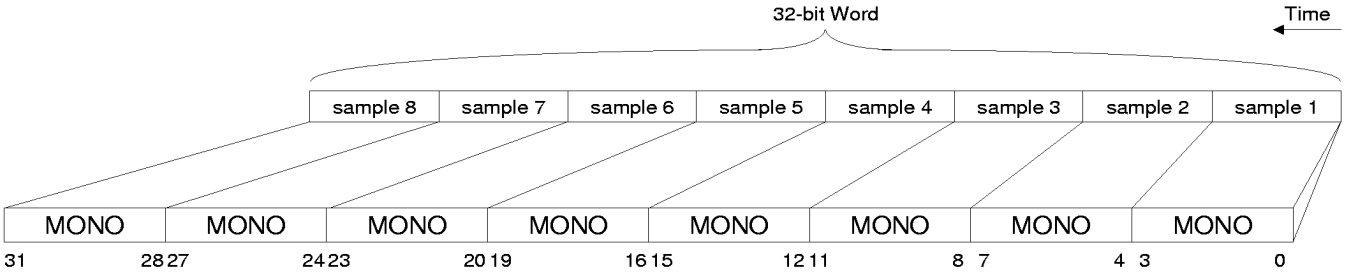


Figure 16. 4-bit Mono, ADPCM Audio Data

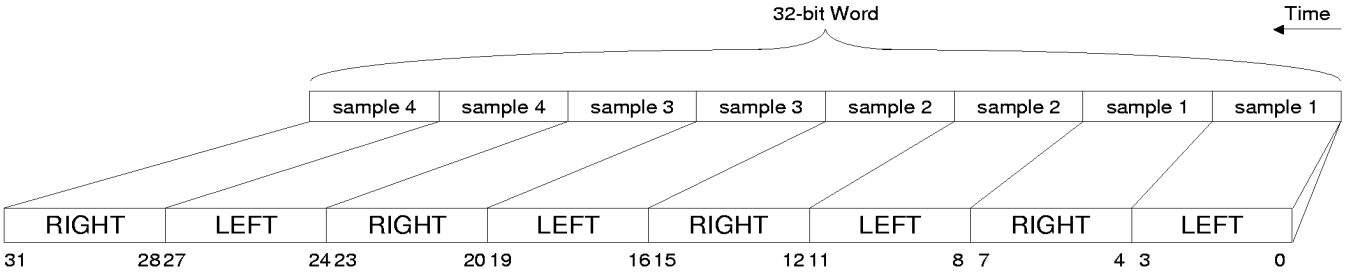


Figure 17. 4-bit Stereo, ADPCM Audio Data

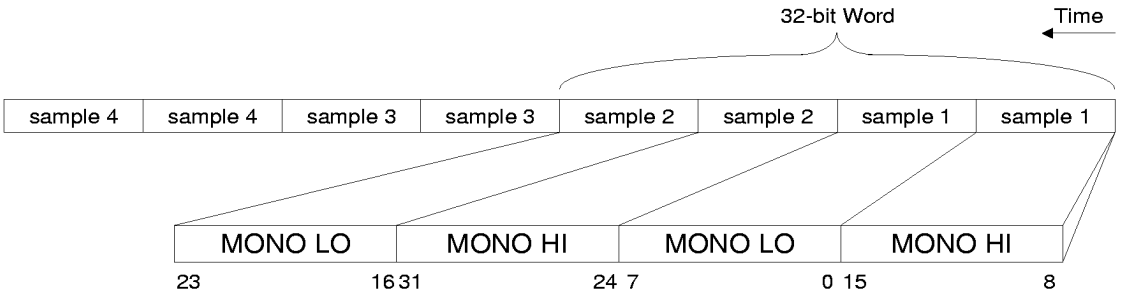


Figure 18. 16-bit Mono, Signed Big Endian Audio Data

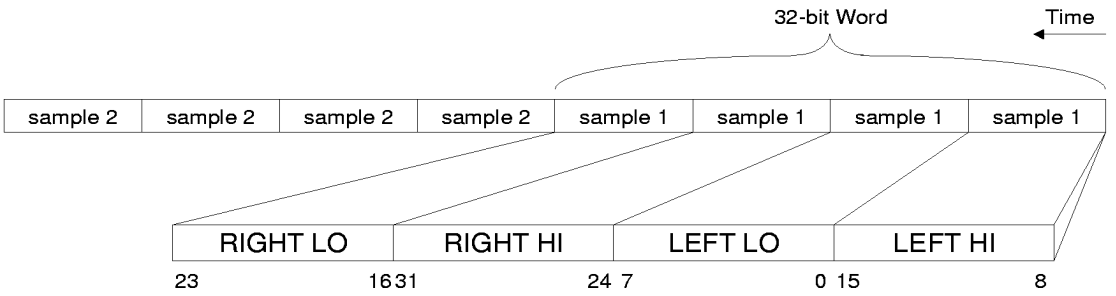


Figure 19. 16-bit Stereo, Signed Big Endian Audio Data

8-BIT COMPANDED

The 8-bit companded formats (A-Law and µ-Law) come from the telephone industry. µ-Law is the standard for the United States/Japan while A-Law is used in Europe. Companded audio allows either 64 dB or 72 dB of dynamic range using only 8-bits per sample. This is accomplished using a non-linear companding transfer function which assigns more digital codes to lower amplitude analog signals with the sacrifice of precision on higher amplitude signals. The µ-Law and A-Law formats of the WSS Codec conform to the CCITT G.711 specifications. Figure 21 illustrates the transfer function for both A- and µ-Law. Please refer to the standards mentioned above for an exact definition.

ADPCM COMPRESSION/DECOMPRESSION

In MODE 2 and 3, the WSS Codec also contains Adaptive Differential Pulse Code Modulation (ADPCM) for improved performance and compression ratios over µ-Law or A-Law. The ADPCM format is compliant with the IMA standard and provides a 4-to-1 compression ratio (i.e. 4 bits are saved for each 16-bit sample captured). For more information on the specifics of the format, contact the IMA at (410) 626-1380. Figures 16 and 17 illustrate the ADPCM data flow.

The ADPCM format is unique with respect to the FIFO depth and the DMA Base register value. The ADPCM format fills the FIFOs completely (64 bytes); therefore, the FIFOs hold 64 stereo samples and 128 mono samples. When samples are being transferred using DMA, the DMA request stays active for four bytes, similar to the 16-bit stereo data mode. In PIO mode, the Status register (R2) indicates which of the four bytes is being transferred.

When CEN is 0 (capture disabled), the ADPCM block's accumulator and step size are cleared. When CEN is enabled, the ADPCM block will start converting. Care should be taken to insure that the "overrun" condition never occurs, otherwise the data may not be constructed properly upon playback. If pausing the capture sequence is desired, the ADPCM Capture Freeze bit (ACF, I23) should be set. When this bit is set, the ADPCM algorithm will continue to operate until a complete word (4 bytes) is written to the FIFO. Then the ADPCM's block accumulator and step size will be frozen. The software must continue

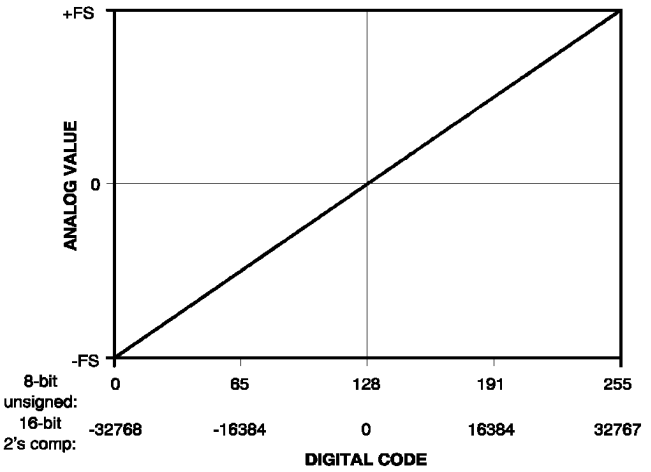


Figure 20. Linear Transfer Functions

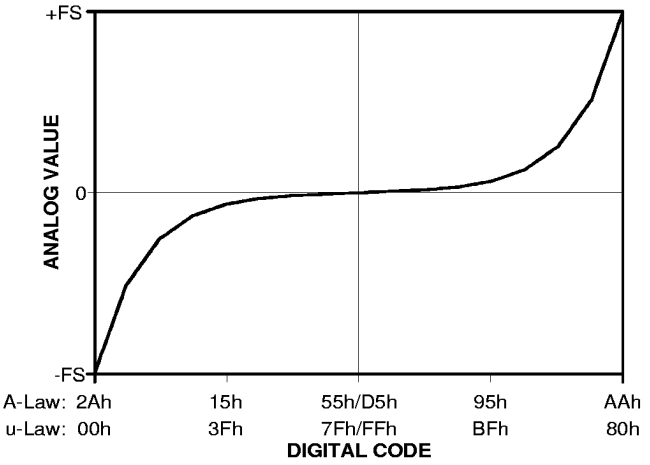


Figure 21. Companded Transfer Functions

reading until the FIFO is empty, at which time the requests will stop. When ACF is cleared, the ADPCM adaptation will continue.

When PEN is cleared (playback disabled), the ADPCM block's accumulator and step size are cleared. When PEN is set, the ADPCM block will start converting. When pausing the playback stream is desired, audio data should not be sent to the codec which will cause a data underrun. This can be accomplished by disabling the DMA controller or not sending data in PIO mode. The underrun will be detected by the WSS Codec and the adaptation will freeze. When data is sent to the codec, adaptation will resume. It is critical that all playback ADPCM samples are sent to the codec, since dropped samples will cause errors in adaptation. Whereas toggling PEN resets the accumulator and step size, the APAR bit (I17) only resets the accumulator without affecting the step size.

DMA Registers

The DMA registers allow easy integration of this part into ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Base registers provide this service.

The act of writing a value to the Upper Base register causes both Base registers to load the Current Count register. DMA transfers are enabled by setting the PEN/CEN bit while PPIO/CPIO is clear. (PPIO/CPIO can only be changed while the MCE bit is set.) Once transfers are enabled, each sample that is transferred by a DMA cycle will decrement the Current Count register (with the exception of the ADPCM format) until zero is reached. The next sample after zero generates an interrupt and reloads the Current Count registers with the values in the Base registers.

For all data formats except ADPCM, the DMA Base registers must be loaded with the number of samples, minus one, to be transferred between "DMA Interrupts". Stereo data contains twice as many samples as mono data; however, 8-bit data and 16-bit data contain the same number of samples. Symbolically:

$$\text{DMA Base register}_{16} = N_S - 1$$

Where N_S is the number of samples transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

For the ADPCM data format, the contents of the DMA Base registers is calculated differently from any other data format. The Base registers must be loaded with the number of BYTES to be transferred between "DMA interrupts", divided by four, minus one. The same equation is used whether the data format is stereo or mono ADPCM. Symbolically:

$$\text{DMA Base register}_{16} = N_b/4 - 1$$

Where N_b is the number of BYTES transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

PLAYBACK DMA REGISTERS

The playback DMA registers (I14/15) are used for sending playback data to the DACs in MODE 2 and 3. In MODE 1, these registers (I14/15) are used for both playback and capture; therefore, full-duplex DMA operation is not possible.

When the playback Current Count register rolls under, the Playback Interrupt bit, PI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Playback Interrupt bit, PI (I24).

CAPTURE DMA REGISTERS

The Capture DMA Base registers (I30/31) provide a second pair of Base registers that allow full-duplex DMA operation. With full-duplex operation capture and playback can occur simultaneously. These registers are provided in MODE 2 and 3 only.

When the capture Current Count register rolls under, the Capture Interrupt bit, CI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Capture Interrupt bit, CI (I24).

Digital Loopback

Digital Loopback is enabled via the LBE bit in the Loopback Control register (I13). This loopback routes the digital data from the ADCs to the DACs. There are two Methods of controlling this loopback. The first method does not allow separate control over the attenuation level of the left and right channels. Changes to the attenuation bits of register I13 will simultaneously affect both the left and the right channels. The other method of controlling loopback, is to set the SLBE bit in register X10. This separates the attenuation levels of the left and right channels. With SLBE enabled, the attenuation bits of register I13 only control the left channel, and the attenuation bits of register X10 control the right channel. The LBE bit in register I13 still enables, or disables digital loopback for both channels. Loopback is then summed into the digital mixer. The digital loopback is illustrated in Figure 4. Since the WSS Codec allows selection of different data formats between capture and playback, if the capture channel is set to mono and the playback channel set to stereo, the mono input (mic) data will be mixed into both channels of the output mixer.

If the sum of the digital mixer inputs is greater than full scale, WSS Codec will send the appropriate full scale value to the DACs (clipping).

Timer Registers

The Timer registers are provided for synchronization, watch dog and other functions where a high resolution time reference is required. This counter is 16 bits and the exact time base, listed in the register description, is determined by the clock base frequency selected.

The Timer register is set by loading the high and low registers to the appropriate values and setting the Timer Enable bit, TE, in the Alternate Feature Enable register (I16). This value will be loaded into an internal Current Count register and will decrement at approximately a 10 µsec rate. When the value of the Current Count register reaches zero, an interrupt will be posted to the host and the Timer Interrupt bit, TI, is set in the Alternate Feature Status register (I24). On the next timer clock the value of the Timer registers will be loaded into the internal Current Count register and the process will begin again. The interrupt is cleared by any write to the Status register (R2) or by writing a "0" to the Timer Interrupt bit, TI, in the Alternate Feature Status register (I24).

WSS Codec Interrupt

The INT bit of the Status register (R2) always reflects the status of the WSS Codec's internal interrupt state. A roll-over from any Current Count register (DMA playback, DMA capture, or Timer) sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register (R2), or by clearing the appropriate bit or bits (PI, CI, TI) in the Alternate Feature Status register (I24).

The Interrupt Enable (IEN) bit in the Pin Control register (I10) determines whether the interrupt assigned to the WSS Codec responds to the interrupt event. When the IEN bit is low, the interrupt is masked and the IRQ pin assigned to the WSS Codec is held low. However, the INT bit in the Status register (R2) always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the WSS Codec in an appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the WSS Codec.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case the last valid sample will be output (assuming DACZ = 0) to the digital mixer. This will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

The overrun and underrun error bits in the *Alternate Feature Status* register, I24, are cleared by first clearing the condition that caused the overrun or underrun error, followed by writing the particular bit to a zero. As an example, to clear the playback underrun bit PU, first a sample must be sent to the WSS Codec, and then the PU bit must be written to a zero.

DIGITAL HARDWARE DESCRIPTION

The best example of hardware connection for the different sections of this part such as joystick connector, ISA bus, and peripheral port connections is the *Reference Design* Data Sheet. The *Reference Design* Data Sheet contains all the schematics, layout plots and a Bill of Materials; thereby providing a complete example.

Bus Interface

The ISA bus interface is capable of driving a 24mA data bus load and therefore does not require any external data bus buffering. See the *Reference Design* Data Sheet for a typical connection diagram.

Volume Control Interface

Three hardware master volume control pins are supported: volume up, volume down, and mute. Hardware volume control is enabled by setting the VCEN bit in the Hardware Configuration data, byte 7 (Misc. Config. Byte). Once VCEN is set, the SCS/UP pin converts to the volume up function and the XTAL1/SINT/ACDCS/DOWN pin converts to the volume down function. The volume control pins affect the master volume control output after the analog output mixer. The UP and DOWN pins, when low, increment and decrement the master volume. These two pins would use SPST momentary switches. The MUTE pin supports three options: push-on/push-off, momentary (similar to the up/down functions), and non-existent where pressing up and down simultaneously mutes the output volume. As shown in Figure 22, the three pins require external pullups and are active low. The circuit also contains an optional RC for EMI and ESD protection.

The volume control range is +12 to -36 dB in 2 dB steps. Pressing the up button, increments the volume. Pressing the down button, decrements the volume. Holding either of these buttons in the low state causes the volume to to continue changing.

The mute function is supported using three formats. These formats are selected using the VCF1 and VCF0 bits in the Hardware Configuration data, Global Config. byte.

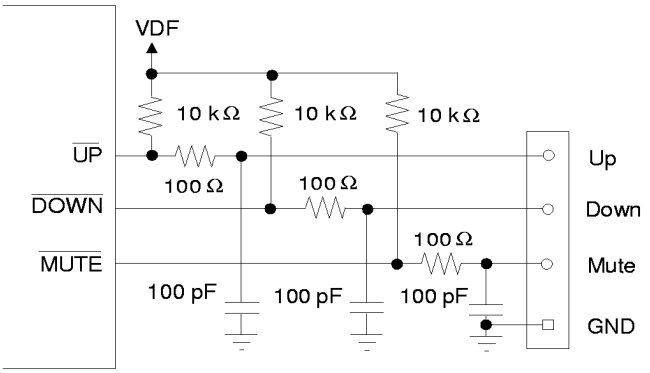


Figure 22. Volume Control Circuit

In the first format, where VCF1,0 = 00, the mute function is a toggle or push-on/push-off style. When the $\overline{\text{MUTE}}$ pin is low, the master out volume is muted. Pressing the up or down buttons have no effect while the mute switch is on.

In the second format, where VCF1,0 = 01, the mute function is a momentary switch (similar to up and down). When $\overline{\text{MUTE}}$ goes low the master out volume mutes if it was un-muted and vise-versa (the mute button alternates between mute and un-mute). If the master volume is muted and up or down is pressed, the volume automatically un-mutes.

In the third format, where VCF1,0 = 10, the MUTE pin is not used. This is a two-button format where pressing up and down simultaneously mutes the master volume. If the master volume is muted and up or down is individually pressed, the volume automatically un-mutes.

The three formats listed above as illustrated in Figure 23.

A fourth format for mute exists, where VCF1,0 = 11, which is backwards compatible with the CS4236. This mode is similar to the two button mode, except the $\overline{\text{MUTE}}$ pin is used as the up function and the $\overline{\text{UP}}$ pin is not used.

Crystal / Clock

Two pins have been allocated to allow the interfacing of a crystal oscillator: XTALI and XTALO. The crystal should be designed as fundamental mode, parallel resonant, with a load capacitor of between 10 and 20 pF. The capacitors connected to each of the crystal pins should be twice the load capacitance specified to the crystal manufacturer.

An external CMOS clock may be connected to the crystal input XTALI in lieu of the crystal. When using an external CMOS clock, the XTALO pin must be left floating with no trace or external connection of any kind.

General Purpose Output Pins

Two general purpose outputs are provided to enable control of external circuitry (i.e. mute function). XCTL1 and XCTL0 in the WSS Codec register I10 are output directly to the appropriate pin when enabled.

Pin XCTL0/XA2 becomes an output for XCTL0 whenever the resource data for the CDROM or Synthesizer specifies a logical device address

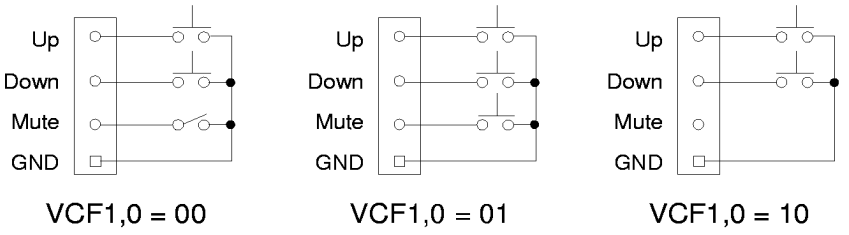


Figure 23. Volume Control Formats

range that is four bytes. If the address range is specified to be eight bytes, then XA2 becomes an output for SA2 from the ISA bus.

Pin XCTL1/SINT/ACDCS/DOWN is initially controlled by the VCEN bit in the Hardware Configuration data. If VCEN is zero, this pin becomes an output for XCTL1 when the state of the XIOW pin is sampled high during a high to low transition of the RESDRV pin. This pin also becomes an output for ACDCS if ACDbase is programmed to a non-zero value. If XIOW is sampled low and ACDbase is never programmed to a non-zero value, SINT becomes an input for the external Synthesizer interrupt. XIOW has an internal pullup resistor. ACDCS takes precedence over the other two functions. The first time ACDbase is programmed to a non-zero value, the pin converts to ACDCS. The only way to convert back to XTAL1 or SINT is to reset the part. VCEN has the highest precedence and will cause this pin to convert to the DOWN function whenever VCEN is set.

Reset and Power Down

A RESDRV pin places the part into maximum power conservation mode. When RESDRV goes high, the PnP registers are reset - all logical devices are disabled, all analog outputs are muted, and the voltage reference then slowly decays to ground. When RESDRV is brought low, an initialization procedure begins which causes a full calibration cycle to occur. When initialization is completed, the registers will contain their reset value and the part will be isolated from the bus. RESDRV is required whenever the part is powered up. The initialization time varies based on whether an E^2PROM is present or not and the size of the data in the E^2PROM. After RESDRV goes low, the CS4236 should not be written to for approximately one and one half second to guarantee that the part is ready to respond to commands. The exact timing is specified in the *Timing Section* in the front of this data sheet.

Software low-power states are available through bits in the Control logical device register space. This part supports the same power down bits contained in the CS4232; however, new power down modes are provided in CTRLbase+2 that allow for a more efficient power management routine. This register allows individual blocks within the part to be powered down. See the *CONTROL INTERFACE* section for more information.

Multiplexed Pin Configuration

On the high to low transition of the RESDRV pin, the part samples the state of the XIOR and XIOW pins. Both of these pins have internal 100kΩ pullups to +5V. If either of these pins is pulled low externally, they must be buffered before connecting to a TTL input (as in a CDROM port) since TTL cannot be pulled low.

The state of XIOR at the time RESDRV is brought low determines the function of the CDROM interface pins. If XIOR is sampled high, then CDCS, CDACK, CDINT, CDRQ are used to input SA12, SA13, SA14, SA15 respectively. If XIOR is sampled low (external pulldown) then CDCS, CDACK, CDINT, CDRQ become the standard CDROM interface pins. Since many CDROM drives do not use DMA, the CDRQ and CDACK pins are further multiplexed with MCS and MINT respectively. MCS is the Modem chip select that responds to COMbase addresses, and MINT is the modem interrupt input. These two pins comprise logical device 5. The first time COMbase is programmed to non-zero (assuming XIOR was sampled low), CDACK/MCS and CDRQ/MINT switch to MCS and MINT respectively. Once this switch occurs, the only way to revert to the CDROM DMA pins is to reset the part or remove power.

The XCTL1/SINT/ACDCS/DOWN pin state is first determined by VCEN. If VCEN is set this pin is forced to the DOWN volume control pin.

If VCEN is zero, then if ACDbase is ever programmed to a non-zero value, this pin converts to the ACDCS pin and keeps this function until the part is reset (or VCEN is set to one). If ACDbase is never programmed non-zero, then the state of XIOW at the time RESDRV is brought low determines whether the pin is XCTL1 or SINT. If XIOW is sampled low (external pulldown) then XCTL1/SINT/ACDCS/DOWN functions as an input for the synthesizer interrupt. If XIOW is sampled high (pin left unconnected) then XCTL1/SINT/ACDCS/DOWN becomes an output for XCTL1.

This part contains another multiplexed pin, SCS/UP. This pin provides the FM synthesizer chip select or the hardware volume control "volume up" feature. Since an internal FM synthesizer exists, this pin would normally be used for the volume control feature. Setting VCEN forces this pin to the UP volume control function. When VCEN is clear, this pin is the SCS chip select function.

ANALOG HARDWARE DESCRIPTION

The analog hardware consist of an MPC Level 2-compatible mixer (four stereo mix sources), three line-level stereo inputs, a stereo microphone input, a mono input, a mono output, and a stereo line output. This section describes the analog hardware needed to interface with these pins.

Line-Level Inputs Plus MPC Mixer

The analog inputs consist of four stereo analog inputs, and one mono input. As shown in Figure 4, the input to the ADCs comes from the Input Mixer that selects any combination of the following: LINE, AUX1, AUX2, MIC, the DAC output, and the output from the analog output mixer. Unused analog inputs should be connected together and then connected through a capacitor to analog ground.

The analog input interface is designed to accommodate four stereo inputs and one mono input. Four of these sources are mixed to the ADC. These inputs are: a stereo line-level input (LINE), a stereo microphone input (MIC), a stereo CD-ROM input (AUX2), and a stereo auxiliary line-level input (AUX1). The LINE and AUX1 inputs have two paths to the Input Mixer. One path is direct with no volume control. The other path goes through an inverting amplifier, which enables volume control. Care should be taken to select only one of these dual paths, because the inverting path will cancel the signal of the non-inverting path at the Input Mixer. The LINE, MIC, AUX1, and AUX2 inputs have paths after their volume controls, to the output mixer. The output mixer has the additional input of a mono input channel. All audio inputs should be capacitively coupled.

To obtain Sound Blaster mixer compatibility, the mapping of external devices to analog inputs is important. An external FM or Wavetable synthesizer analog output must be connected to the LINE input. The internal FM's volume control, when enabled, maps to the LINE analog mixer registers. The CDROM analog outputs must be connected to the AUX2 inputs, and the external Line Inputs must be connected to the AUX1 analog inputs.

Since some analog inputs can be as large as 2 V_{RMS}, the circuit shown in Figure 24 can be used to attenuate the analog input to 1 V_{RMS} which is the maximum voltage allowed for the line-level inputs.

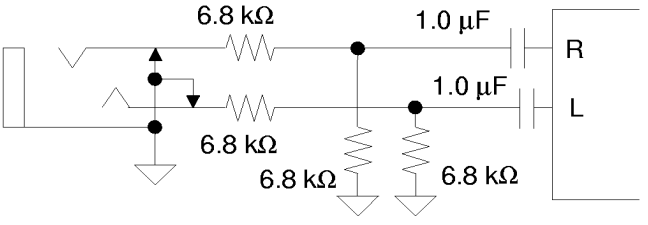


Figure 24. Line Inputs

The AUX2 line-level inputs have an extra pin, CMAUX2, which provides a pseudo-differential input for both LAUX2 and RAUX2. This pin takes the common-mode noise out of the AUX2 inputs when connected to the ground coming from the AUX2 analog source. Connecting the AUX2 pins as shown in Figure 25 provides extra noise attenuation coming from the CDROM drive, thereby producing a higher quality signal. Since the better the resistors match, the better the common-mode attenuation, one percent resistors are recommended. If CMAUX2 is not used, it should be connected through an AC cap to analog ground.

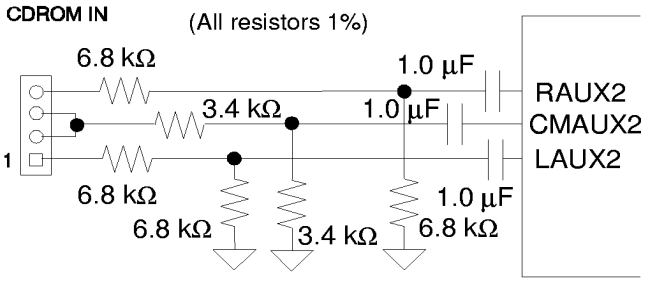


Figure 25. Differential CDROM In

Microphone Level Inputs

The microphone level inputs, LMIC and RMIC, include a selectable -22.5 dB to +22.5 dB gain stage for interfacing to an external microphone. An additional 20 dB gain block is available in the path to the output mixer. The 20 dB gain block can be switched off to provide another stereo line-level input. Figure 26 illustrates a single-ended microphone input buffer circuit that will support lower gain mics. If a mono microphone is all that is desired, the RMIC input should be connected to the output of the mono op amp, used for LMIC, through its own AC coupling capacitor. The circuit in Figure 26 supports dynamic mics and phantom-powered mics that use the right channel of the jack for power.

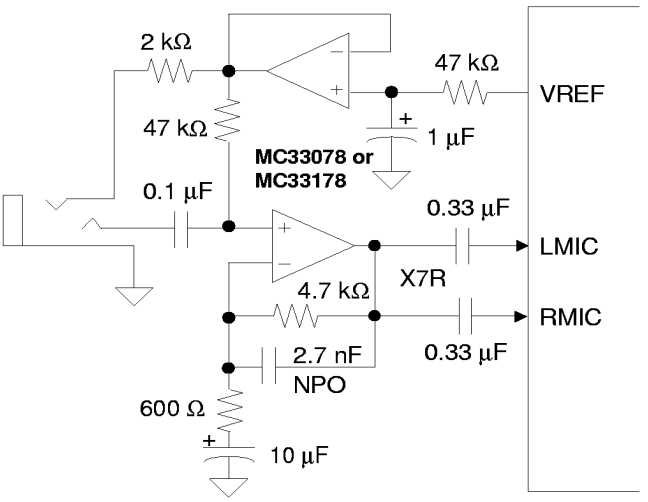


Figure 26. Left or Mono Microphone Input

Mono Input

The mono input, MIN, is useful for mixing the output of the "beeper" (timer chip), provided in all PCs, with the rest of the audio signals. The attenuation control allows 16 levels in -3dB steps. In addition, a mute control is provided. The attenuator is a single channel block with the resulting signal sent to the output mixer where it is mixed with the left and right outputs. Figure 27 illustrates a typical input circuit for the Mono In. If MIN is driven from a CMOS gate, the 4.7kΩ should be tied to AGND instead of VA+. Although this input is described for a low-quality beeper, the input is of the same high-quality as all other analog inputs and may be used for other purposes. At power-up, the MIN line is connected directly to the MOUT pin (with 9 dB of attenuation) allowing the initial beeps, heard when the computer is initializing, to pass through.

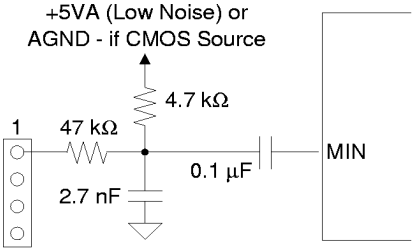


Figure 27. Mono Input

Line Level Outputs

The analog output section provides a stereo line-level output. The other output types (headphone and speaker) can be implemented with external circuitry. LOUT and ROUT outputs should be capacitively coupled to external circuitry. Both LOUT and ROUT need 1000 pF NPO capacitors between the pin and AGND.

Mono Output with Mute Control

The mono output, MOUT, is a sum of the left and right output channels, attenuated by 6dB to prevent clipping at full scale. The mono out channel can be used to drive the PC-internal mono speaker using an appropriate drive circuit. This approach allows the traditional PC-sounds to be integrated with the rest of the audio system. Figure 28 illustrates a typical speaker driver circuit. The mute control is independent of the line outputs allowing the mono channel to mute the speaker without muting the line outputs. The power-up default has MIN connected to MOUT providing a pass-through for the beeps heard at power-up.

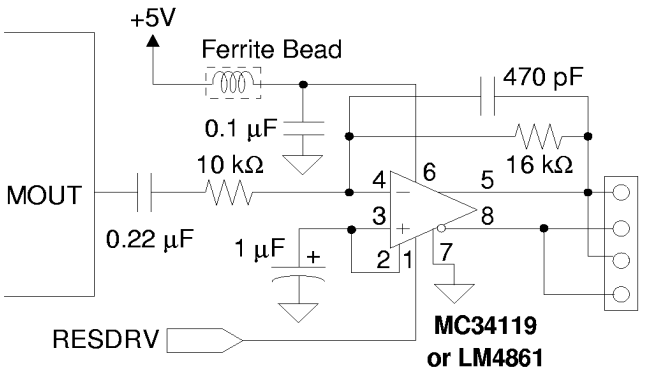


Figure 28. Mono Output

Miscellaneous Analog Signals

The LFILT and RFILT pins must have a 1000 pF NPO capacitor to analog ground. These capacitors, along with an internal resistor, provide a single-pole low-pass filter used at the inputs to the ADCs. By placing these filters at the input to the ADCs, low-pass filters at each analog input pin are avoided.

The REFFLT pin is used to lower the noise of the internal voltage reference. A 1µF (must not be greater than 1µF) and 0.1µF capacitor to analog ground should be connected with a short wide trace to this pin. No other connection should be made, as any coupling onto this pin will degrade the analog performance of the codec. Likewise, digital signals should be kept away from REFFLT for similar reasons.

The VREF pin is typically 2.2 V and provides a common mode signal for single-supply external circuits. VREF only supports light DC loads and should be buffered if AC loading is needed. For typical use, a 0.1 µF in parallel with a 10 µF capacitor should be connected to VREF.

GROUNDING AND LAYOUT

Figure 29 is a suggested layout for motherboard designs and Figure 30 is a suggested layout for add-inn cards. For optimum noise performance, the device should be located across a split analog/digital ground plane. The digital ground plane should extend across the ISA bus pins as well as the internal digital interface pins. DGND1 is ground for the data bus and should be electrically connected to the digital ground plane which will minimize the effects of the bus

interface due to transient currents during bus switching. SGND1-4 are the substrate grounds and should also be connected to the digital ground plane to minimize coupling into the analog section. Figure 31 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the part. The vias shown go through to the ground and power plane layers. Vias, power supply traces, and REFFLT traces should be as large as possible to minimize the impedance.

POWER SUPPLIES

The power supply providing analog power should be as clean as possible to minimize coupling into the analog section and degrading analog performance.

The VD1 is isolated from the rest of the power supply pins and provide digital power for the asynchronous parallel ISA bus (except for DRQA). The VD1 pin can be connected directly to the system digital power supply. VD1 can also be connected to a 3.3V supply providing a 3.3V ISA interface. When connected to a 3.3V supply, all ISA bus input pins (SA15-0, SD7-0, DACKs, etc.) must be at 3.3V levels (not 5V), with the exception of the DRQA pin. DRQA is internally connected to the VDF supplies and remains a 5 Volt pin even when the ISA bus is run at 3.3 Volts. When the ISA bus is powered from 3.3 Volts, DRQA can be be used through a level translator, or DRQA can remain used. If DRQA is not used, all references to this pin should be removed in the PnP Resource data. Even though the ISA bus is at 3.3V, the peripheral port is still at a 5V potential including XD7-0 and all chip select and address pins.

VDF1 through VDF4 provide power to internal digital sections of the codec and should be quieter than VD1. This can be achieved by using a

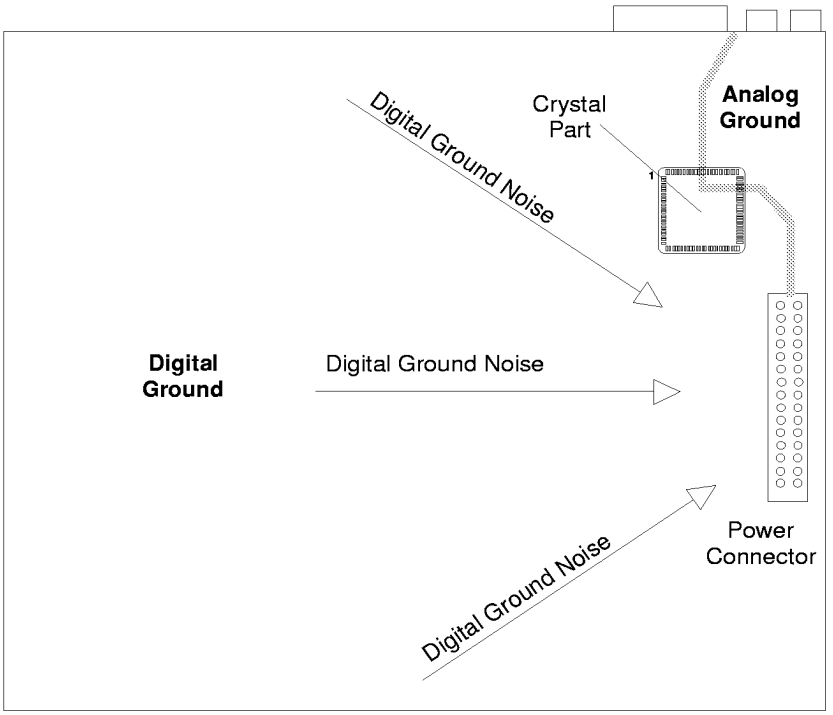


Figure 29. Suggested Motherboard Layout

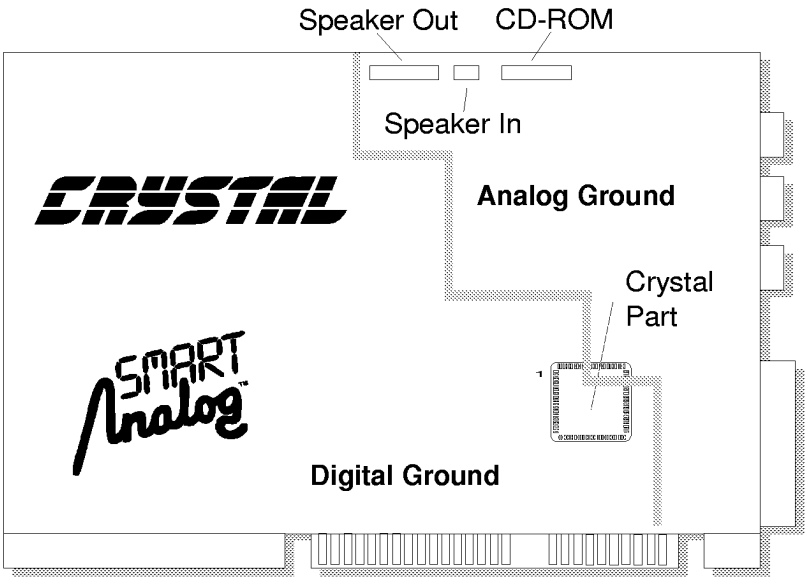


Figure 30. Suggested Add-In Card Layout

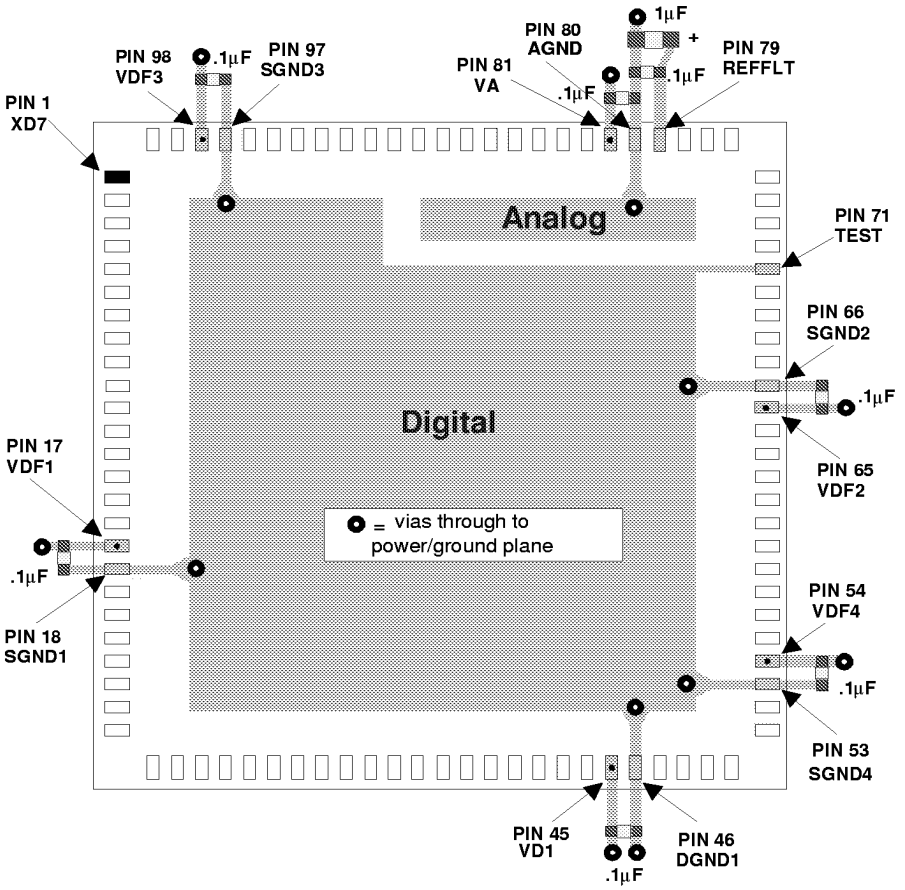


Figure 31. Recommended Decoupling Capacitor Positions

ferrite bead to the VD1 supply as shown in the *Reference Design* Data Sheet. These pins must be connected to a 5V supply.

VA provides power to the sensitive analog sections of the chip and should have a clean, regulated supply to minimize power supply coupled noise in the analog inputs and outputs.

ADC/DAC FILTER RESPONSE PLOTS

Figures 32 through 37 show the overall frequency response, passband ripple, and transition band for the ADCs and DACs. Figure 38 shows the DACs' deviation from linear phase. Since the filter response scales based on sample frequency selected, all frequency response plots x-axis are shown from 0 to 1, where 1 is equivalent to Fs. Therefore, for any given sample frequency, multiply the x-axis values by the sample frequency selected to get the actual frequency.

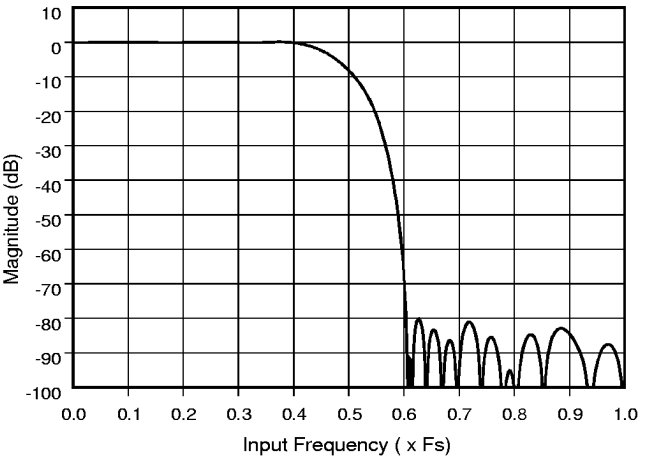


Figure 32. ADC Filter Response

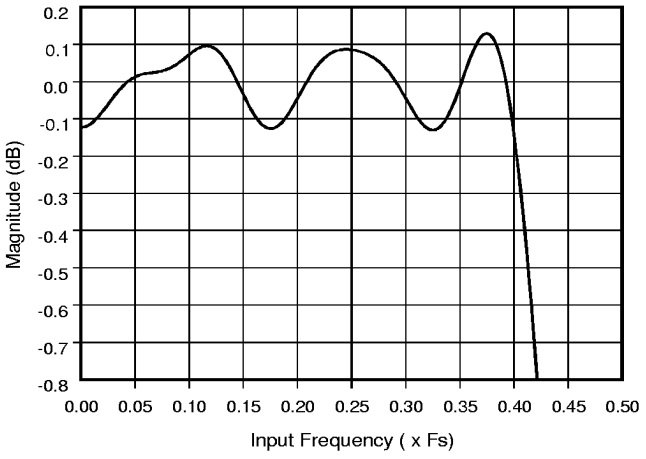


Figure 33. ADC Passband Ripple

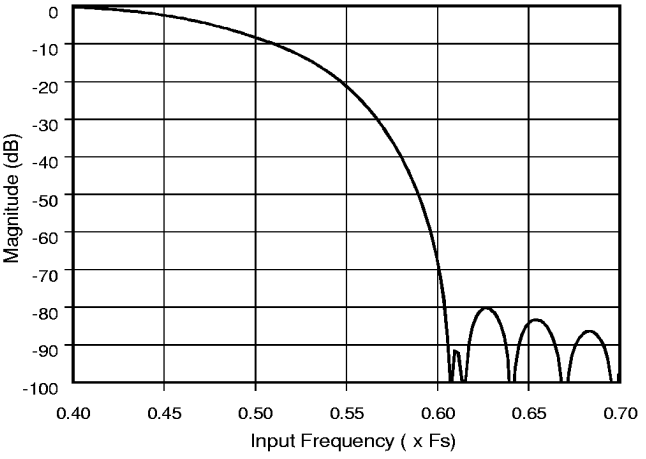


Figure 34. ADC Transition Band

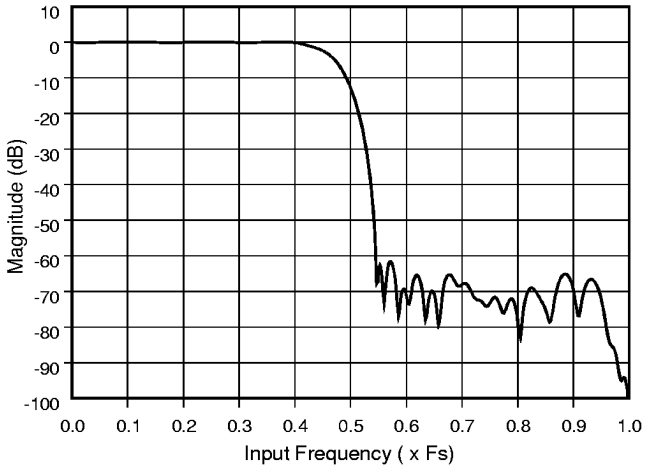


Figure 35. DAC Filter Response

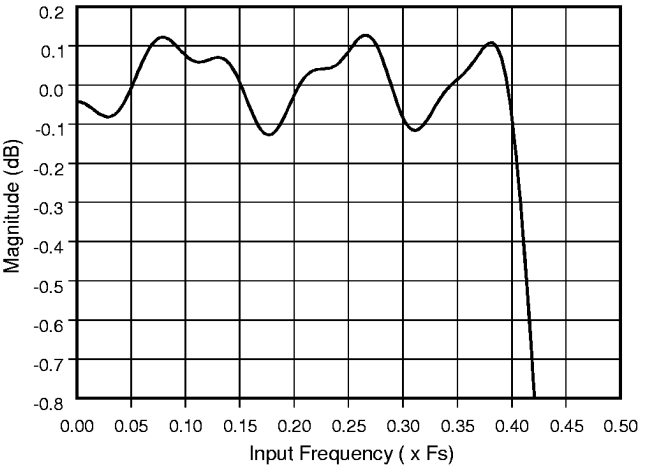


Figure 36. DAC Passband Ripple

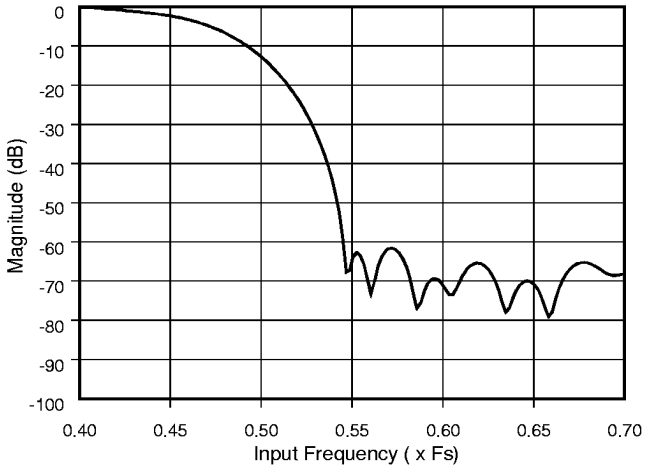


Figure 37. DAC Transition Band

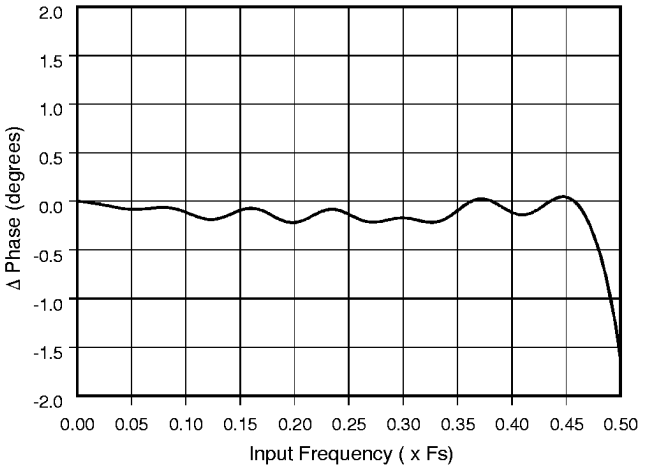
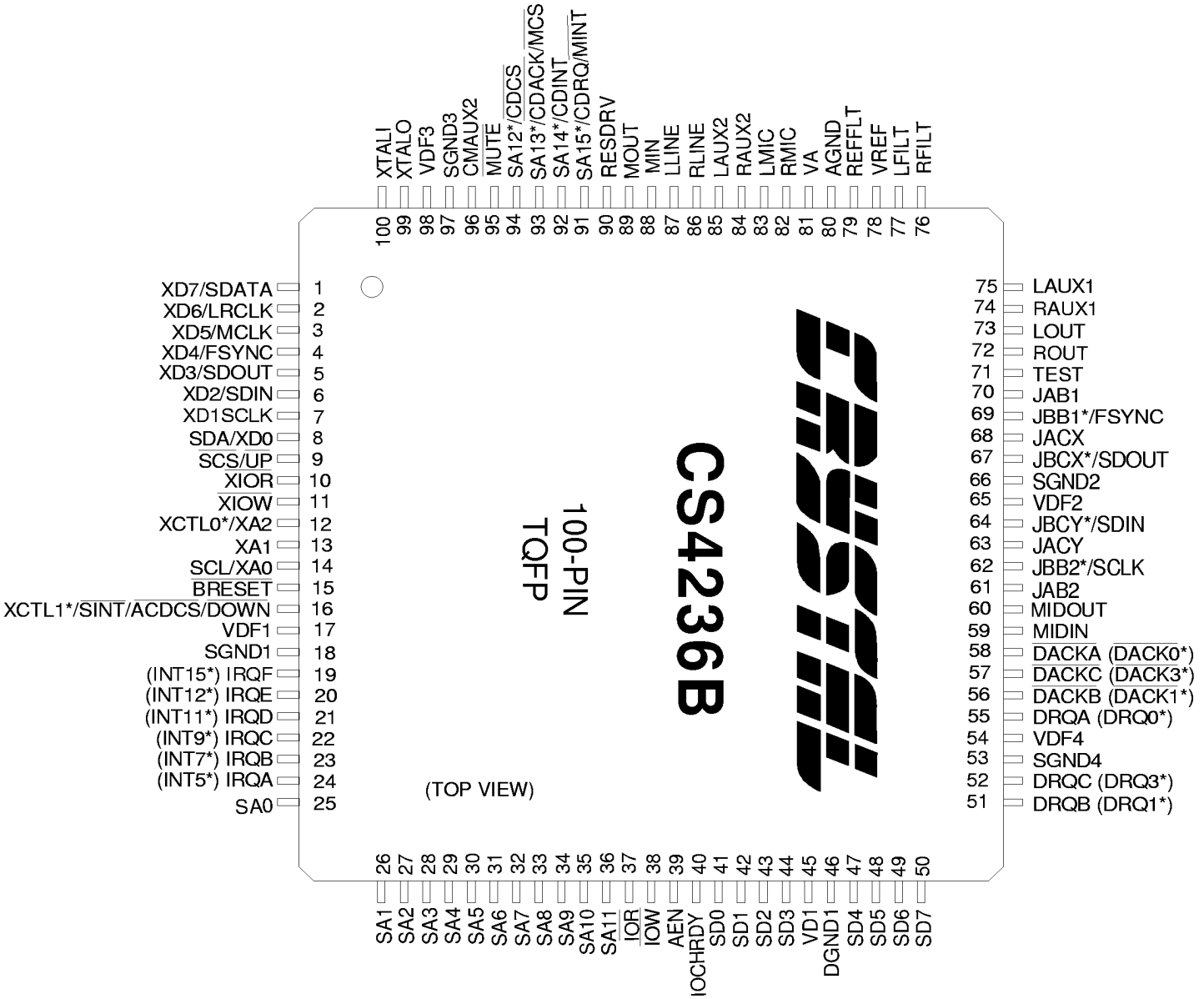


Figure 38. Deviation from Linear Phase

PIN DESCRIPTIONS



* **Defaults** – See individual pin descriptions for more details

ISA Bus Interface Pins

SA<11:0> - System Address Bus, Inputs

These signals are decoded during I/O cycles to determine access to the various functional blocks within the part as defined by the configuration data written during a Plug and Play configuration sequence.

SA<15:12> - Upper System Address Bus, Inputs

These signals are multi-function pins, shared with the CDROM and modem interface, that default to the upper address bits SA12 through SA15. These pins are generally used for motherboard designs that want to eliminate address decode aliasing. Using these pins as upper address bits forces the part to only accept valid address decodes when A12-A15 = 0. If these pins are not used for address decodes (or for CDROM support), they should be tied to SGND.

SD<7:0> - System Data Bus, Bi-directional, 24mA drive

These signals are used to transfer data to and from the part and associated peripheral devices. Reads from peripheral devices can be disabled (the part does not drive the SD<7:0> pins) by setting the SDD bit in the Hardware Configuration data. Reads from peripheral devices are automatically disabled whenever the XD pins are used as serial port pins (SPS/SPE or WTEN set to one).

AEN - Address Enable, Input

This signal indicates whether the current bus cycle is an I/O cycle or a DMA cycle. This signal is low during an I/O cycle and high during a DMA cycle.

$\overline{\text{IOR}}$ - Read Command Strobe, Input

This active low signal defines a read cycle to the part. The cycle may be a register read or a read from the part's DMA registers.

$\overline{\text{IOW}}$ - Write Command Strobe, Input

This active low signal indicates a write cycle to the part. The cycle may be a write to a control register or a DMA register.

IOCHRDY - I/O Channel Ready, Open Drain Output, 8mA drive

This signal is driven low by the part during ISA bus cycles in which the part is not able to respond within a minimum cycle time. IOCHRDY is forced low to extend the current bus cycle. The bus cycle is extended until IOCHRDY is brought high.

DRQ<A,B,C> - DMA Requests, Outputs, 24mA drive

These active high outputs are generated when the part is requesting a DMA transfer. This signal remains high until all the bytes have been transferred as defined by the current transfer data type. The DRQ<A,B,C> outputs must be connected to 8-bit DMA channel request signals only. The defaults on the ISA bus are DRQA = DRQ0, DRQB = DRQ1, and DRQC = DRQ3. The defaults can be changed by modifying the Hardware Resource data. Note that DRQA is a 5 Volt-only pin. When the ISA bus is run at 3.3 Volts, DRQA can either be used with the proper level translator, or DRQA can be left unconnected and not used.

$\overline{\text{DACK}}$<A,B,C> - DMA Acknowledge, Inputs

The assertion of these active low signals indicate that the current DMA request is being acknowledged and the part will respond by either latching the data present on the data bus (write) or putting data on the bus (read). The $\overline{\text{DACK}}$<A,B,C> inputs must be connected to 8-bit DMA channel acknowledge lines only. The defaults on the ISA bus are $\overline{\text{DACKA}}$ = $\overline{\text{DACK0}}$, $\overline{\text{DACKB}}$ = DACK1, and $\overline{\text{DACKC}}$ = DACK3. The defaults can be changed by modifying the Hardware Resource data.

IRQ <A:F>- Host Interrupt Pins, Outputs, 24mA drive

These signals are used to notify the host of events which need servicing. They are connected to specific interrupt lines on the ISA bus. The IRQ<A:F> are individually enabled as per configuration data that is generated during a Plug and Play configuration sequence. The defaults on the ISA bus are IRQA = INT5, IRQB = INT7, IRQC = INT9, IRQD = INT11, IRQE = INT12, IRQF = INT15. The defaults can be changed by modifying the Hardware Configuration data loaded from the E^2PROM.

Analog Inputs

LLINE - Left Line Input

Nominally 1 V_{RMS} max analog input for the Left LINE channel, centered around VREF. A programmable gain block provides volume control and is located in either I18 or X0 based on how synthesis is mapped. LLINE is typically used for Left Channel Synthesis (FM or Wavetable).

RLINE - Right Line Input

Nominally 1 V_{RMS} max analog input for the Right LINE channel, centered around VREF. A programmable gain block provides volume control and is located in either I19 or X1 based on how synthesis is mapped. RLINE is typically used for Right Channel Synthesis (FM or Wavetable).

LMIC - Left Mic Input

Microphone input for the Left MIC channel, centered around VREF. A programmable gain block provides volume control and is located in X2. In MODE 3, the output mixer has an extra selectable 20 dB of gain controlled by the LMBST bit.

RMIC - Right Mic Input

Microphone input for the Right MIC channel, centered around VREF. A programmable gain block provides volume control and is located in X3. In MODE 3, the output mixer has an extra selectable 20 dB of gain controlled by the RMBST bit.

LAUX1 - Left Auxiliary #1 Input

Nominally 1 V_{RMS} max analog input for the Left AUX1 channel, centered around VREF. A programmable gain block provides volume control and is located in I2. Typically used for an external Left line-level input.

RAUX1 - Right Auxiliary #1 Input

Nominally 1 V_{RMS} max analog input for the Right AUX1 channel, centered around VREF. A programmable gain block provides volume control and is located in I3. Typically used for an external Right line-level input.

LAUX2 - Left Auxiliary #2 Input

Nominally 1 V_{RMS} max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block provides volume control and is located in I4. Typically used for the Left channel CDROM input.

RAUX2 - Right Auxiliary #2 Input

Nominally 1 V_{RMS} max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block provides volume control and is located in I5. Typically used for the Right channel CDROM input.

CMAUX2 - Common Mode Auxiliary #2 Input

Common mode ground input for the LAUX2 and RAUX2 inputs. Typically connected to the CDROM ground input to provide common-mode noise rejection. The impedance on this pin should be one half the impedance on the LAUX2 and RAUX2 inputs.

MIN - Mono Input

Nominally 1 V_{RMS} max analog input, centered around VREF, that goes through a programmable gain stage (I26) into both channels of the output mixer. This is a general purpose mono analog input that is normally used to mix the typical "beeper" signal on most computers into the audio system.

Analog Outputs

LOUT - Left Line Level Output

Analog output from the mixer for the left channel. Nominally 1 V_{RMS} max centered around VREF. This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

ROUT - Right Line Level Output

Analog output from the mixer for the Right channel. Nominally 1 V_{RMS} max centered around VREF. This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

MOUT - Mono Output

MOUT is nominally 1 V_{RMS} max analog output, centered around VREF. This output is a summed analog output from both the left and right output channels of the mixer. MOUT typically is connected to a speaker driver that drives the internal speaker in most computers. In MODE2, MOM in I26 mutes both channels going into MOUT. In MODE 3, MOM in I26 mutes the left channel and MOMR in X5 mutes the right channel.

MIDI Interface

MIDOUT - MIDI Out Transmit Data, Output, 4mA drive

This output is used to send MIDI data serially out to a external MIDI device. Normally connected to pin 12 of the joystick connector for use with breakout boxes.

MIDIN - MIDI In Receive Data, Input

This input is used to receive serial MIDI data from an external MIDI device. This pin should have a 4.7 kΩ pullup attached and is normally connected to pin 15 of the joystick connector for use with breakout boxes.

External FM Synthesizer Interface

$\overline{\text{SCS}}$ - Synthesizer Chip Select, Output, 4 mA drive

By default, $\overline{\text{SCS}}$/UP is an active low output forced low when a valid address decode to an external FM synthesizer, as defined in the Plug and Play configuration registers, has occurred. When the internal FM synthesizer is enabled, this pin is no longer used as an FM synthesizer chip select. This pin can be used for a hardware volume up pin by setting VCEN in the Hardware Configuration data.

$\overline{\text{SINT}}$ - Synthesizer Interrupt, Input

This pin, XCTL1/$\overline{\text{SINT}}$/$\overline{\text{ACDCS}}$/$\overline{\text{DOWN}}$, defaults to the XCTL1 output which is controlled by the XCTL1 bit in the WSS register I10. If VCEN in the Hardware Configuration data is set, this pin converts to the $\overline{\text{DOWN}}$ volume control function. If VCEN is zero, and ACDbase is never programmed to a non-zero value, this pin can be changed to $\overline{\text{SINT}}$ input by connecting a 10 kΩ resistor between the $\overline{\text{XIOW}}$ pin and SGND. The polarity of $\overline{\text{SINT}}$ can be programmed through CTRLbase+1 register, the ISH bit, or the Hardware Configuration data. $\overline{\text{SINT}}$ defaults to an active low input that should be driven by the external FM synthesizer interrupt output pin. This pin can also be configured at a second CDROM Chip Select, $\overline{\text{ACDCS}}$, to support the alternate IDE CDROM decode. (See the CDROM section for more information.) The pin is switched to the CDROM alternate chip select when VCEN is zero and the base address is first programmed to non-zero through the E^2PROM data or PnP commands.

External Peripheral Port

XD<7:1> - External Data Bus bits 7 through 1, Bi-directional, 4mA drive

These pins are used to transfer data between the ISA bus and external devices such as the modem and CDROM. These pins are also multiplexed with two serial ports. A DSP serial port can be connected through the XD4-XD1 pins. This interface is multiplexed onto these external data bus pins OR the 2nd Joystick pins based on the SPS (Serial Port Switch) bit. The second serial port connects to the CS9236 Single-Chip Wavetable Music Synthesizer and uses pins XD7-XD5. This serial port is enabled via the WTEN bit. Both SPS and WTEN are located in either C8 in the Control logical device, or the Global Configuration byte in the E^2PROM Hardware Configuration data.

SDA/XD0 - External Data Bus bit 0/E^{2}PROM Data Pin, Bi-directional, Open Drain,4mA sink

This open-drain pin must have an external pullup (3.3 kΩ) and is used to transfer data between the ISA bus bit 0, SD0, and external devices such as a modem or CDROM. SDA/XD0 is also used in conjunction with SCL/XA0 to access an external serial E^{2}PROM. When an E^{2}PROM is used, the SDA/XD0 pin should be connected to the data pin of the E^{2}PROM device and provides a bi-directional data port. The E^{2}PROM is used to set the Plug and Play resource data.

XCTL0/XA2 - XCTL0 or External Address SA2, Output, 4mA drive

This pin either outputs ISA bus address SA2 or XCTL0 depending on the Hardware Configuration data. The default is XCTL0 which is controlled by the XCTL0 bit in the WSS register I10. This pin changes to address bit XA2 if the Hardware Configuration data indicates that the peripheral port requires more than four I/O addresses.

XA1 - External Address, Output, 4mA drive

This pin outputs ISA bus address SA1.

XA0/SCL - External Address, Output/Serial Clock, Output, 4mA drive

This pin outputs the ISA bus address SA0. When E^{2}PROM access is enabled, via EEN in CTRLbase+1, then SCL is used as a clock output to the E^{2}PROM.

$\overline{\text{BRESET}}$ - Buffered Reset, Output, 4mA drive

This active low signal goes low whenever the RESDRV pin goes high. This pin is also software controllable through the BRES bit in register C8 in the Control Logical Device space. BRES provides a software power down and reset control over devices connected to the Crystal Codec such as the CS9236 Single-Chip Wavetable Music Synthesizer.

$\overline{\text{XIOR}}$ - External Read Strobe, Output, 4mA drive (SA12-SA15/CDROM selection)

This active low signal goes low whenever ($\overline{\text{SCS}}$, $\overline{\text{CDCS}}$, or $\overline{\text{MCS}}$) and $\overline{\text{IOR}}$ goes low. When RESDRV goes low, this pin also selects either the CDROM/Modem port or SA12 - SA15 and contains an internal pullup of approximately 100 kΩ. When $\overline{\text{XIOR}}$ is left high (default), pins 91-94 are SA15-SA12 respectively. To enable the CDROM and Modem ports, an external 10kΩ resistor must be tied between this pin and SGND.

$\overline{\text{XIOW}}$ - External Write Strobe, Output, 4mA drive (XCTL1/$\overline{\text{SINT}}$/$\overline{\text{ACDCS}}$/$\overline{\text{DOWN}}$ selection)

This active low signal goes low whenever ($\overline{\text{SCS}}$ or $\overline{\text{CDCS}}$ or $\overline{\text{MCS}}$) and $\overline{\text{IOW}}$ goes low. When RESDRV goes low, this pin also selects either XCTL1 or $\overline{\text{SINT}}$ and contains an internal pullup of approximately 100 kΩ. When $\overline{\text{XIOW}}$ is left high (default), pin 16 is the XCTL1 function (or $\overline{\text{ACDCS}}$, based on a non-zero value being programmed into the alternate CDROM address register). To change the pin to $\overline{\text{SINT}}$, an external 10kΩ resistor must be tied between this pin and SGND.

Joystick/DSP Serial Port Interface

JACX, JACY - Joystick A Coordinates, Input

These pins and are the X/Y coordinates for Joystick A. They should have a 5.6nF capacitor to ground and a 2.2kΩ resistor to the joystick connector pins 3 and 6, respectively.

JAB1, JAB2 - Joystick A Buttons, Input

These pins are the switch inputs for Joystick A. They should be connected to joystick connector pins 2 and 7, respectively; as well as have a 1nF capacitor to ground, and a 4.7kΩ pullup resistor.

JBCX/SDOUT - Joystick B Coordinate X/Serial Data Output, Input/Output

When this pin is used as a second joystick, it is the X coordinates input for Joystick B; and should have a 5.6nF capacitor to ground and a 2.2kΩ resistor to the joystick connector pin 11. When the serial port is enabled, SPE = 1 in I16, this pin is the serial data output. The DSP serial port SDOUT pin can be switched to XD3 via the SPS bit. This would facilitate using the DSP serial port and the second joystick simultaneously.

JBCY/SDIN - Joystick B Coordinate Y/Serial Data Input, Input

When this pin is used as a second joystick, it is the Y coordinates input for Joystick B; and should have a 5.6nF capacitor to ground and a 2.2kΩ resistor to the joystick connector pin 13. When the serial port is enabled, SPE = 1 in I16, this pin is the serial data input. The DSP serial port SDIN pin can be switched to XD2 via the SPS bit. This would facilitate using the DSP serial port and the second joystick simultaneously.

JBB1/FSYNC - Joystick B Button 1/Frame Sync, Input/Output

When this pin is used as a second joystick, it is the switch 1 input for Joystick B; and should be connected to joystick connector pin 10; as well as have a 1nF capacitor to ground, and a 4.7kΩ pullup resistor. When the serial port is enabled, SPE = 1 in I16, this pin is the serial frame sync output. The DSP serial port FSYNC pin can be switched to XD4 via the SPS bit. This would facilitate using the DSP serial port and the second joystick simultaneously.

JBB2/SCLK - Joystick B Button 2/Serial Clock, Input/Output

When this pin is used as a second joystick, it is the switch 2 input for Joystick B; and should be connected to joystick connector pin 14; as well as have a 1nF capacitor to ground, and a 4.7kΩ pullup resistor. When the serial port is enabled, SPE = 1 in I16, this pin is the serial clock output. The DSP serial port SCLK pin can be switched to XD1 via the SPS bit. This would facilitate using the DSP serial port and the second joystick simultaneously.

CS9236 Wavetable Serial Port Interface

A digital interface to the Crystal CS9236 Single-Chip Wavetable Music Synthesizer is provided that allows the CS9236 PCM audio data to be summed digitally on the Crystal Codec without the need for an external DAC. The Wavetable Serial Port interface pins are multiplexed with the XD7-XD5 external bus pins. This serial port is enabled via the WTEN bit which is located in the Global Configuration byte in the E^2PROM Hardware Configuration data, or C8. The interface typically consists of the three pins listed below as well as:
connecting the Crystal Codec MIDOUT pin to the CS9236 MIDI_IN pin, and
connecting the Crystal Codec BRESET pin to the CS9236 PDN and RST pins.
(The BRES bit in C8 provides a maximum software power-down mode for the CS9236 by driving the BRESET signal low whenever BRES is set.)

SDATA - Wavetable Serial Audio Data, Input

This pin is multiplexed with the XD7 external data bus pin. When use as SDATA, this input supplies the serial audio PCM data to be digitally mixed to the DACs of the Crystal codec. The data consists of left and right channel 16-bit data delineated by LRCLK. This pin should be connected to the SOUT output pin on the CS9236. This pin should also have a weak pull-down resistor of approx. 100 kΩ to minimize power-down currents and allow for stuffing options.

LRCLK - Wavetable Serial Left/Right Clock, Input

This pin is multiplexed with the XD6 external data bus pin. When use as LRCLK, this input supplies the serial data alignment signal that delineates left from right data. This pin should be connected to the LRCLK output pin on the CS9236. This pin should also have a weak pull-down resistor of approx. 100 kΩ to minimize power-down currents and allow for stuffing options.

MCLK - Wavetable Master Clock, Output

This pin is multiplexed with the XD5 external data bus pin. When use as MCLK, this output supplies the 16.9344 MHz master clock that controls all the timing on the CS9236. This pin should be connected to the MCLK5I input pin on the CS9236. MCLK can be disabled in software using the DMCLK bit in C8 in the Control logical device space. DMCLK provides a partial software power-down mode for the CS9236.

CDROM and Modem Interface

The four CDROM pins are multi-function and default to ISA upper address bits SA12-SA15. To enable the CDROM port, an external 10kΩ resistor must be tied between $\overline{\text{XIOR}}$ and SGND. $\overline{\text{XIOR}}$ is sampled on the falling edge of RESDRV. If the CDROM interface doesn't support DMA, the two CDROM DMA pins can be converted to support Logical Device 5, a modem interface.

$\overline{\text{CDCS}}$ - CDROM Chip Select, Output, 4mA drive

This output goes low whenever an address is decoded that matches the value programmed into the CDROM base address register.

$\overline{\text{ACDCS}}$ - Alternate CDROM Chip Select, Output, 4mA drive

This pin, XCTL1/SINT/ACDCS/DOWN, is multiplexed with three other functions, and defaults to the XCTL1 output which is controlled by the XCTL1 bit in the WSS I10. This pin can also be configured at a second CDROM Chip Select, $\overline{\text{ACDCS}}$, to support the alternate IDE CDROM decode. The pin is switched to the CDROM alternate chip select when the base address ACDbase is first programmed to non-zero through the E^2PROM data or PnP commands. This output then goes low whenever an address is decoded that matches the value programmed into the CDROM alternate base address register, ACDbase. This pin can also be used as the volume up pin $\overline{\text{DOWN}}$ by setting VCEN in Control register C0 or the Hardware Configuration data. VCEN has the highest precedence over the other pin functions.

CDINT - CDROM Interrupt, Input

This pin is used to input an interrupt signal from the CDROM interface. The part can be programmed, through the plug-and-play resource data, to output this signal to the appropriate ISA bus interrupt line. The polarity if this input can be programmed through CTRLbase+1 register, bit ICH, or the Hardware Configuration data; the default is active high.

CDRQ/MINT - CDROM DMA Request, or Modem Interrupt, Input

This pin can be used to input the DMA request signal from the CDROM interface. The part can be programmed, through the plug-and-play resource data, to output this signal to the appropriate ISA bus DRQ line.

This pin can also be used to input an interrupt signal from a modem. The pin is switched to MINT when the LD5 base address, COMbase, is first programmed to non-zero through the PnP data or a hostload. The polarity of MINT can be programmed through CTRLbase+1 register, IMH bit, or the Hardware Configuration data; the default is active low.

$\overline{\text{CDACK}}$/$\overline{\text{MCS}}$ - CDROM DMA Acknowledge, or Modem Chip Select, Output, 4mA drive

This pin can be used to output the ISA bus-generated DMA acknowledge signal to the $\overline{\text{CDROM}}$ interface. Alternately, this pin can be used to output an active low Modem chip select, $\overline{\text{MCS}}$. The pin is switched to the modem chip select when the LD5 base address, COMbase, is first programmed to non-zero through the PnP data or a hostload.

Volume Control

The volume control pins are enabled by setting VCEN in the Hardware Configuration data, Misc. Hardware Config. byte. The VCF1,0 bits in the Hardware Configuration data, Global Configuration byte, set the format for the volume control pins. Each pin must have an external pullup resistor (10kΩ) and either a momentary or toggle style switch based on format. Typically a 100Ω series resistor and a capacitor to ground, capacitor on the switch side of the series resistor, would be included on each pin for ESD protection and to help with EMI emissions.

$\overline{\text{UP}}$ - Volume Up

The SCS/$\overline{\text{UP}}$ pin is multiplexed with the external Synthesizer chip select. This pin is switched to the $\overline{\text{UP}}$ function when VCEN is set. When $\overline{\text{UP}}$ is low, the master volume output for left and right channels are incremented.

$\overline{\text{DOWN}}$ - Volume Down

The XCTL1/$\overline{\text{SINT}}$/$\overline{\text{ACDCS}}$/$\overline{\text{DOWN}}$ is a multiplexed pin that can be used as XCTL1, the external FM synthesizer interrupt, the alternate CDROM chip select, or the Volume Down pin. This pin is switched to the $\overline{\text{DOWN}}$ function when VCEN is set. When $\overline{\text{DOWN}}$ is low, the master volume output for left and right channels are decremented.

$\overline{\text{MUTE}}$ - Volume Mute

The $\overline{\text{MUTE}}$ pin function can be toggle, momentary, or non-existent based on the VCF1,0 bits. The $\overline{\text{MUTE}}$ function is enabled when VCEN is set.

Miscellaneous

XTALI - Crystal Input

This pin will accept either a crystal, with the other pin attached to XTALO, or an external CMOS clock. XTAL must have a crystal or clock source attached for proper operation. The crystal frequency must be 16.9344 MHz and designed for fundamental mode, parallel resonance operation.

XTALO - Crystal Output

This pin is used for a crystal placed between this pin and XTALI. If an external clock is used on XTALI, this pin must be left floating with no traces or components connected to it.

RESDRV - Reset Drive, Input

Places the part in lowest power consumption mode. All sections of the part are shut down and consuming minimal power. The part is reset and in power down mode when this pin is logic high. The falling edge also latches the state of $\overline{\text{XIOR}}$ and $\overline{\text{XIOW}}$ to determine the functionality of dual mode pins. This signal is typically connected to the ISA bus signal RESDRV. RESDRV must be asserted whenever the part is powered up to initialize the internal registers to a known state. This pin, when high, also drives the $\overline{\text{BRESET}}$ pin low.

VREF - Voltage Reference, Output

All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered.

REFFLT - Reference Filter, Input

Voltage reference used internal to the part. A 0.1 µF and a 1 µF (must not be bigger than 1 µF) capacitor with short fat traces must be connected to this pin. No other connections should be made to this pin.

LFILT - Left Channel Antialias Filter Input

This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

RFILT - Right Channel Antialias Filter Input

This pin needs a 1000 pF NPO capacitor attached and tied to analog ground.

TEST - Test

This pin must be tied to ground for proper operation.

Power Supplies

VA - Analog Supply Voltage

Supply to the analog section of the codec.

AGND - Analog Ground

Ground reference to the analog section of the codec. This pin should be placed on an analog ground pin separate from other chip grounds.

VD1 - Digital Supply Voltage

Digital supply for the parallel data bus section of the codec.

DGND1 - Digital Ground

Digital ground reference for the parallel data bus section of the part. These pins are isolated from the other grounds and should be connected to the digital ground section of the board (see Figure 31).

VDF1, VDF2, VDF3, VDF4 - Digital Filtered Supply Voltage

Digital supply for the internal digital section of the codec (except for the parallel data bus). These pins should be filtered, using a ferrite bead, from VD1.

SGND1, SGND2, SGND3, SGND4 - Substrate Ground

Substrate ground reference for the codec . These pins are connected to the substrate of the die. Optimum layout is achieved by placing SGND1/2/3/4 on the digital ground plane with the DGND pin as shown in Figure 31.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

Total Dynamic Range

TDR is the ratio of the RMS value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale RMS signal to the RMS noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the RMS sum of all the in-band harmonics of the test signal. THD is measured using an input signal which is 3dB below typical full-scale, and referenced to typical full scale.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

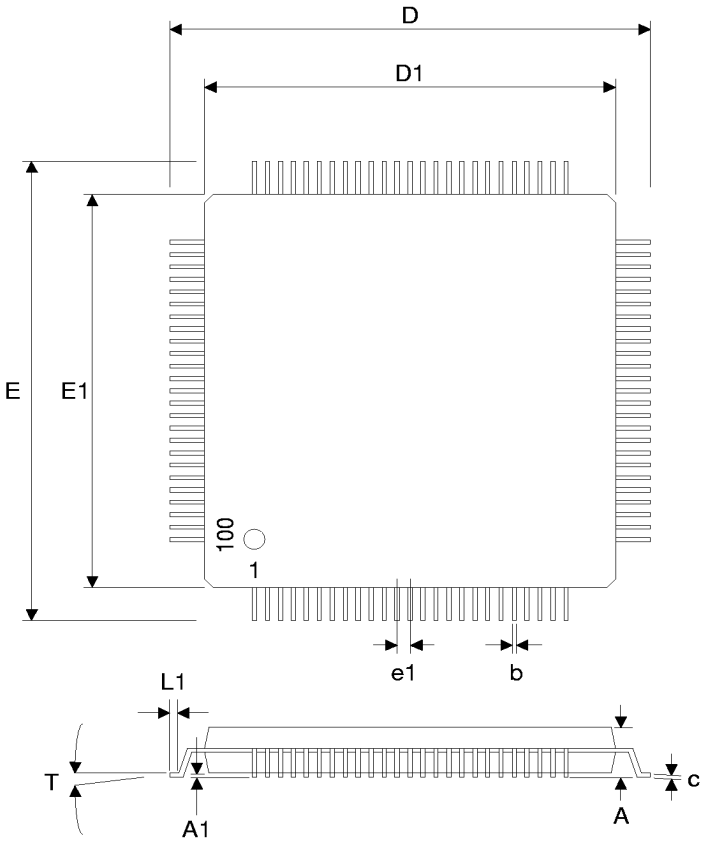
Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation in volts of the output from VREF with mid-scale input code.

PACKAGE PARAMETERS



100-pin TQFP - Package Code 'Q'

Symbol	Description	MIN	NOM	MAX
N	Lead Count		100	
A	Overall Height			1.66
A1	Stand Off	0.00		
b	Lead Width	0.14	0.20	0.26
c	Lead Thickness	0.077	0.127	0.177
D	Terminal Dimension	15.70	16.00	16.30
D1	Package Body		14.0	
E	Terminal Dimension	15.70	16.00	16.30
E1	Package Body		14.0	
e1	Lead Pitch	0.40	0.50	0.60
L1	Foot Length	0.30	0.50	0.70
T	Lead Angle	0.0°		12.0°

Notes:
1) Dimensions in millimeters.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm.
3) Coplanarity is 0.004 in.
4) Lead frame material is AL-42 or copper, and lead finish is solder plate.
5) Pin 1 identification may be either ink dot or dimple.
6) Package top dimensions can be smaller than bottom dimensions by 0.20 mm.
7) The "lead width with plating" dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
8) Ejector pin marks in molding are present on every package.

APPENDIX A: TYPICAL MOTHERBOARD E^{2}PROM DATA

```
; EEPROM Validation Bytes
   DB       055H, 0BBH                  ; EEPROM Validation Bytes: CS4236B

   DB       001H                         ; EEPROM data length upper byte
   DB       00FH                         ; lower byte, Listed Size = 271

; Hardware Configuration Data
   DB       000H                         ; ACDbase Addr. Mask Length = 1 bytes
   DB       003H                         ; COMbase Addr. Mask Length = 4 bytes
   DB       080H                         ; MCB: IHCD
   DB       080H                         ; GCB1: IFM
   DB       00BH                         ; Code Base Byte
   DB       020H                         ; RESERVED
   DB       004H                         ; RESERVED
   DB       008H                         ; RESERVED
   DB       010H                         ; RESERVED
   DB       080H                         ; RESERVED
   DB       000H                         ; RESERVED
   DB       000H                         ; RESERVED

; Hardware Mapping Data
   DB       000H                         ; 00=4/08=8 peripheral port size, XCTL0/XA2
   DB       048H                         ; RESERVED
   DB       075H                         ; IRQ selection A & B - B= 7,   A=5
   DB       0B9H                         ; IRQ selection C & D - D=11,   C=9
   DB       0FCH                         ; IRQ selection E & F - F=15,   E=12
   DB       010H                         ; DMA selection A & B - B= 1,   A=0
   DB       003H                         ; DMA selection C      -         C=3

; PnP Resource Header - PnP ID for CS4236B IC, OEM ID = 42
   DB       00EH, 063H, 042H, 035H, 0FFH,0FFH,0FFH,0FFH,002H  ; CSC4235 FFFFFFFF
   DB       00AH, 010H, 001H          ; PnP version 1.0, Vender version 0.1
   DB       082H, 009H, 000H, 'CMB4236B', 000H ; ANSI ID

; LOGICAL DEVICE 0 (Windows Sound System & SBPro)
   DB       015H, 00EH, 063H, 000H, 000H, 000H ; EISA ID: CSC0000

   DB       082H, 007H, 000H, 'WSS/SB', 000H ; ANSI ID
   DB       031H, 000H                ; DF Best Choice
   DB       02AH, 002H, 028H          ; DMA: 1   - WSS & SBPro
   DB       02AH, 009H, 028H          ; DMA: 0,3   - WSS & SBPro capture
   DB       022H, 020H, 000H          ; IRQ: 5   Interrupt Select 0
   DB       047H, 001H, 034H, 005H, 034H, 005H, 004H, 004H ;16b WSSbase: 534
   DB       047H, 001H, 088H, 003H, 088H, 003H, 008H, 004H ;16b SYNbase: 388
   DB       047H, 001H, 020H, 002H, 020H, 002H, 020H, 010H ;16b SBbase: 220

   DB       031H, 001H                ; DF Acceptable Choice 1
   DB       02AH, 00AH, 028H          ; DMA: 1,3   - WSS & SBPro
   DB       02AH, 00BH, 028H          ; DMA: 0,1,3   - WSS & SBPro capture
   DB       022H, 0A0H, 09AH          ; IRQ: 5,7,9,11,12,15   Interrupt Select 0
```

```
   DB       047H, 001H, 034H, 005H, 0FCH, 00FH, 004H, 004H ;16b WSSbase: 534-FFC
   DB       047H, 001H, 088H, 003H, 088H, 003H, 008H, 004H ;16b SYNbase: 388
   DB       047H, 001H, 020H, 002H, 060H, 002H, 020H, 010H ;16b SBbase: 220-260

   DB       031H, 002H                ; DF Suboptimal Choice 1
   DB       02AH, 00BH, 028H          ; DMA: 0,1,3  - WSS & SBPro
   DB       022H, 0A0H, 09AH          ; IRQ: 5,7,9,11,12,15  Interrupt Select 0
   DB       047H, 001H, 034H, 005H, 0FCH, 00FH, 004H, 004H ;16b WSSbase: 534-FFC
   DB       047H, 001H, 088H, 003H, 0F8H, 003H, 008H, 004H ;16b SYNbase: 388-3F8
   DB       047H, 001H, 020H, 002H, 000H, 003H, 020H, 010H ;16b SBbase: 220-300

   DB       038H                      ; End of DF for Logical Device 0


; LOGICAL DEVICE 1 (Game Port)
   DB       015H, 00EH, 063H, 000H, 001H, 000H ; EISA ID: CSC0001

   DB       082H, 005H, 000H, 'GAME', 000H ; ANSI ID
   DB       031H, 000H                ; DF Best Choice
   DB       047H, 001H, 000H, 002H, 000H, 002H, 008H, 008H ;16b GAMEbase: 200

   DB       031H, 001H                ; DF Acceptable Choice 1
   DB       047H, 001H, 008H, 002H, 008H, 002H, 008H, 008H ;16b GAMEbase: 208

   DB       038H                      ; End of DF for Logical Device 1


; LOGICAL DEVICE 2 (Control)
   DB       015H, 00EH, 063H, 000H, 010H, 000H ; EISA ID: CSC0010

   DB       082H, 005H, 000H, 'CTRL', 000H ; ANSI ID
   DB       047H, 001H, 020H, 001H, 0F8H, 00FH, 008H, 008H ;16b CTRLbase: 120-FF8

; LOGICAL DEVICE 3 (MPU-401)
   DB       015H, 00EH, 063H, 000H, 003H, 000H ; EISA ID: CSC0003

   DB       082H, 004H, 000H, 'MPU', 000H ; ANSI ID
   DB       031H, 000H                ; DF Best Choice
   DB       022H, 000H, 002H          ; IRQ: 9  Interrupt Select 0
   DB       047H, 001H, 030H, 003H, 030H, 003H, 008H, 002H ;16b MPUbase: 330

   DB       031H, 001H                ; DF Acceptable Choice 1
   DB       022H, 000H, 09AH          ; IRQ: 9,11,12,15  Interrupt Select 0
   DB       047H, 001H, 030H, 003H, 060H, 003H, 008H, 002H ;16b MPUbase: 330-360

   DB       031H, 002H                ; DF Suboptimal Choice 1
   DB       047H, 001H, 030H, 003H, 0E0H, 003H, 008H, 002H ;16b MPUbase: 330-3E0

   DB       038H                      ; End of DF for Logical Device 3


   DB       079H, 0A0H                ; End of Resource Data, Checksum
```

APPENDIX B: DIFFERENCES BETWEEN THE CS4236 AND THE CS4236B

This part is designed to be hardware and software backwards compatible with the CS4236 and will drop into an existing CS4236 socket without any hardware modifications. Properly written code for the CS4236 will run on the this Codec. However, the CS4236B has enhancements over the CS4236 that provide extra functionality.

The differences are as follows:

1. CTRLbase+3 is redefined to be an indirect address register and CTRLbase+4 is redefined to be an indirect data register. These registers allows access to C0 through C8 indirect registers.
2. CDSDD in the Global Configuration byte of the Hardware Configuration data has been renamed SDD and its function expanded. On this part, setting SDD disables peripheral port reads from driving the ISA data bus for ALL peripheral port devices, e.g. CDROM and MODEM. On the CS4236, setting CDSDD disables peripheral port reads for the CDROM device ONLY.
3. The Serial Port works continuously once enabled. CEN and PEN do not have any effect on the serial port. On the CS4236, CEN and PEN disabled their respective part of the serial port when set to zero.
4. The GAME Logical Device (Joystick) only aliases from GAMEbase+0 to GAMEbase+5. GAMEbase+6 and GAMEbase+7 are reserved.
5. I25 was defined as a Version and Chip ID register in the CS4236. This register is now redefined as a Compatibility register and is identical to the CS4236 to allow software written to the CS4236 to work properly on this part. The Version and Chip ID for this chip has been moved to Control indirect register C1 and WSS indirect register X25 (Rev. C or greater).
6. I27 and I29 in the WSS space are reserved.
7. When IFM is enabled (and remapping is enabled) I18/I19 return the same value written when mute is enabled. On the CS4236, I18/19 returns 0xBF when mute is enabled.

8 The OLB bit in I16 is no longer functional and internally is set as if OLB is on.

9. The MIC input impedance is now 8 kΩ minimum.

The added features over the CS4236 are as follows:

10. A Wavetable Serial Port interface is added for connection to the CS9236 Single-Chip Wavetable Music Synthesizer. The pins are multiplexed with the XD7-XD5 pins and are controlled by the WTEN bit in C8 or the Global Configuration byte in the Hardware Configuration data.
11. The DSP serial port can be multiplexed to the XD4-XD1 pins to allow the DSP serial port and the second joystick to be used simultaneously. The multiplexing is controlled by the SPS bit in C8 or the Global Configuration byte in the Hardware Configuration data.
12. ISA bus now supports 3.3V by connecting a 3.3V supply to VD1.
13. Hardware volume control supports 4 formats.
14. New bits are added to the Global Configuration byte of the Hardware Configuration data:
    VCF1 and VCF0 Hardware Volume Control Format bits
    SLAD which disables Sound Blaster Synthesis volume changes from affecting LINE volume.
    WTEN to enable the Wavetable Serial Port
    SPS to switch the DSP serial port pins from the second joystick to the XD4-XD1 pins
15. Serial Port Format 3 (I16) is a new DSP serial port format.
16. A symmetrical mixer (the input mixer is new) is included and is supported by a new mode, MODE 3. This mode is enabled by setting the CMS1,0 bits in WSS I12 to 11. Note that the CS4236 MODE2 bit has been renamed CMS1 (Codec Mode Select 1). CMS1 is backwards compatible with the CS4236 MODE2 bit.
17. The MIC can be mixed directly to the output mixer with full volume control.
18. Hardware Configuration byte 9 was reserved in the CS4236 (at 0x43) and is now used as a Code Base Byte that determines the firmware code compatibility in the EEPROM. When firmware code for this part is loaded in the EEPROM this byte must be changed to 0x0B. This provides backwards compatibility by ignoring CS4236-based firmware code, which has this byte set to 0x43, while still reading the Hardware Configuration and PnP data from CS4236-programmed EEPROM.
19. 3.3 Volt ISA bus support is added. This includes all ISA pins except DRQA (which still runs at 5 Volts). When the VD1 pin is powered from a 3.3 Volt supply, the ISA bus connected to it must also run at 3.3 Volts.