Features

- 16M Bit (1M x 16) Flash Memory
- 3.0 ± 10% Read/Write
- Random Access Time - 100 ns
- Burst Access Time - 25 ns
- Sector Erase Architecture
  - Thirty 32K Word (64K Byte) Sectors with Individual Write Lockout
  - Two 16K Word (32K Byte) Sectors with Individual Write Lockout
  - Eight 4K Word (8K Byte) Sectors with Individual Write Lockout
- Typical Word Programming Time - 30 µs
- Typical Sector Erase Time: 32K Word Sectors - 500 ms; 4K Word Sectors - 100 ms
- Dual Plane Organization, Permitting Concurrent Read while Program/Erase
  - Memory Plane A: Eight 4K Word, Two 16K Word and Six 32K Word Sectors
  - Memory Plane B: Twenty-four 32K Word Sectors
- Erase Suspend Capability
  - Supports Reading/Programming Data from any Sector by Suspending Erase of any Different Sector
- Low-Power Operation
  - 30 mA Active
  - 10 µA Standby
- Data Polling and Toggle Bit for End of Program Detection
- Optional VPP Pin for Fast Programming
- $\overline{\text{RESET}}$ Input for Device Initialization
- BGA Package

16-megabit (1M x 16) Burst Mode 3-volt Only Flash Memory

AT49BP1604 AT49BP1604T

Advance Information

Rev. 1030B–05/99

Product Description

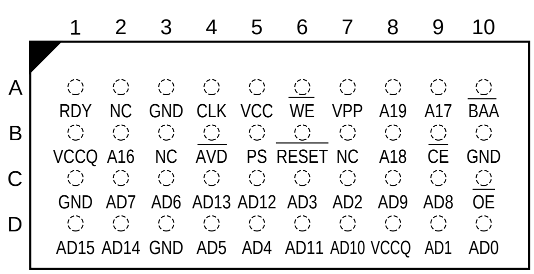
The AT49BP1604(T) is a 2.7 volt 16-megabit Flash memory. The memory is divided into 40 blocks for erase operations. It's synchronous architecture allows fast sequential "burst" accesses of 25 ns after an initial random access of 100 ns. The 16 data lines are multiplexed with 16 address lines (A0-A15) to reduce pin count. Four address lines (A16-A19) are not multiplexed. This device can be read or repro-

(continued)

Pin Configurations

Pin Name	Pin Function
AD0-AD15	Multiplexed Address/Data
A16-A19	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{AVD}}$	Address Latch Enable
$\overline{\text{BAA}}$	Advance
CLK	Clock
$\overline{\text{RESET}}$	Reset
VPP	Optional Power Supply for Faster Program/ Erase Operations
VCCQ	Output Power Supply
RDY	Ready
PS	Power Save

BGA Top View



grammed off a single 2.7V power supply, making it ideally suited for in-system programming. The output voltage can be separately controlled down to 1.65V through the VCCQ supply pin.

The device is segmented into two memory planes. Reads from memory plane B may be performed even while program or erase functions are being executed in memory plane A and vice versa. This operation allows improved system performance by not requiring the system to wait for a program or erase operation to complete before a read is performed. To further increase the flexibility of the device, it contains an Erase Suspend feature. This feature will put the Erase on hold for any amount of time and let the user read data from or program data to any of the remaining sectors. The end of program or Erase is detected by data polling, or toggle bit.

A VPP pin is provided to improve program/erase times. This pin does not need to be utilized. If it is not used the pin should be connected to ground. To take advantage of faster programming, the pin should supply 4.5 to 5.5 volts during program and erase operations.

With V_{PP} at 5V, a six byte command to remove the requirement of entering the three byte program sequence is offered to further improve programming time. After entering the six byte code, only single pulses on the write control lines are required for writing into the device. This mode is exited by powering down the device, by taking the $\overline{RESET}$ pin to GND or by a high to low transition on the V_{PP} input. This mode is not exited by the read reset command. Erase, Erase Suspend/Resume and Read Reset commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six byte code reside in the software of the final product but only exist in external programming code.

Device Operation

RANDOM READ: The random read operation of the device is controlled by $\overline{CE}$, $\overline{OE}$, and $\overline{AVD}$ inputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention. The data at the address location defined by AD0-AD15 and A16-A19 and captured by the $\overline{AVD}$ signal will be read when $\overline{CE}$ and $\overline{OE}$ are low. The address location passes into the device when $\overline{CE}$ and $\overline{AVD}$ are low; the address is latched on the low to high transition of $\overline{AVD}$. Low input levels on the $\overline{OE}$ and $\overline{CE}$ pins allow the data to be driven out of the device. $\overline{AVD}$ must be high whenever $\overline{OE}$ is low. The access time is measured from stable address, falling edge of $\overline{AVD}$ or falling edge of $\overline{CE}$, whichever occurs last. The $\overline{BAA}$ signal must be held high, and no clock signal is provided during random reads.

BURST READ: The burst read operation of the device is controlled by $\overline{CE}$, $\overline{OE}$, CLK, $\overline{BAA}$ and $\overline{AVD}$ inputs. The initial read location is determined as for the random read operation; it can be any memory location in the device. A low input on the $\overline{BAA}$ signal indicates that a burst read will occur. In the burst access, the address is latched on the rising edge of the first clock pulse when $\overline{AVD}$ is low or the rising edge of the $\overline{AVD}$ signal whichever occurs first. The CLK signal controls the flow of data from the device for a burst operation. To perform a burst read, the $\overline{BAA}$ signal should go low during the clock cycle prior to the beginning of the burst. When the $\overline{BAA}$ signal is low, the data at the next sequential address in memory is read for each following clock cycle.

During a given burst mode read, any number of addresses can be read from the memory. When a page boundary in the memory is transitioned, additional time may be required for the device to continue the burst read. To indicate that it is not ready to continue the burst, the device will drive the RDY pin low during the clock cycles in which new data is not being presented. Once the RDY pin is driven high, the next data will be valid. Starting with address zero, page boundaries occur every 128 words in the memory. During the burst mode, depending on the initial address that is read, the first page boundary transition may occur before 128 words are read. The RDY signal will be tri-stated when the $\overline{CE}$ or $\overline{OE}$ signal is high.

In the "Burst Read Cycle Waveform" as shown on page 13, the data D0 is valid asynchronously from point A, the point when the addresses are latched. The low to high transition of the clock at point B results in no change of data because the RDY signal is low. The low to high transition of the clock at point C results in the first burst word, D1, being read. The transition of the clock at point D results in a burst read of the last word of the page, D127. The clock transition at point E does not cause new data to appear on the output lines because the RDY signal goes low after the clock transition which signifies that a page boundary in the memory has been crossed and that new data is not available. The clock transition at point F does cause a burst read of data D128 because the RDY signal goes high after the clock transition indicating that new data is available. As long as the $\overline{BAA}$ signal is low, additional clock transitions, like at point G, will continue to result in burst reads until the next page boundary is crossed between word D255 and D256.

COMMAND SEQUENCES: The device powers on in the read mode. Command sequences are used to place the device in other operating modes such as program and erase. The command sequences are written by applying a low pulse on the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high. Prior to the low going pulse on the $\overline{WE}$ signal, the address input must be latched by a low to high transition on the $\overline{AVD}$ signal. Valid data is asserted when the $\overline{WE}$ signal is low and latched on the rising edge of the $\overline{WE}$ pulse. The addresses used in the command sequences are not affected by entering the command sequences.

RESET: A RESET input pin is provided to ease some system applications. When RESET is at a logic high level, the device is in its standard operating mode. A low level on the RESET pin halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the RESET pin, the device returns to Read or Standby mode, depending upon the state of the control pins. By applying a 12 ± 0.5V input signal on the RESET pin any sector can be reprogrammed even if the sector lockout feature has been enabled.

ERASE: Before a word can be reprogrammed it must be erased. The erased state of the memory bits is a logical “1”. The entire memory can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase commands.

CHIP ERASE: Chip Erase is a six bus cycle operation. The automatic Erase begins on the rising edge of the last WE pulse. Chip Erase does not alter the data of the protected sectors. After the full chip Erase the device will return back to the read mode. The hardware reset during Chip Erase will stop the Erase but the data will be of unknown state. Any command during chip Erase except erase suspend will be ignored.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into 40 sectors that can be individually erased. The Sector Erase command is a six bus cycle operation. The sector whose address is valid at the sixth falling edge of WE will be erased provided the given sector has not been protected.

WORD PROGRAMMING: The device is programmed on a word by word basis. Programming is accomplished via the internal device command register and is a four bus cycle operation. The programming address and data are latched in the fourth cycle. The device will automatically generate the required internal programming pulses. Please note that a “0” cannot be programmed back to a “1”; only Erase operations can convert “0”s to “1”s. During the programming mode, the clock signal must be held low or high and cannot toggle.

SECTOR PROGRAMMING LOCKOUT: Each sector has a programming lockout feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. The sectors that are locked out can contain secure code that can bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the memory is updated. This feature does not have to be activated; any sector’s usage as a write protected region is optional to the user. Once the feature is enabled, the data in the protected sector can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the remaining sectors can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed.

SECTOR LOCKOUT DETECTION: A software method is available to determine if programming of a sector is locked out. When the device is in the software product identification mode (see Software product Identification Entry and Exit sections) a read from address location 00002H within a sector will show if programming the sector is locked out. If the data on D0 is low, the sector can be programmed; if the data on D0 is high, the program lockout feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

SECTOR PROGRAMMING LOCKOUT OVERRIDE: The user can override the sector programming lockout by taking the RESET pin to 12V ± 0.5 volts. By doing this protected data can be altered through a chip erase, sector erase or word programming. When the RESET pin is brought back to TTL levels, the sector programming lockout feature is again active.

POWER SAVE: The power savings pin, PS, has an open drain configuration which is actively pulled low during the read operation. During non-read operations, the power saving pin can be driven high or low by the bus controller.

DATA POLLING: The AT49BP1604(T) features DATA bar polling to indicate the end of a program cycle. During a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on D7. Once the program or erase cycle has been completed, true data will be read from the device. Data bar polling may begin at any time during the program cycle. Please see “Status Bit Table” on page 18 for more details.

TOGGLE BIT: In addition to DATA bar polling the AT49BP1604(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in D6 toggling between a “1” and “0”. Once the program cycle has completed, D6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

An additional toggle bit is available on D2 which can be used in conjunction with the toggle bit which is available on D6. While a sector is erase suspended, a read or a program operation from the suspended sector will result in the D2 bit toggling. Please see “Status Bit Table” on page 18 for more details.

ERASE SUSPEND/RESUME: The Erase suspend allows the user to interrupt a Sector Erase operation and then perform a data read on the remaining sectors. This feature is only allowed during the sector erase operation. The device will take up to a maximum of 20 µs to suspend the Erase.

To resume the erase operation, the erase resume command sequence should be written to the device. The sector erase operation will then continue. Another erase suspend command can be written after the chip has resumed erasing.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49BP1604(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.3V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$, and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The D lines can only be driven from 0 to V_{CCQ} + 0.6V.

OUTPUT LEVELS: Output High Levels (V_{OH}) are equal to V_{CCQ} - 0.1V (not V_{CC}). For 2.7V - 3.3V output levels, V_{CCQ} must be tied to V_{CC}. For 1.65V - 2.2V output levels, V_{CCQ} must be regulated to 2.0V ± 10% while V_{CC} must be regulated to 2.7V - 3.0V (for minimum power).

Command Definition in Hex[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[3][4]	30
Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Bypass Unlock	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	A0
Single Pulse Word Program	1	Addr	D_{IN}										
Sector Lockout	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[3][4]	40
Erase Suspend	1	xxxx	B0										
Erase Resume	1	PA[5]	30										
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit[2]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit[2]	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: D15 - D8 (Don’t Care); D7 - D0 (Hex). The ADDRESS FORMAT in each bus cycle is as follows: A15 - A0 (Hex), A14 - A19 (Don’t Care).
2. Either one of the Product ID Exit commands can be used.
3. SA = sector address. Any word address within a sector can be used to designate the sector address (see next four pages for details).
4. When the sector programming lockout feature is not enabled, the sector will erase (from the same sector erase command). Once the sector has been protected, data in the protected sectors cannot be changed unless the $\overline{RESET}$ pin is taken to 12V ± 0.5V.
5. PA is the plane address (A19 - A18).

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AT49BP1604 Memory Plane A - Bottom Boot

Sector	Size (Words)	Address Range (A19 - A0)
SA0	4K	00000 - 00FFF
SA1	4K	01000 - 01FFF
SA2	4K	02000 - 02FFF
SA3	4K	03000 - 03FFF
SA4	4K	04000 - 04FFF
SA5	4K	05000 - 05FFF
SA6	4K	06000 - 06FFF
SA7	4K	07000 - 07FFF
SA8	16K	08000 - 0BFFF
SA9	16K	0C000 - 0FFFF
SA10	32K	10000 - 17FFF
SA11	32K	18000 - 1FFFF
SA12	32K	20000 - 27FFF
SA13	32K	28000 - 2FFFF
SA14	32K	30000 - 37FFF
SA15	32K	38000 - 3FFFF

AT49BP1604 Memory Plane B - Bottom Boot

Sector	Size (Words)	Address Range (A19 - A0)
SA16	32K	40000 - 47FFF
SA17	32K	48000 - 4FFFF
SA18	32K	50000 - 57FFF
SA19	32K	58000 - 5FFFF
SA20	32K	60000 - 67FFF
SA21	32K	68000 - 6FFFF
SA22	32K	70000 - 77FFF
SA23	32K	78000 - 7FFFF
SA24	32K	80000 - 87FFF
SA25	32K	88000 - 8FFFF
SA26	32K	90000 - 97FFF
SA27	32K	98000 - 9FFFF
SA28	32K	A0000 - A7FFF
SA29	32K	A8000 - AFFFF
SA30	32K	B0000 - B7FFF
SA31	32K	B8000 - BFFFF
SA32	32K	C0000 - C7FFF
SA33	32K	C8000 - CFFFF
SA34	32K	D0000 - D7FFF
SA35	32K	D8000 - DFFFF
SA36	32K	E0000 - E7FFF
SA37	32K	E8000 - EFFFF
SA38	32K	F0000 - F7FFF
SA39	32K	F8000 - FFFFF

AT49BP1604T Memory Plane B - Top Boot

Sector	Size (Words)	Address Range (A19 - A0)
SA0	32K	00000 - 07FFF
SA1	32K	08000 - 0FFFF
SA2	32K	10000 - 17FFF
SA3	32K	18000 - 1FFFF
SA4	32K	20000 - 27FFF
SA5	32K	28000 - 2FFFF
SA6	32K	30000 - 37FFF
SA7	32K	38000 - 3FFFF
SA8	32K	40000 - 47FFF
SA9	32K	48000 - 4FFFF
SA10	32K	50000 - 57FFF
SA11	32K	58000 - 5FFFF
SA12	32K	60000 - 67FFF
SA13	32K	68000 - 6FFFF
SA14	32K	70000 - 77FFF
SA15	32K	78000 - 7FFFF
SA16	32K	80000 - 87FFF
SA17	32K	88000 - 8FFFF
SA18	32K	90000 - 97FFF
SA19	32K	98000 - 9FFFF
SA20	32K	A0000 - A7FFF
SA21	32K	A8000 - AFFFF
SA22	32K	B0000 - B7FFF
SA23	32K	B8000 - BFFFF

AT49BP1604T Memory Plane A - Top Boot

Sector	Size (Words)	Address Range (A19 - A0)
SA24	32K	C0000 - C7FFF
SA25	32K	C8000 - CFFFF
SA26	32K	D0000 - D7FFF
SA27	32K	D8000 - DFFFF
SA28	32K	E0000 - E7FFF
SA29	32K	E8000 - EFFFF
SA30	16K	F0000 - F3FFF
SA31	16K	F4000 - F7FFF
SA32	4K	F8000 - F8FFF
SA33	4K	F9000 - F9FFF
SA34	4K	FA000 - FAFFF
SA35	4K	FB000 - FBFFF
SA36	4K	FC000 - FCFFF
SA37	4K	FD000 - FDFFF
SA38	4K	FE000 - FEFFF
SA39	4K	FF000 - FFFFF

DC and AC Operating Range

		AT49BP1604(T)-10
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.3V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{BAA}$	V_{PP} (6)	Ai	D
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Burst Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	Ai	D_{OUT}
Program/Erase(2)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	5V ± 10%	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X(1)	X	V_{IH}	X	X	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}	V_{IH}	X		
Program Inhibit	X	V_{IL}	X	V_{IH}	V_{IH}	X		
Output Disable	X	V_{IH}	X	V_{IH}	X	X		High Z
Reset	X	X	X	V_{IL}	V_{IH}	X	X	High Z
Product Identification								
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}		A1 - A19 = V_{IL}, A9 = V_H(3), A0 = V_{IL}	Manufacturer Code(4)
							A1 - A19 = V_{IL}, A9 = V_H(3), A0 = V_{IH}	Device Code(4)
Software(5)				V_{IH}			A0 = V_{IL}, A1 - A19 = V_{IL}	Manufacturer Code(4)
							A0 = V_{IH}, A1 - A19 = V_{IL}	Device Code(4)

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 001FH,
   Device Code: 00C5H–AT49BP1604,
   00C1H–AT49BP1604T.
5. See details under Software Product Identification Entry/Exit.
6. The use of the VPP pin is optional.

DC Characteristics

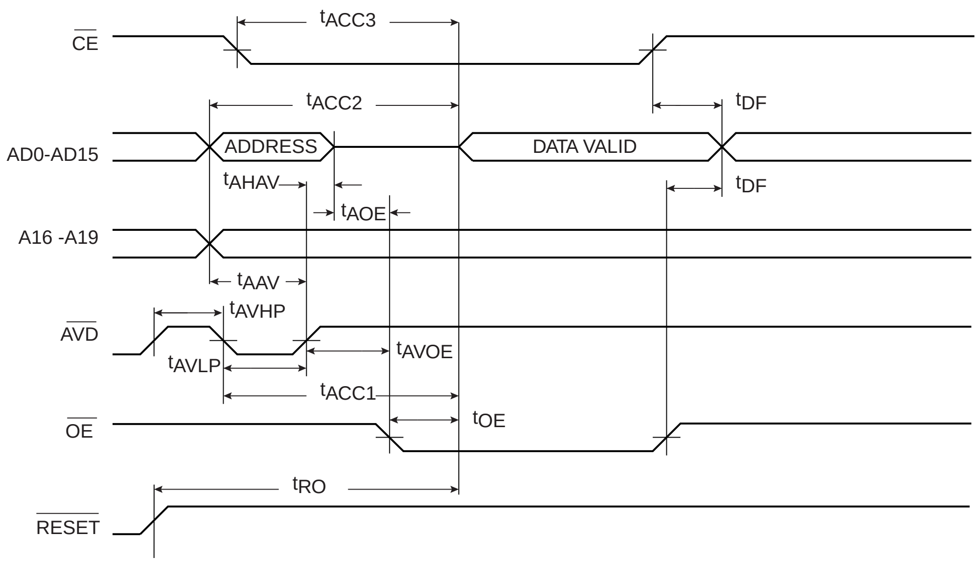
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CCQ}		10	µA
I_{LO}	Output Leakage Current	V_D = 0V to V_{CCQ}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CCQ}		10	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CCQ}		1	mA
I_{CC} (1)	V_{CC} Active Current	f = 40 MHz; I_{OUT} = 0 mA		30	mA
I_{CCRE}	V_{CC} Read While Erase Current	f = 40 MHz; I_{OUT} = 0 mA		50	mA
I_{CCRW}	V_{CC} Read While Write Current	f = 40 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage	V_{CCQ} = 1.65V - 2.2V	V_{CCQ} - 0.2		V
		V_{CCQ} = 2.7V - 3.3V	2.0		
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CCQ} = 1.65V - 2.2V	V_{CCQ} - 0.1		V
		I_{OH} = -400 µA; V_{CCQ} = 2.7V - 3.3V	2.4		

Note: 1. In the erase mode, I_{CC} is 30 mA.

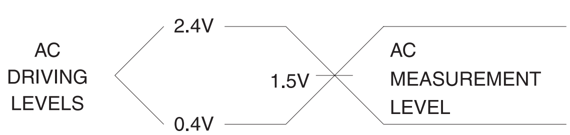
AC Random Read Timing Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{ACC1}	Access, $\overline{AVD}$ To Data Valid		100	ns
t_{ACC2}	Access, Address to Data Valid		100	ns
t_{ACC3}	Access, $\overline{CE}$ to Data Valid		100	ns
t_{OE}	$\overline{OE}$ to Data Valid		25	ns
t_{AHAV}	Address Hold from $\overline{AVD}$	0		ns
t_{AVLP}	$\overline{AVD}$ Low Pulsewidth	25		ns
t_{AVHP}	$\overline{AVD}$ High Pulsewidth	25		ns
t_{AAV}	Address Valid to $\overline{AVD}$	15		ns
t_{AOE}	Address Valid to $\overline{OE}$	3		ns
t_{AVOE}	$\overline{AVD}$ to $\overline{OE}$	3		ns
t_{DF}	$\overline{CE}$, $\overline{OE}$ High to Data Float		25	ns
t_{RO}	$\overline{Reset}$ to Output Delay		800	ns

Random Read Cycle Waveform

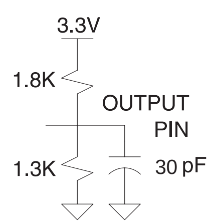


Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C(1)

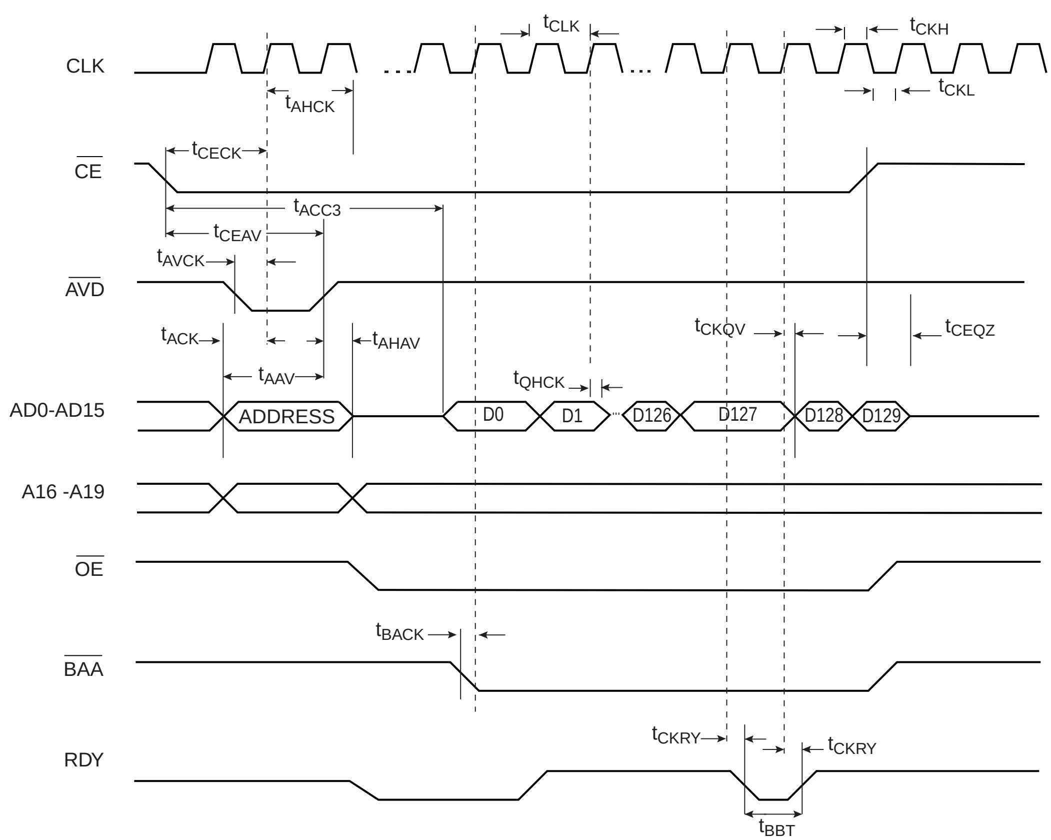
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

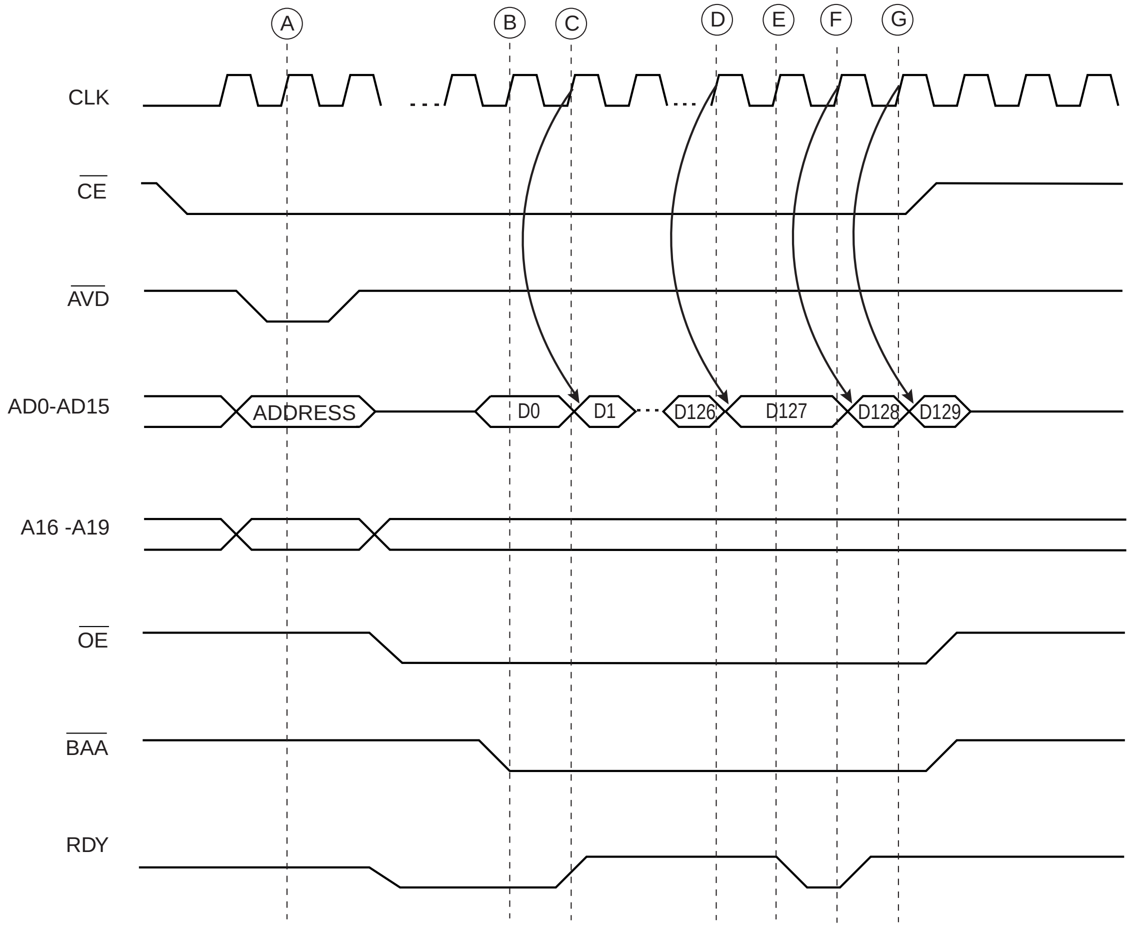
AC Burst Read Timing Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{CLK}	CLK Period	25		ns
t_{CKH}	CLK High Time	7		ns
t_{CKL}	CLK Low Time	7		ns
t_{CKRT}	CLK Rise Time		5	ns
t_{CKFT}	CLK Fall Time		5	ns
t_{ACK}	Address Valid to Clock	7		ns
t_{AVCK}	$\overline{AVD}$ low to Clock	7		ns
t_{CECK}	$\overline{CE}$ low to Clock	7		ns
t_{QHCK}	Output Hold from Clock	3		ns
t_{AHCK}	Address Hold from Clock	10		ns
t_{CKRY}	Clock to RDY Delay		20	ns
t_{BACK}	$\overline{BAA}$ Setup to Clock	7		ns
t_{CEAV}	$\overline{CE}$ Setup to $\overline{AVD}$	25		ns
t_{AAV}	Address Valid to $\overline{AVD}$	15		ns
t_{AHAV}	Address Hold From $\overline{AVD}$	10		ns
t_{CKQV}	CLK to Data Delay		20	ns
t_{CEQZ}	$\overline{CE}$ High to Output High Z		25	ns
t_{BBT}	Burst Busy Time		150	ns

Burst Read Cycle Waveform



Burst Read Cycle Waveform

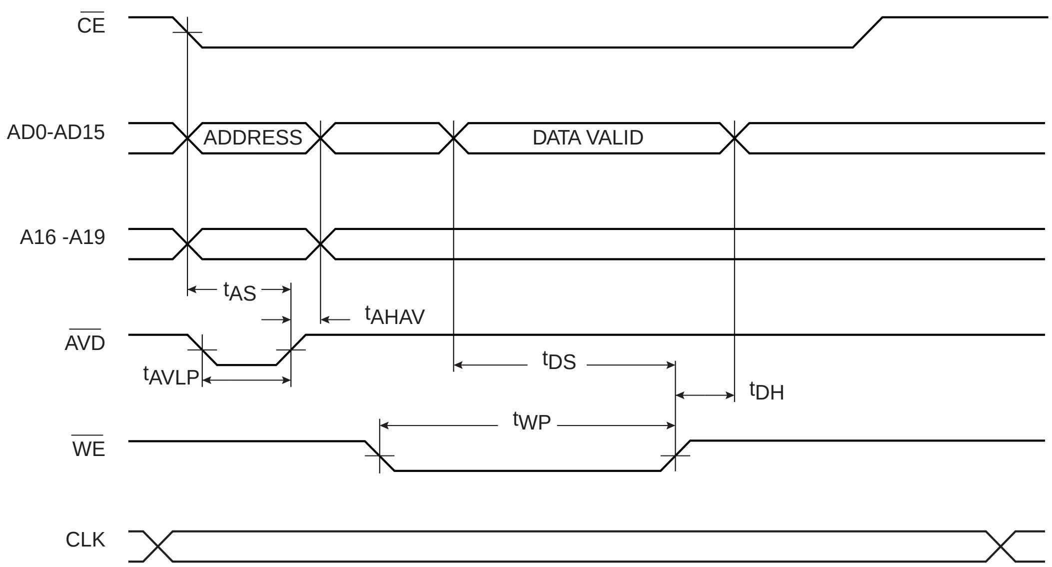


AC Word Load Characteristics

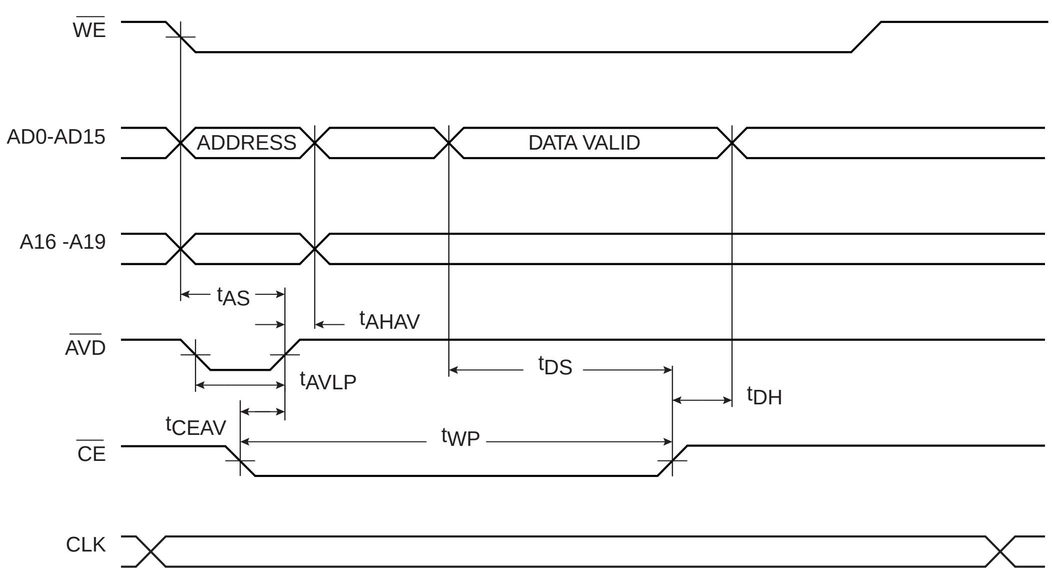
Symbol	Parameter	Min.	Max.	Units
t_{AS}	Address, $\overline{CE}$ Setup Time to $\overline{AVD}$ High	15		ns
t_{AHAV}	Address Hold Time	10		ns
t_{AVLP}	$\overline{AVD}$ Low Pulsewidth	25		ns
t_{DS}	Data Setup Time	15		ns
t_{DH}	Data Hold Time	0		ns
t_{CEAV}	$\overline{CE}$ Setup to $\overline{AVD}$	25		ns
t_{WP}	$\overline{CE}$ or $\overline{WE}$ Low Pulsewidth	100		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



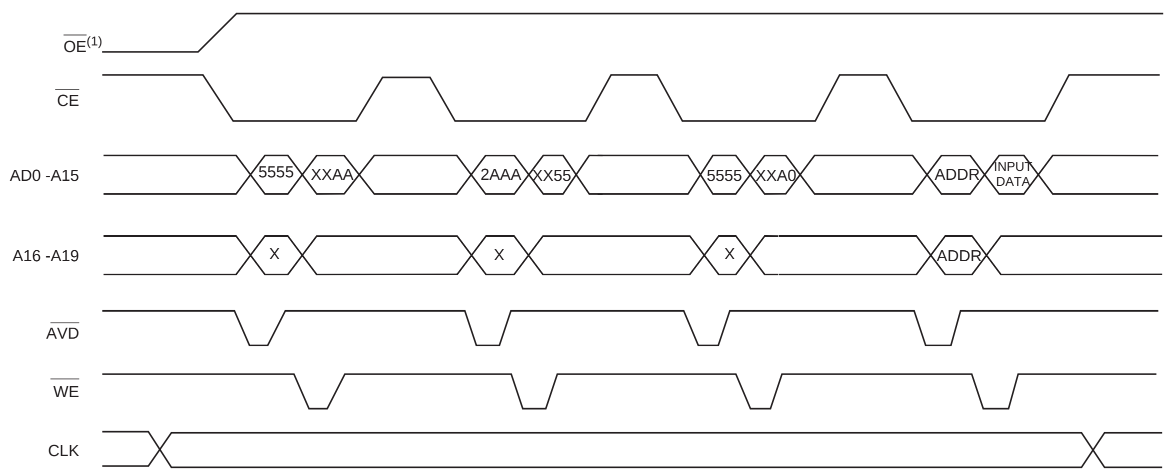
$\overline{CE}$ Controlled



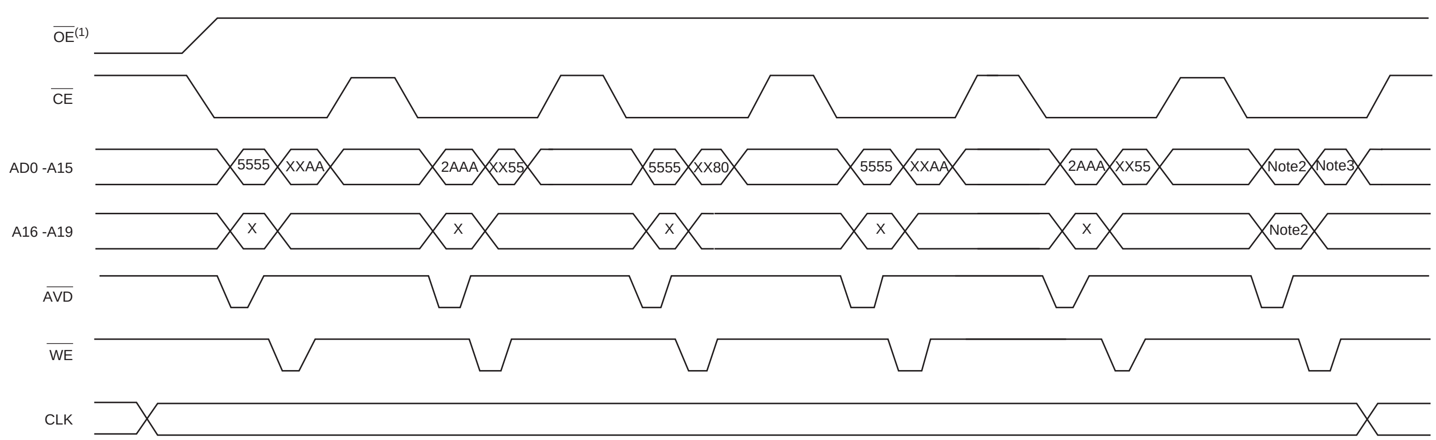
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		30	50	µs
t_{AS}	Address Set-up Time	15			ns
t_{AHAV}	Address Hold Time	10			ns
t_{DS}	Data Set-up Time	15			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{WPH}	Write Pulse Width High	50			ns
t_{SEC1}	Sector Erase Cycle Time (4K word sectors)		100		ms
t_{SEC2}	Sector Erase Cycle Time (32K word sectors)		500		ms
t_{EC}	Chip Erase Cycle Time			10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 3 under command definitions.)
3. For chip erase, the data should be XX10H, and for sector erase, the data should be XX30H.

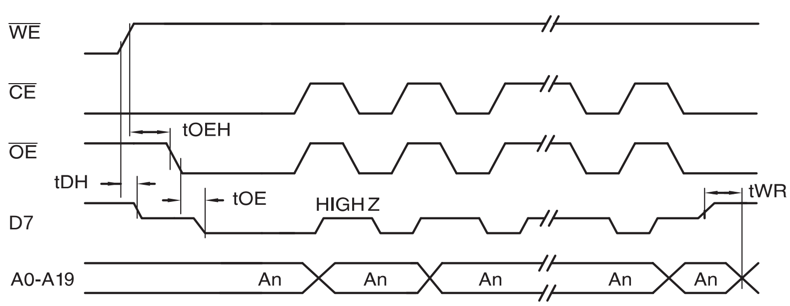
Data Polling Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms



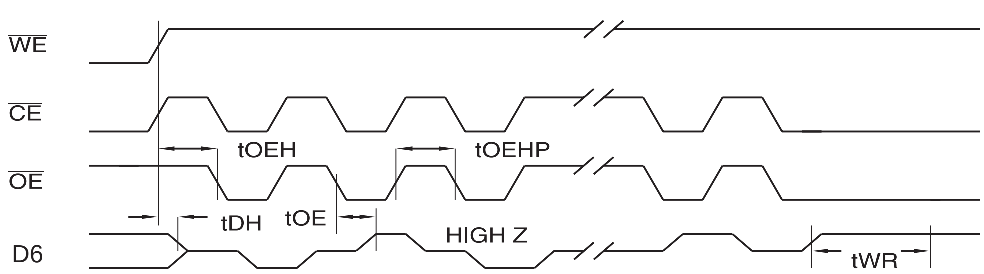
Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{\text{OE}}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms(1)(2)(3)

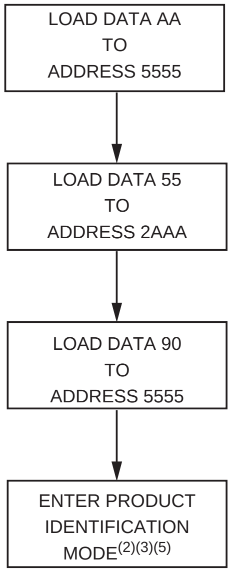


Notes: 1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).

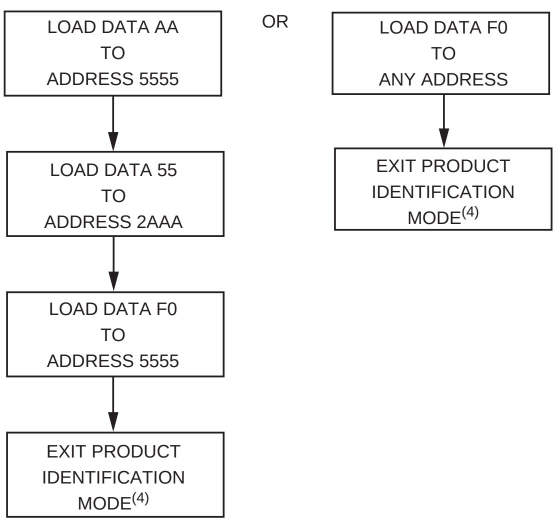
2. Beginning and ending state of D6 will vary.

3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

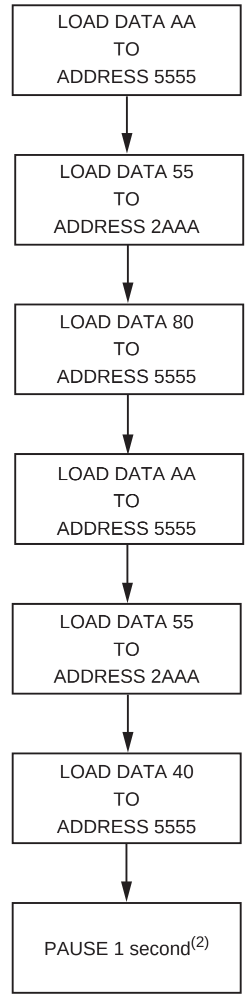


Software Product Identification Exit[1][6]



Notes:
1. Data Format: D15 - D8 (Don’t Care); D7 - D0 (Hex)
   Address Format: A15 - A0 (Hex), A15 - A19 (Don’t Care).
2. A1 - A19 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 001FH
   Device Code: 00C5H–AT49BP1604,
   00C1H–AT49BP1604T
6. Either one of the Product ID Exit commands can be used.

Sector Lockout Enable Algorithm[1]



Notes:
1. Data Format: D15 - D8 (Don’t Care); D7 - D0 (Hex)
   Address Format: A15 - A0 (Hex), A15 - A19 (Don’t Care).
2. Sector lockout feature enabled.

Status Bit Table

	Status Bit					
	D 7		**D 6**		**D 2**	
Read Address In	**Plane A**	**Plane B**	**Plane A**	**Plane B**	**Plane A**	**Plane B**
While						
Programming in Plane A	$\overline{D7}$	DATA	TOGGLE	DATA	1	DATA
Programming in Plane B	DATA	$\overline{D7}$	DATA	TOGGLE	DATA	1
Erasing in Plane A	0	DATA	TOGGLE	DATA	TOGGLE	DATA
Erasing in Plane B	DATA	0	DATA	TOGGLE	DATA	TOGGLE
Erase Suspended & Read Erasing Sector	1	1	1	1	TOGGLE	TOGGLE
Erase Suspended & Read Non-Erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA
Erase Suspended & Program Erasing Sector	1	1	1	1	TOGGLE	TOGGLE
Erase Suspended & Program Non-Erasing Sector in Plane A	$\overline{D7}$	DATA	TOGGLE	DATA	TOGGLE	DATA
Erase Suspended & Program Non-Erasing Sector in Plane B	DATA	$\overline{D7}$	DATA	TOGGLE	DATA	TOGGLE

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