Socket 754 Design and Qualification Requirements

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Revision History

Date	Rev	Description
July 2003	3.07	Corrected the base opening measurements given in Note 14 and Note 15 of Figure 3, Socket 754 Outline.
November 2002	3.01	Initial public release.

1 Introduction

1.1 Objective

This document defines the Socket 754, shown in Figure 1 as it is intended for use in value and performance desktop and workstation applications using an AMD Athlon™ 64 processor. Socket 754 is a Zero Insertion Force (ZIF) Micro Pin Grid Array (µPGA) Socket using Ball Grid Array (BGA) surface mount technology on 1.27 mm pitch.

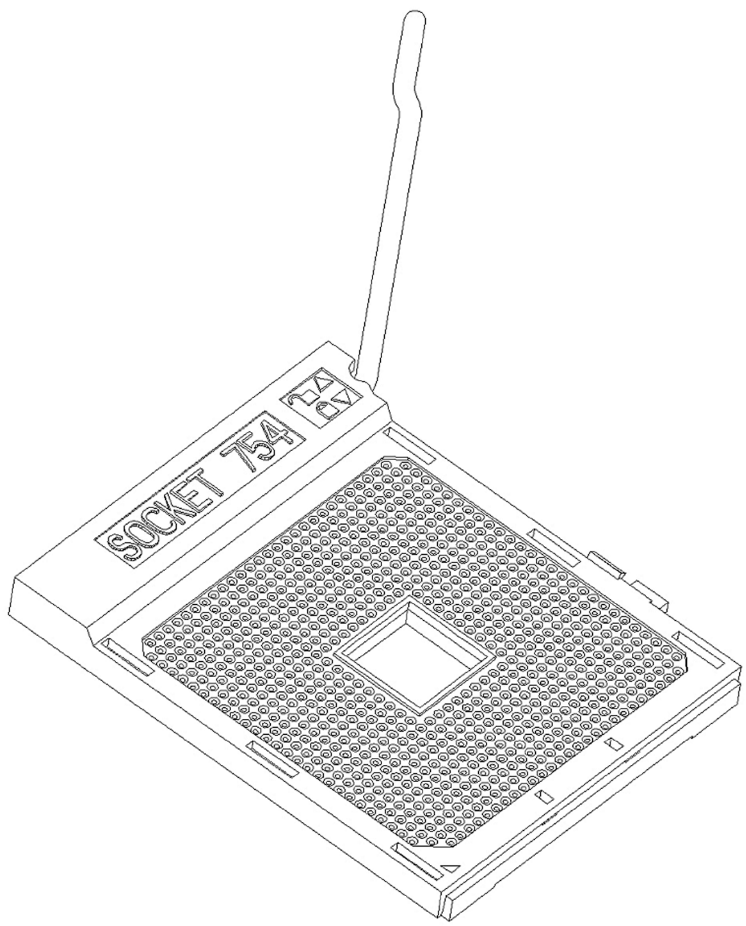


Figure 1. A 3-D View of Socket 754

Socket 754 dimensional, performance, and qualification testing requirements are defined and designed to ensure that Socket 754 performs to the AMD electrical and mechanical design requirements.

This document includes Socket 754 outline and qualification tests required for a supplier to become qualified by AMD as a Socket 754 vendor. Socket 754 is designed for the AMD product line of microprocessors.

1.2 Related Information

The following documents contain additional information related to the Socket 754 microprocessor:

***Note**: EIA standards are referenced throughout this document to help perform measurements. The EIA standards from Global Engineering can be found on the Global Engineering Website at http://global.ihs.com or by calling 1-800-624-3974.*

EIA 364–09	Durability Test Procedure for Electrical Connectors and Contacts
EIA 364–11	Resistance to Solvents Test Procedure for Electrical Connectors and Sockets
EIA 364–17	Temperature Life with or without Electrical Load Test Procedure for Electrical Connectors and Sockets
EIA 364–20	Withstanding Voltage Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts
EIA 364–21	Insulation Resistance Test Procedure for Electrical Connectors Sockets and Coaxial Contacts
EIA 364–23	Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets
EIA 364–27	Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors
EIA 364–28	Vibration Test Procedure for Electrical Connectors and Sockets
EIA 364–30	Capacitance Test Procedure for Electrical Connectors
EIA 364–31	Humidity Test Procedure for Electrical Connectors and Sockets
EIA 364–32	Thermal Shock (Temperature Cycling) Test Procedure for Electrical Connectors and Sockets
EIA 364–48	Test Procedure for Metallic Coating Thickness Measurements of Contacts
EIA 364–56	Resistance to Soldering Heat Test Procedure for Electrical Connectors
EIA 364–60	Test Procedure No.60 General Methods for Porosity Testing of Contact Finishes for Electrical Connectors
EIA 364–65	Mixed Flowing Gas
EIA 364–70	Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
EIA 364–90	Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable assemblies or Interconnection Systems
EIA 364–103	Propagation Delay Test procedure for Electrical Connectors, Sockets, Cable Assemblies, or Interconnection Systems
EIA 364–108	Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Cable Assemblies or Interconnection Systems

1.3 Abbreviations

Table 1 shows a list of abbreviations used in this document.

Table 1 List of Abbreviations

Abbreviation	Definition
AMD	Advanced Micro Devices
EIA	Electronic Industries Association
LCP	Liquid Crystal Polymer
LLCR	Low Level Contact Resistance
µs	Microsecond
µBGA	Micro Ball Grid Array
µPGA	Micro Pin Grid Array
MΩ	Mega-Ohm
mA	Milliampere
mV	Millivolt
mΩ	Milli-Ohm
µOPGA	Micro Organic Pin Grid Array
PCB	Printed Circuit Board
ps	Picosecond
UL	Underwriters Laboratories

2 Processor Package Descriptions

The 754-pin µOPGA processor package is illustrated in Figure 2. The Pin A1 designator is shown in the Pin A1 location.

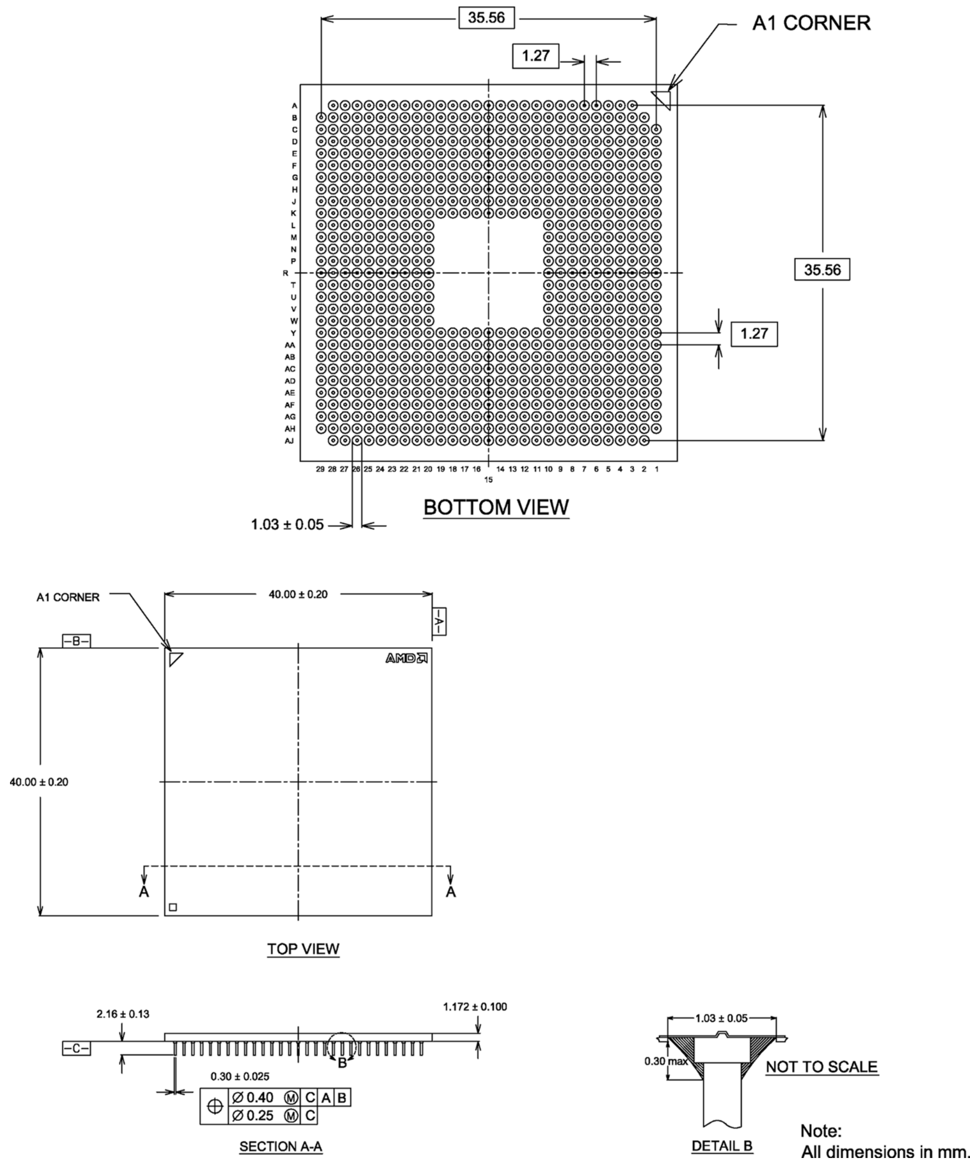


Figure 2. 754-Pin µOPGA Package Drawing

Note: *Socket 754 must be designed so that a 1.95 mm µOPGA package pin length makes full electrical contact.*

3 Socket 754 Design Requirements

This chapter shows the design requirements for the socket 754, including:

- Socket 754
- Base and cover
- Vendor markings
- Other markings
- Contact material and plating

3.1 Socket 754

A Socket 754 outline is illustrated in Figure 3 on page 16. The critical dimensions and required notes are shown. The Pin A1 designator is shown on the Socket 754 outline. The µPGA pin pattern is not symmetrical. The µOPGA processor package may only be inserted one way into Socket 754. The Socket 754 does not incorporate tabs for heat sink attachment. The recommended PCB keepout for Socket 754 is shown in Figure 4 on page 17.

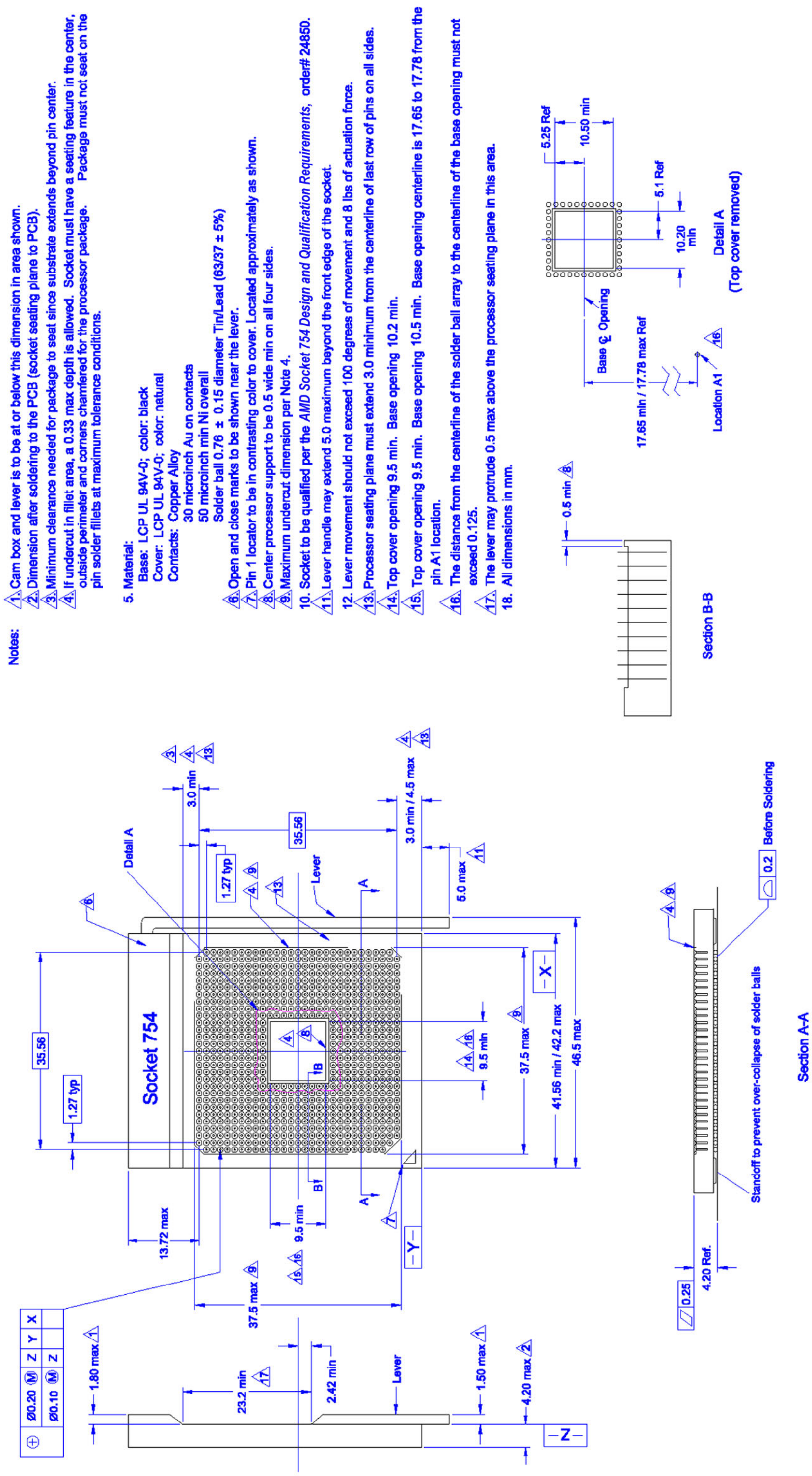


Figure 3. Socket 754 Outline

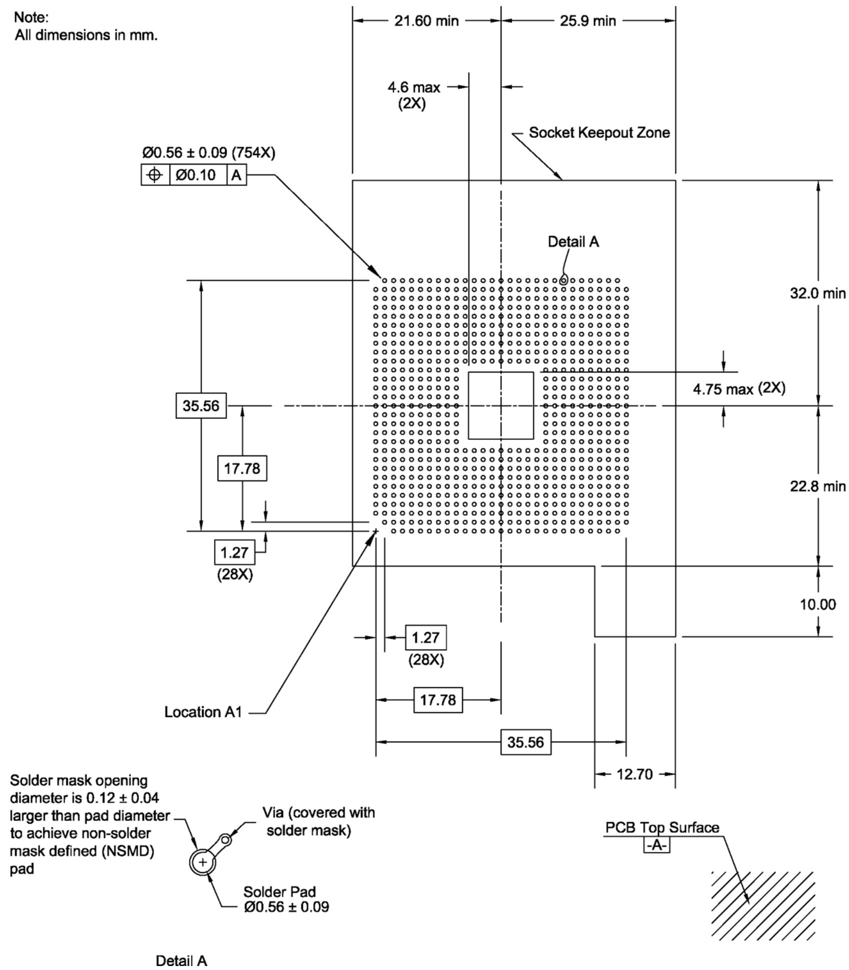


Figure 4. Recommended PCB Keepout

3.2 Base and Cover

Socket 754 base and cover is made of liquid crystal polymer (LCP) with a UL flammability rating of 94V-0. The base color is black and the cover is natural in color.

3.2.1 Socket 754 Vendor Marking

Socket 754 must be molded into the CAM box as shown in Figure 3 on page 16. The vendors UL approved trademark identifier and lot traceability number must be shown on the Socket 754 such that, after soldering to the printed circuit board (PCB), it is visible and readable. The lot traceability number can be ink stamped or laser marked.

3.2.2 Other Socket 754 Markings

An open and close designator must be molded into the CAM box in close proximity to the lever handle.

3.3 Socket 754 Contact Material and Plating

The contact material must be high strength copper alloy. Plating must be 30 micro inches (minimum) gold over 50 micro inches minimum nickel in the contact area. The solder ball on the bottom side must be 0.76 ± 0.15 millimeter diameter, tin/lead (63/37 ± 5%). The contact must be plated to create a solder barrier that prevents the solder from wicking up into the contact area during soldering.

4 Socket 754 Qualification Requirements

All qualification testing must be conducted in AMD's designated test facilities. Qualification testing expenses are the responsibility of the Socket 754 supplier. Qualification testing must be performed on production lots of Socket 754.

4.1 Qualification Test Report

A test report must be written for each test listed in Figure 5 on page 23. All test reports for Groups 1 to 8 and Group 10 must be presented in one folder. Group 9 can be presented in a separate folder. The test report must contain the following for each test conducted:

- Title of the test
- Number of specimen and description
- Specimen lot numbers
- Test equipment used and date of both the last and next calibration
- Test procedure, including test method, cycling rate, fixtures used, and number of cycles
- Photographs, sketches, or drawings of the test set-up
- Copy of all raw data taken
- All raw data reduced to tables and/or graphs for clear concise understanding of results
- Statement that all specimens passed all requirements or the number of specimens that failed
- Date of test and name of operator
- Sample calculations to reduce data
- Other data as required in each EIA document

4.2 Testing

Please contact the local AMD field applications engineer (FAE) for testing locations. The local AMD FAE can be reached at 1-800-538-8450.

5 Documentation Requirements

The supplier of the Socket 754 must submit a minimum amount of documentation to AMD.

- Socket 754 drawing and specifications in supplier's format
- Qualification Test Report (See Section 4.1 on page 19)
- Socket 754 first article inspection report, with the raw data
- Recommended soldering parameters
- Recommended PCB layout guidelines
- Supplier's Part Number for each qualified Socket 754
- Sample of Socket 754 from qualification test lot

The documentation package, as specified in Chapter 5, must be submitted to AMD. If all testing parameters are met, AMD will add the Socket 754 supplier data to the AMD development partners listing.

6 Mechanical Test Procedure Conditions and Requirements

6.1 Test Matrix

The Socket 754 qualification matrix is shown in Figure 5.

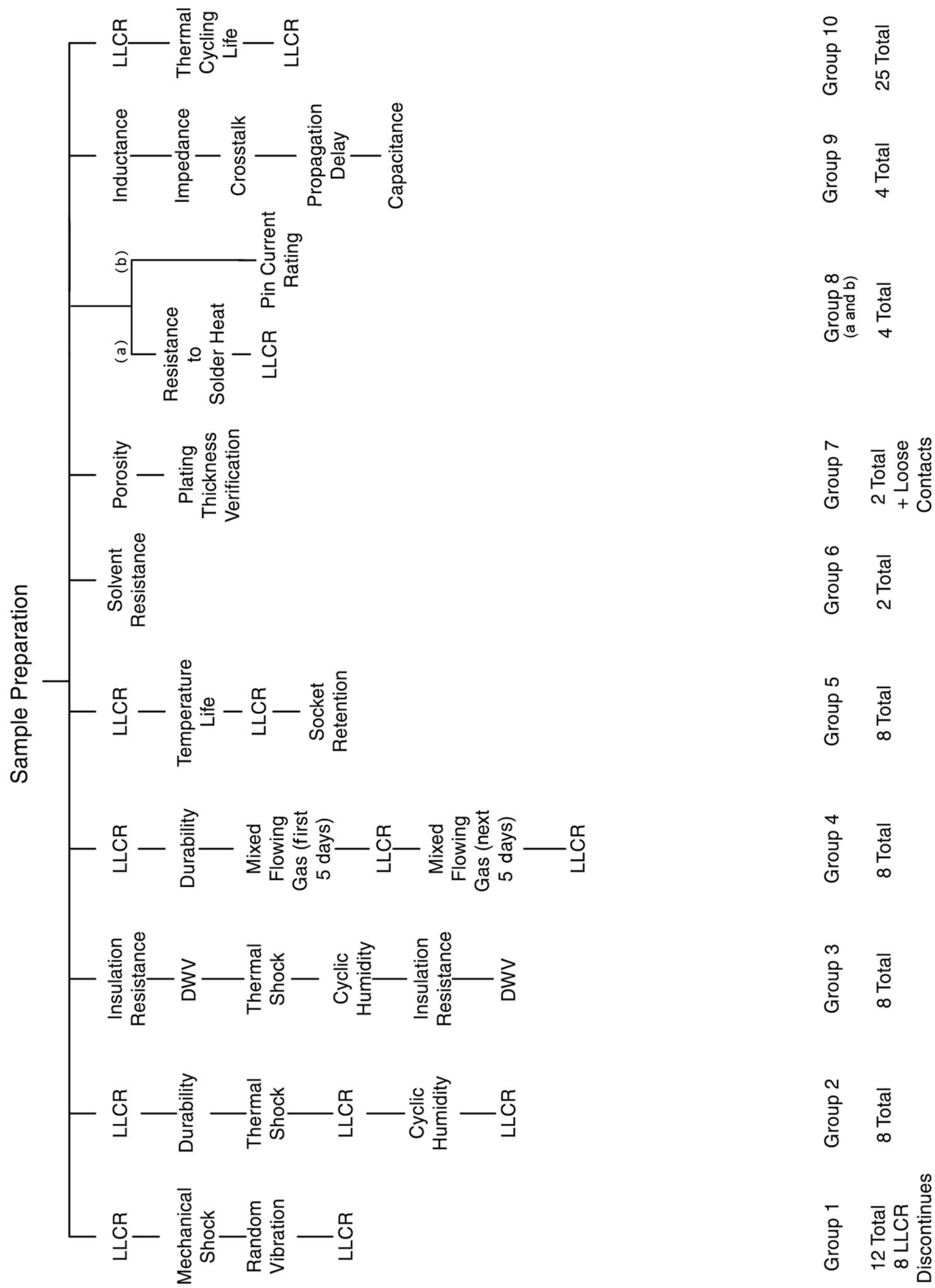


Figure 5. Socket 754 Qualification Test Matrix

For a Socket 754 to be added to the AMD development partners list, they must meet all mechanical requirements listed in Table 2 and Electrical requirements shown in Section 7 on page 29, when tested in the sequence listed in Figure 5 on page 23.

Table 2. Mechanical Qualification Test Procedures

Test Procedure	Test Condition	Requirements
Low Level Contact Resistance (LLCR)		
EIA 364-23	100 mA maximum, 20 mV 336 contacts (168 contact pairs) (minimum) monitored per test sample	Record initially After testing, LLCR-per-contact must not exceed 20.0 mΩ with alloy-194 pins.
Mechanical Shock		
EIA 364-27 Condition A	50 G, 11 ms, half-sine Conducted with 450 g heatsink test mass attached to the retention mechanism and PCB assembly	No physical damage No contact interruptions greater than 1.0 µs.
Random Vibration		
EIA 364–28, Condition VII, Level D	3.1 G rms, 20 to 500 Hz, 15 minutes per axis duration Conducted with 450 g heatsink test mass attached to the retention mechanism and PCB Assembly	No physical damage No contact interruptions greater than 1.0 µs. LLCR 20.0 mΩ maximum per contact
Durability		
EIA 364–09	Fifty cycles per test sample	No physical damage LLCR 20.0 mΩ maximum per contact
Thermal Shock		
EIA 364–32	–55°C to +110°C, 30 minutes at each extreme, five cycles Group 2 samples exposed to the environment mated Group 3 samples exposed to the environment unmated	No physical damage Group 2—LLCR 20 mΩ maximum per contact Group 3—Insulation resistance 1000 MΩ minimum then DWV 650 Vac (See IR and DWV test procedures on page 25)

Table 2. Mechanical Qualification Test Procedures (Continued)

Test Procedure	Test Condition	Requirements
Cyclic Humidity		
EIA 364-31 Method III Condition C	25 to 65°C, at 90 to 95% relative humidity Group 2 samples exposed to the environment mated Group 3 samples exposed to the environment unmated	No physical damage Group 2—LLCR – 20.0 mΩ maximum per contact (measured at 250 and 504 hours) Group 3—Insulation resistance 1000 MΩ minimum then DWV 400 Vac (See IR and DWV test procedures below)
Insulation Resistance (IR)		
EIA 364-21	20 Adjacent contacts, 500 Vdc	1000 MΩ minimum
Dielectric Withstanding Voltage (DWV)		
EIA 364-20	20 Adjacent contacts, 650 Vac	No breakdown, flashover, arcing, etc.
Mixed Flowing Gas		
EIA 364-65 Condition IIA	Chlorine 10 ppb Hydrogen Sulfide 10 ppb Nitrogen Dioxide 200 ppb Sulfur Dioxide 100 ppb Temperature 30°C Relative Humidity 70 % Duration 10 days total: First five days one half samples mated and one half unmated Second five days all samples are mated	No physical damage LLCR 20.0 mΩ maximum per contact
Temperature Life		
EIA 364-17 Method A	+115°C, 432 hours	No physical damage LLCR 20.0 mΩ maximum per contact (measured at 250 and 432 hours)

Table 2. Mechanical Qualification Test Procedures (Continued)

Test Procedure	Test Condition	Requirements
Solvent Resistance		
EIA 364-11	Four Solution Test in Table 1 of EIA 364-11	No physical damage and markings are legible
Socket Retention		
	Clamp Socket 754 so that a µPGA package is accessible. Place a µPGA package in the clamped Socket 754, then close and lock the socket. With Socket 754 locked, pull the µPGA package out of the socket and record the force required.	Extraction force to be 8 kg minimum Record the forces required.
Porosity (Gold Contacts Only)		
EIA 364-60	Test loose contacts (quantity - 20) Procedure 1.1.1 (Au/Ni): Nitric Acid Technique	Count and record pores.
Plating Thickness		
EIA 364-48 Method C	20 contacts–measure the gold and nickel thickness. Thickness may be measured by X-ray, florescence, or cross sectioning.	30 microinch minimum–Gold 50 microinch minimum–Nickel
Resistance To Solder Heat		
EIA 364-56	Using convection reflow, solder the Socket 754 to the PCB. Assembly is to be reflowed three times.	No physical damage Reflow soldering, solder stencil parameters and solder paste percentage tin and lead specified Measured after three passes through reflow Flatness per Figure 3 on page 16, Section A-A, before and after soldering. LLCR 20.0 mΩ maximum per contact

Table 2. Mechanical Qualification Test Procedures (Continued)

Test Procedure	Test Condition	Requirements
Pin Current Rating		
EIA 364-70 Method 2	330 contacts must be in series. Thermocouple to be placed under socket 754 between pins (P22, P23, R22, and R23) During testing 12 V power must be supplied to the fan.	Generate graph Temperature Rise vs. Current 1.2 Amp per pin at T – rise of 20°C maximum Continue testing until delta T – rise is 30°C.
Thermal Cycling Life		
EIA 364-32	Sample size 25 minimum Temperature cycle with the retention mechanism load applied, then remove the applied load for each LLCR measurement. –55°C to 110°C, (temperature ± 5°C solder ball temperature Maximum of 2 cycles per hour Once the solder ball junction reaches the temperature specified, soak for 5 minutes. The chamber temperature may be raised or lowered to speed the temperature change at the solder ball. All samples must be mated during testing.	No physical damage LLCR 20.0 mΩ max. per contact over 336 contacts (168 pin pairs). LLCR to be measured each 250 cycles until failure A socket has failed if one contact exceeds the 20.0 mΩ maximum LLCR measurements recorded until 60% of the sockets have a failure or 3000 cycles completed 1000 cycles minimum with no failures

7 Electrical Qualification Requirements

7.1 Fixture

All test fixtures that are required to conduct the electrical qualification requirements will be furnished by AMD to the AMD designated testing facility.

7.1.1 Capacitance and Inductance Matrices

The partial "loop" inductance and Maxwell capacitance matrices (see Section 7.6 on page 36 for definitions) are measured for the three mated pin configurations shown in Figure 6 on page 29. For the pin configurations, the size of the Maxwell capacitance matrix is 2 x 2, as is the size of the partial "loop" inductance matrix.

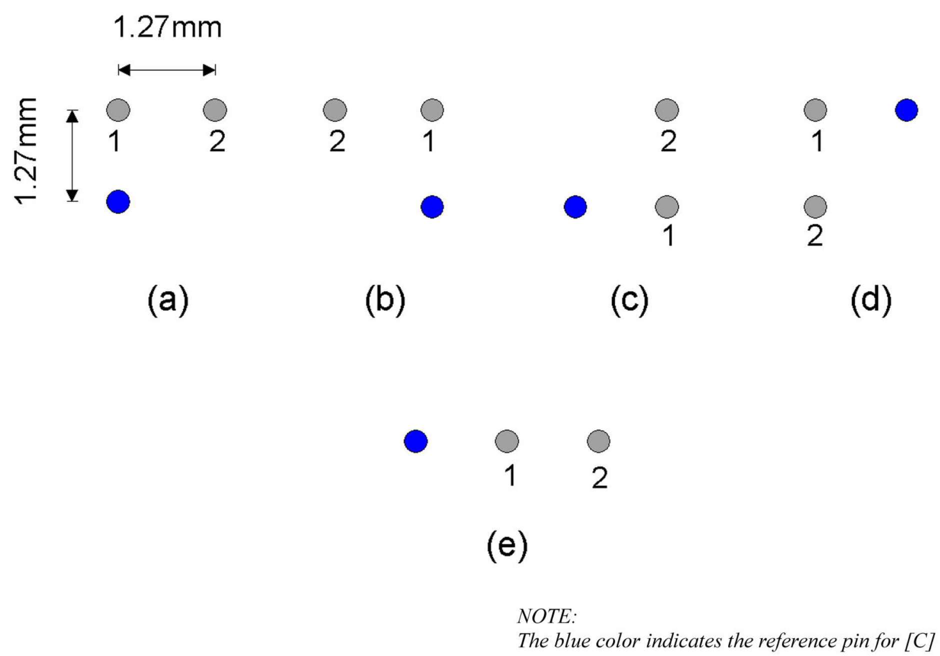


Figure 6. Pin Configuration for the Maxwell Capacitance and Partial Inductance Matrix Measurement

7.1.2 Mated Partial Self Inductance

The following procedures are required to properly test for mated partial self-inductance.

7.1.2.1 Test Procedure

Use a validated "industry-standard" 3-D EM field solver. This is the only quantity in the specification that need not be measured. Values obtained from an accurate detailed 3-D EM field solver model are acceptable. This computed quantity must not be used in any calculations involving measured data.

7.1.2.2 Test Condition

- Test Frequencies are 500 MHz and 2 GHz.
- Use a validated "industry standard" 3-D EM field solver.
- The computed data is not used in any calculations involving measured data.

7.1.2.3 Requirements

Mated partial self-inductance is 4 nH maximum, assuming the current return is at infinity.

7.1.3 Mated Loop Inductance

The following procedures are required to properly test for mated loop inductance.

7.1.3.1 Test Procedure

The inductance of a loop is formed by a pair of pins. All current is injected in one pin and returned through the other. On a vector network analyzer using one port measurement, read the values from the Smith chart at the specified frequencies.

7.1.3.2 Test Condition

- Test Frequencies: 10 MHz (or 500 MHz) and 2 GHz
- See Figure 6 on page 29 for pin placement.

7.1.3.3 Requirements

Mated Loop inductance shall be 3 nH ± 10%—two nearest pins, current in one pin, return the other pin. Record all pin pattern readings, but use only the nearest neighbors for qualification.

7.1.4 Mated Partial Loop Inductance Matrix

The following procedures are required to properly test for mated partial loop inductance from measured mated loop inductance data.

Figure 7 shows the loop measurement for extracting $[L_P]$ for a mated three-pin combination

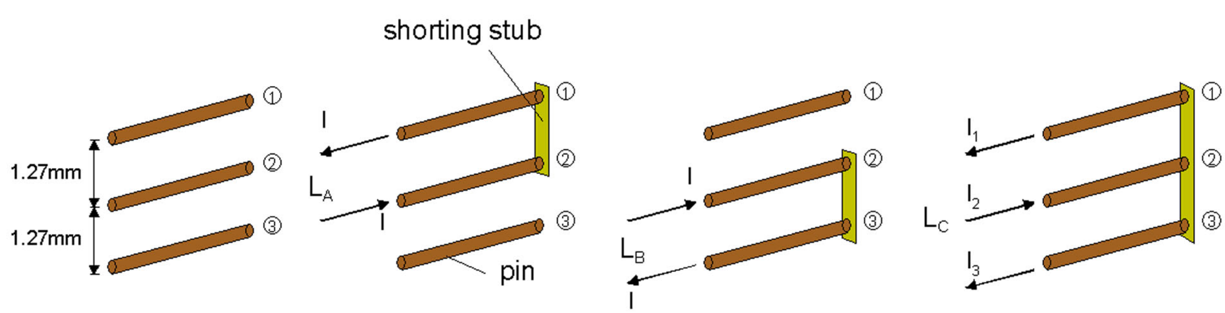


Figure 7. Loop Measurement for Extracting $[L_P]$ for a Mated Three-Pin Combination

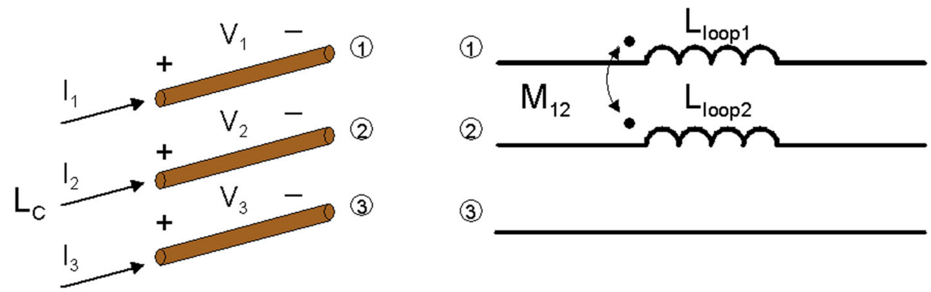


Figure 8. Current/Voltage Definitions and Equivalent Circuit of the Partial "Loop" Inductance Matrix

7.1.4.1 Test Procedure

As shown in Figure 7 on page 30, the partial inductance matrix of a mated three-pin combination that is extracted from a mated two-pin loop inductance measurements with one of the pins used as the reference (current return). Use the formula in Equation (1) below to calculate the Mated Partial Loop Inductance from measured mated loop inductance data.

$$M_{12} = \frac{L_{loop1} + L_{loop2} - L_{loop3}}{2} \quad . \qquad (1)$$

7.1.4.2 Test Condition

Test Frequencies are 500 MHz and 2 GHz.

7.1.4.3 Requirements

- M < 2 nH ± 10%—three pin loop with one pin used as reference.
- Measurement of the off diagonal entries in the loop partial inductance matrix.
- Diagonal entries of this matrix correspond to Mated Loop Inductance and must meet specified values in Section 7.1.3.3. on page 30.

7.2 Differential Impedance Definition

If the dimensions of the socket pins and the spacing between them are small compared to the wavelength of the highest frequency component of interest, then the impedance of the three-pin configuration shown in Figure 6 on page 29 and Figure 8 on page 31 can be calculated approximately from the lumped "loop" inductance and Maxwell capacitance matrices. When pins 1 and 2 in (Figure 8 on page 31) are driven differentially, with pin 3 acting as ground, then the differential impedance of the transmission line formed by this pin configuration is given by

$$Z_{diff} = 2\sqrt{\frac{L_{loop} - M_{12}}{C + C_{12}}} \quad . \qquad (2)$$

The Equation (2) definition of the differential impedance assumes that the driven (or signal) conductors have the same geometrical shape

***Note**: Equation (2) is only valid for non-symmetric differential lines in homogenous media.*

The differential impedance should be measured for all combinations of the three-pin arrangements as shown in Figure 6 on page 29. The pins are intentionally numbered in a specific manner as to yield identical $\lfloor L_{loop} \rfloor$ and $[C]$matrices for pin configurations (a) through (d). This is not the case for the pin arrangement in Figure 6e on page 29.

7.2.1 Differential Impedance

The following procedures are required to properly test for differential impedance.

7.2.1.1 Test Procedure

- Use the procedures shown in EIA-364-108 or see the equations in terms of partial loop inductance and Maxwell capacitance matrices. If the time domain method is used in measurement, then the signal should have rise time of 35 to 150 ps for signal amplitude to go from 10 – 90%.
- The differential transmission line impedance for three mated pins, using one pin as the voltage/current reference.
- Any frequency domain test equipment recommended in EIA-364-108 may be used to perform the measurements.
- If time domain equipment is used, it should have sufficient sampling rates to resolve the specified frequencies.

7.2.1.2 Test Condition

- Frequency or Time Domain Method
- Time Domain method uses a Rise Time: 35 to 150 ps, 10 to 90%
- Frequency Domain method use 500MHz and 2 GHz
- The differential impedance measured for a three-pin configuration (S1, S2, G).

7.2.1.3 Requirements

The acceptable range for differential impedance is 100 ± 10% Ω with an additional ± 2-Ω measurement error.

7.3 Differential and Single Ended Crosstalk

The following procedures are required to properly test for crosstalk.

7.3.1 Test Procedure

Use the procedures shown in EIA 364–90, Method A or B, for the definitions of crosstalk in terms of the elements of the measured $\left[L_{loop}^{partial}\right]$ and Maxwell capacitance matrices.

7.3.2 Test Condition

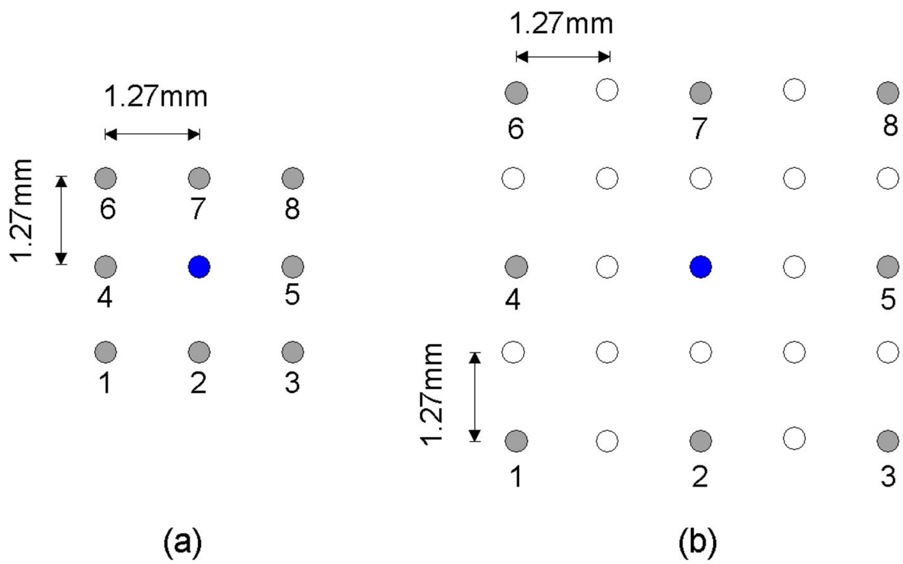
- Frequency or Time Domain Method
- For Time Domain method use Rise Time 35 to 150 ps, 10 to 90%
- For Frequency Domain method use 500 MHz and 2 GHz
- Measurements performed for specified pin pattern differential in Figure 6 on page 29 and single ended in Figure 9 on page 34 that include, minimum, the nearest, and next to nearest neighboring pins.

7.3.3 Requirements

Crosstalk should be recorded and serve as an accuracy check for the partial "loop" inductance $\left[L_{loop}^{partial}\right]$ and the Maxwell capacitance matrices.

7.4 Propagation Delay Skew

The propagation delay skew for single-ended signal pins is to be measured for the pin configurations shown in Figure 9 on page 34.



Note:
The blue color ( ) indicates the reference (or ground) pin.
The gray color ( ) indicates the driven pin.

Figure 9. Pin Configurations for the Propagation Delay Skew Measurements of Single-Ended Signals

Each measurement consists of driving one (gray-shaded) pin as signal and using the center pin (blue) as return. The propagation delay skew for all signal pins in Figure 9(a) are measured. The maximum allowable deviation for all the pins in the array must be less than the specified value. An identical set of measurements must also be repeated for the pin array shown inFigure 9(b).

The differential propagation delay skew is measured for every pin configuration shown in Figure 6 on page 29.. In each measurement the two gray-shaded pins (denoted 1 and 2) and driven as signals in differential form, using the blue pin as ground. The maximum allowable deviation in the propagation delay skew for all specified pin configurations must be less than the specified value.

7.4.1 Single Ended Propagation Delay Skew

The following procedures are required to properly test for single ended propagation delay.

7.4.1.1 Test Procedure

Use the procedures shown in EIA-364-103 for testing the single ended propagation delay skew.

Propagation delay skew can also be measured using a time delay reflectometer (TDR) by launching the signals through the designated pins, such as those inFigure 9. The signals are launched from the interposer and the delay skew is observed at the test board. The difference in the propagation times (delay skew) through different pins in the socket can be clearly seen and measured at the open circuited end of the test board.

7.4.1.2 Test Condition

For the time domain method:
Time delay of single-ended signals between the top pads of the interposer and the pads on the bottom side fixture.

The ground return for the specified signal pin pattern of single ended signals is to be located as specified

7.4.1.3 Requirements

- Delta delay (skew) among single ended pins between the top of the µPGA package and PCB under the Socket 754 must be 10 ps maximum plus 3 ps maximum measurement error.
- Three pins S1, S2, and G should be used for this measurement.

7.4.2 Differential Propagation Delay Skew

The following procedures are required to properly test for differential propagation delay skew.

7.4.2.1 Test Procedure

Use the procedures shown in EIA-364–103 and section 7.4.1.1 on page 34.

7.4.2.2 Test Condition

For the time domain method:
Time delay of a differential signal between the top pads of the interposer and the pads on the bottom side of the fixture.

7.4.2.3 Requirements

- Delta delay (skew) of a differential signal between the top of the µPGA Package and PCB under the Socket 754 must be 10 ps maximum plus 3 ps maximum measurement error.
- Three Pins S1, S2 and G should be used for this measurement

7.5 Capacitance

At low frequencies, the measurement of the capacitance should be carried out according to the EIA Standard EIA-364-30. Two types of measurements are required—single capacitance between the two nearest pins that are separated by 1.27mm and Maxwell capacitance matrix for multiple pins.

7.5.1 Test Procedures

Use the procedures shown in EIA-364-30 and section7.1.2.2 on page 30.

7.5.2 Test Condition

Test Frequencies: 500 MHz and 2 GHz

> ***Note***: *Do not short pins for this test.*

The matrix is defined as the Maxwell (not circuit) capacitance matrix.

7.5.3 Requirements

- The mated capacitance matrix of any two adjacent pins is 1 pF maximum.
- Measure from the top or bottom of the Socket.
- Mated capacitance of three neighboring pins is 1 pF maximum.
- The Maxwell capacitance matrix is measured for a specified mated three-pin configuration.
- The capacitance matrix of three neighboring pins that are in the same pattern as those used to extract the mated partial inductance matrix.

7.6 Electrical Specifications

Table 3 on page 37 contains a summary of the electrical parameter specification for Socket 754. The specifications do not include the effects of the fixtures.

Note: *Proper calibration should be used to de-embed the parasitic contributions for the fixture of the specified electrical parameter.*

Table 3. Summary of Required Measurements for the Socket 754

Measured Quantity	Definition	Specified Value(s)	Measurement	Applicable Standard
Mated partial self-inductance of a single pin. This is the only quantity in the specification that need not be measured. Values obtained from an accurate detailed 3-D EM field solver model are acceptable.	Partial self-inductance of a single mated (interposer-socket combination) pin that is calculated using a 3-D EM field solver.	Four nH maximum assuming the current return at infinity.	This quantity cannot be measured directly nor can it be calculated uniquely from the measurements.	See, Section 7.1.2, Mated Partial Self Inductance on page 29, for the discussion on the mated self-partial inductance. Use a validated "industry-standard" 3D EM field solver. This computed quantity *must not be* used in any calculations involving measured data.
Mated loop inductance of two nearest pins (i.e., pins separated by shortest distance).	The inductance of a loop formed by two nearest mated pins. All current is injected into one pin and returned through the other.	Three nH ± 10%	The inductance of a loop formed by two nearest pins, which are shorted at the bottom of the socket, with current injected into one pin and returned through the other.	See Section 7.1.3, Mated Loop Inductance, on page 30, for specified pin configurations.
Mated partial "loop" inductance matrix $\left[L_{loop}^{partial}\right]$ of three neighboring pins.	Partial inductance matrix of a mated three-pin combination extracted from mated two-pin loop- inductance measurements. One of the pins is used as the reference (current return).	$L_{loop} \leq 3\text{nH} \pm 10\%$ These are the diagonal entries in the "loop" partial inductance matrix. $M_{12} < 2$ nH ± 10%. These are the off-diagonal entries in the "loop" partial inductance matrix.	The partial inductance matrix is extracted from a series of two-pin loop inductance measurements (as described above) for specified three-pin configurations.	See Section7.1.4, Mated Partial Loop Inductance on page 30 for the definition of this matrix and the measurements that should be used to back-calculate the self and mutual partial "loop" inductances. Use the formulas in paragraph 7.1.4, Mated Partial Loop Inductance Matrix, equation (1)provided in this document.

Table 3. Summary of Required Measurements for the Socket 754 (Continued)

Measured Quantity	Definition	Specified Value(s)	Measurement	Applicable Standard
Mated capacitance between two nearest pins (i.e., pins separated by shortest distance).	The capacitance between two nearest mated pins.	One pF max.	Capacitance between two nearest pins measured from the top or bottom side of the socket. The pins are not to be shorted together for this measurement.	Use the EIA-364-30 standard for low frequency (10 MHz) measurements. Or, use the network analyzer for S-parameter measurements with minimum frequency of 500 MHz or lower. See Section 7.5.1, Test Procedures, on page 35
Mated capacitance matrix of three neighboring pins. The matrix is defined as the Maxwell (not circuit) capacitance matrix	The capacitance matrix of three neighboring pins that are in the same pattern as those used to extract the mated partial inductance matrix.	All entries in the matrix should not exceed 1pF.	The Maxwell capacitance matrix measured for the specified mated three-pin configurations. ***Note***: *The pins are not to be shorted together for this measurement.*	Use the EIA-364-30 standard for low frequency (10MHz) measurements. Or, use the network analyzer for S-parameter measurements with minimum frequency of 500 MHz or lower. See Section 7.5.1, Test Procedures, on page 35
Differential impedance between two nearest pins (i.e., pins separated by shortest distance).	The transmission line impedance of the odd mode for three mated pins, using one pin as the voltage/current reference.	100 Ω ± 10% with an additional ± 2-Ω measurement error	The differential (or an odd mode) impedance measured for a three-pin configuration (S1, S2, G). If equipment permits, this quantity may be measured directly. If not, it can be calculated from the measured mated partial “loop” inductance and Maxwell capacitance matrices according to equations provided in this document.	Use the EIA-364-108 standard or see the equations in terms of partial inductance and Maxwell capacitance matrices, Section 7.5, Capacitance, on page 35. If the time domain method is used in measurement, then the signal should have rise time of 35 to 150 ps for signal amplitude to go from 10 – 90%.

Table 3. Summary of Required Measurements for the Socket 754 (Continued)

Measured Quantity	Definition	Specified Value(s)	Measurement	Applicable Standard
Propagation delay skew among single ended signals.	Deviation in the propagation delay skew of a single ended signal through different mated (single) pins in the socket.	Ten ps max plus 3 ps max measurement error.	Time delay of single ended signal between the top pads of the interposer and the pads on the bottom side fixture. The ground return for the specified signal pin pattern of single ended signals is to be located as specified.	Use EIA-364-103 standard or provided in Section 7.4.1.1, Test Procedure, on page 34. See Figure 6 on page 29 for specified signal pin patterns, which also include the location of the current return pin.
Propagation delay skew among differential signal pairs.	Deviation in the propagation delay skew of differential signals through mated pin pairs in the socket.	Ten ps max plus 3 ps max measurement error.	Time delay of a differential signal between the top pads of the interposer and the pads on the bottom side of the fixture. The specified three-pin (S1, S2, G) arrangement should be used.	Use EIA-364-103 standard or provided in Section 7.4.1.1, Test Procedure, on page 34. See Figure 6 on page 29 for specified differential pin-pair patterns, which also include the location of the current return pin
Frequencies for the inductance measurements.	The frequencies at which inductance is to be measured.	500 MHz and 2 GHz	Any frequency domain test equipment recommended in EIA standards may be used to perform the measurements. If time domain equipment is used, it should have sufficient sampling rates to resolve the specified frequencies.	
Frequencies for the capacitance measurements.	The frequencies at which capacitance is to be measured.	500 MHz and 2 GHz	Any frequency domain test equipment recommended in EIA standards may be used to perform the measurements. If time domain equipment is used, it should have sufficient sampling rates to resolve the specified frequencies.	

Table 3. Summary of Required Measurements for the Socket 754 (Continued)

Measured Quantity	Definition	Specified Value(s)	Measurement	Applicable Standard
Cross talk between nearest single-ended and differential signals. This quantity should be reported and should serve as an accuracy check for the partial "loop" inductance $\left[L_{loop}^{partial}\right]$ and the Maxwell capacitance matrices.	Cross talk is defined as the voltage (and current) induced on quiet (non-driven) transmission lines (single-ended or differential) due to the nearest driven (single-ended or differentially driven) neighbors.	Cross talk should be measured and compared to the results predicted from the measured $\left[L_{loop}^{partial}\right]$ and Maxwell capacitance matrices.	Measurements are to be performed for specified pin patterns that will include, at least, the nearest and next to nearest neighbors.	Use EIA-364-90 standard: Method A or Method B for pin patterns specified in Figure 6 on page 29. See Section7.3, and Section 7.3.1, on page 33 for the definitions of cross talk in terms of the elements of the measured $\left[L_{loop}^{partial}\right]$ and capacitance matrices.
Resistance of a single mated pin. Minimum number of pin pairs to be tested is 168.	DC resistance of a single mated pin.	20 mΩ maximum for Alloy-194 at the end-of-life	The resistance measured between the top of the pin and the solder pad.	Use EIA-364-23 standard.
Minimum pin current rating.	DC current flowing through the mated pin.	1.2 Amps/pin at voltages ≤ 2 V for Alloy-194– The temperature rise for a specified pattern of currents due to heating should not exceed 20°C.		Use EIA-364-70 standard
Minimum breakdown voltage of the insulator.	Dielectric materials ability to withstand the stress due to the applied electric fields.	650 Vac		Use EIA-364-20 standard