



W2013 Indirect Quadrature Modulator with Gain Control

Features

- Wide supply range: 2.7 V to 5.5 V
- Operation over 2 GHz
- -10 dBm output into 50 Ω load (single ended) at 1.5 GHz
- Internal 90° phase shifter is accurate over an IF range from 50 MHz to 300 MHz
- Double-balanced active mixers minimize carrier feedthrough, require low local-oscillator (LO) power
- Automatic power control (APC) capability
- Low-current sleep mode

Applications

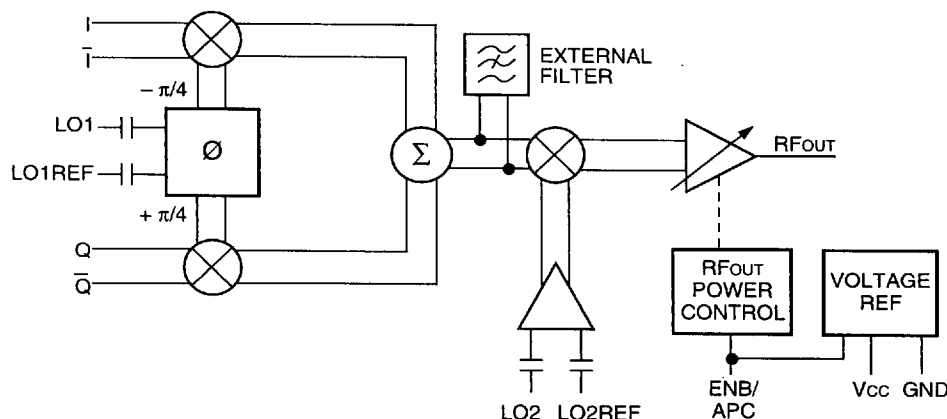
- North American IS-136/137
- Personal Digital Cellular (Japan RCR-27)
- Personal Handy Phone (Japan RCR-28)
- GSM/DCS-1800/PCS
- CDMA (IS-95)

Description

The W2013 is a monolithic integrated circuit that provides indirect, quadrature modulation of an RF carrier by I & Q baseband inputs. The function performed by the W2013 is particularly suited for hand-held digital and cellular cordless telephones that operate between 800 MHz and 2 GHz.

The circuit block diagram is shown below. From a single local-oscillator input (LO1), the phase shifter produces two LO signals with 90° phase separation and equal amplitude (see Figure 1). The LO signals are fed to the in-phase (I) and quadrature (Q) double-balanced mixers. The resulting signals are summed and fed into an RF mixer where the frequency can be translated to over 2 GHz. Outputs between the summer and RF mixer are available for external filtering. Finally, the signal is amplified to provide -10 dBm nominal at a 50 Ω single-ended output (1400 MHz).

The ENB/APC input with a logic low allows the device to be put into a powerdown mode, which typically consumes less than 1 μ A of supply current. Above the logic low threshold of about 0.9 V, the device enters a power control mode that provides a range of output power levels. Full output power is achieved when ENB/APC is above 2.5 V, independent of Vcc.

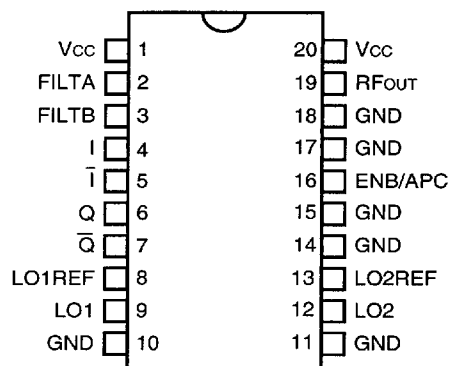


12-2787 (C)
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Figure 1. Circuit Block Diagram

0050026 0022254 5T9

Pin Information



12-2680 (C)

Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Name/Description
1	VCC	Positive Supply Voltage. For low-power/small-signal subcircuits.
2, 3	FILTA, FILTB	Filter. Nodes A & B for parallel resonant LC.
4, 5	I, $\bar{I}$	Differential Baseband Inputs.
6, 7	Q, $\bar{Q}$	Differential Baseband Inputs.
8, 9	LO1REF, LO1	First Local Oscillator Input. Either pin may be directly grounded.
10, 11, 14 15, 17, 18	GND	Power Supply Ground.
12, 13	LO2, LO2REF	Second Local Oscillator Input. Either pin may be directly grounded.
16	ENB/APC	Enable/Automatic Power Control.
19	RFOUT	RF Output.
20	VCC	Positive Supply Voltage. For high-power output stage.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	TA	-35	100	°C
Storage Temperature	Tstg	-65	150	°C
Lead Temperature (soldering, 10 s)	TL	—	300	°C
Positive Supply Voltage	VCC	—	6.0	Vdc
Power Dissipation	PD	—	750	mW
Output Current (continuous)	IOUT	—	160	mA
ac Input Voltage	—	—	VCC	VP-P
Enable Input Voltage	VENB	—	VCC	Vdc

Electrostatic Discharge Caution

This device may be damaged by electrostatic discharge (ESD) as low as 200 V. Protective measures should be taken during handling.

Operating Ranges

This table lists the ranges of external conditions in which the W2013 provides general functionality that may be useful in specific applications without risk of permanent damage. However, performance is not guaranteed over the full range of all possible conditions. The conditions for guaranteed performance are described in the Electrical Characteristics table.

Parameter	Min	Max	Unit
VCC	2.7	5.5	V
fLO1	50	300	MHz
PL01	-15	-5	dBm
fLO2	100	2100	MHz
PL02	-15	-5	dBm
fRF	<800	>2200	MHz
Maximum Output Power (frequency dependent)	-15	-5	dBm
I & Q Input Range of dc Bias for 1 VP-P Differential Input	1.3	VCC - 1.05	Vdc
I & Q Input Range of dc Bias for 1 VP-P Single-Ended Input	1.5	VCC - 1.05	Vdc
I (Q) to $\bar{I}$ ($\bar{Q}$) Differential Input Swing	—	1.1 V	VP-P
Ambient Operating Temperature	-35	85	°C

Electrical Characteristics

Table 2. Electrical Characteristics

Conditions (unless otherwise specified): $T_A = 25^\circ\text{C}$ nominal, $V_{CC} = 2.7\text{ V} \pm 50\text{ mV}$, $R_L = 50\ \Omega$, $f_{LO1} = 178\text{ MHz}$, $f_{LO2} = 1620\text{ MHz}$, $P_{LO1} = P_{LO2} = -10 \pm 3\text{ dBm}$, $V_{BIAS(I)} = V_{BIAS(\bar{I})} = V_{BIAS(Q)} = V_{BIAS(\bar{Q})} = 1.5\text{ Vdc}$, $I - \bar{I} = 0.5 \cdot \cos(2\pi t \cdot 80\text{ kHz} - \pi/2)$, $Q - \bar{Q} = 0.5 \cdot \cos(2\pi t \cdot 80\text{ kHz})$, $f_{RFOUT} = 1442.08\text{ MHz}$, $V_{APC} = 2.5\text{ Vdc}$, R_{FOUT} matched to $50\ \Omega$ ($V_{SWR} < 2:1$).

Parameter	Min	Typ	Max	Unit
Vcc Supply Current:				
Active Mode	—	38	44	mA
Sleep Mode @ $V_{CC} = 3.3\text{ V}$	—	<1	10	μA
Sleep Mode @ $V_{CC} = 5.5\text{ V}$	—	<1	150	μA
I & Q:				
I and Q Signal Path 1 dB Bandwidth	—	3.8	—	MHz
I and Q Signal Path 3 dB Bandwidth	—	7.5	—	MHz
I and Q Input Bias Current	—	500	1500	nA
I and Q Differential Input Signal for Maximum Output	—	1	—	V _{P-P}
LO1:				
LO1 Suppression (relative to output power)	—	45	—	dBc
LO2:				
LO2 Suppression (relative to output power)	20	35	—	dBc
Modulation Accuracy:				
Carrier Suppression (relative to wanted sideband)	35	50	—	dBc
Lower Sideband Suppression	35	45	—	dBc
Transmitted I and Q Amplitude Error	—	± 0.1	—	dB
Transmitted I and Q Phase Error	—	± 1	—	°
Error Vector Magnitude	—	1.3	5	%

Electrical Characteristics (continued)

Table 2. Electrical Characteristics (continued)

Conditions (unless otherwise specified): $T_A = 25^\circ\text{C}$ nominal, $V_{CC} = 2.7\text{ V} \pm 50\text{ mV}$, $R_L = 50\ \Omega$, $f_{LO1} = 178\text{ MHz}$, $f_{LO2} = 1620\text{ MHz}$, $P_{LO1} = P_{LO2} = -10 \pm 3\text{ dBm}$, $V_{BIAS}(I) = V_{BIAS}(\overline{I}) = V_{BIAS}(Q) = V_{BIAS}(\overline{Q}) = 1.5\text{ Vdc}$, $I - \overline{I} = 0.5 \cdot \cos(2\pi t \cdot 80\text{ kHz} - \pi/2)$, $Q - \overline{Q} = 0.5 \cdot \cos(2\pi t \cdot 80\text{ kHz})$, $f_{RFOUT} = 1442.08\text{ MHz}$, $V_{APC} = 2.5\text{ Vdc}$, R_{FOUT} matched to $50\ \Omega$ (VSWR < 2:1).

Parameter	Min	Typ	Max	Unit
RF Output:				
Output Power	-13	-10	-5	dBm
Output Power Dynamic Range of APC Control	32	40	—	dB
S11 (Normalized to 50 Ω):				
Output Impedance @ 836 MHz ($C_1 = 33\text{ pF}$)	—	$0.74 \angle 127.5^\circ$	—	mag/phase
Output Impedance @ 900 MHz ($C_1 = 33\text{ pF}$)	—	$0.75 \angle 123.8^\circ$	—	mag/phase
Output Impedance @ 1440 MHz ($C_1 = 22\text{ pF}$)	—	$0.74 \angle 96.4^\circ$	—	mag/phase
Output Impedance @ 1800 MHz ($C_1 = 10\text{ pF}$)	—	$0.78 \angle 76.4^\circ$	—	mag/phase
Output Impedance @ 1900 MHz ($C_1 = 10\text{ pF}$)	—	$0.79 \angle 71.2^\circ$	—	mag/phase
Output Impedance @ 2400 MHz ($C_1 = 10\text{ pF}$)	—	$0.81 \angle 46.0^\circ$	—	mag/phase
Adjacent Channel Suppression:				
0.35-DQPSK Modulation per IS54/136				
±30 kHz	—	-40	—	dBc
±60 kHz	—	-62	—	dBc
±90 kHz	—	-67	—	dBc
0.5-DQPSK Modulation per Japan PDC (RCR-STD27)				
±50 kHz	—	-63	—	dBc
±100 kHz	—	-70	—	dBc
0.5-DQPSK Modulation per Japan PHS (RCR-STD28)				
±600 kHz	—	-62	—	dBc
±900 kHz	—	-63	—	dBc
Enable/APC:				
V_{IHMIN} (higher voltage turns device on)	—	0.75	0.9	V
V_{ILMAX} (lower voltage turns device off)	0.4	0.6	—	V
I_{ILMAX} ($V_{ENABLE}/APC = 0.4\text{ V}$)	—	0	15	μA
I_{IHMAX} ($V_{ENABLE}/APC = 2.7\text{ V}$)	—	40	60	μA
Powerup/Powerdown Time	—	1	—	μs
APC Voltage for Minimum Output Power	—	—	1.0	Vdc
APC Voltage for Maximum Output Power	2.5	—	V_{CC}	Vdc
APC Bandwidth	—	10	—	MHz

Error Vector Magnitude (EVM) Testing

Error vector magnitude (EVM) is estimated by feeding signals to the W2013 as described at the top of the electrical specifications table. A hypothetical narrow-band, sine-wave modulation output spectrum appears in Figure 3.

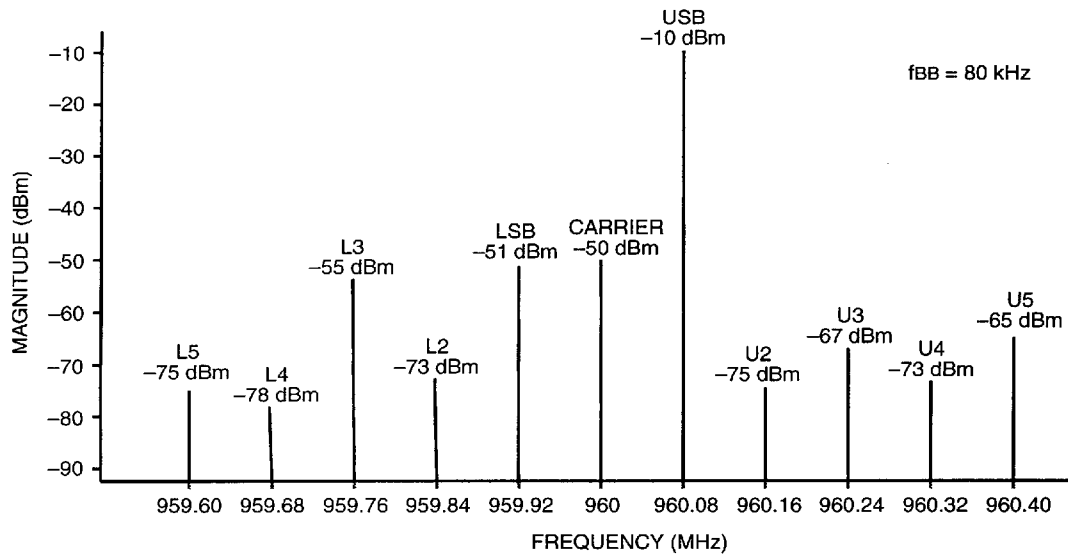


Figure 3. W2013 Sine Wave Modulation Output Spectrum

Data from this spectrum are used to estimate EVM by the formula:

$$\text{EVM (\%)} = 100 \cdot [10^{P(L5)/20} + 10^{P(L4)/20} + 10^{P(L3)/20} + 10^{P(L2)/20} + 10^{P(LSB)/20} + 10^{P(U2)/20} + 10^{P(U3)/20} + 10^{P(U4)/20} + 10^{P(U5)/20}] / 10^{P(USB)/20}$$

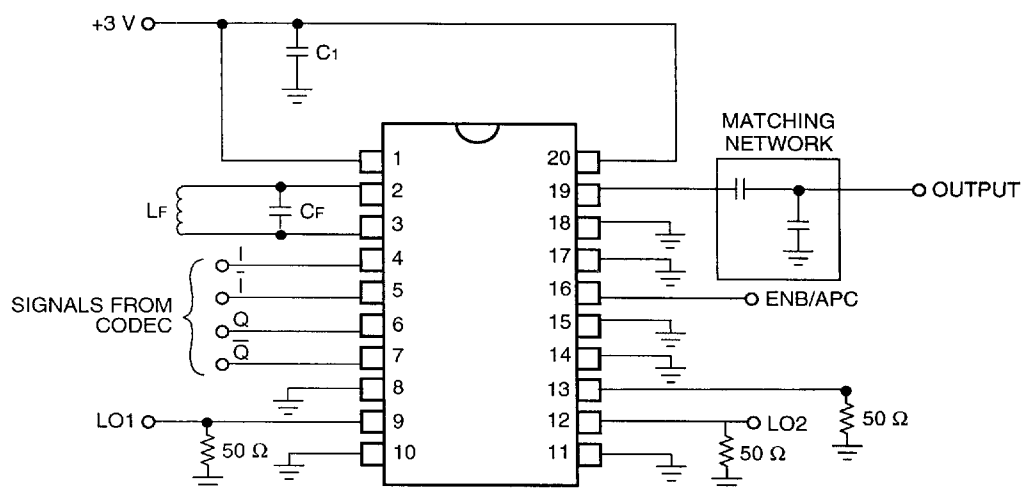
The data presented in the spectrum above would yield:

$$\begin{aligned} \text{EVM (\%)} &= 100 \cdot [179\text{e-}6 + 126\text{e-}6 + 1778\text{e-}6 + 224\text{e-}6 \\ &\quad + 2818\text{e-}6 + 178\text{e-}6 + 447\text{e-}6 + 224\text{e-}6 + 562\text{e-}6] / 316\text{e-}3 \\ &= 2.1\% \end{aligned}$$

This approximates worst-case digital modulation results because the sinewave modulation estimate assumes all spurious outputs are in phase and adds their magnitudes as scalars. In addition, this estimate includes full-amplitude measurements of spurious peaks which would appear in adjacent and alternate channels, where a receiver would otherwise provide attenuation. The L3 third-order intermodulation peak and LSB (lower sideband) are normally the unwanted output frequencies which dominate the EVM estimate.

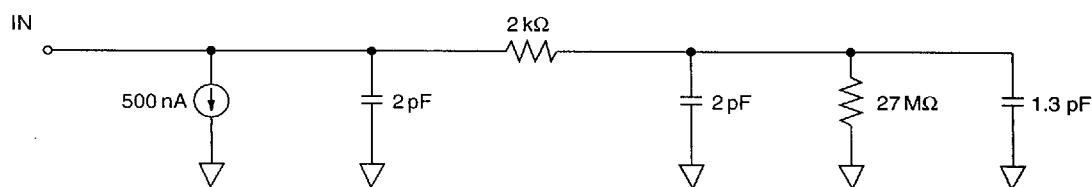
Application Circuits

A typical application circuit for the W2013 is shown in Figure 4. The LC filter components, L_F and C_F , are chosen to have a parallel resonance at the same frequency as LO1. The matching network will vary depending on the application, but must include a series capacitor to block dc connections to the W2013 output pin. For optimum performance, the bypass capacitor, C_1 , should have a series self-resonant frequency that is close to the output frequency and should be mounted near pin 20.



12-3258 (C)

Figure 4. Typical Application Circuit



5-4801 (C)
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Figure 5. Baseband Input Equivalent Circuit

Using the W2013

ENB/APC Function

The ENB/APC lead is used to turn the device on and to control the output power. If the voltage on this lead is below 0.6 V, then the device is in a low-current mode. Between 0.95 V and about 2.5 V, the device draws full supply current and is in a power-control mode. In this region, the output power will vary with the voltage on the ENB/APC lead as shown in Figure 6. Above 2.5 V, the device will transmit at full power.

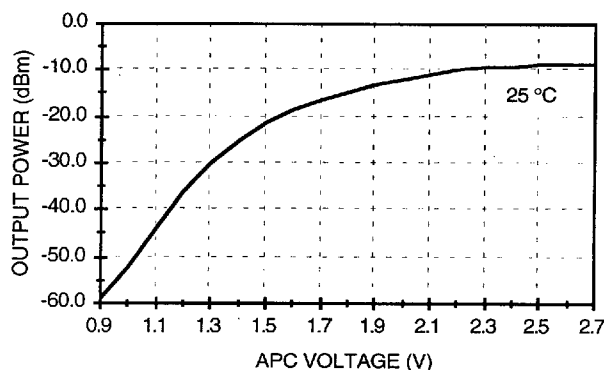


Figure 6. Typical Output Power vs. APC Voltage

Characteristic Curves

Unless otherwise specified, the test conditions are identical to those listed for Table 2.

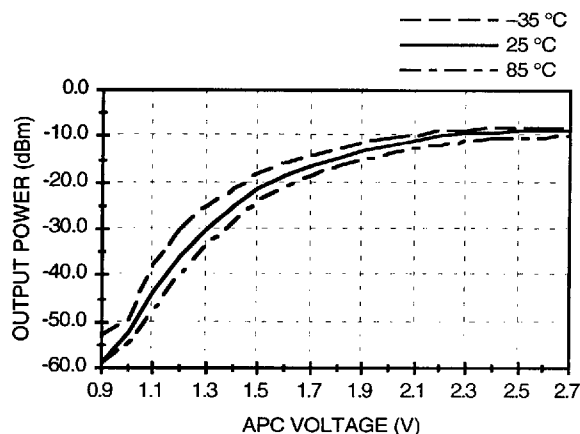


Figure 7. Output Power vs. APC Voltage

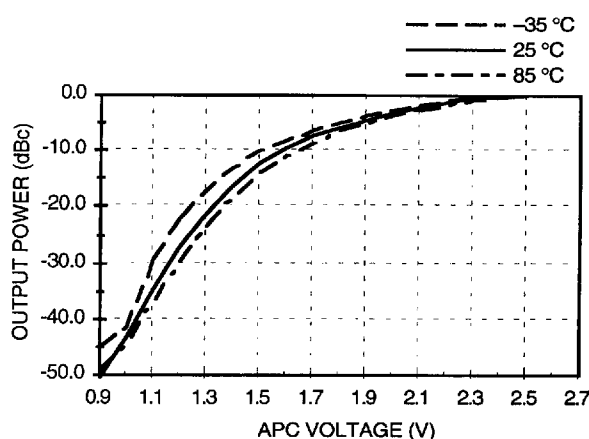


Figure 8. Output Attenuation vs. APC Voltage

Characteristic Curves (continued)

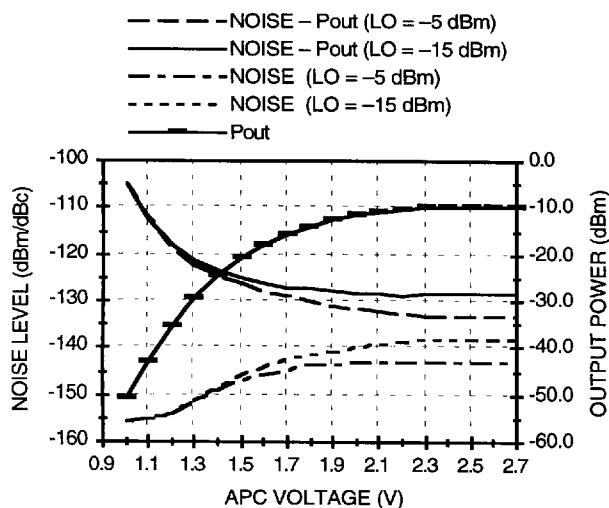


Figure 9. Noise vs. APC Voltage and LO Level

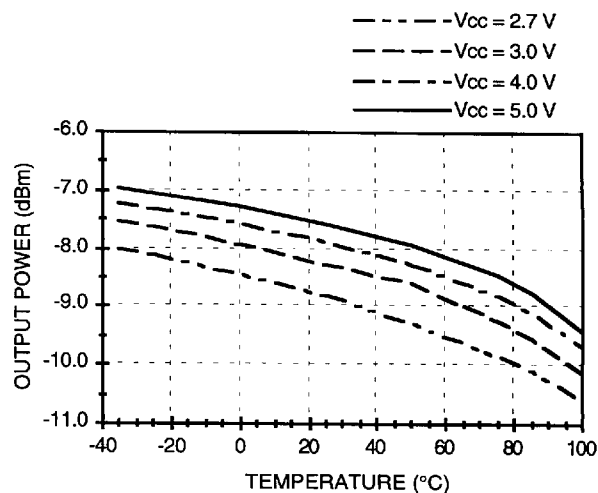


Figure 11. Output Power vs. Temperature

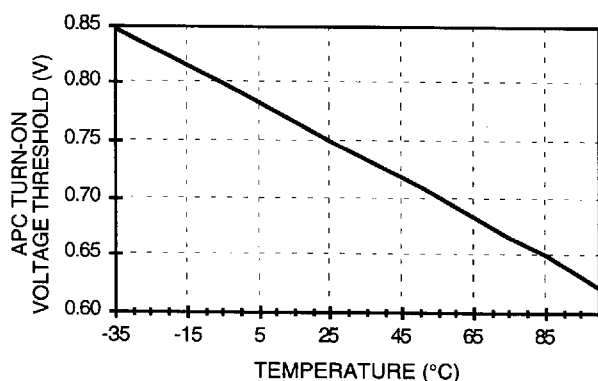


Figure 10. ENB/APC Turn-on Threshold Voltage vs. Temperature

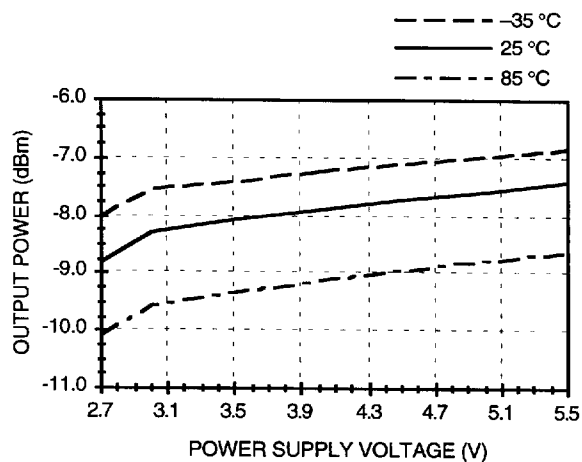


Figure 12. Output Power vs. Power Supply Voltage

Characteristic Curves (continued)

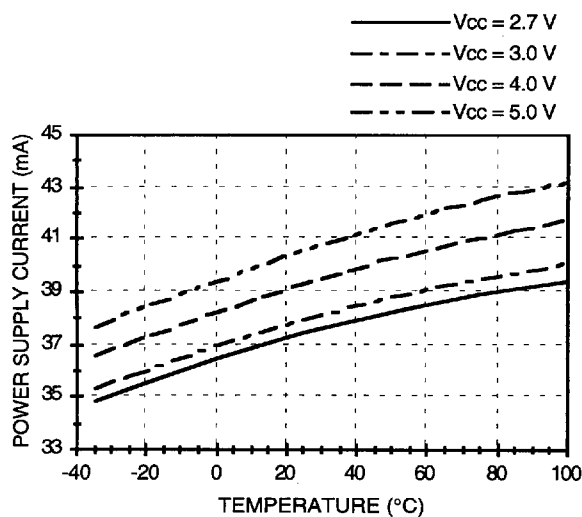


Figure 13. Power Supply Current vs. Temperature

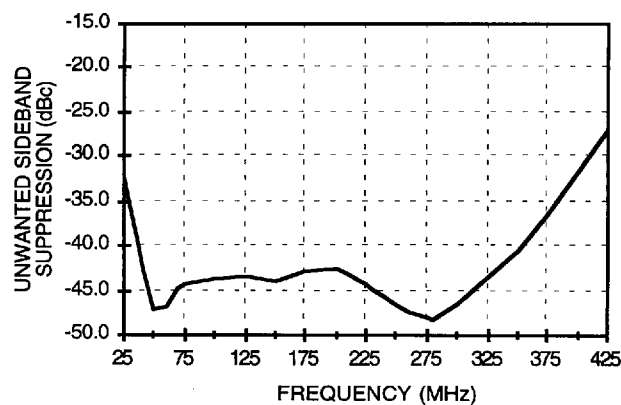


Figure 15. Unwanted Sideband Suppression vs. LO1 Frequency

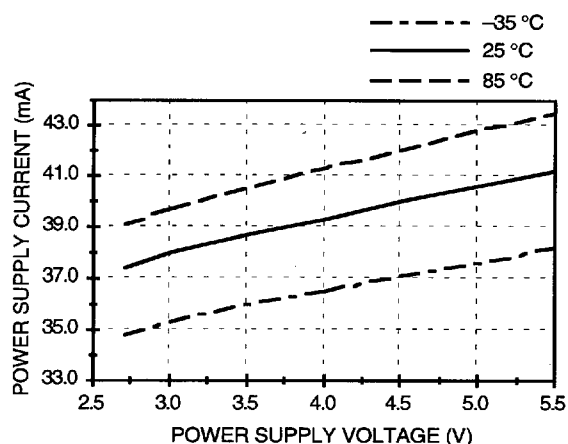


Figure 14. Power Supply Current vs. Power Supply Voltage

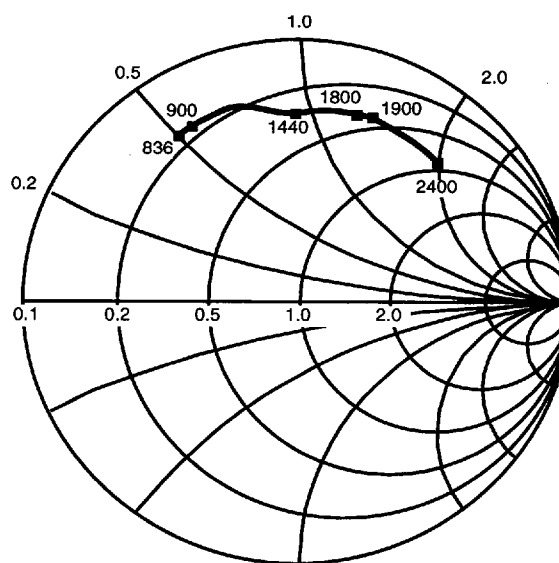
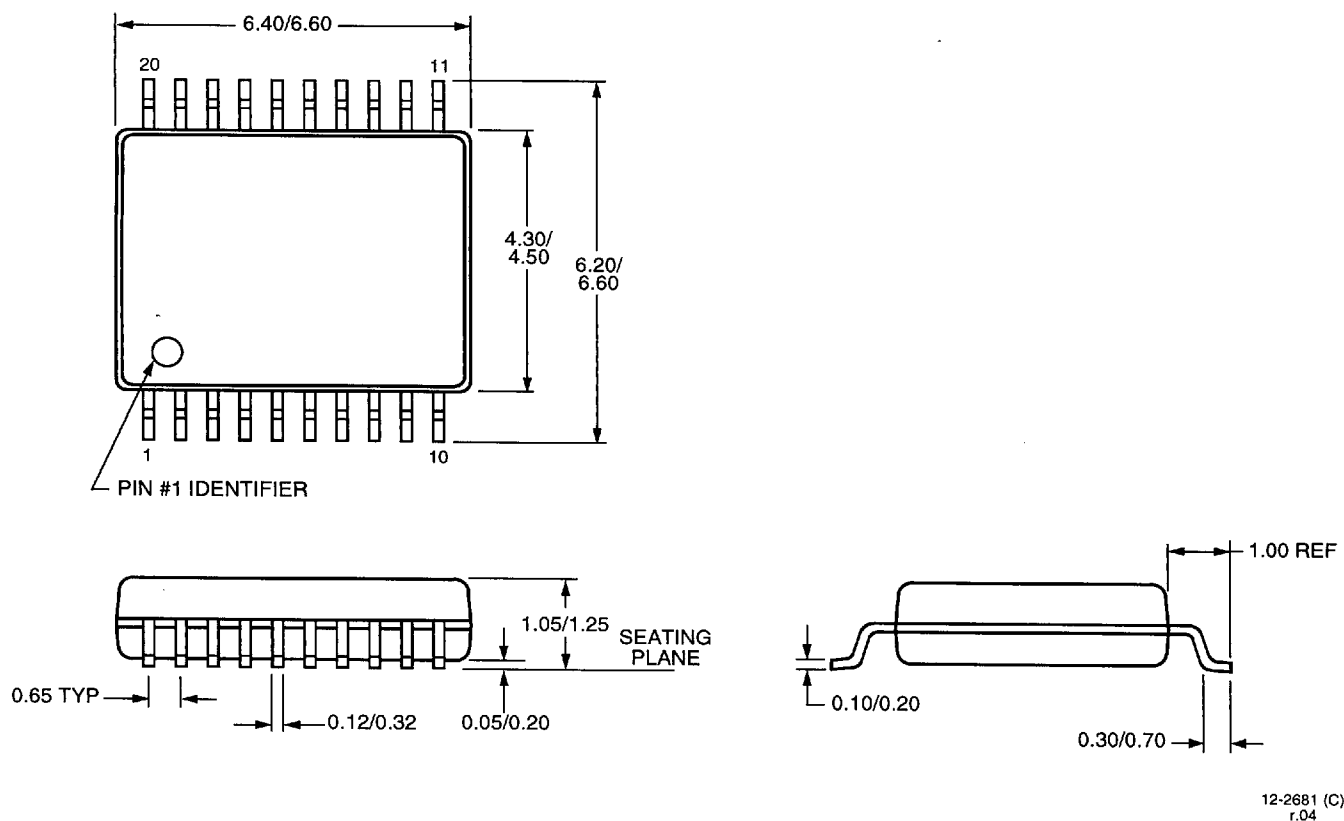


Figure 16. RF Output Impedance vs. Frequency (MHz) ($C1 = 0$ pF)

Package Outline

20-Pin SSOP

Dimensions are in millimeters.



Ordering Information

Device Code	Description	Package	Comcode
W2013CBY	Indirect RF Modulator	20-pin SSOP	107 410 904
W2013CBY-DT*		20-pin SSOP, dry-packed and tape and reel	107 410 953
EVB2013A	Evaluation Board	—	107 740 929

* Contact your Microelectronics Group Account Manager for minimum order requirements.

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