TMC2068P7C

Demonstration Board for the TMC22x5y Multistandard Digital Video Decoder

Features

- Accepts 10-bit digital composite, YC, or 8-bit analog composite.
- Outputs 10-bit digital RGB, D1, or YC_BC_R
- Locks to studio reference
- R-bus serial interface compatibility
- Fairchild demo board compatibility

Applications

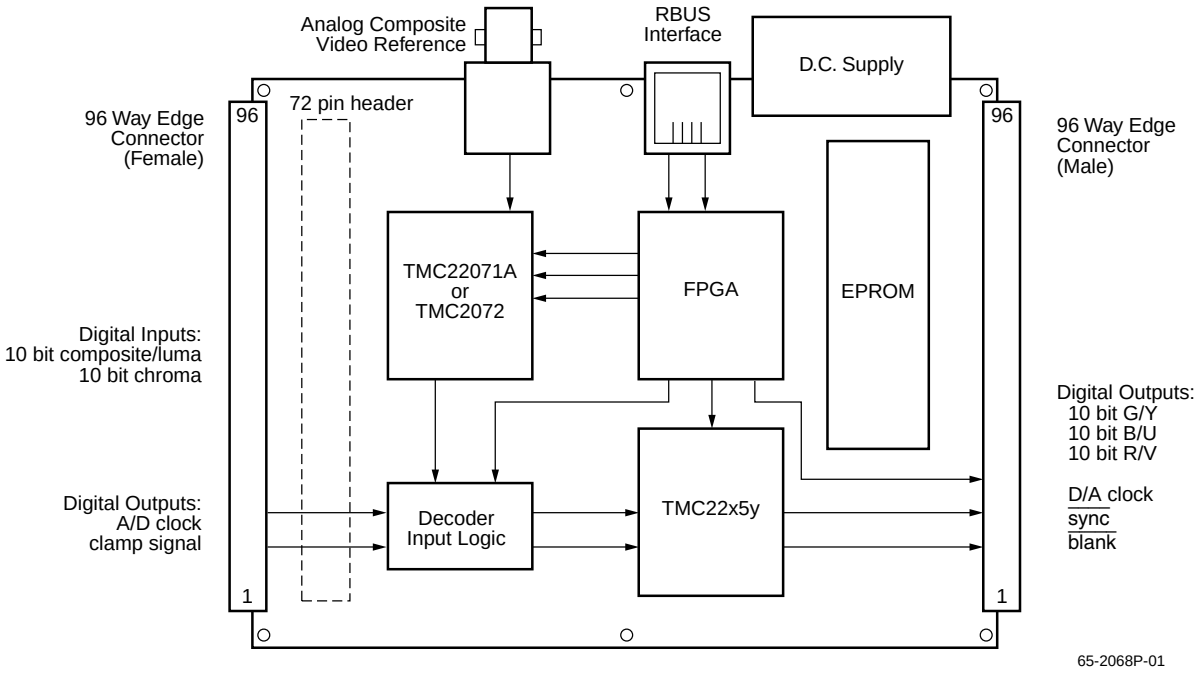
- Evaluation of TMC22x5y Digital Video Decoder
- Output for TMC2067P7C ADC demo board
- Input for Genesis 10-bit Line Doubler board
- Input for TMC2069P7C DAC demo board
- System Breadboarding

Description

The TMC2068P7C Demonstration Board showcases the TMC22x5y Digital Video Decoder. When used with a 10-bit A/D front-end, the decoder accepts digitized composite or YC and outputs D1, digital RGB, or YC_BC_R. When used without the 10-bit A/D front-end, the on-board TMC22071A or TMC2072 Genlocking Video Digitizer produces an 8-bit digital CVBS signal which the decoder uses to generate outputs.

Preliminary Information

Block Diagram



Functional Description

The TMC2068P7C is designed to demonstrate the performance of the TMC22x5y Digital Video Decoder. For complete descriptions of the TMC22x5y and TMC22071A/ TMC2072, please refer to the Fairchild Semiconductor Data Book. The TMC2068P7C is designed to be used in conjunction with other Fairchild demo boards, namely the TMC2067P7C ADC and TMC2069P7C DAC boards. The 96 pin edge connectors plug easily into each other. When used together, the boards demonstrate a high performance 10-bit digital video decoding system.

Note: To run the TMC2068P7C using the 10-bit TMC2067P7C input, set E2 to "YSEL", and close JP3. To run the TMC2068P7C as a stand-alone, using the 8-bit Genlock CVBS data, set E2 to "YSEL" and open JP3.

TMC22x5y Digital Video Decoder

The TMC2068P7C Decoder Demonstration Board was designed to showcase the TMC22x5y.

The TMC22x5y accepts digitized video input on two 10-bit buses, "YOVER[9:0]" and "COVER[9:0]". Based on the status of its control registers, it then outputs the data to the output edge connector of the board in a variety of formats. Please see Table 1 for a listing of video standards and output formats that are loadable to the control registers. The "FPGA" section of this documentation contains detailed instructions on how to program the TMC22x5y.

After the TMC22x5y control registers have been initially loaded by the FPGA and EPROM, subsequent changes to the control registers may be made through the R-bus interface and Raydemo software.

It is important that the control registers be loaded correctly in order to obtain the desired output. Once the control registers have been set to output the correct data from the TMC22x5y, then several board switches must also be correctly configured. A bank of switches labeled JP6 allows the user to select between digital RGB and D1 as outputs from the board to the output edge connector. Please see Table 3.

TMC22071A or TMC2072 Genlocking Video Digitizer

The TMC22071A or TMC2072 Genlocking Video Digitizer accepts analog composite data through a BNC on the top edge of the board. A 20MHz clock crystal provides the Genlock with an input clock. The TMC22071A or TMC2072 outputs digitized CVBS data, horizontal and vertical syncs, and a 27MHz clock. The clock is used to drive the Decoder and FPGA. Like the TMC22x5y, the Genlock part must be programmed at startup. Detailed instructions on how to do this are in the "FPGA" section of this documentation.

If the board is run as a stand-alone (i.e. no front-end supplying digital video), the Genlock accepts analog composite through the BNC and generates 8-bit digital CVBS data as well as horizontal and vertical syncs and a pixel clock.

When a 10-bit front end such as the TMC2067P7C is used to supply digital video to the Decoder, the Genlock still provides horizontal and vertical syncs and a clock to the Decoder and FPGA. The Genlock receives the incoming analog video through either the BNC labeled J1, or through the input edge connector. The option to use analog composite from the input edge connector is default selected at programming. In cases where this video may be too noisy, a short coaxial cable should be connected between J2 on the TMC2067P7C and J1 on the TMC2068P7C. Then the default Genlock register maps must be changed to accept input from the BNC instead of the input edge connector. This may be done by selecting the "VIN1" option for incoming video through the Raydemo software.

FPGA

An Altera EPF8820ATC144-4 FPGA executes several essential board functions. The FPGA controls initial programming of the Genlock and Decoder, a clamp pulse for the A/D board, a serial interface for the Genlock (unless a TMC2072 is installed), and several other important control signals (please see Figure 1).

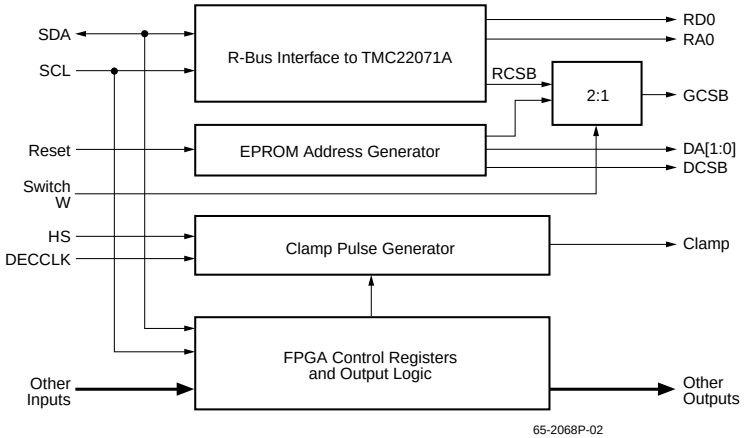


Figure 1. FPGA Block Diagram

The Altera 8820 controls the EPROM during Genlock and Decoder register map programming. The FPGA generates serial interface clocks and address information. It also provides the EPROM with addressing for the concurrent parallel interface data output. To program the Decoder and Genlock, the EA_{2-0} switches must be set to the mode of the incoming analog video (see Table 1.). Verify that switch W, along the bottom edge of the board, is HIGH (in the UP position). After the W and EA_{2-0} switches are set correctly, press the RESET button (S2) and the parts will program.

Table 1. TMC2068P7C Incoming Video Standard Selection

EA_{2-0}	Input Format	Video Standard	Output Format
000	(FPGA CONFIGURE)	N/A	N/A
001	composite	NTSC	YUV
010	Y/C	NTSC	D1
011	composite	PAL	YUV
100	Y/C	NTSC	YUV
101	composite	NTSC	D1
110	Y/C	PAL	YUV
111	composite	PAL	D1

The FPGA also generates a clamp pulse which is sent back to the A/D board over the 96 way edge connector. The default clamp pulse goes low exactly 199 pixel clock cycles after the horizontal sync pulse (HS) goes low and stays low for exactly 12 pixel clock cycles.

If a TMC22071A is the installed Genlock, the FPGA provides R-bus control of this part by interfacing R-bus data onto the 22071A parallel port. To perform this function, switch W must be LOW (in the DOWN position). The Raydemo reserved TMC22071A R-bus address is 0000000.

The FPGA control registers may also be written to using the Raydemo software. The Raydemo FPGA R-bus address is 0000001.

Several other control signals are inputs to or outputs of the FPGA. They are briefly described in Table 2. For a more complete description of signals going to or coming from the TMC22x5y and TMC22071A/TMC2072, please refer to the Fairchild Semiconductor Data Book.

Note: At powerup, the FPGA will only configure itself if the EA_{2-0} switches are all set low. If the board was powered up with the switches in a different position, adjust the EA_{2-0} switches so that they are all low and press the CONF (S4) button.

Table 2. FPGA Input and Output Signal Descriptions

Signal Name	Input/Output	Origin/Destination	Description
$\overline{\text{BLANK}}$ (DAC)	Output	Output edge connector	Signal supplied to output connector.
BUFFER	Output	Decoder	Decoder control register select bit .
CLAMP	Output	Input edge connector	FPGA supplied negative-going clamp pulse for the A/D board triggered by HS (horizontal sync) input.
CLKSEL	Output	U43 (multiplexer)	Selects either Genlock generated clocks and syncs or externally generated clocks and syncs from the input edge connector.
COE10	Output	Input edge connector	When E20 is set to “CSEL” and E21 is set to “CFPGA” this signal controls enabling of the external “C” data.
CONF	Input	S4 (pushbutton labeled “CONF”)	Triggers FPGA configuration sequence when pressed then released.
COVER[9:0]	Output	Decoder	Decoder 10-bit input data to VIDEO_B[9:0] input pins
CREF	Output	Output edge connector	Signal supplied to output connector.
CVBS[7:0]	Input	Genlock	Digitized 8-bit Genlock output.
D1	Output	Output edge connector	Signal supplied to output connector.
D1ENFS	Output	Output edge connector	Signal supplied to output connector.
DA0	Output	Decoder	Initial programming parallel interface control signal.
DA1	Output	Decoder	Initial programming parallel interface control signal.

Preliminary Information

Table 2. FPGA Input and Output Signal Descriptions (continued)

Signal Name	Input/Output	Origin/Destination	Description
DCSB	Output	Decoder	Initial programming parallel interface control signal
DECCLK	Input	U43 (multiplexer)	Mux-selected pixel clock (either supplied by Genlock or from input edge connector)
$\overline{\text{DRST}}$	Output	Decoder	Decoder reset control
DRW	Output	Decoder	Decoder control signal
EPEN	Output	U37 (EPROM)	EPROM enable control
FSER	Output	P2 (72 pin header)	Control signal for framestore board
FSOE	Output	P2 (72 pin header)	Control signal for framestore board
GCSB	Output	Genlock	Initial programming parallel interface control signal
GLSDA	Output	Genlock	Genlock control signal
$\overline{\text{GRST}}$	Output	Genlock	Genlock reset control
HREF	Output	Output edge connector	Signal supplied to output connector
HS	Input	U43 (multiplexer)	Mux-selected negative-going horizontal sync pulse (either supplied by Genlock or from input edge connector)
IMASTER/ SLAVE	Input	Input edge connector	Signal which informs the FPGA if the previous board wishes to supply clocks and syncs or not
MASTER[1:0]	Output	Decoder	Decoder control select bits
NTSC/PAL	Output	Output edge connector	Signal supplied to output connector
PGM_IN	Input	Input edge connector	Negative-going reset pulse specific to this board logically ANDed with PGM_START and $\overline{\text{RESET}}$
PGM_OUT	Output	Output edge connector	Negative-going reset pulse for the board connected to the output connector
PGM_START	Input	S2 (pushbutton labeled “RESET”)	Local signal to reset Genlock and Decoder control registers logically ANDed with PGM_IN and $\overline{\text{RESET}}$
RA0	Output	Genlock	R-bus to parallel interface control signal
RCSB	Output	Genlock	R-bus to parallel interface control signal
RD0	Output	Genlock	R-bus to parallel interface control signal
$\overline{\text{RESET}}$	Input/output	Input/Output edge connectors	Universal negative-going reset pulse logically ANDed with PGM_START and PGM_IN (disable universality with JP42)
RGB	Output	Output edge connector	Signal supplied to output connector
SWW	Input	S1 (switch bank)	R-bus enable bit (low to enable)
VREF	Output	Output edge connector	Signal supplied to output connector
VS	Input	U43 (multiplexer)	Mux-selected negative-going vertical sync pulse (either supplied by Genlock or from input edge connector)
XRS[3:0]	Input	Input edge connector	Externally generated TRS data

Quick Setup/Verification for Composite NTSC Input, YUV Output

1. Configure jumpers:

   If running with 10-bit front-end, JP3 must be closed (connected)

   If running with 8-bit Genlock CVBS, JP3 must be open (not connected)

   If using R-Bus interface, JP1 must be closed (connected)

2. Configure slider-switches (push red slider TOWARD specified marking on board) :

   E3Hum Rejection “ON”
   E4“PXCK4”
   E68“DVS”
   E67“DHS”
   E26“LDV”
   E25“LDV”
   E24“GPXCK”
   E23“GPXCK”
   E21“CON”
   E20“COFF”
   E2“YSEL”
   E1“SETV”
   JP6[0:9]all set to “GY”

3. Ensure BNC J1 (VIN1) is connected to composite NTSC signal. This may be done by attaching a scope probe to TP7.

4. Ensure piano-key switch W is in the “HIGH” (up) position.

5. Ensure piano-key switches $EA_{2\text{-}0}$, Y are in the “LOW” (down) position.

6. If using R-Bus, ensure R-Bus connector plugged-in and switches T, U, V match desired TMC22x5y $SA_{2\text{-}0}$ serial address.

7. Plug in power-supply connector and apply power. LED’s corresponding to applied voltages should light-up. The EPF8820 CONF_DONE pin (attached to H25) should go “HIGH” to signify that the FPGA is correctly programmed. This may be carefully checked with either a scope probe or a DVM.

8. Flip piano-key switch EA0 to the “HIGH” (up) position.

9. Press and release the RESET button (S2). The TMC22071A and TMC22x5y should both be programmed. To verify the TMC22071A is functioning correctly, check for presence of sync pulses, VS (TP67) and HS (TP68). Likewise, to verify the TMC22x5y is functioning correctly, check for presence of DHSYNC (TP5) and DVSYNC (TP6).

10. To utilize R-Bus, switch W must be set “LOW” (down). However, it must be returned to “HIGH” (up) for every reset of the board.

Table 3. TMC2068P7C Switch and Jumper Descriptions

Switch/Jumper Designator (location on board)	Option	Switch Setting
E1 (bottom middle of board)	Manual control of Decoder $\overline{SET}$ pin	“SETX” to control with switch X, “SETV “ to set to VSYNC pulse
E2 (lower middle column)	Manual control of Y data through JP3	when “YSEL” high and JP3 closed, external Y enabled (Genlock CVBS disabled) when “YSEL” high and JP3 open, external Y disabled (Genlock CVBS enabled)
E20 (lower middle column)	Manual control of C data	“COFF” to disable, “CSEL” to defer control to E21
E21 (lower middle column)	Select Enabling of C data	“CON” to enable, “CFPGA” to defer control to FPGA
E23, E24 (lower middle column)	Clock Multiplexer bypass	“GPXCK” to bypass mux and operate on Genlock PXCK “MUX” to drive clock from selected mux output (E26)
E25 (lower middle column)	Select Regular/Inverted LDV Genlock Pixel Clock	“LDV” for regular, “$\overline{LDV}$” for inverted
E26 (lower middle column)	Select LDV or VSYNC as a source for external clock option (E24)	“LDV” for Genlock pixel clock, “VSYNC” for external VSYNC

Table 3. TMC2068P7C Switch and Jumper Descriptions (continued)

Switch/Jumper Designator (location on board)	Option	Switch Setting
E3 (upper middle of board)	Select Hum Rejection	"ON" for normal operation (If switch is set to "OFF" position, incoming composite signal must have an external DC bias)
E4 (middle right column)	Select Regular/Inverted Output Clock	"PXCK4" for regular, "$\overline{\text{PXCK4}}$" for inverted
E67 (middle right column)	Select Regular/Inverted Output HSYNC	"DHS" for regular, "$\overline{\text{DHS}}$" for inverted
E68 (middle right column)	Select Regular/Inverted Output VSYNC	"DVS" for regular, "$\overline{\text{DVS}}$" for inverted
EA0 (bottom right)	Sets MSB of EPROM address	Up to set HIGH, down to set LOW
EA1 (bottom right)	Sets 2nd to MSB of EPROM address	Up to set HIGH, down to set LOW
EA2 (bottom right)	Sets 3rd to MSB of EPROM address	Up to set HIGH, down to set LOW
JP1 (top middle)	Enable R-bus serial interface	Closed to enable R-bus, open to disable
JP3 (lower middle)	Enable Y input	When E2 set to "YSEL", JP3 is closed to enable Y input, open to disable (closed for 10-bit front end operation, open to use Genlock 8-bit digitized data)
JP42 (middle right)	Enable S2 (pushbutton) as universal board reset to reset every component on TMC2068P7C and all other boards connected through input and output connectors	Closed to enable universal reset open to enable reset to FPGA only
JP5 (middle right)	Set D1 input to FPGA	Closed to set low, open to set high
JP6 (switch column in lower right)	Select between Digital RGB (e.g. TMC2069P7C) or D1 output (e.g. Genesis line doubler) through the output connector	All set to "GY" (left) for digital RGB All set to "RV" (right) for D1
Q (bottom left)	Sets Genlock SA0 R-bus address if TMC2072 is installed	Up to set HIGH, down to set LOW
R (bottom left)	Sets Genlock SA1 R-bus address if TMC2072 is installed	Up to set HIGH, down to set LOW
S (bottom left)	Sets Genlock SA2 R-bus address if TMC2072 is installed	Up to set HIGH, down to set LOW
T (bottom left)	Sets Decoder SA0 R-bus address	Up to set HIGH, down to set LOW
U (bottom left)	Sets Decoder SA1 R-bus address	Up to set HIGH, down to set LOW
V (bottom left)	Sets Decoder SA2 R-bus address	Up to set HIGH, down to set LOW
W (bottom left)	R-bus enable	down to enable R-bus, up to disable

Table 3. TMC2068P7C Switch and Jumper Descriptions (continued)

Switch/Jumper Designator (location on board)	Option	Switch Setting
X (bottom left)	Sets “SETX” signal high or low	Up to set “SETX” HIGH, down to set LOW. Used in conjunction with E1 as a decoder input
Y (bottom right)	Factory Test Bit	Set low

Power Supply Requirements

The TMC2068P7C power supply connector is on the top edge of the board toward the right side. The TMC2068P7C board alone requires a DC power supply voltage of +5V. The connectors for -5V, +12V, and -12V are also made available as a convenience option to power the TMC2067P7C, TMC2068P7C, and TMC2069P7C through a single connector on the TMC2068P7C. The TMC2067P7C and TMC2069P7C do have separate connectors which may be used instead.

The +5V supply provides power and voltage references to the TMC22x5y and TMC22071A/TMC2072, as well as driving TTL logic devices. It is for this reason that a bench power supply with short cable lengths is recommended.

Schematics

Preliminary Information

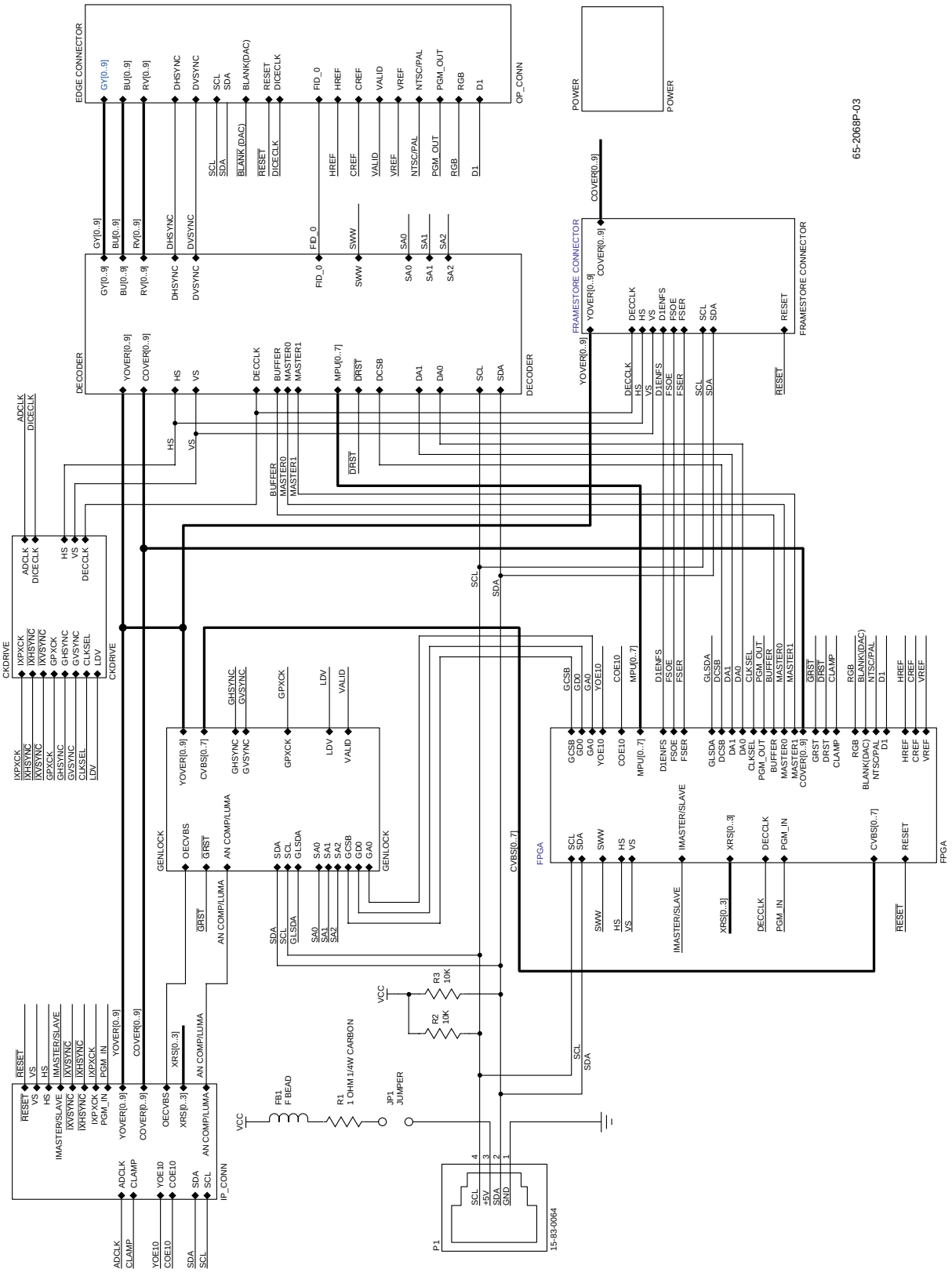


Figure 2. TMC22x5y.SCH

Schematics (continued)

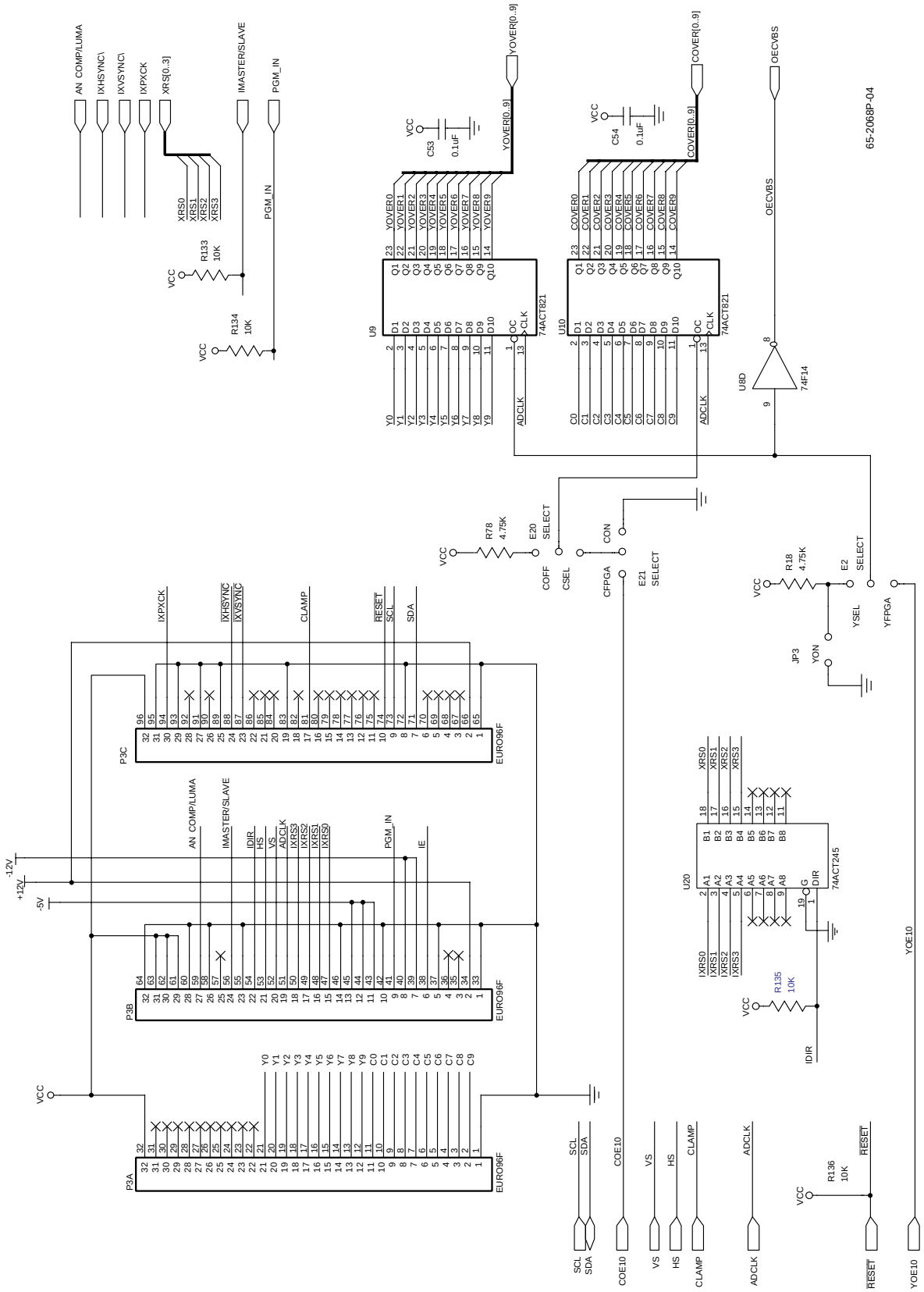


Figure 3. IP_CONN.SCH

Schematics (continued)

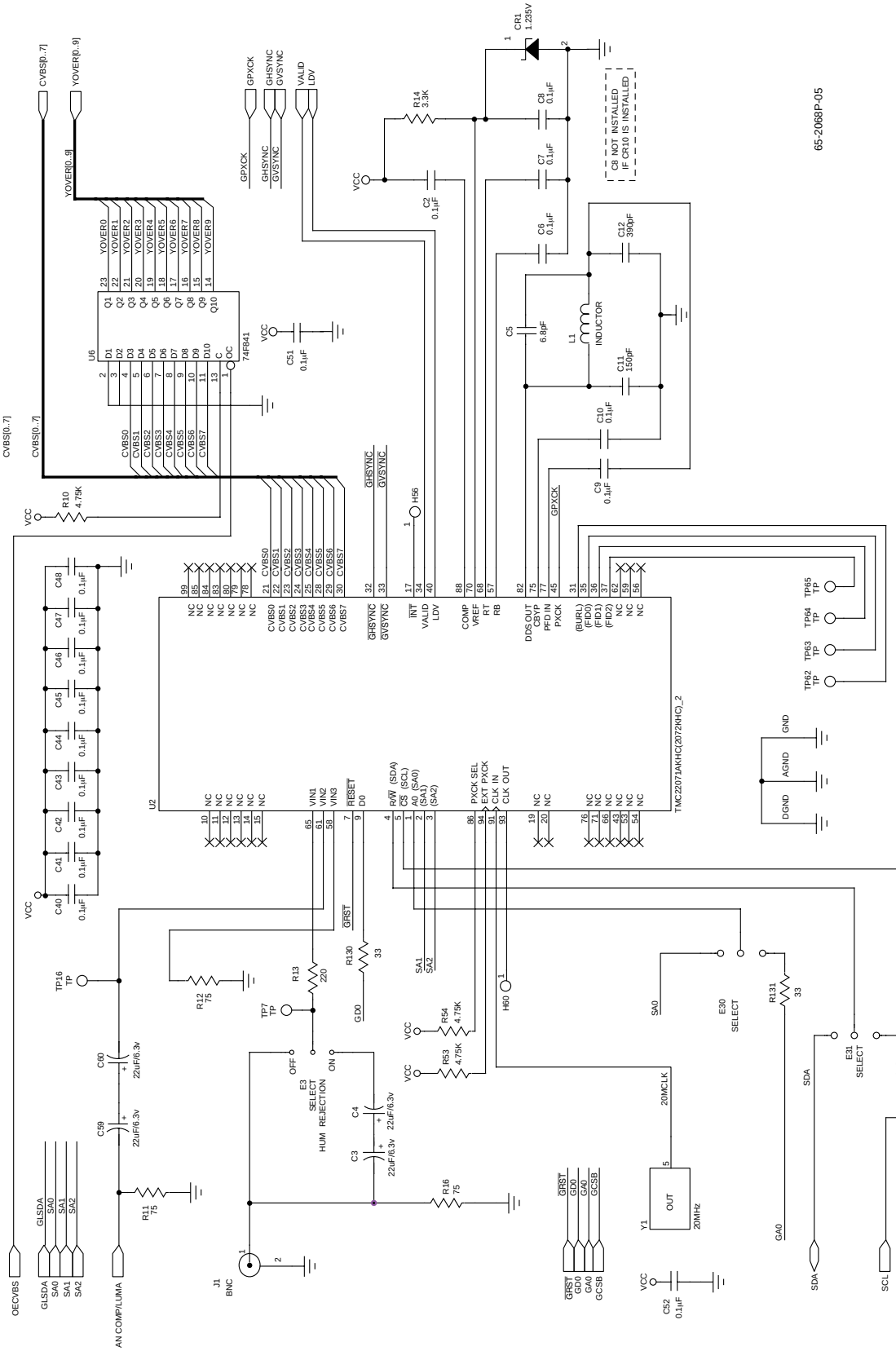


Figure 4. GENLOCK.SCH

Schematics (continued)

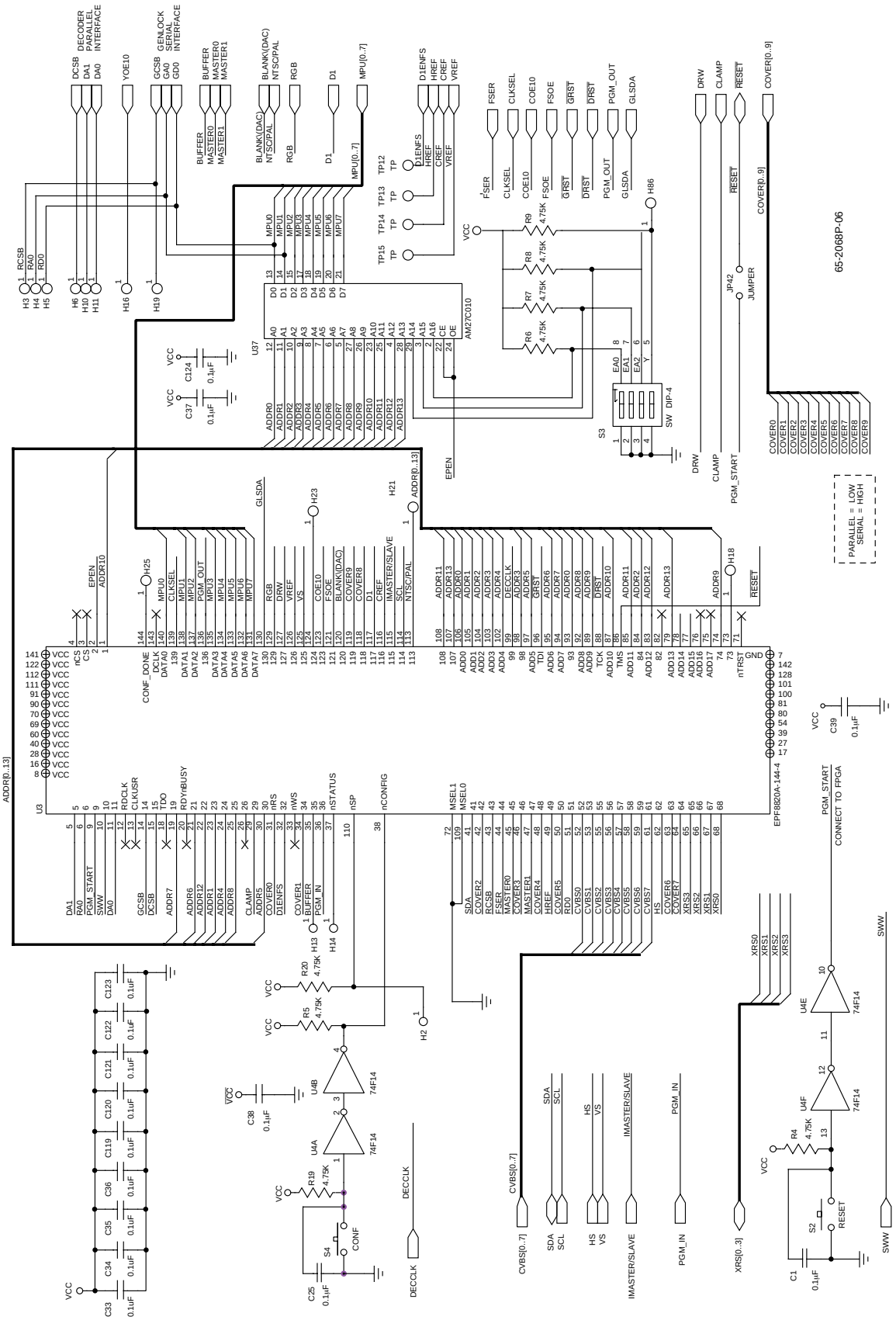


Figure 5. FPGA.SCH

Schematics (continued)

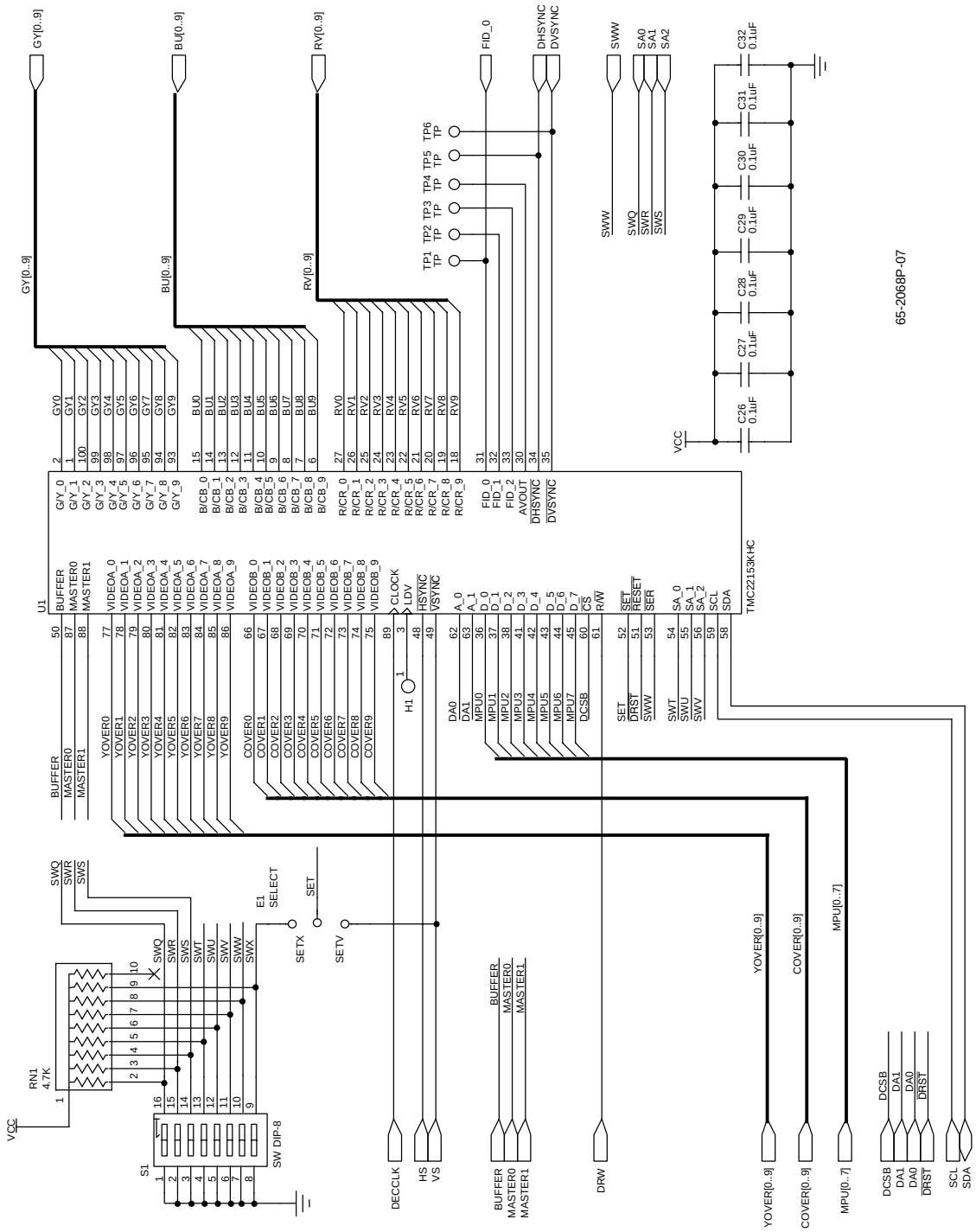


Figure 6. Decoder.SCH

Preliminary Information

Schematics (continued)

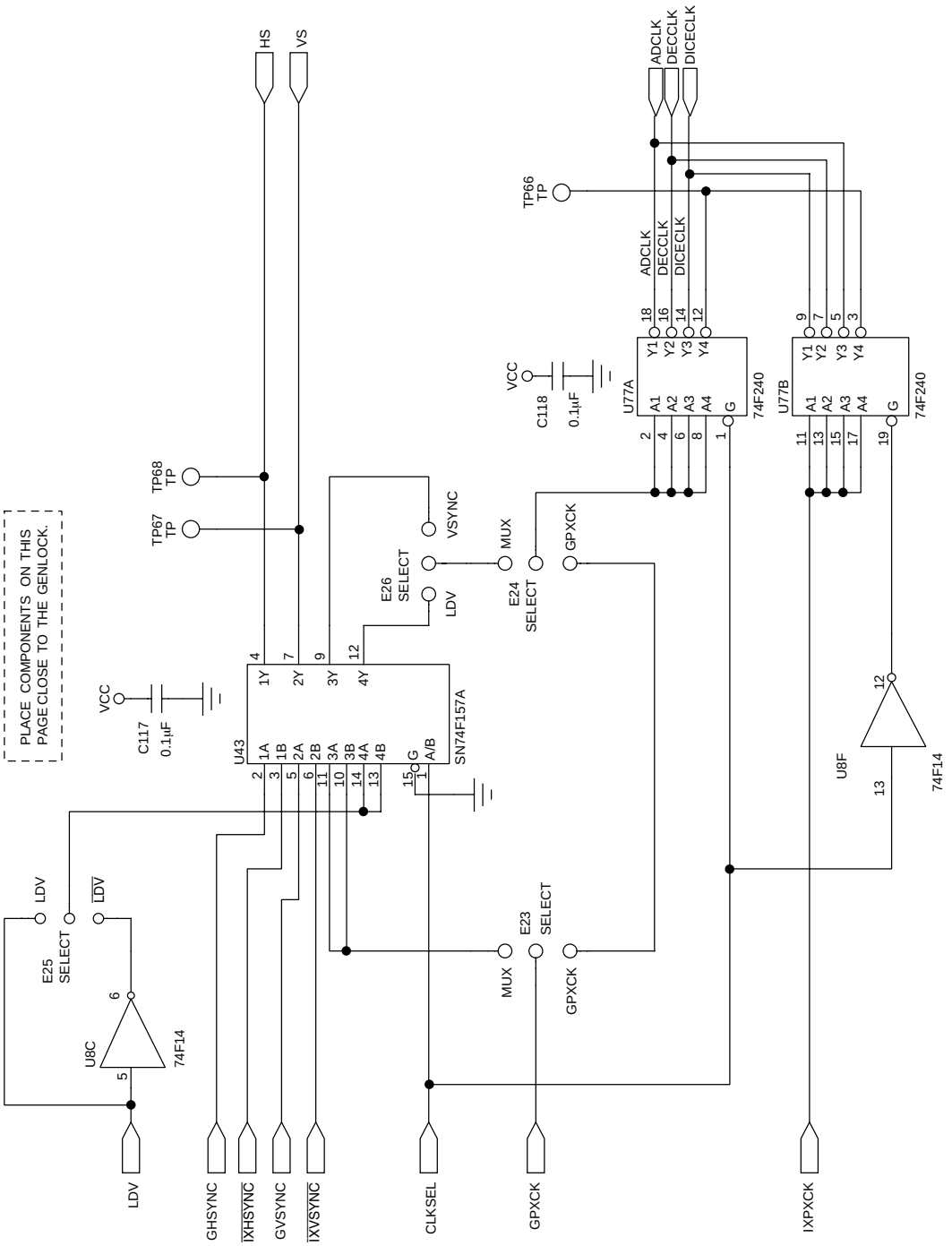


Figure 7. CKDRIVE.SCH

Preliminary Information

Schematics (continued)

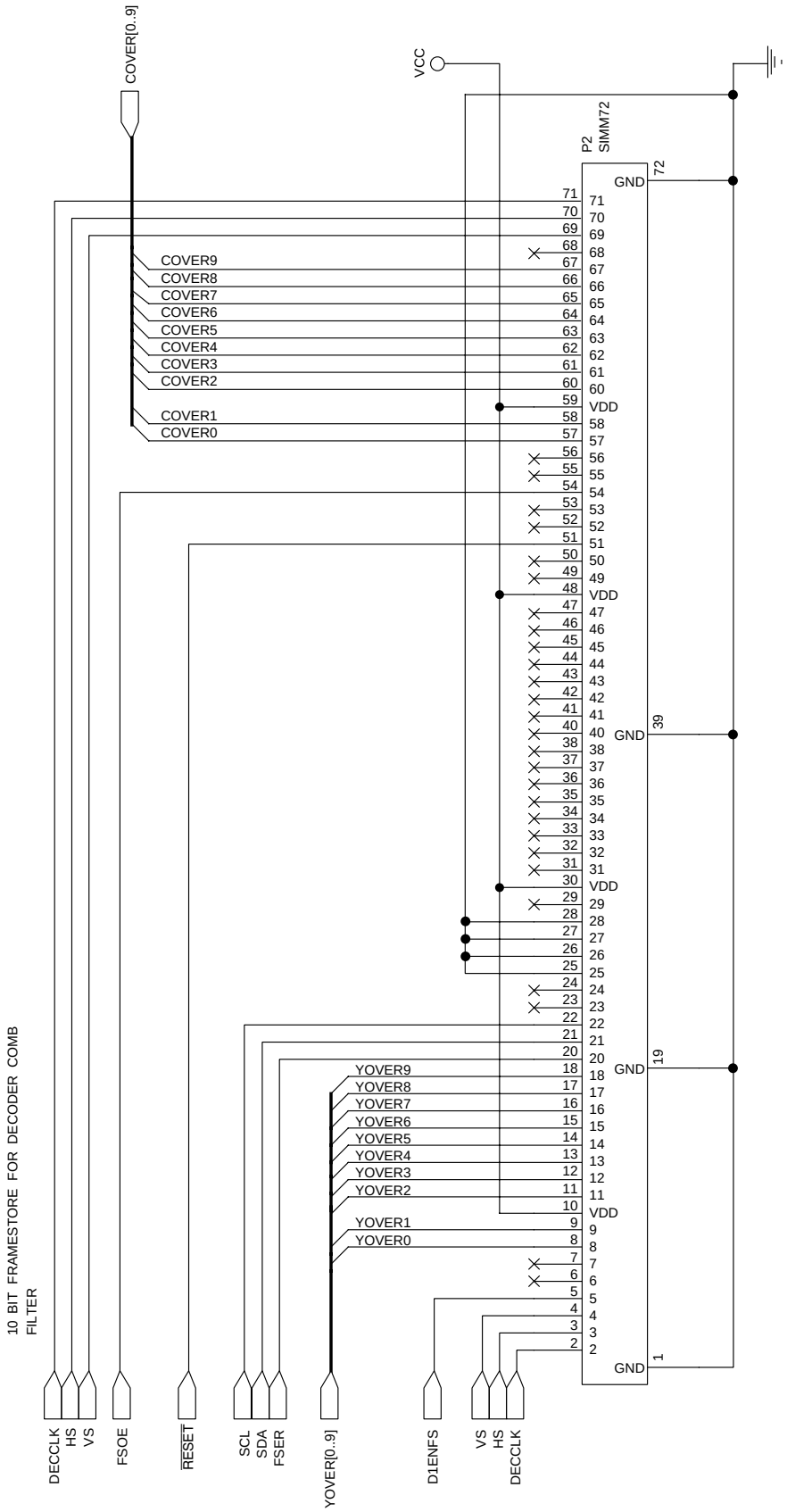


Figure 8. Framestore Connector

Preliminary Information

Schematics (continued)

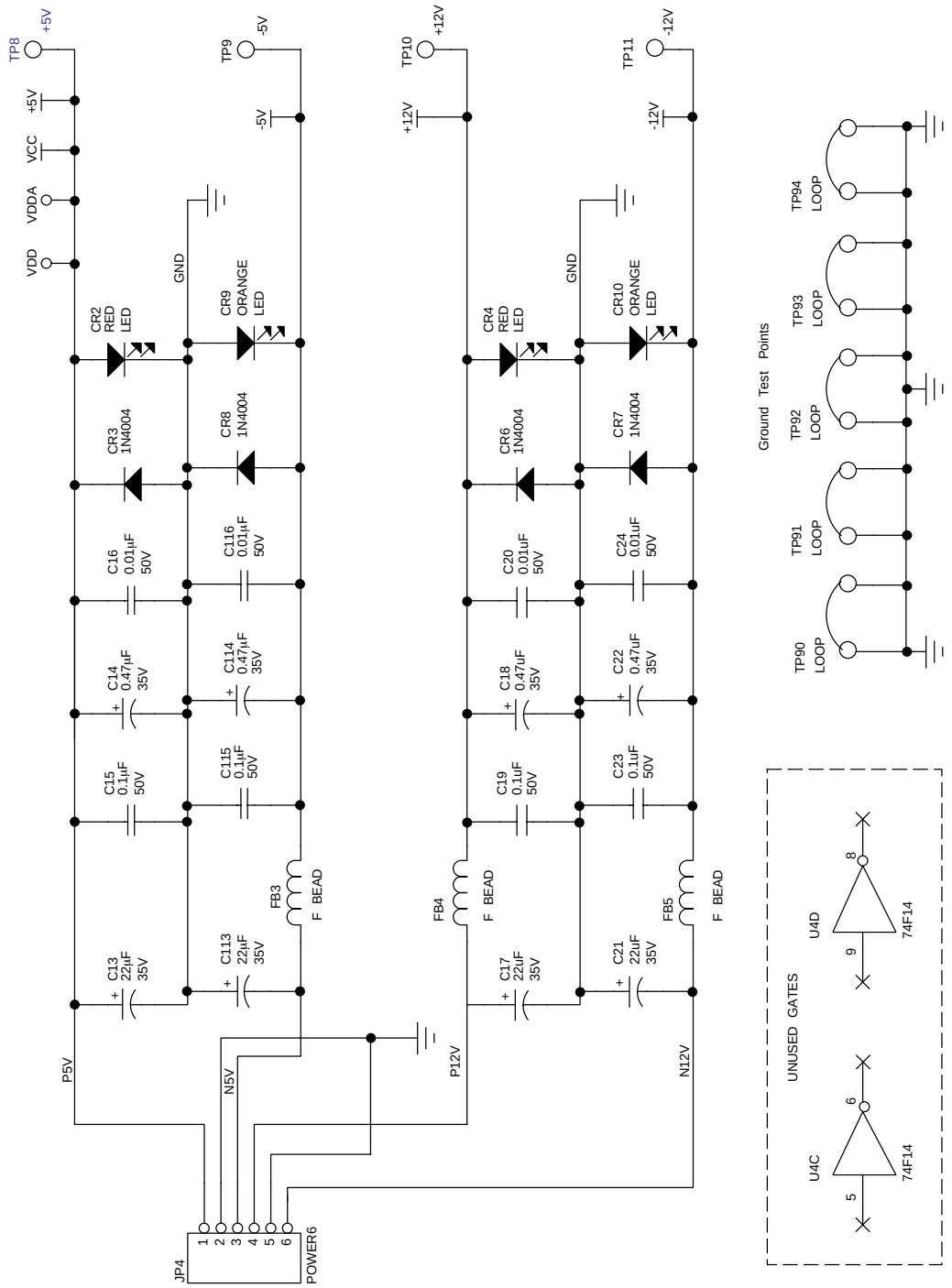


Figure 9. Power.SCH

Schematics (continued)

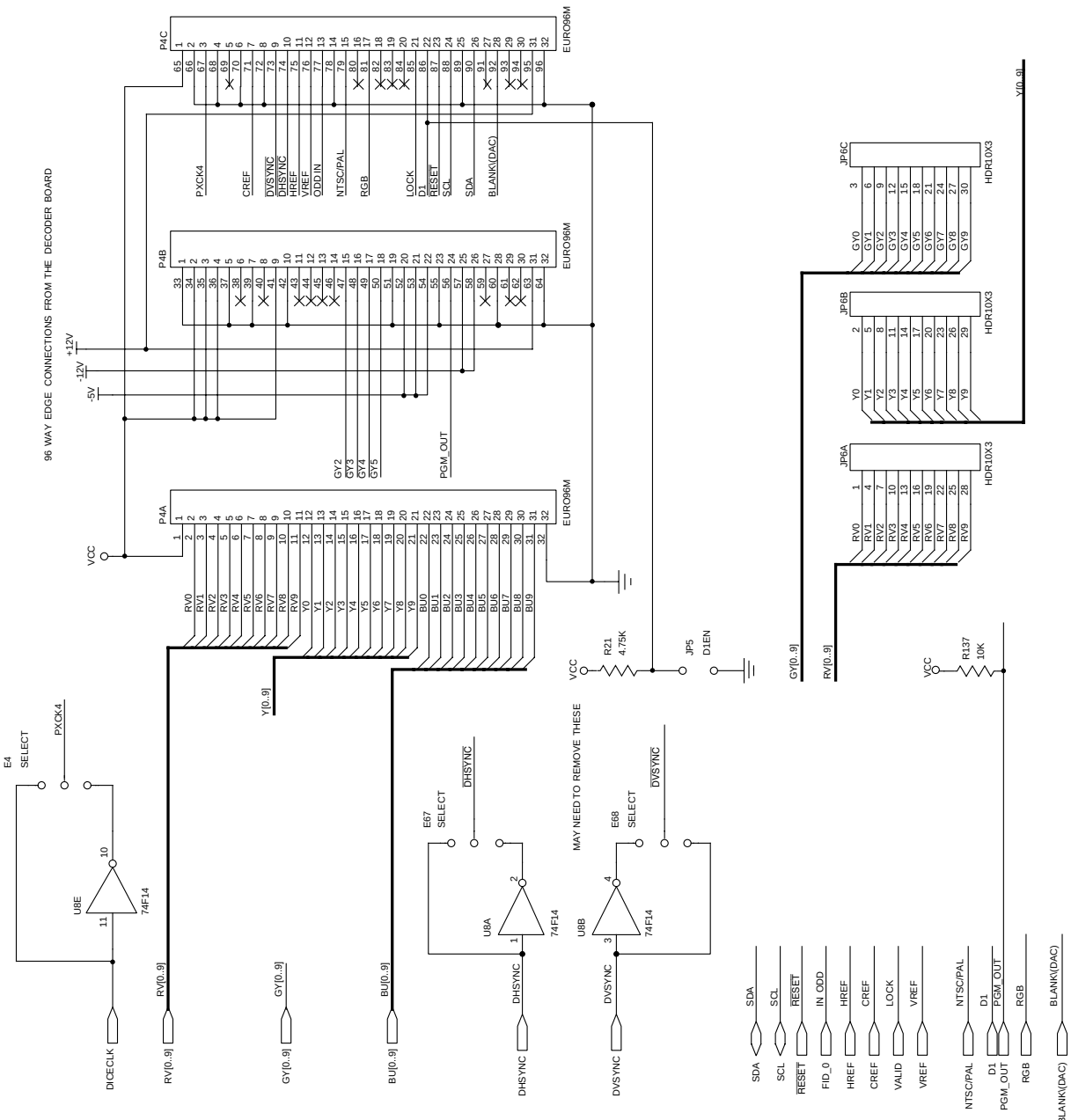


Figure 10. OP_CONN.SCH

INPUT 96 Way Connector (Female) Description and Notes

Row A		Row B		Row C	
32	+5v	32	GND	32	+5v
31	D1 or R/V [bit 0]	31	+5V	31	GND
30	D1 or R/V [bit 1]	30	+5V	30	PXCK
29	D1 or R/V [bit 2]	29	+5V	29	GND
28	D1 or R/V [bit 3]	28	GND	28	PCK
27	D1 or R/V [bit 4]	27	Analog Composite/luma	27	GND
26	D1 or R/V [bit 5]	26	GND	26	CREF
25	D1 or R/V [bit 6]	25	Analog chroma	25	GND
24	D1 or R/V [bit 7]	24	XEN	24	$\overline{\text{VSYNC}}$
23	D1 or R/V [bit 8]	23	GND	23	$\overline{\text{HSYNC}}$
22	D1 or R/V [bit 9]	22	XDIR	22	HREF
21	Comp, G/Y, or Luma [bit 0]	21	$\overline{\text{XHSYNC}}$	21	VREF
20	Comp, G/Y, or Luma [bit 1]	20	$\overline{\text{XVSYNC}}$	20	ODD IN
19	Comp, G/Y, or Luma [bit 2]	19	XPXCK	19	GND
18	Comp, G/Y, or Luma [bit 3]	18	XRS [bit 3]	18	NTSC/PAL
17	Comp, G/Y, or Luma [bit 4]	17	XRS [bit 2]	17	CLAMP pulse
16	Comp, G/Y, or Luma [bit 5]	16	XRS [bit 1]	16	RGB
15	Comp, G/Y, or Luma [bit 6]	15	XRS [bit 0]	15	
14	Comp, G/Y, or Luma [bit 7]	14	GND	14	
13	Comp, G/Y, or Luma [bit 8]	13	-5V	13	
12	Comp, G/Y, or Luma [bit 9]	12	-5V	12	LOCK
11	Chroma or B/U [bit 0]	11	-5V	11	D1
10	Chroma or B/U [bit 1]	10	GND	10	$\overline{\text{RESET}}$
9	Chroma or B/U [bit 2]	9	PGM_IN	9	SCL
8	Chroma or B/U [bit 3]	8	-12V	8	GND
7	Chroma or B/U [bit 4]	7	-12V	7	SDA
6	Chroma or B/U [bit 5]	6	IE (input enable)	6	OE (output enable)
5	Chroma or B/U [bit 6]	5	GND	5	$\overline{\text{BLANK}}$ (DAC)
4	Chroma or B/U [bit 7]	4		4	
3	Chroma or B/U [bit 8]	3		3	
2	Chroma or B/U [bit 9]	2	+12V	2	+12V
1	GND	1	GND	1	GND

Input Edge Connector Design Notes

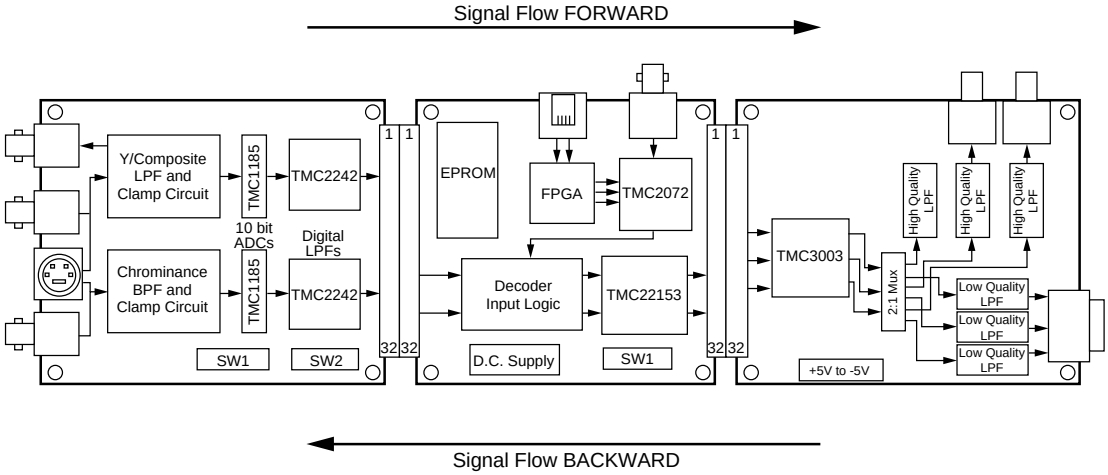


Figure 11.

- Boards with different revision letters may not be compatible; damage may occur if they are connected together.
- XPXCK is a two times pixel clock fed BACKWARD
- XHSYNC and XVSYNC are timing reference signals fed BACKWARD
- The MASTER/SLAVE signal states if a board is a MASTER or a SLAVE board. This signal is fed FORWARD.
  A MASTER board produces the PXCK, HSYNC, and VSYNC signals, and a SLAVE board expects to receive XPXCK, XHSYNC, XVSYNC, etc .
- XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
- PGM_IN is a negative going pulse, logically ANDed with the onboard program start pulse, for initiating the programming sequence for components on that board. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. Minimum width of PGM_IN is 1uS.
- The RESET pin on the input edge connector should be connected directly to the RESET pin on the output connector.
  A link should be used to connect any pulse to the RESET line.
- The MASTER/SLAVE, XDIR, PGM_IN and RESET pins on the input edge connector should be connected to +5V through a 10k pull up resistor.
- The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

OUTPUT 96 Way Connector (male) Description and Notes

Row A		Row B		Row C	
1	+5v	1	GND	1	+5v
2	D1 or R/V [bit 0]	2	+5V	2	GND
3	D1 or R/V [bit 1]	3	+5V	3	PXCK
4	D1 or R/V [bit 2]	4	+5V	4	GND
5	D1 or R/V [bit 3]	5	GND	5	PCK
6	D1 or R/V [bit 4]	6	Analog Composite/luma	6	GND
7	D1 or R/V [bit 5]	7	GND	7	CREF
8	D1 or R/V [bit 6]	8	Analog chroma	8	GND
9	D1 or R/V [bit 7]	9	XEN	9	$\overline{\text{VSYNC}}$
10	D1 or R/V [bit 8]	10	GND	10	$\overline{\text{HSYNC}}$
11	D1 or R/V [bit 9]	11	XDIR	11	HREF
12	Comp, G/Y, or Luma [bit 0]	12	$\overline{\text{XHSYNC}}$	12	VREF
13	Comp, G/Y, or Luma [bit 1]	13	$\overline{\text{XVSYNC}}$	13	ODD IN
14	Comp, G/Y, or Luma [bit 2]	14	XPXCK	14	GND
15	Comp, G/Y, or Luma [bit 3]	15	XRS [bit 3]	15	NTSC/PAL
16	Comp, G/Y, or Luma [bit 4]	16	XRS [bit 2]	16	CLAMP pulse
17	Comp, G/Y, or Luma [bit 5]	17	XRS [bit 1]	17	RGB
18	Comp, G/Y, or Luma [bit 6]	18	XRS [bit 0]	18	
19	Comp, G/Y, or Luma [bit 7]	19	GND	19	
20	Comp, G/Y, or Luma [bit 8]	20	-5V	20	
21	Comp, G/Y, or Luma [bit 9]	21	-5V	21	LOCK
22	Chroma or B/U [bit 0]	22	-5V	22	D1
23	Chroma or B/U [bit 1]	23	GND	23	$\overline{\text{RESET}}$
24	Chroma or B/U [bit 2]	24	PGM_OUT	24	SCL
25	Chroma or B/U [bit 3]	25	-12V	25	GND
26	Chroma or B/U [bit 4]	26	-12V	26	SDA
27	Chroma or B/U [bit 5]	27	IE (input enable)	27	OE (output enable)
28	Chroma or B/U [bit 6]	28	GND	28	$\overline{\text{BLANK}}$ (DAC)
29	Chroma or B/U [bit 7]	29		29	
30	Chroma or B/U [bit 8]	30		30	
31	Chroma or B/U [bit 9]	31	+12V	31	+12V
32	GND	32	GND	32	GND

Preliminary Information

Output Edge Connector Design Notes

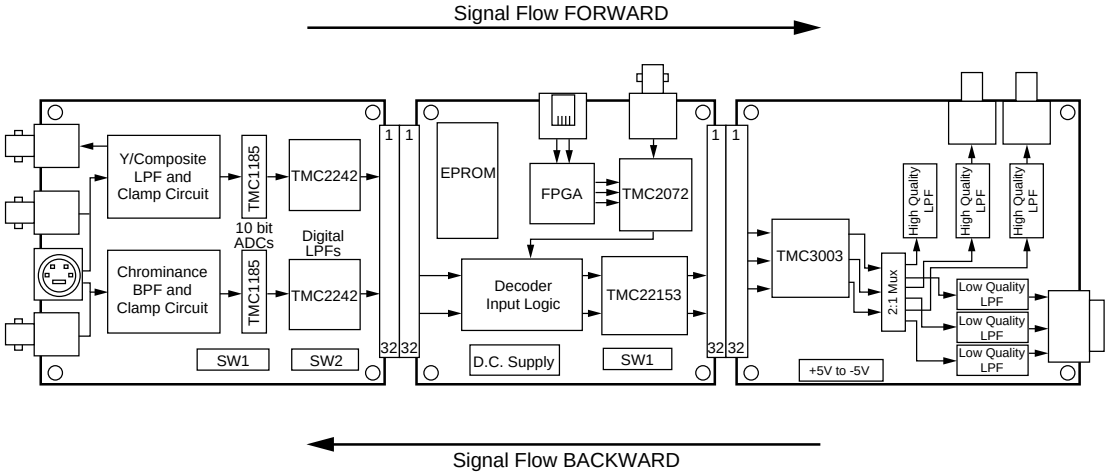


Figure 12.

- Boards with different revision letters may not be compatible; damage may occur if they are connected together.
- XPXCK is a two times pixel clock fed BACKWARD
- XHSYNC and XVSYNC are timing reference signals fed BACKWARD
- The MASTER/SLAVE signal states if a board is a MASTER or a SLAVE board. This signal is fed FORWARD.
  A MASTER board produces the PXCK, HSYNC, and VSYNC signals, and a SLAVE board expects to receive XPXCK, XHSYNC, XVSYNC, etc .
- XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
- PGM_OUT negative going signal pulse for initiating programming of down stream boards, generated once the devices on the board have been programmed. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. The Minimum width of PGM_OUT is 1μS.
- The RESET pin on the output edge connector should be connected directly to the RESET pin on the input connector.
  A link should be used to connect any pulse to the RESET line.
- The MASTER/SLAVE, XDIR, PGM_OUT and RESET pins on the output edge connector should be connected to +5V through a 10k pull up resistor.
- The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

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Table 4. TMC2068P7C Parts List

Item	Qty.	Part Name	Reference Designator	Description
1	1	Linear Technology LT1004CH-1.235	CR1	1.235V
2	1	Hewlett Packard: hlmp-1600	CR2,	RED
3	1	Hewlett Packard: hlmp-1601	CR4	RED
4	4	MiniReel: 76-4004	CR3,CR6,CR7, CR8	1N4004
5	1	Hewlett Packard: hlmp-1620	CR9	ORANGE
6	1	Hewlett Packard: hlmp-1621	CR10	ORANGE
7	46	MiniReel: 605-611	C1,C2,C6,C7,C8,C9,C10 C15,C19,C23,C25,C26 C27,C28,C29,C30,C31 C32,C33,C34,C35,C36 C37,C38,C39,C40,C41 C42,C43,C44,C45,C46 C47,C48,C51,C52,C53 C54,C115,C117,C118 C119,C120,C121,C122 C123	0.1uF
8	4	MiniReel: 643-822	C3,C4,C59,C60	22 uF/10v
9	1	MiniReel: 605-168	C5	6.8pF
10	1	MiniReel: 605-315	C11	150pF
11	1	MiniReel: 605-339	C12	390pF
12	4	MiniReel: 645-823	C13,C17,C21,C113	22uF/ 25v
13	4	MiniReel: 641-647	C14,C18,C22.C114	0.47uF/ 25v
14	4	MiniReel: 605-510	C16,C20,C24,C116	0.01uF
15	15	SECMA: 090320102	E1,E2,E3,E4,E20,E21,E23E24,E 25,E26,E30,E31,E32E67,E68	SELECT
16	5	Fair-Rite: 2743019447	FB1,FB2,FB3,FB4,FB5	F BEAD
17	19		H1,H2,H3,H4,H5,H6,H10 H11,H13,H14,H16,H18 H19,H21,H23,H25,H56 H60,H86	PTH
18	2	AMP: 103747-2	JP1,JP42	Jumper
19	1	AMP: 103747-2	JP3	YON
20	1	BEAU: 870503 BEAU: 871803	JP4	POWER6, Terminal block and socket
21	1	AMP: 103747-2	JP5	D1EN
22	1	AMP: 103817-8	JP6	HDR10X3
23	1	Amphenol: 31-5431	J1	BNC
24	1	MiniReel: 667-210	L1	10 uH 1210
25	1	Molex: 15-83-0064	P1	R-Bus
26	1	AMP: 4-103186-0	P2	HDR40X2 (SIMM72)
27	1	AMP: 650461-4	P3	EURO96F
28	1	AMP: 650473-5	P4	EURO96M
29	1	DALE: CSC10A-01-472	RN1	4.7K
30	1	ROHM: R25XT-68J1R0	R1	1 OHM 1/4W Carbon

Item	Qty.	Part Name	Reference Designator	Description
31	6	MiniReel: 615-510	R2,R3,R133,R134,R136 R137	10K
32	14	MiniReel: 615-447	R4,R5,R6,R7,R8,R9,R10 R18,R19,R20,R21,R53 R54,R78	4.75K
33	3	MiniReel: 615-275	R11,R12,R16	75
34	1	MiniReel: 615-822	R13	220
35	1	MiniReel: 615-844	R14	3.3K
36	3	MiniReel: 615-808	R130,R131,R132	33
37	1	ALCOSWITCH: ADP-8	S1	SW DIP-8
38	1	ITT Canon:KSC221JB	S2, S4	RESET, CON
39	1	ALCOSWITCH: ADP-4	S3	SW DIP-4
40	19	Mouser: ME151-203-100	TP1,TP2,TP3,TP4,TP5 TP6,TP7,TP12,TP13,TP14TP15, TP16,TP62,TP63 TP64,TP65,TP66,TP67 TP68	TP
41	1	Mouser: ME151-203-100	TP8	+5V
42		Mouser: ME151-203-100	TP9	-5V
43	1	Mouser: ME151-203-100	TP10	+12V
44	1	Mouser: ME151-203-100	TP11	-12V
45	5		TP90,TP91,TP92,TP93 TP94	LOOP
46	1	Fairchild: TMC22153KHC	U1	TMC22153KHC
47	1	Fairchild: TMC22071AKHC	U2	TMC22071AKHC (2072KHC)_2
48	1	ALTERA: EPF8820A-144-4	U3	FPGA, EPF8820A-144-4
49	2	Motorola: MC74F14D	U4,U8	74F14
50	1	Phillips: 74F841D	U6	74F841
51	2	Phillips: 74F821D	U9,U10	SN74ACT821
52	1	AMP: 544223-3	U37	EPROM Socket, 32 Pin
53	1	Motorola: MC74F157AD	U43	74F157A
54	1	Motorola: MC74F240DW	U77	74F240
55	1	ABROCON: ACH-20.000MHz-C	Y1	20MHz

Related Products

- TMC2067P7C Decoder demonstration board
- TMC2069P7C ADC demonstration board
- TMC2070P7C R-bus interface board
- RayDemo software

Notes:

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2068P7C	25°C	27 MHz	Commercial	4" by 5" Printed Circuit Board	TMC2068P7C

The TMC2070P7C parallel port to R-bus board, interface cable, RayDemo software, and all relevant documentation are included in the TMC2068P7C purchase price.

The TMC2067P7C, TMC2068P7C, TMC2069P7C, TMC2070P7C, cable, software and documentation are available in the TMC2068 Kit.

A schematic database is available in OrCAD™ format, along with EPROM maps. More information on the FPGA design is also available. Contact the factory.

The TMC2068P7C Demonstration Board, design documentation, and software are provided as a design example for the customers of Fairchild. Fairchild makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

FCC Compliance

This board is intended for the evaluation of Fairchild products only. This device has not been approved by the Federal Communications Commission (FCC). This device is not and may not be offered for sale or lease or sold or leased until the approval of the FCC has been obtained.

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