

The SL2524 is a pin compatible replacement for the SL2521 and SL2522 series of log amplifiers, and exhibits a superior stability performance. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth. The two stages can be operated independently.

When six stages (three SL2524s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of  $\pm 1.0\text{dB}$ . The balanced limited output also offers accurate phase information with input amplitude.

**FEATURES**

- 1.3GHz Bandwidth (-3dB)
- Balanced IF limiting
- 3ns Rise Times/5ns Fall Times (six stages)
- 20ns Pulse Handling (six stages)
- Temperature Stabilised
- Surface Mountable

**APPLICATIONS**

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage ( $V_{CC}$ above $V_{EE}$ )	+7.0V
Storage temperature	-65°C to +150°C
Operating temperature range	
SL2524/B/LC	-40°C to +85°C
SL2524/C/HP	-30°C to +85°C
Junction temperature - LC20	+175°C
- HP20	+150°C
Applied DC voltage to RF input	$\pm 0.4\text{V}$ (between RF I/P pins)
Applied RF power to RF input	+15dBm
Value of $R_{SET}$ resistors	NOT less than 180Ω
Thermal resistance:-	
Die to case -LC 20	28°C/W
- HP20	20°C/W
Die to ambient - LC20	73°C/W
- HP20	82°C/W

**ORDERING INFORMATION**

- SL2524/B/LC (Ceramic leadless chip carrier package)
- SL2524/C/HP (Plastic J lead chip carrier package)
- SL2524/NA/1C (DC probe tested bare die)
- 5962 - 92315 (SMD)

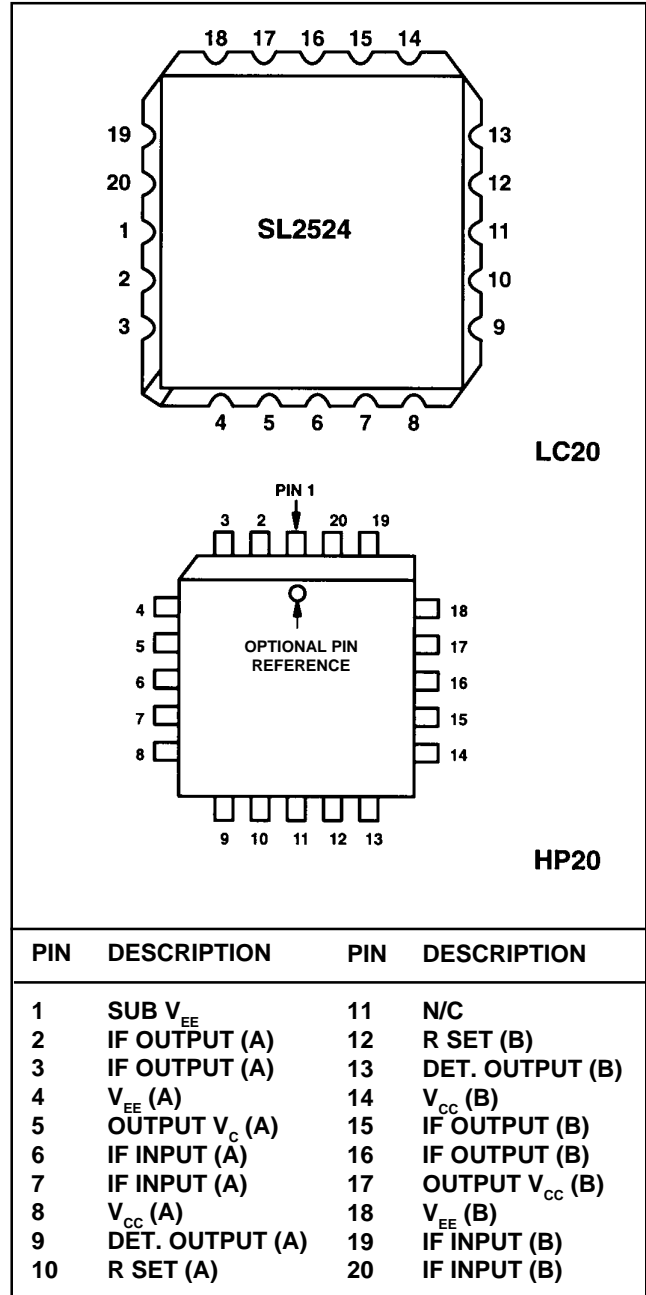


Fig.1 Pin connections top view

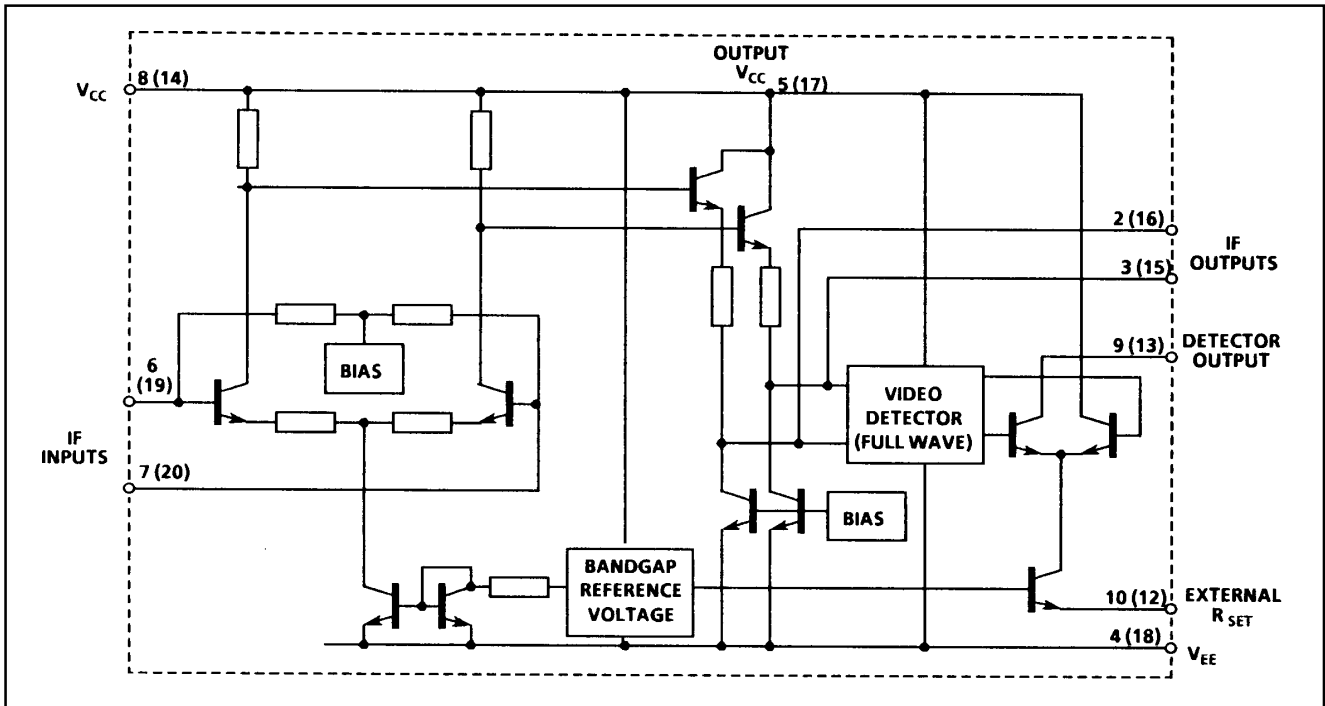


Fig.2 Circuit diagram of single stage A - (stage B pin Nos bracketed)

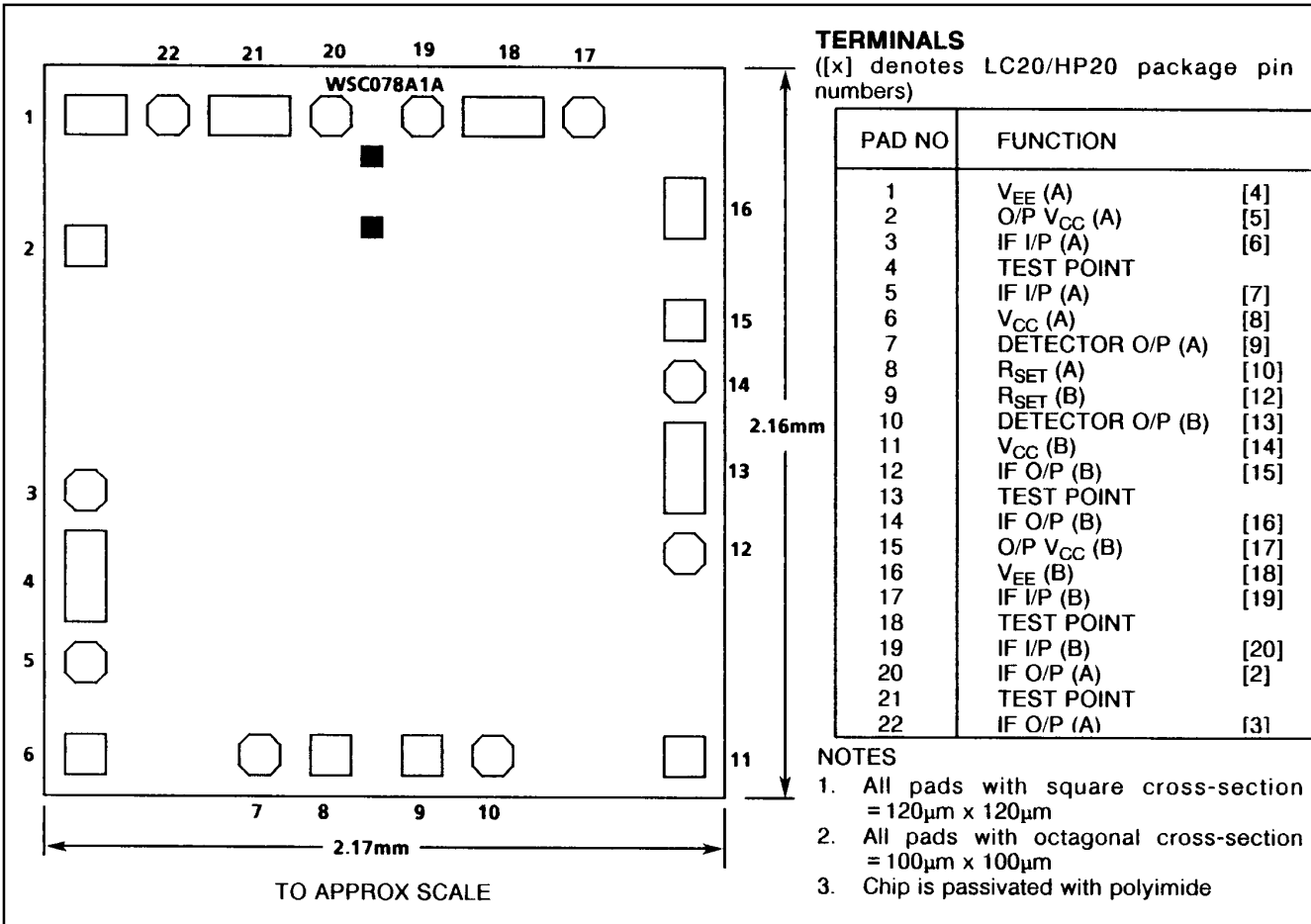


Fig.3 Pad map for SL2524 naked die

**ELECTRICAL CHARACTERISTICS - SL2524B****Guaranteed at the following test conditions unless otherwise stated**

Frequency = 200MHz,  $T_{amb} = +25^{\circ}\text{C}$ , Input power = -30dBm,  $V_{CC} = 6V \pm 0.1V$ , Source Impedance = 50 $\Omega$ .  
 Load impedance = 50 $\Omega$ , Test Circuit = Fig. 4,  $R_{SET} = 300\Omega$ . Tested as a dual stage.

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Supply current	70	87	100	mA	
Small signal gain (dual stage, single ended)	9.6	11.4	13.0	dB	$T_{amb} = +25^{\circ}\text{C}$ f = 25MHz See Notes 1, 3
	10.1	11.6	13.1	dB	$T_{amb} = -40^{\circ}\text{C}$ f = 200MHz See Notes 2, 3
	9.9	11.3	12.7	dB	$T_{amb} = +25^{\circ}\text{C}$ f = 200MHz See Note 3
	9.5	11.0	12.5	dB	$T_{amb} = +85^{\circ}\text{C}$ f = 200MHz See Notes 2, 3
	9.7	11.2	12.7	dB	$T_{amb} = -40^{\circ}\text{C}$ f = 500MHz See Notes 2, 3
	9.3	10.7	12.1	dB	$T_{amb} = +25^{\circ}\text{C}$ f = 500MHz See Note 3
	8.2	9.7	11.2	dB	$T_{amb} = +85^{\circ}\text{C}$ f = 500MHz See Notes 2, 3
	Detected output current (max)	3.20	3.45	3.70	mA
3.05		3.25	3.45	mA	$T_{amb} = -40^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 200MHz See Note 2
3.15		3.30	3.45	mA	$T_{amb} = +25^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 200MHz
3.10		3.30	3.50	mA	$T_{amb} = +85^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 200MHz See Note 2
2.80		3.10	3.30	mA	$T_{amb} = -40^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 500MHz See Note 2
2.90		3.15	3.45	mA	$T_{amb} = +25^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 500MHz
2.85		3.10	3.65	mA	$T_{amb} = +85^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 500MHz See Note 2
Detected output current (no signal)		0.85	0.95	1.15	mA
	0.80	0.93	1.10	mA	$T_{amb} = +25^{\circ}\text{C}$ , See Note 2
	0.80	0.90	1.10	mA	$T_{amb} = +85^{\circ}\text{C}$ , See Note 2
Upper cut off frequency (RF)	600	1100		MHz	-3dB w.r.t 200MHz, $T_{amb} = -40^{\circ}\text{C}$ See Note 2
	900	1100		MHz	-3dB w.r.t 200MHz, $T_{amb} = +25^{\circ}\text{C}$
	600	800		MHz	-3dB w.r.t 200MHz, $T_{amb} = +85^{\circ}\text{C}$ See Note 2
Lower cut off frequency (RF)		0.35	1	MHz	-3dB w.r.t 200MHz, $T_{amb} = +25^{\circ}\text{C}$
Detector cut off frequency		700		MHz	50% O/P current w.r.t. 200MHz
Limited IF O/P voltage	135	155	175	mV	I/P power = 0dBm, $T_{amb} = +25^{\circ}\text{C}$
Phase variation with input level (normalised to -30dBm)		0 $\pm$ 2.0	0 $\pm$ 3.0	Degree	Frequency = 70MHz, -55 to +3dBm See Note 2
		-4.0 $\pm$ 2.0	-4.0 $\pm$ 3.0	Degree	Frequency = 200MHz, -55 to +3dBm See Note 2
Limited O/P var with temp.		$\pm$ 12	$\pm$ 25	mV	See Note 1
Noise figure		14		dB	
Max I/P before overload		15		dBm	
Input impedance		1		k $\Omega$	1k $\Omega$ in parallel with 2pF
Output impedance		50		$\Omega$	

## NOTES

- Parameter guaranteed but not tested
- Tested at 25 $^{\circ}\text{C}$  only, but guaranteed at temperature
- Gain will typically increase by 6dB, when RF outputs use 1k $\Omega$  loads in place of 50 $\Omega$

**ELECTRICAL CHARACTERISTICS - SL2524C**

**Guaranteed at the following test conditions unless otherwise stated**

Frequency = 200MHz,  $T_{amb} = +25^{\circ}\text{C}$ , Input power = -30dBm,  $V_{CC} = 6\text{V} \pm 0.1\text{V}$ , Source Impedance = 50 $\Omega$ .

Load impedance = 50 $\Omega$ , Test Circuit = Fig. 4,  $R_{SET} = 300\Omega$ . Tested as a dual stage.

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Supply current	70	87	100	mA	
Small signal gain (dual stage, single ended)	9.6	11.4	13.0	dB	$T_{amb} = +25^{\circ}\text{C}$ f = 25MHz See Note 3
	9.6	11.6	13.6	dB	$T_{amb} = -30^{\circ}\text{C}$ f = 200MHz See Notes 2, 3
	9.4	11.3	13.2	dB	$T_{amb} = +25^{\circ}\text{C}$ f = 200MHz See Note 3
	9.0	11.0	13.0	dB	$T_{amb} = +85^{\circ}\text{C}$ f = 200MHz See Notes 2, 3
	9.2	11.2	13.2	dB	$T_{amb} = -30^{\circ}\text{C}$ f = 500MHz See Notes 1, 3
	8.8	10.7	12.6	dB	$T_{amb} = +25^{\circ}\text{C}$ f = 500MHz See Note 1
	7.7	9.7	11.7	dB	$T_{amb} = +85^{\circ}\text{C}$ f = 500MHz See Notes 1, 3
Detected output current (max)	3.20	3.45	3.70	mA	$T_{amb} = +25^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 25MHz
	2.95	3.25	3.55	mA	$T_{amb} = -30^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 200MHz
					See Note 2
	3.05	3.30	3.55	mA	$T_{amb} = +25^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 200MHz
	3.00	3.30	3.50	mA	$T_{amb} = +85^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 200MHz
					See Note 2
	2.70	3.10	3.30	mA	$T_{amb} = -30^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 500MHz
2.80	3.15	3.55	mA	$T_{amb} = +25^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 500MHz	
				See Note 1	
					$T_{amb} = +85^{\circ}\text{C}$ , $V_{IN} = 0\text{dBm}$ , f = 500MHz
					See Note 1
Detected output current (no signal)	0.75	0.95	1.25	mA	$T_{amb} = -30^{\circ}\text{C}$ , See Note 2
	0.70	0.93	1.20	mA	$T_{amb} = +25^{\circ}\text{C}$ , See Note 2
	0.70	0.90	1.20	mA	$T_{amb} = +85^{\circ}\text{C}$ , See Note 2
Upper cut off frequency (RF)		1000		MHz	-3dB w.r.t 200MHz, $T_{amb} = +25^{\circ}\text{C}$ See Note 1
Lower cut off frequency (RF)		0.35	2	MHz	-3dB w.r.t 200MHz, $T_{amb} = +25^{\circ}\text{C}$
Detector cut off frequency		600		MHz	50% O/P current w.r.t. 200MHz
Limited IF O/P voltage	105	135	175	mV	I/P power = 0dBm, $T_{amb} = +25^{\circ}\text{C}$
Phase variation with input level (normalised to -30dBm)		0 $\pm$ 2.0		Degree	Frequency = 70MHz, -55 to +3dBm
		-4.0 $\pm$ 2.0		Degree	Frequency = 200MHz, -55 to +3dBm
					See Note 1
Limited O/P var with temp.		$\pm$ 12	$\pm$ 25	mV	See Note 1
Noise figure		14		dB	
Max I/P before overload		15		dBm	
Input impedance		1		k $\Omega$	1k $\Omega$ in parallel with 2pF
Output impedance		50		$\Omega$	

## NOTES

1. Parameter guaranteed but not tested
2. Tested at 25 $^{\circ}\text{C}$  only, but guaranteed at temperature
3. Gain will typically increase by 6dB, when RF outputs use 1k $\Omega$  loads in place of 50 $\Omega$

**GENERAL DESCRIPTION**

The SL2524 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic amplifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See figs 5 and 6.)

A six stage strip also offers balanced IF limiting, linearity (log accuracy) of  $< \pm 1.0\text{dB}$ , temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set ( $R_{\text{SET}}$ ) pin which allows the major characteristics of the detector to be programmed. With six stage strip it is possible to vary the value of  $R_{\text{SET}}$  on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (no video filter). The video bandwidth of a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than  $5^\circ$  of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously, so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

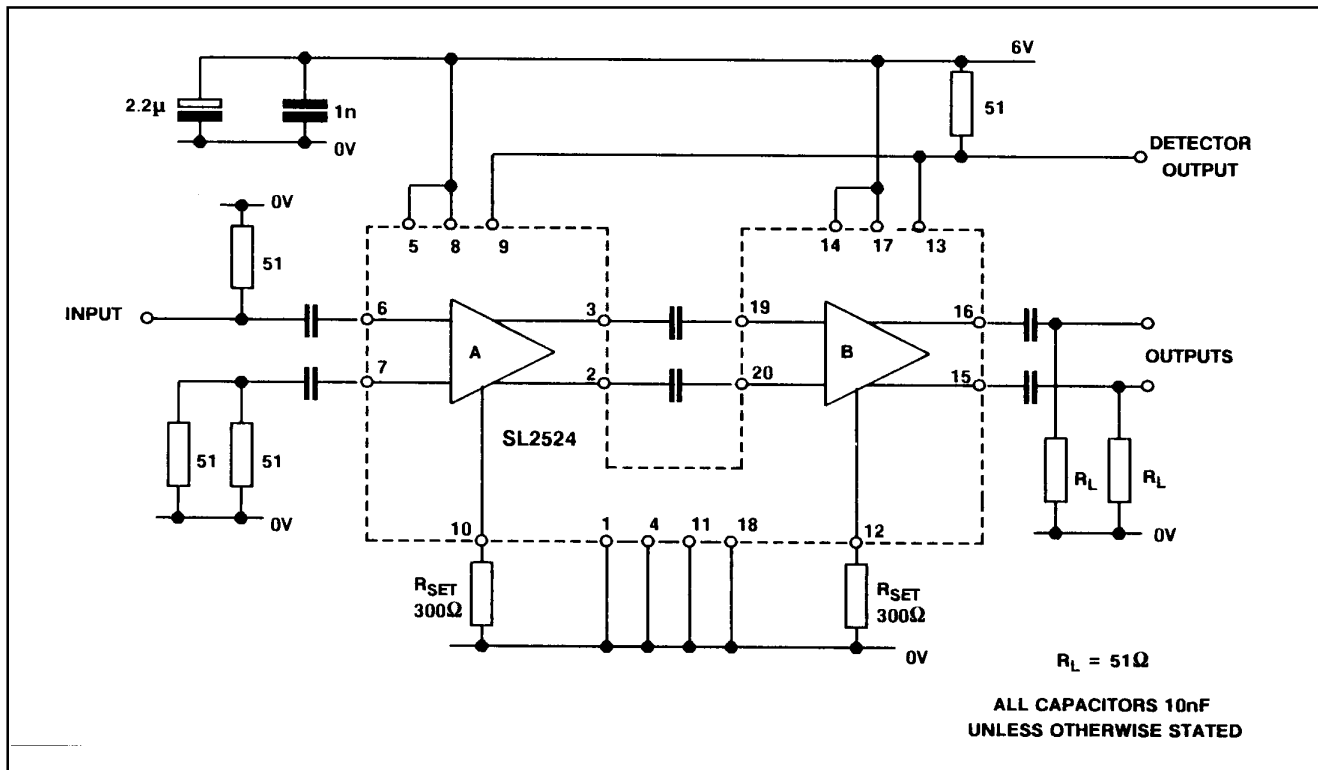


Fig.4 Test circuit

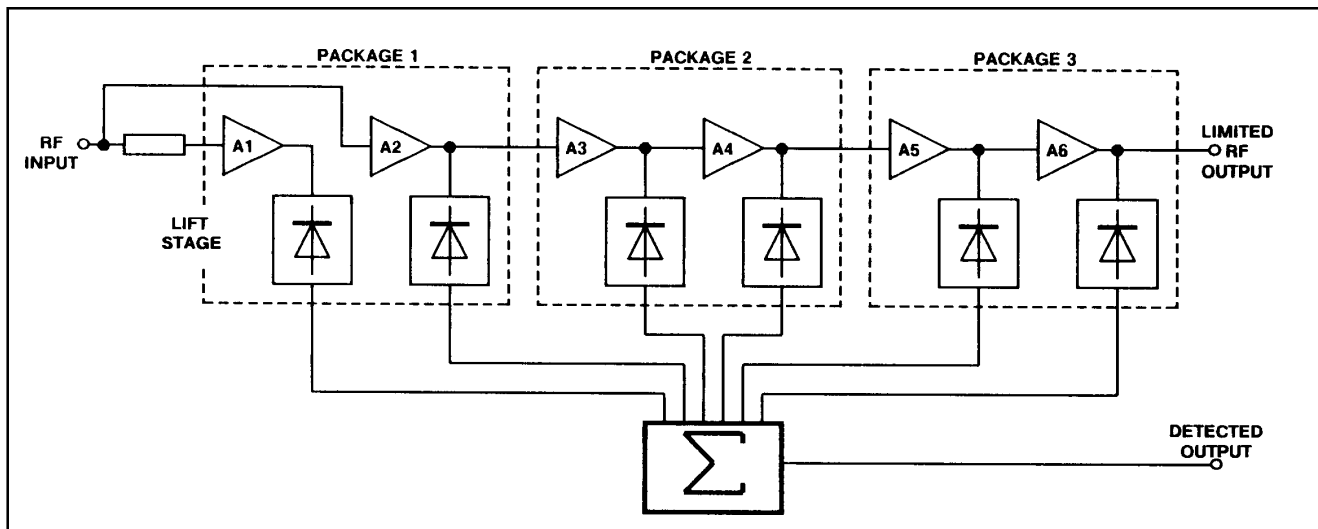


Fig.5 Schematic diagram showing configuration of SD Log strip

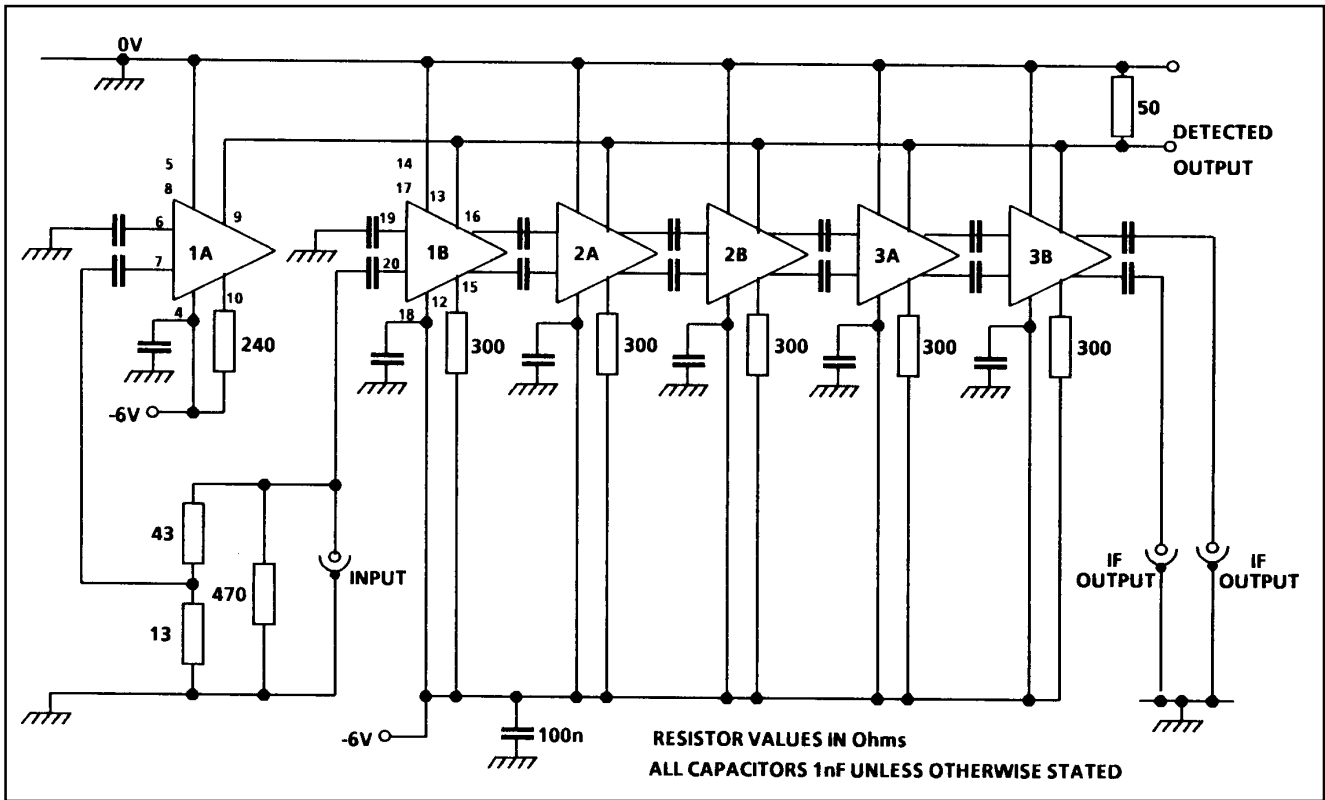


Fig.6 Circuit diagram for 6-log strip (results shown in figs. 11 to 24 were achieved with this circuit)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524)

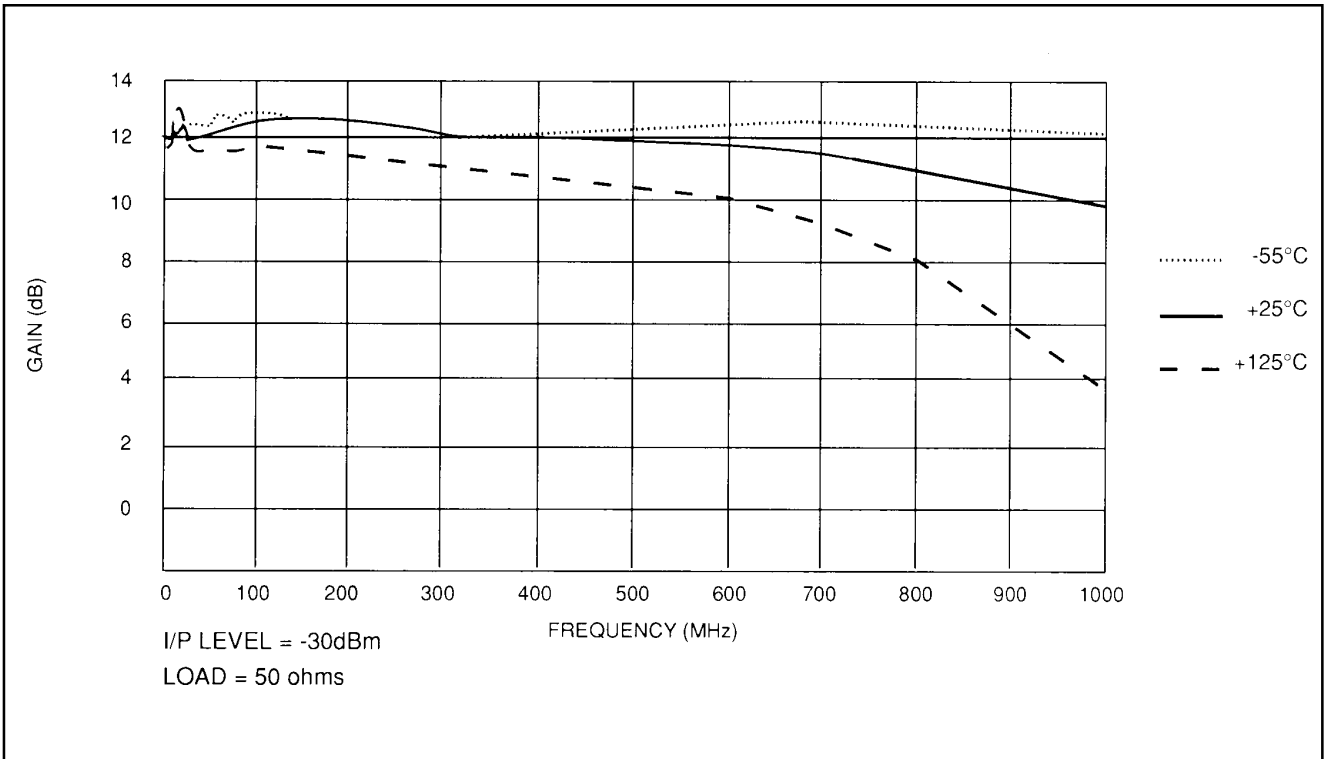


Fig.7 IF Gain vs frequency of 2 amplifiers (One SL2524)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524) cont.

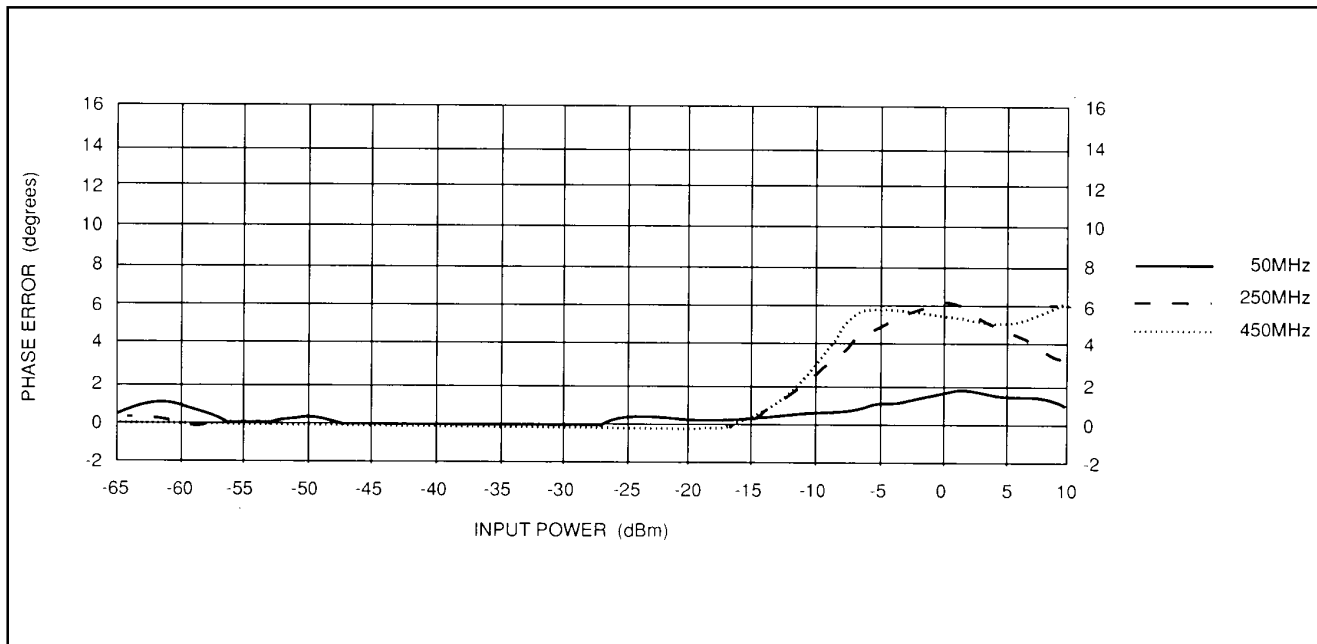


Fig.8 Normalised phase vs CW input level at 50, 250 and 450MHz for 50Ω O/P termination (25°C)

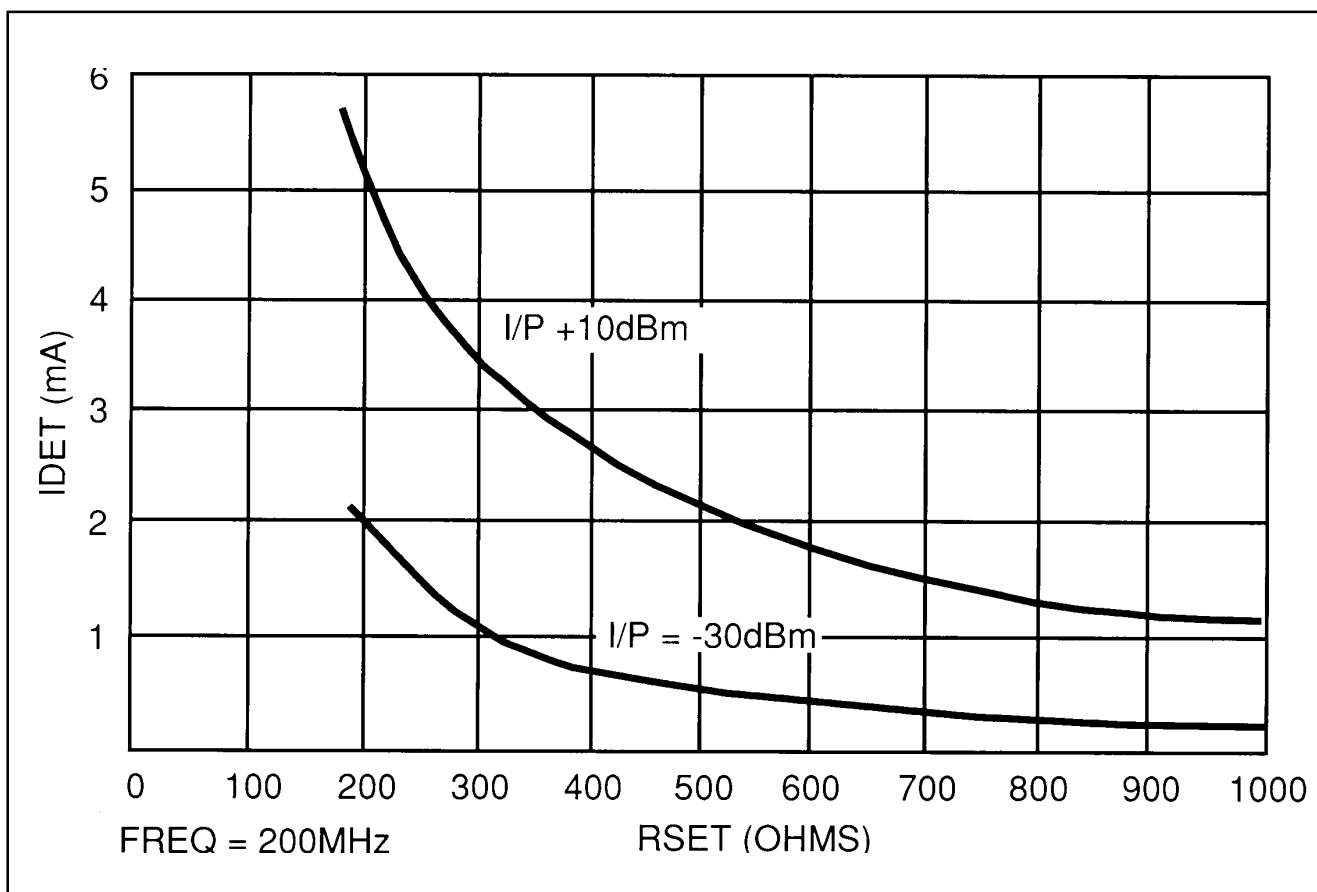


Fig.9 Detector current vs  $R_{SET}$  at 200MHz (25°C)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524) cont.

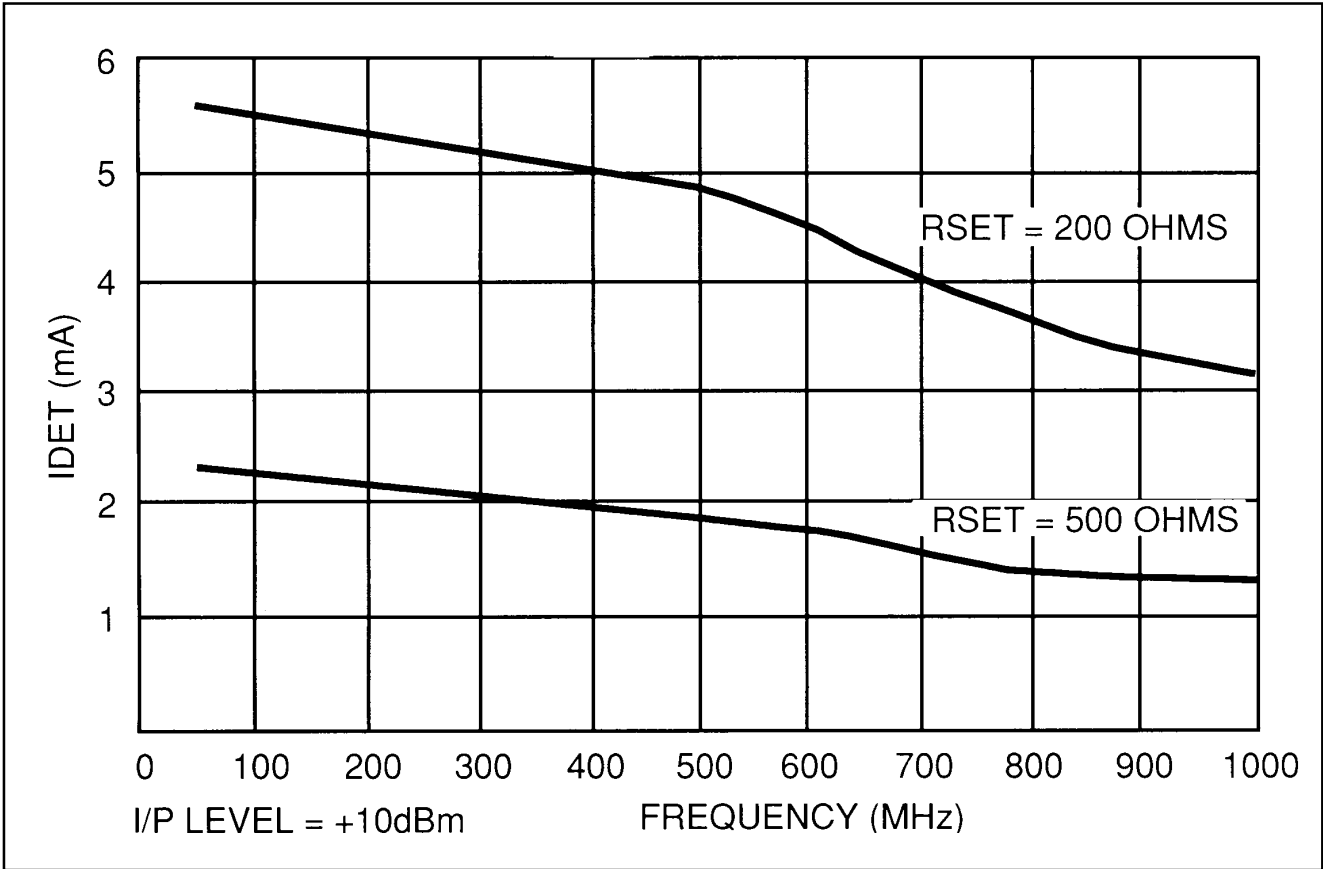


Fig.10 Detector current vs frequency at RSET = 200Ω and 500Ω (25°C)

Typical characteristics for a six stage strip, using detected output (Ref. figs 5 & 6)

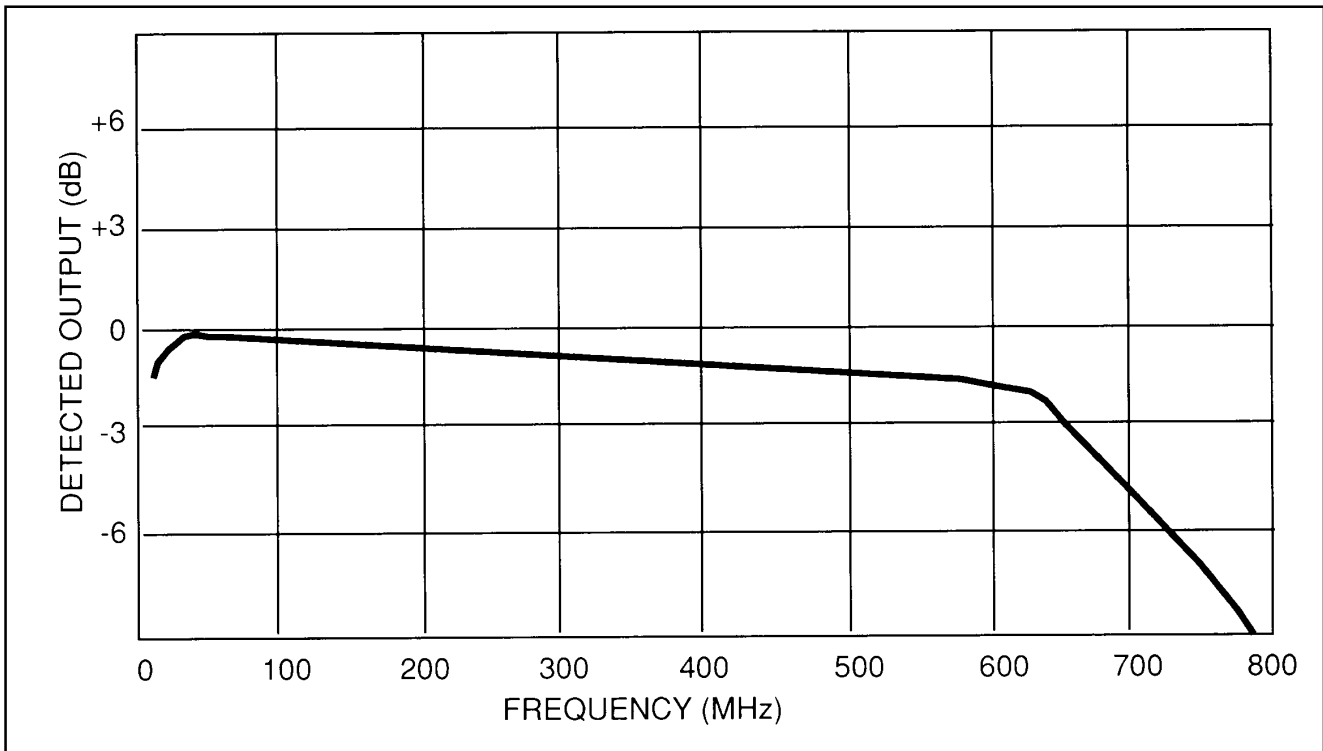


Fig.11 Detector bandwidth (25°C)



Typical characteristics for a six stage strip, using detected output (Ref. figs 5 & 6) cont.

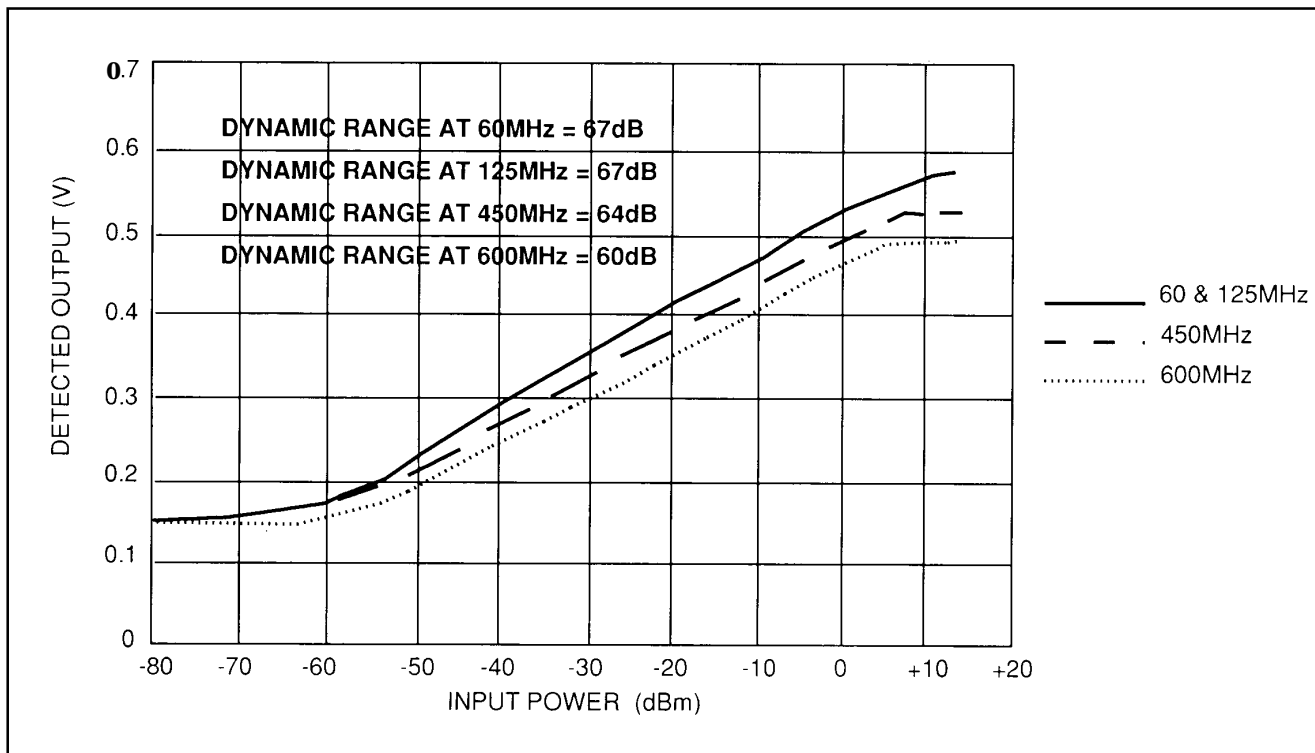


Fig.12 Detected O/P vs CW input at 60, 125, 450 and 600MHz at 25°C

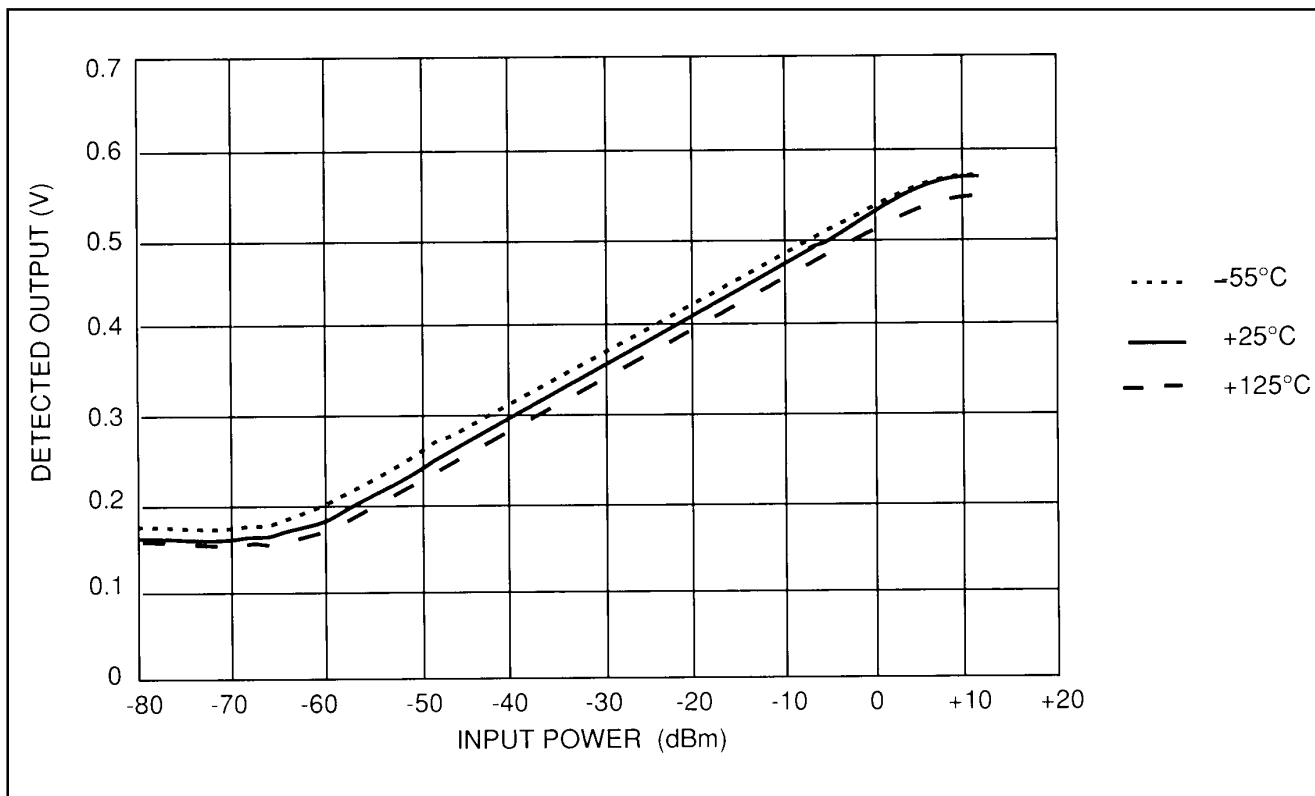


Fig.13 Detected O/P vs CW input level and temperature at 60 and 125MHz

Typical characteristics for a six stage strip, using detected output (Ref. figs 5 & 6) cont.

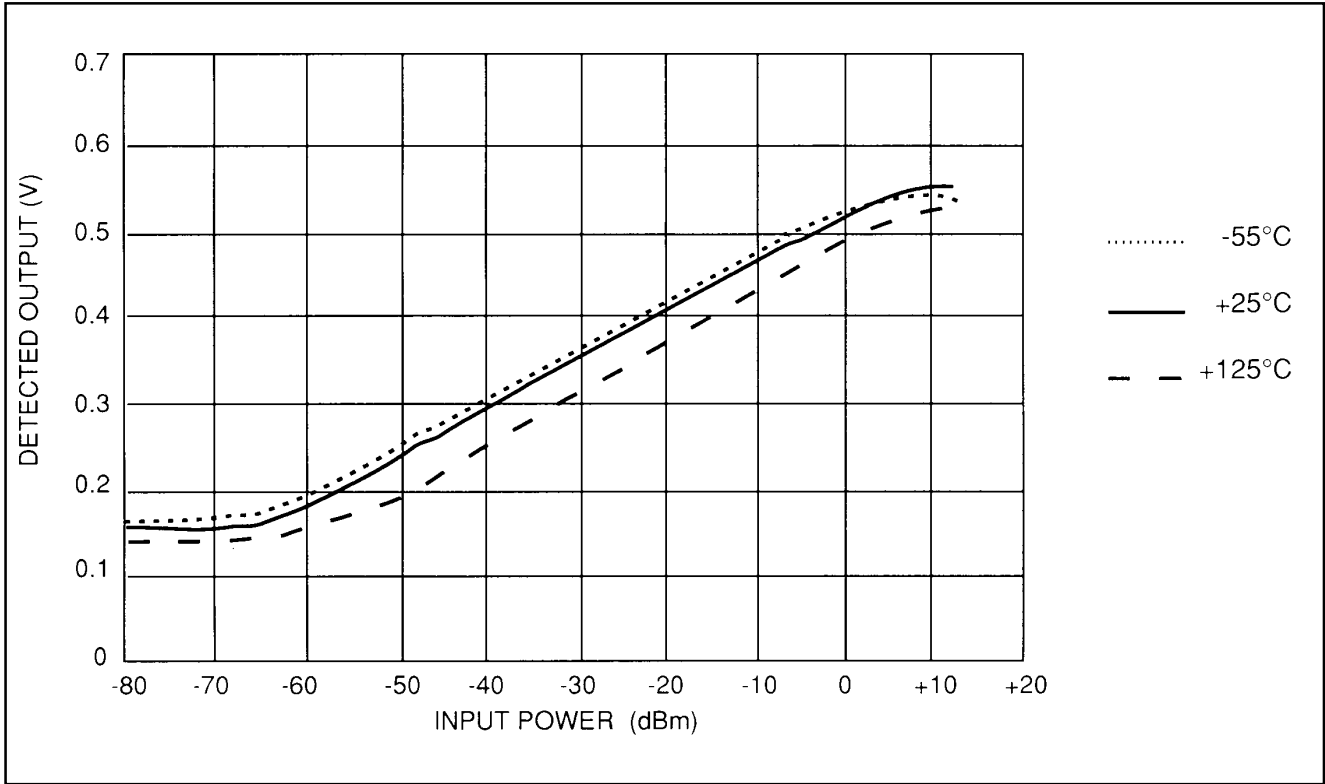


Fig.14 Detected O/P vs CW input level at 450MHz across temperature

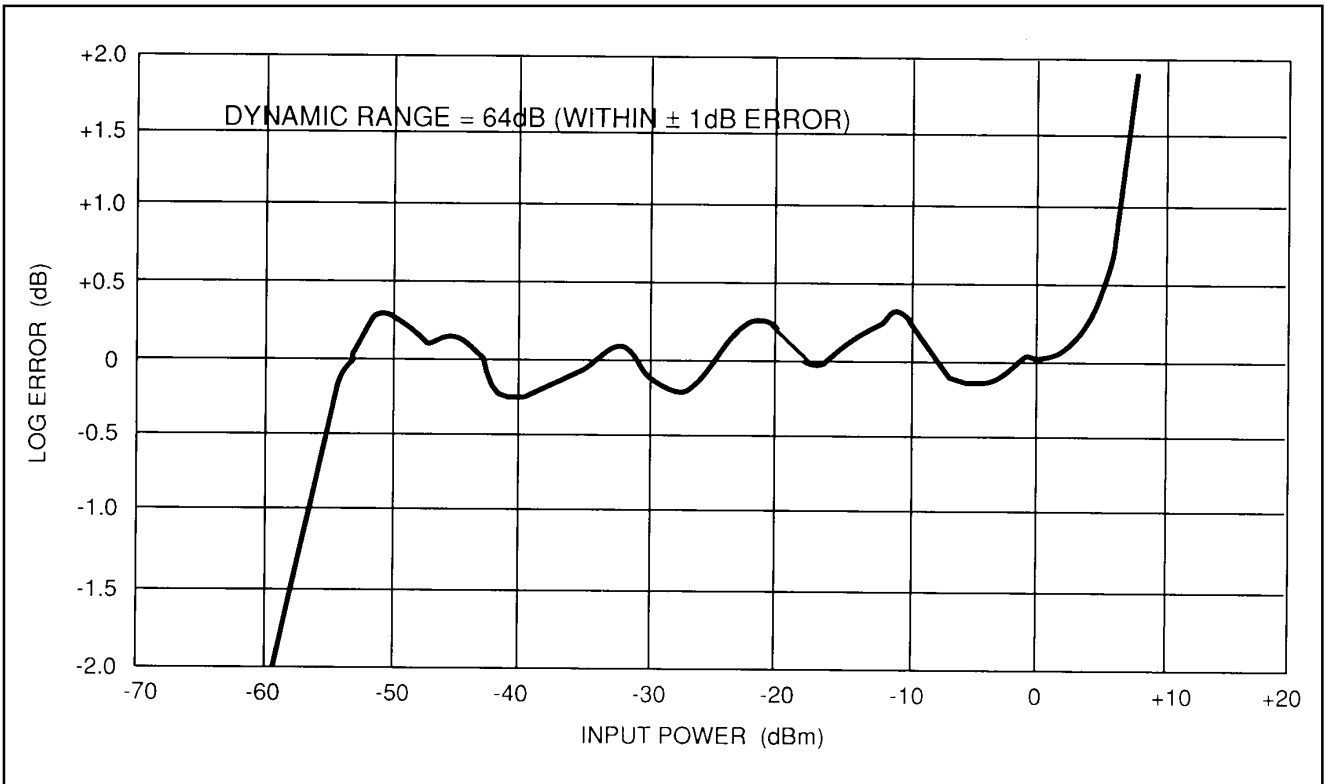


Fig.15 Typical log linearity of detected output measured at 450MHz (25°C)

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

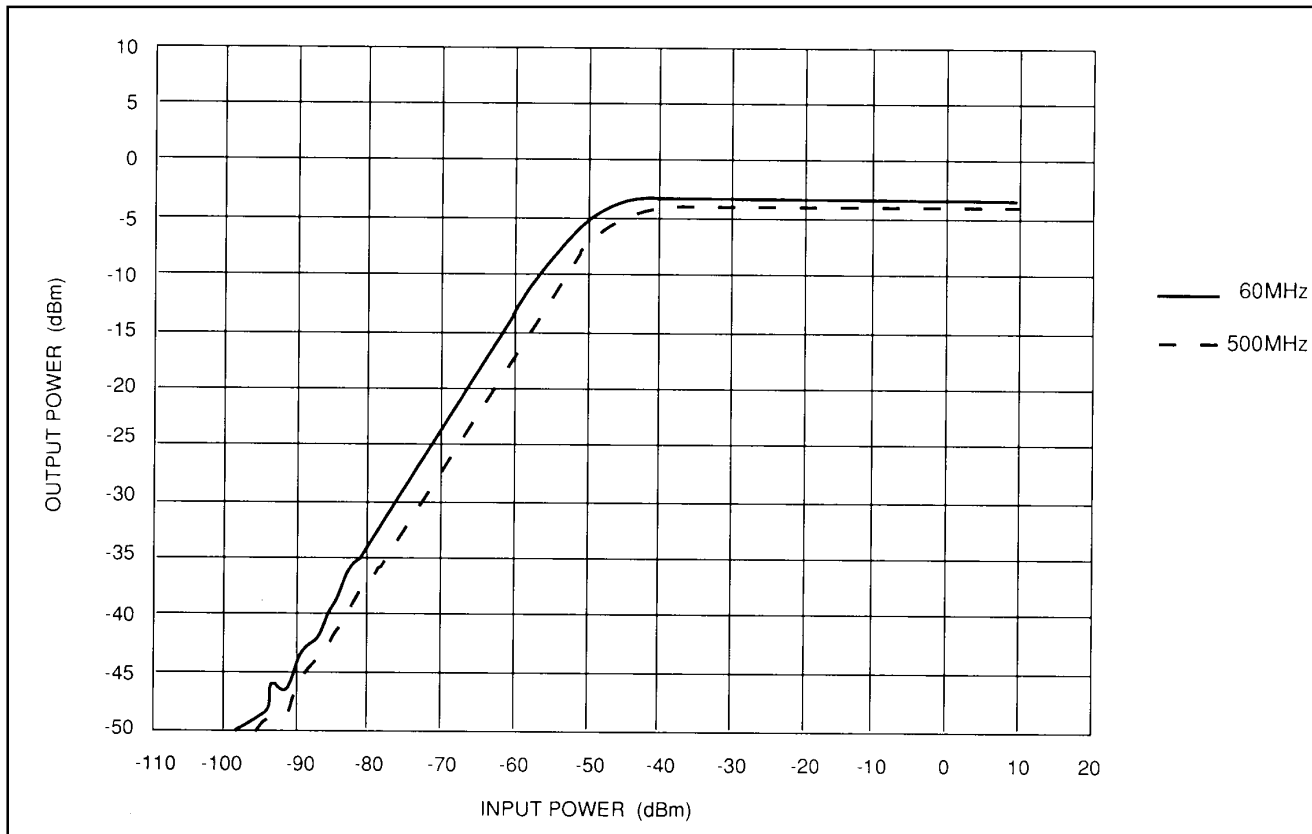


Fig.16 IF limiting characteristics at 60MHz and 500MHz (25°C)

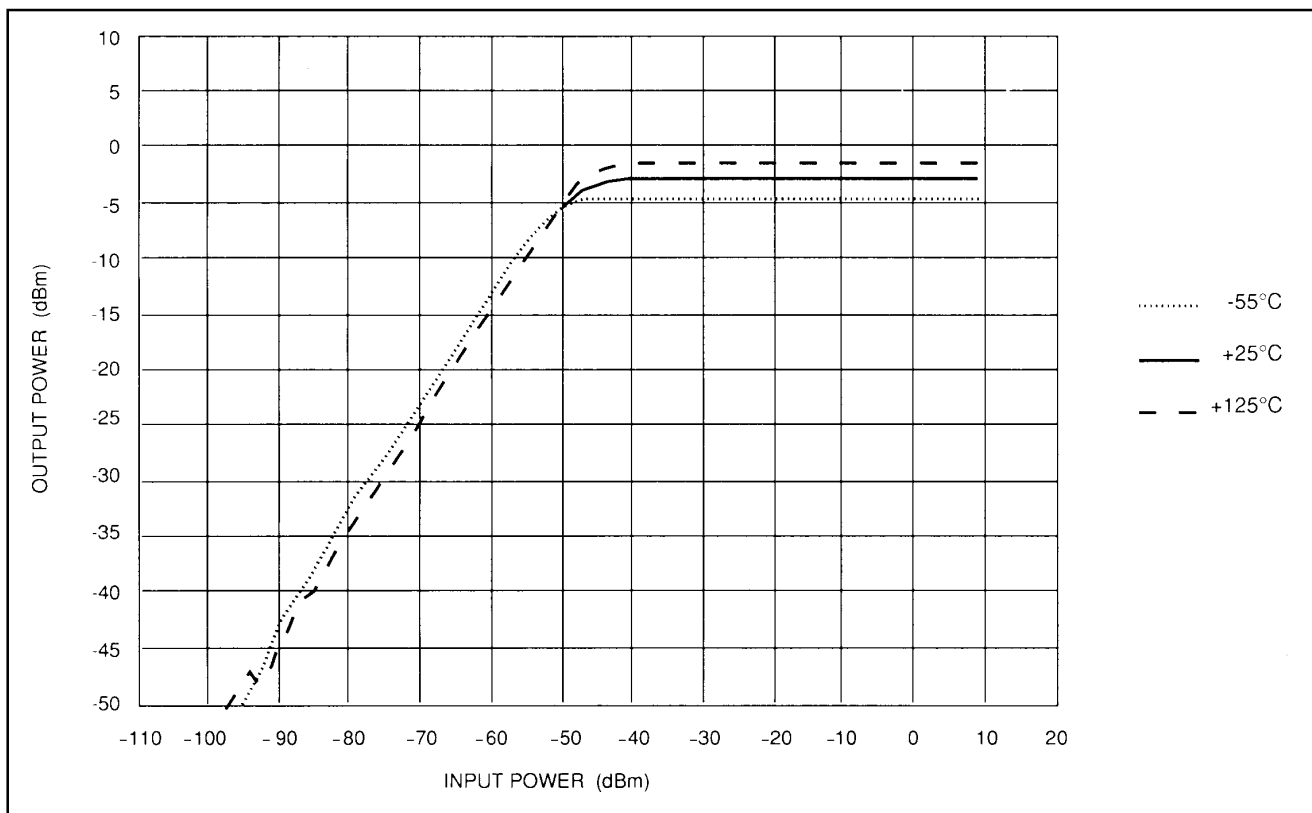


Fig.17 IF limiting characteristic at 60MHz across temperature

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

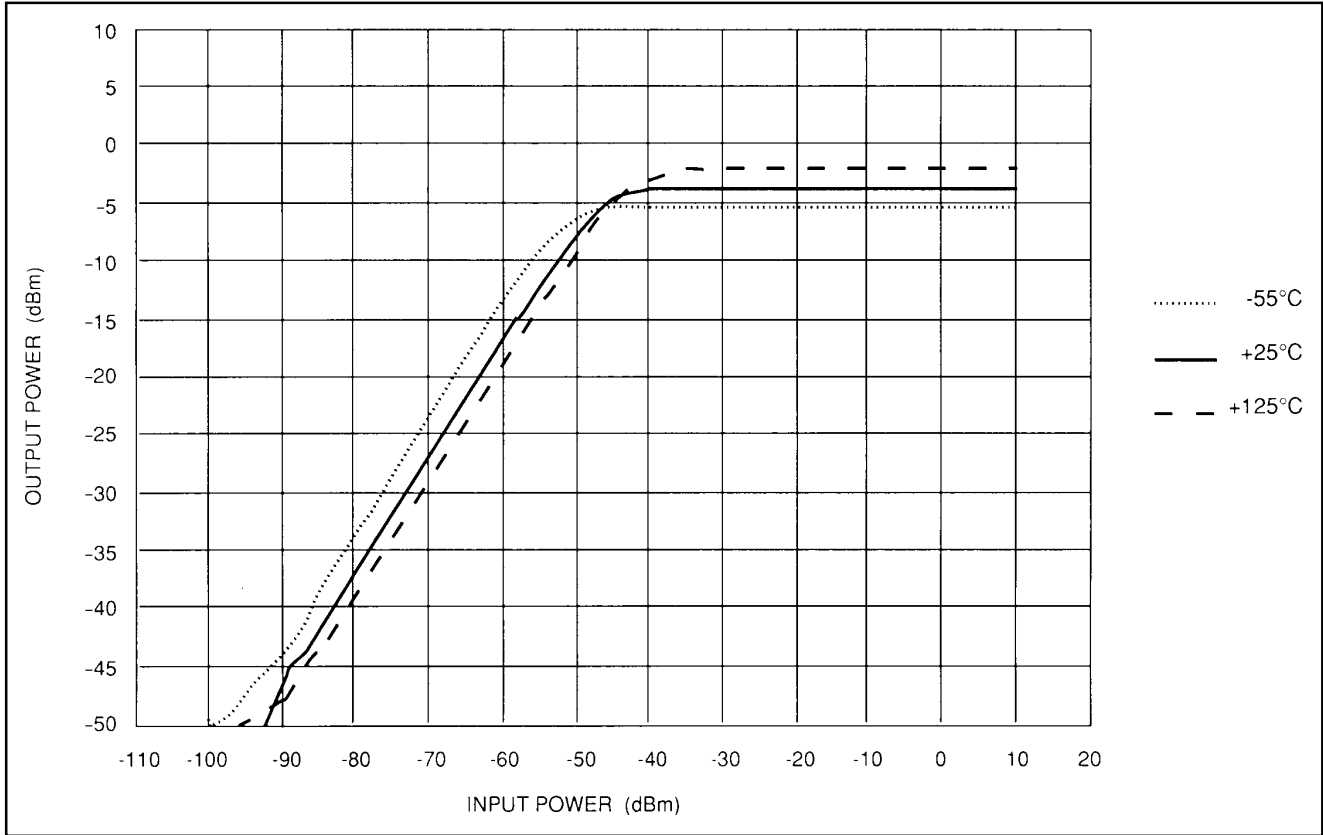


Fig.18 IF limiting characteristic at 500MHz across temperature

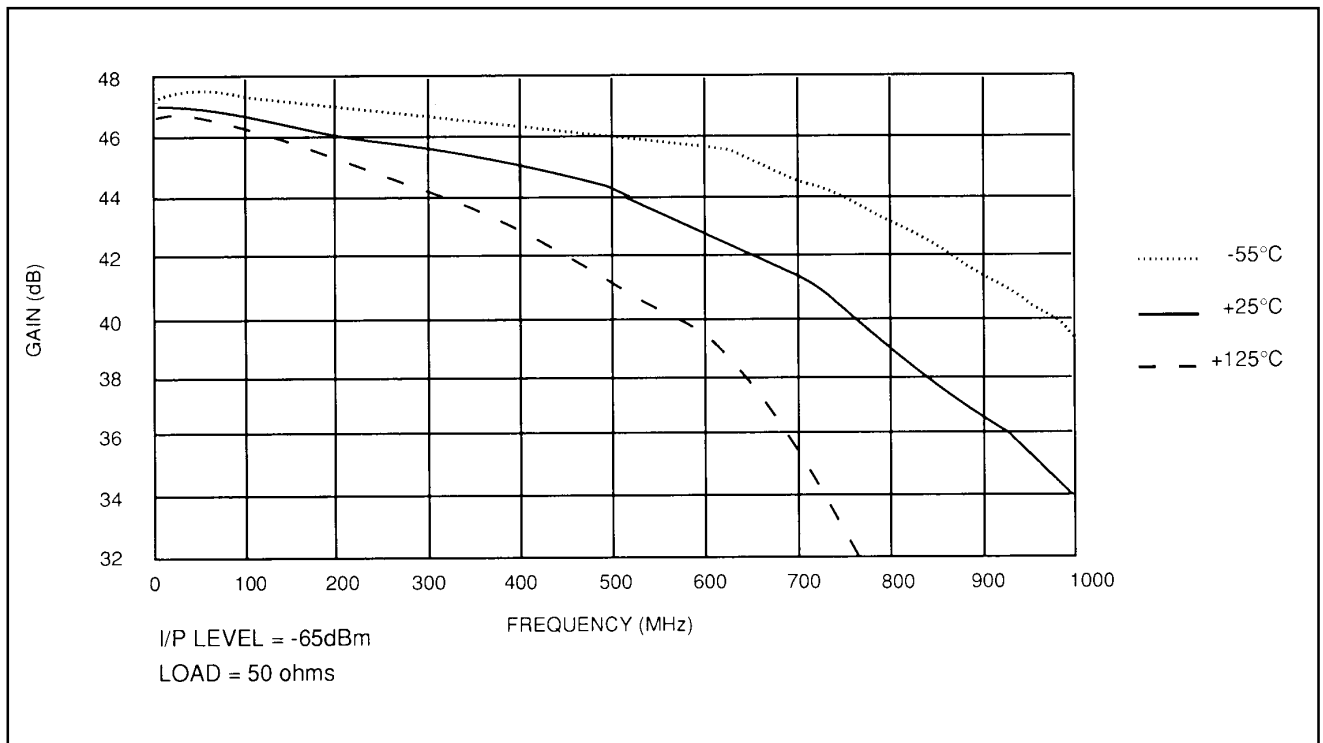


Fig.19 Small signal gain vs frequency across temperature

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

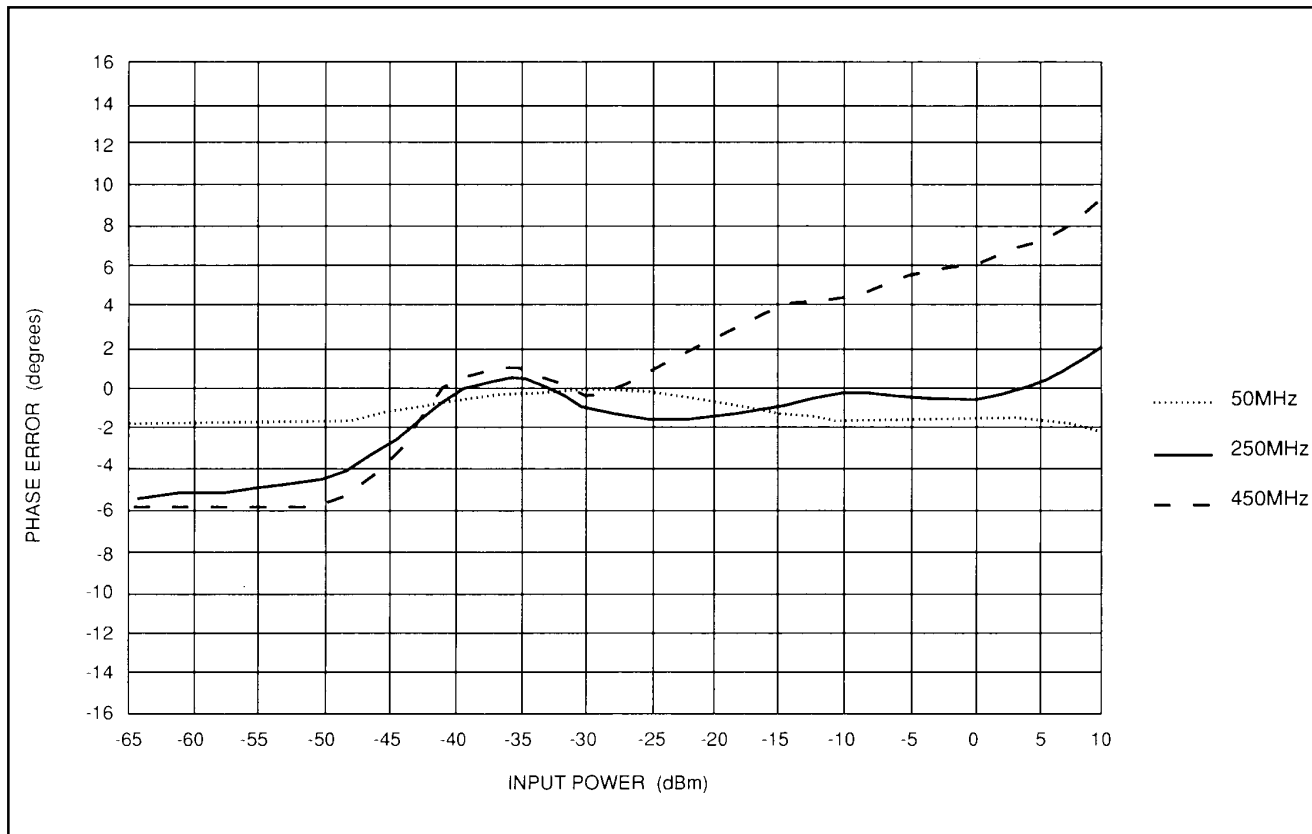


Fig.20 Phase deviation vs CW input level (normalised at -30dBm) at 25°C across input frequency

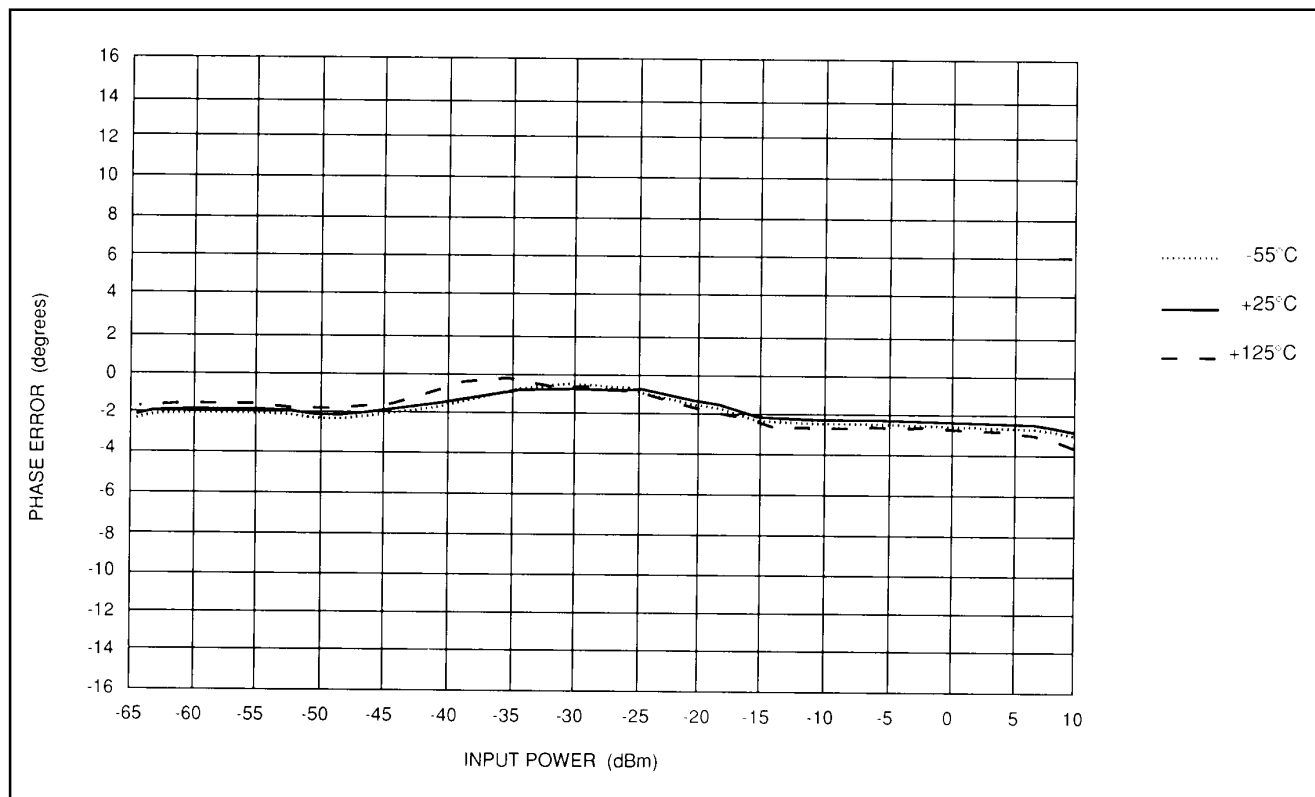


Fig.21 Phase deviation vs CW input level (normalised at -30dBm) at 50MHz across temperature

Typical characteristics for a six stage strip as a low phase shift wideband limiter (Ref. figs 5 & 6)

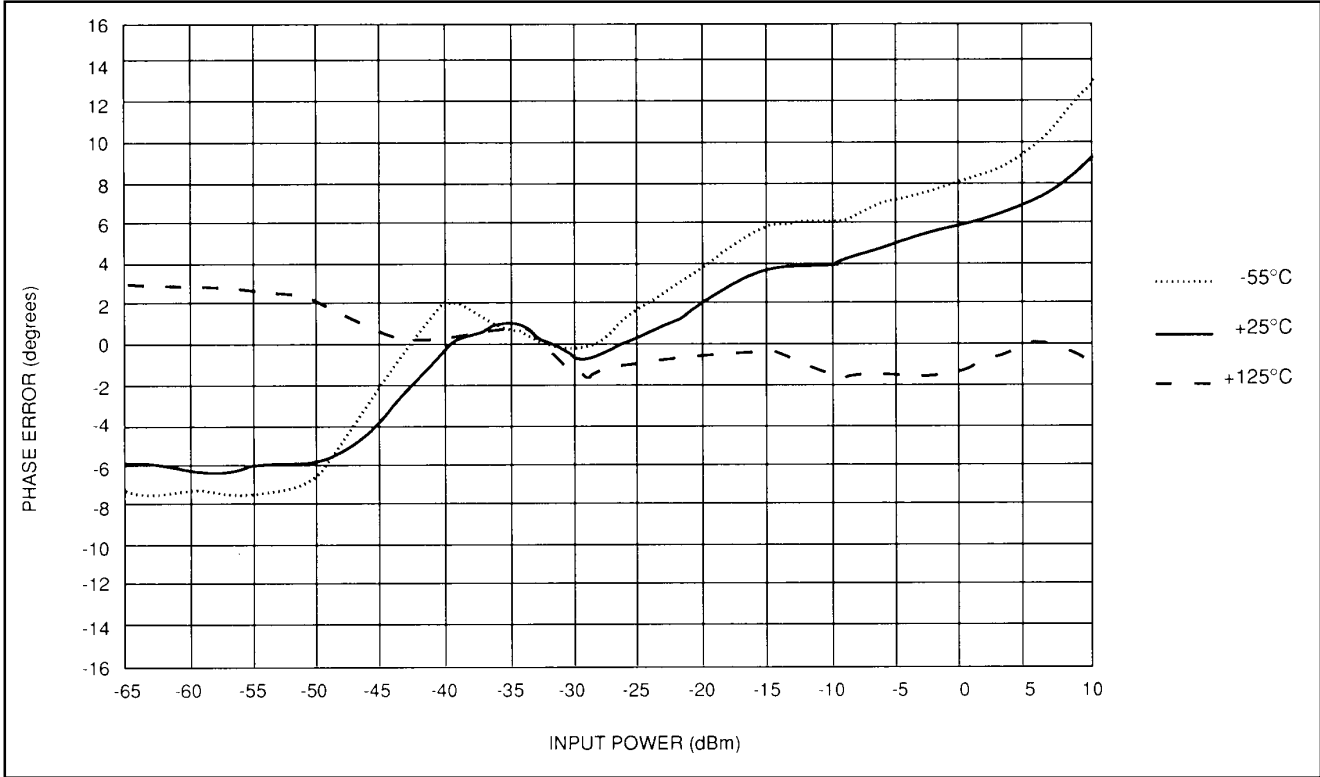


Fig.22 Phase deviation vs CW input level (normalised at -30dBm) at 450MHz across temperature

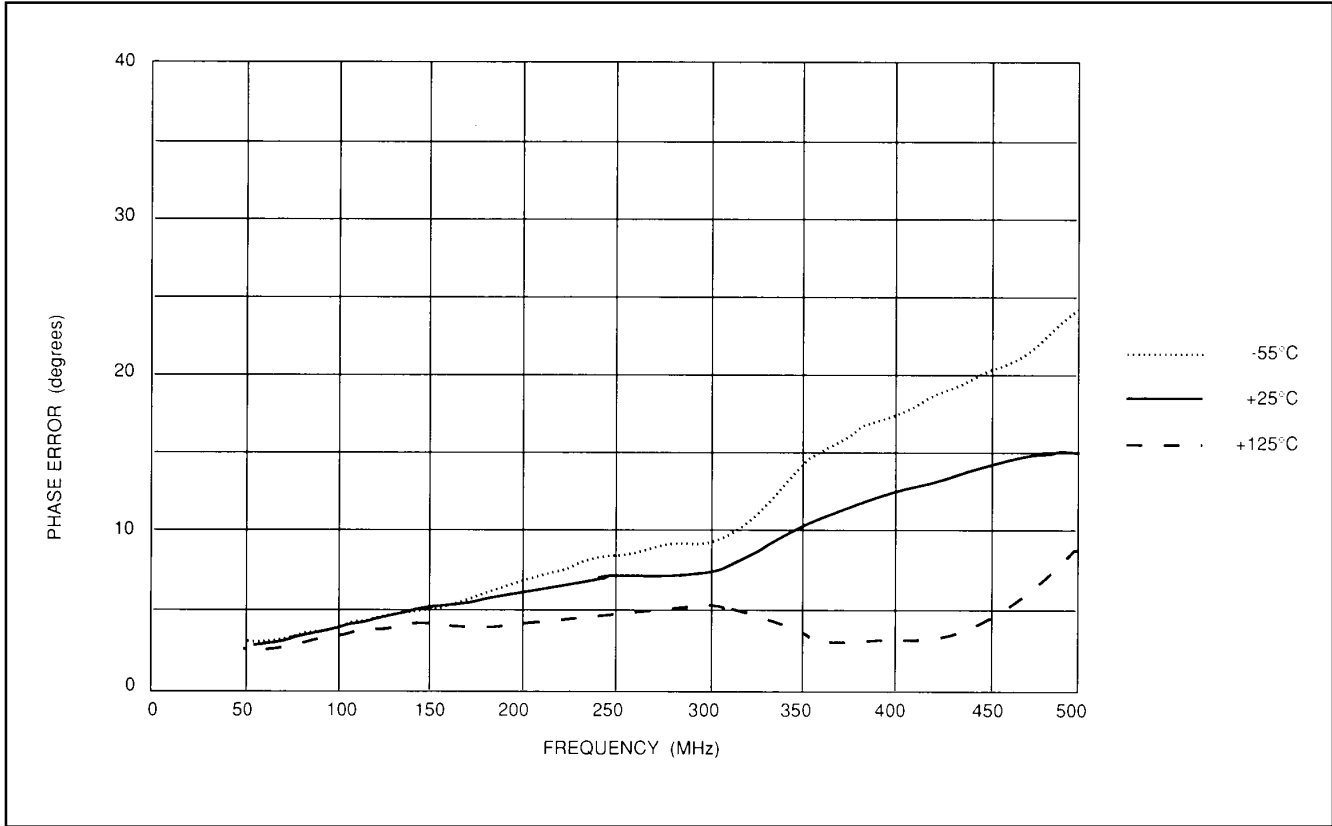
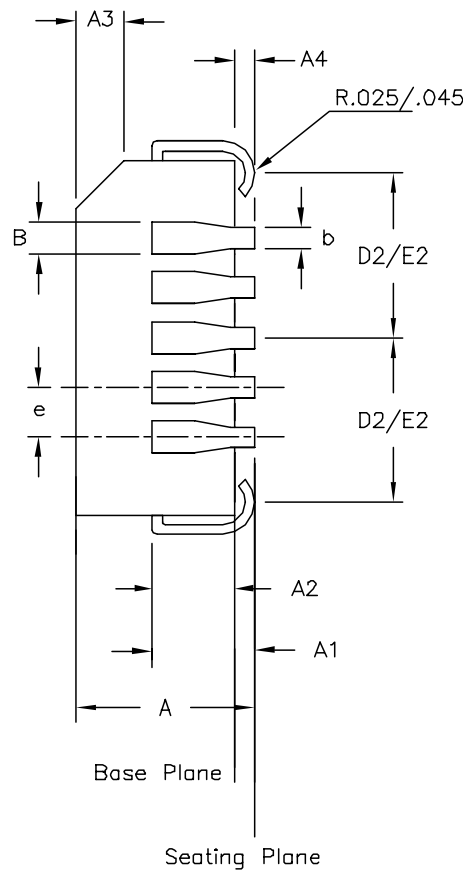
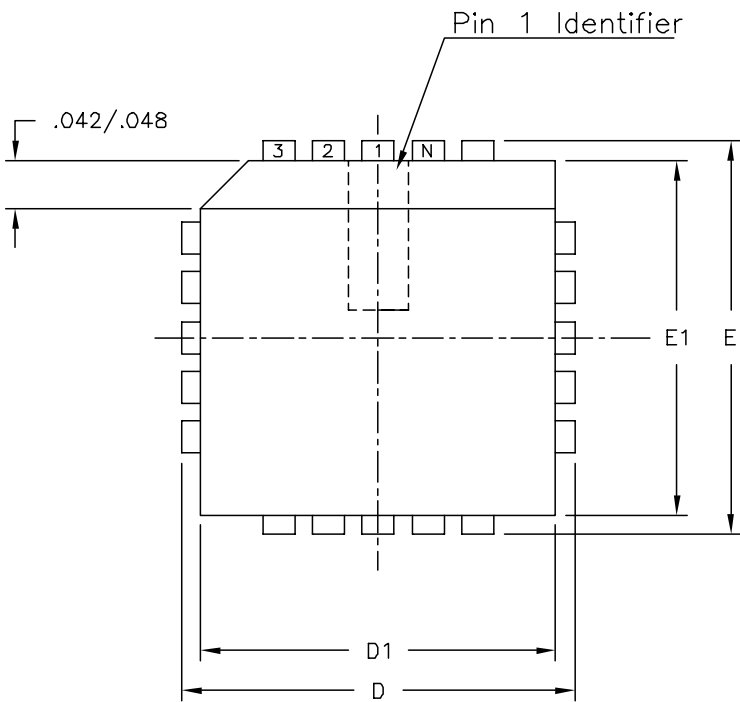


Fig.23 Peak phase deviation over -65dBm → +10dBm CW input level vs CW input frequency. Across temperature



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	—	0.51	—
D	0.385	0.395	9.78	10.03
D1	0.350	0.356	8.89	9.04
D2	0.141	0.169	3.58	4.29
E	0.385	0.395	9.78	10.03
E1	0.350	0.356	8.89	9.04
E2	0.141	0.169	3.58	4.29
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050	BSC	1.27	BSC
Pin features				
ND	5			
NE	5			
N	20			
Note	Square			
Conforms to JEDEC MS-018AA Iss. A				

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

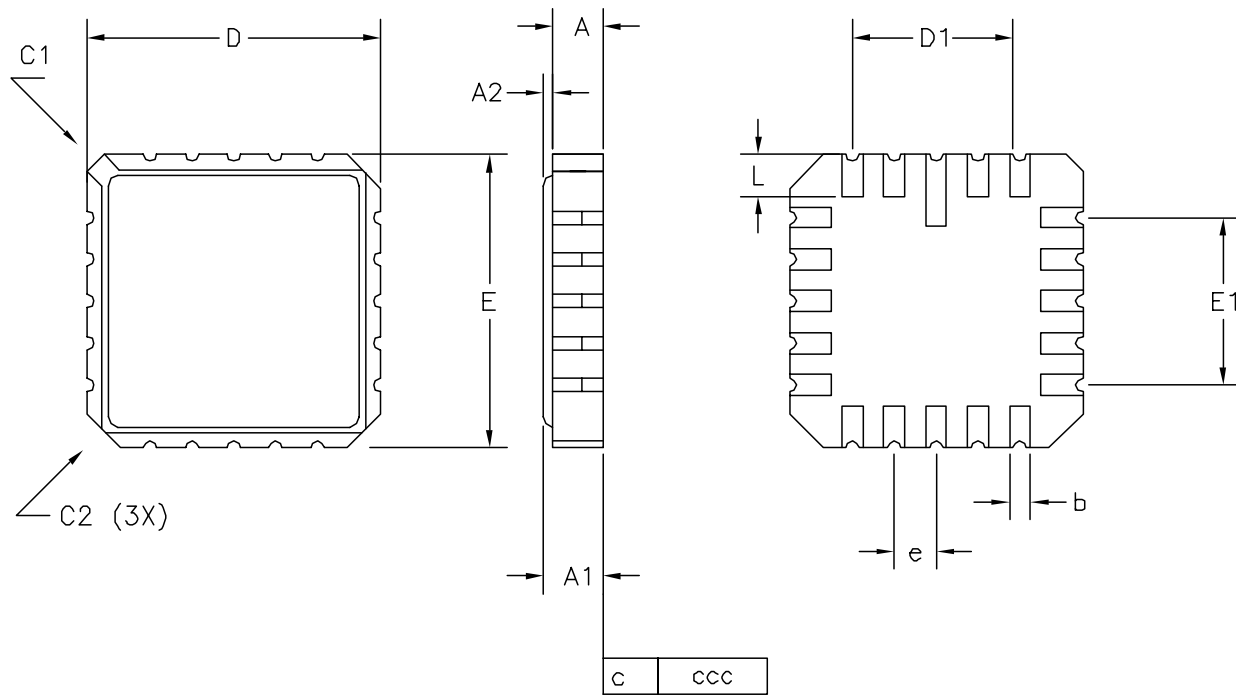
ISSUE	1	2			
ACN	5958	207468			
DATE	15AUG94	10SEP99			
APPD.					

Title: Package Outline for  
20 Lead PLCC

Drawing Number

GPD00001

ORIGINATING SITE: Swindon



CONTROL DIMENSIONS ( inch )			
SYMBOL	MIN.	NOM.	MAX.
A	0.054		0.066
A1	0.064		0.080
A2	0.010		0.014
D	0.342		0.358
D2	0.315REF		
E	0.342		0.358
E2	0.315REF		
e	0.050BSC		
b	0.025		
C1	0.020		
C2	0.040		
L	0.045		0.055
L1	0.077		0.093
R1	0.007		0.011
ccc			.003

Complies with Jeduc MS004-CB  
Supersedes 418/ED/39509/102

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ORIGINATING SITE: Swindon

ISSUE	1				
ACN	205177				
DATE	28SEP98				
APPROVED					

MITEL SEMICONDUCTOR

Title: Customer Outline Drawing for  
20 Ceramic Leadless Chip Carrier  
(0.35 x 0.35 x 0.08"), 0.05" pitch

Drawing Number  
GPD00562





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