CA1524, CA2524, CA3524

Regulating Pulse Width Modulator

Features:

- *Complete PWM power control circuitry*
- *Separate outputs for single-ended or push-pull operation*
- *Line and load regulation of 0.2% typ.*
- *Internal reference supply with 1% max. oscillator and reference voltage variation over full temperature range*
- *Standby current of less than 10 mA*
- *Frequency of operation beyond 100 kHz*
- *Variable-output dead time of 0.5 to 5 μs*
- *Low V_{CE}(sat) over the temperature range*

The RCA-CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

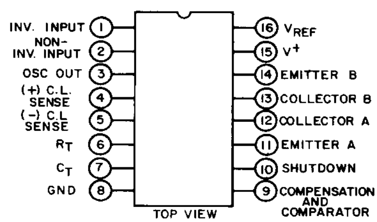
The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524, respectively. A block diagram of the CA1524 series is shown in Fig. 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converters, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converters, as well as other power-control applications.

The CA1524 is specified for the military temperature range of -55°C to +125°C.

The CA2524 and CA3524 are specified for the commercial temperature range of 0°C to 70°C. All types operate over a supply voltage range of 8 to 40 V, have a rated operating temperature range of -55°C to +125°C, and are supplied in 16-lead, dual-in-line plastic packages (E suffix, and dual-in-line frit-seal hermetic packages (F suffix). The CA3524 is available in chip form (H suffix).

Applications:

- *Positive and negative regulated supplies*
- *Dual-output regulators*
- *Flyback converters*
- *DC-DC transformer-coupled regulating converters*
- *Single-ended DC-DC converters*
- *Variable power supplies*



92CS-32664RI

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

INPUT VOLTAGE (BETWEEN V_{IN} AND GROUND TERMINALS)	40 V
OPERATING VOLTAGE RANGE (V_{IN} TO GROUND)	8 to 40 V
OUTPUT CURRENT EACH OUTPUT: (TERMINALS 11, 12 or 13, 14)	100 mA
OUTPUT CURRENT (REFERENCE REGULATOR)	50 mA
OSCILLATOR CHARGING CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25°C	1 W
Above $T_A \doteq$ 25°C	Derate linearly 8 mW/°C
OPERATING TEMPERATURE RANGE	-55 to +125°C
STORAGE TEMPERATURE RANGE	-65 to +150°C

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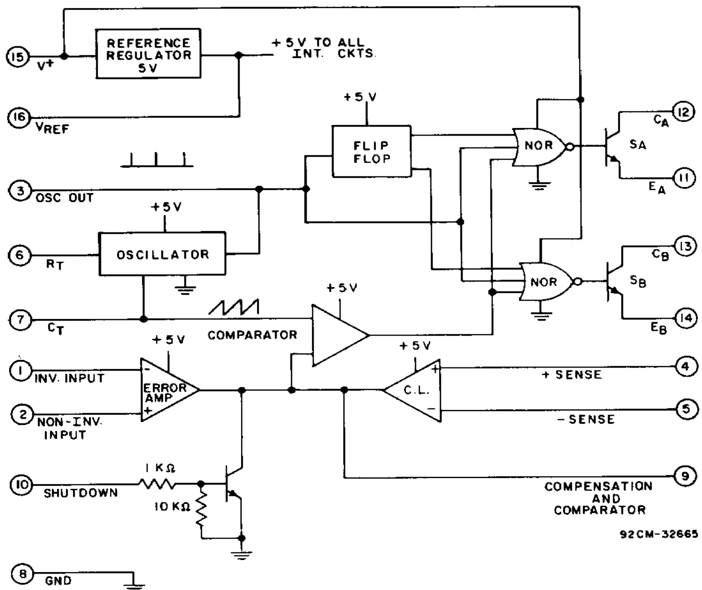

Fig. 1 - Functional block diagram of CA1524 series.

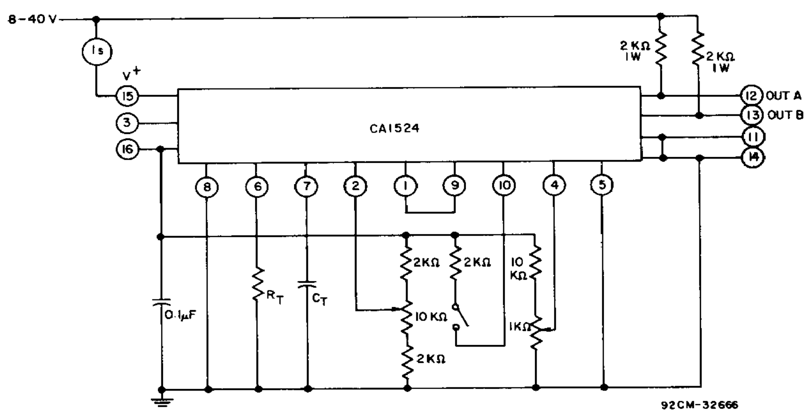

Fig. 2 - Open loop test circuit for CA1524 series.

CA1524, CA2524, CA3524

ELECTRICAL CHARACTERISTICS at T_A=-55 to +125°C for CA1524, 0 to +70°C for the CA2524 and CA3524; V+=20 V and f=20 kHz, unless otherwise stated.

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section:								
Output Voltage		4.8	5	5.2	4.6	5	5.4	V
Line Regulation	V+=8 to 40 V	—	10	20	—	10	30	mV
Load Regulation	I_L=0 to 20 mA	—	20	50	—	20	50	mV
Ripple Rejection	f=120 Hz, T_A=25°C	—	66	—	—	66	—	dB
Short Circuit Current Limit	V_{REF}=0, T_A=25°C	—	100	—	—	100	—	mA
Temperature Stability	Over Operating Temperature Range	—	0.3	1	—	0.3	1	%
Long Term Stability	T_A=25°C	—	20	—	—	20	—	mV/khr
Oscillator Section:								
Maximum Frequency	C_T=0.001 μF, R_T=2 KΩ	—	300	—	—	300	—	kHz
Initial Accuracy	R_T and C_T constant	—	5	—	—	5	—	%
Voltage Stability	V+=8 to 40 V, T_A=25°C	—	—	1	—	—	1	%
Temperature Stability	Over Operating Temperature Range	—	—	2	—	—	2	%
Output Amplitude	Terminal 3, T_A=25°C	—	3.5	—	—	3.5	—	V
Output Pulse Width (Pin 3)	C_T=0.01 μF, T_A=25°C	—	0.5	—	—	0.5	—	μs
* Ramp Voltage Low	Pin 7	—	0.6	—	—	0.6	—	V
* Ramp Voltage High	Pin 7	—	3.5	—	—	3.5	—	V
Capacitor Charging Current Current Range	Pin 7 (5-2 V_{BE})/RT	0.03	—	2	0.03	—	2	mA
Timing Resistance Range	Pin 6	1.8	—	120	1.8	—	120	KΩ
Charging Capacitor Range	Pin 7	0.001	—	0.1	0.001	—	0.1	μF
Dead Time Expansion Capacitor on Pin 3 (when a small osc. cap is used)	Pin 3	100	—	1000	100	—	1000	pF
Error Amplifier Section:								
Input Offset Voltage	V_{CM}=2.5 V	—	0.5	5	—	2	10	mV
Input Bias Current	V_{CM}=2.5 V	—	1	10	—	1	10	μA
Open Loop Voltage Gain		72	80	—	60	80	—	dB
Common Mode Voltage	T_A=25°C	1.8	—	3.4	1.8	—	3.4	V
Common Mode Rejection Ratio	T_A=25°C	—	70	—	—	70	—	dB
Small Signal Bandwidth	A_V= 0 dB, T_A=25°C	—	3	—	—	3	—	MHz
Output Voltage	T_A=25°C	0.5	—	3.8	0.5	—	3.8	V
Amplifier Pole		—	250	—	—	250	—	Hz
Pin 9 Shutdown Current	External Sink	—	200	—	—	200	—	μA
Comparator Section:								
Duty Cycle	% Each Output On	0	—	45	0	—	45	%
Input Threshold	Zero Duty Cycle	—	1	—	—	1	—	V
Input Threshold	Max. Duty Cycle	—	3.5	—	—	3.5	—	V
Input Bias Current		—	1	—	—	1	—	μA
Current Limiting Section:								
Sense Voltage For 25% Output Duty Cycle	Terminal 9=2 V with Error Amplifier Set for Max Out, T_A=25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.		—	0.2	—	—	0.2	—	mV/°C
Common Mode Voltage		-1	—	+1	-1	—	+1	V
Rolloff Pole of R51 C3 + Q64		—	300	—	—	300	—	Hz

*Ramp voltage at Pin 7 } High / Low  where t = OSC period in microseconds
t ≅ R_TC_T with C_T in microfarads and R_T in ohms.

Output frequency at each output transistor is half OSC frequency when each output is used separately and is equal to the OSC frequency when each output is connected in parallel.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA1524, CA2524 Min.	Typ.	Max.	CA3524 Min.	Typ.	Max.	UNITS
Output Section: (Each Output)								
Collector-Emitter Voltage		40	—	—	40	—	—	V
Collector Leakage Current	V_{CE}=40 V	—	0.1	50	—	0.1	50	μA
Saturation Voltage	V+=40 V, I_C=50 mA	—	0.8	2	—	0.8	2	V
Emitter Output Voltage	V+=20 V	17	18	—	17	18	—	V
Rise Time	R_C=2 KΩ, T_A=25°C	—	0.2	—	—	0.2	—	μs
Fall Time	R_C=2 KΩ, T_A=25°C	—	0.1	—	—	0.1	—	μs
Total Standby Current:• I_S	V+=40 V	—	4	10	—	4	10	mA

•Excluding oscillator charging current, error and current limit dividers, and with outputs open.

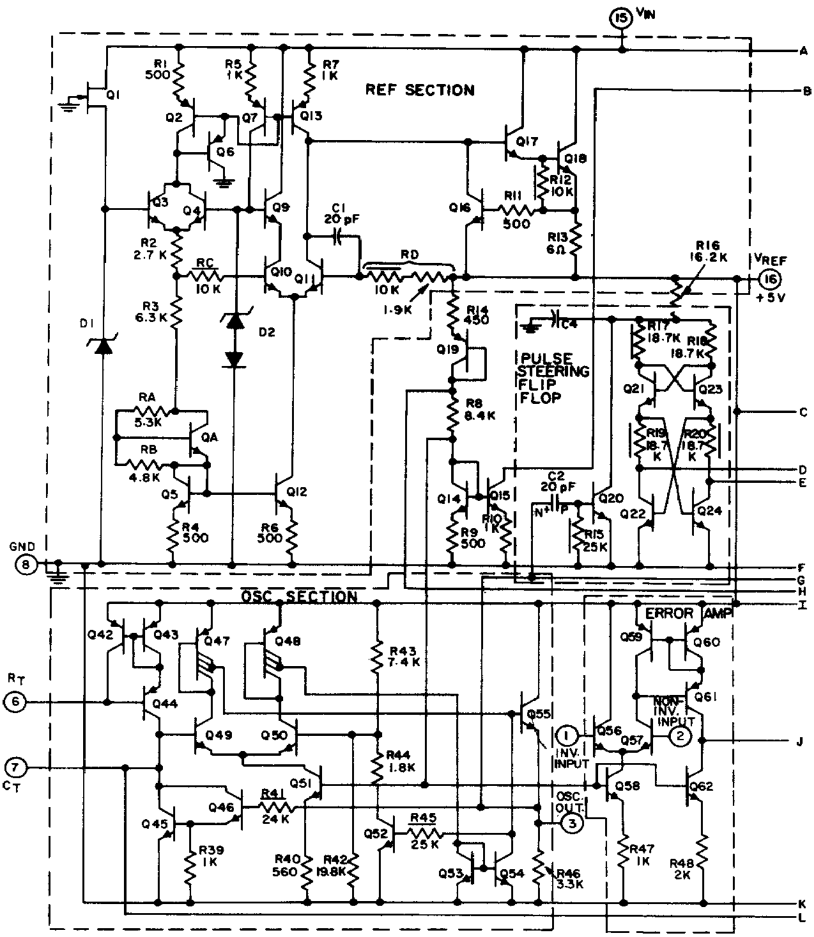

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Fig. 3 - Schematic diagram.

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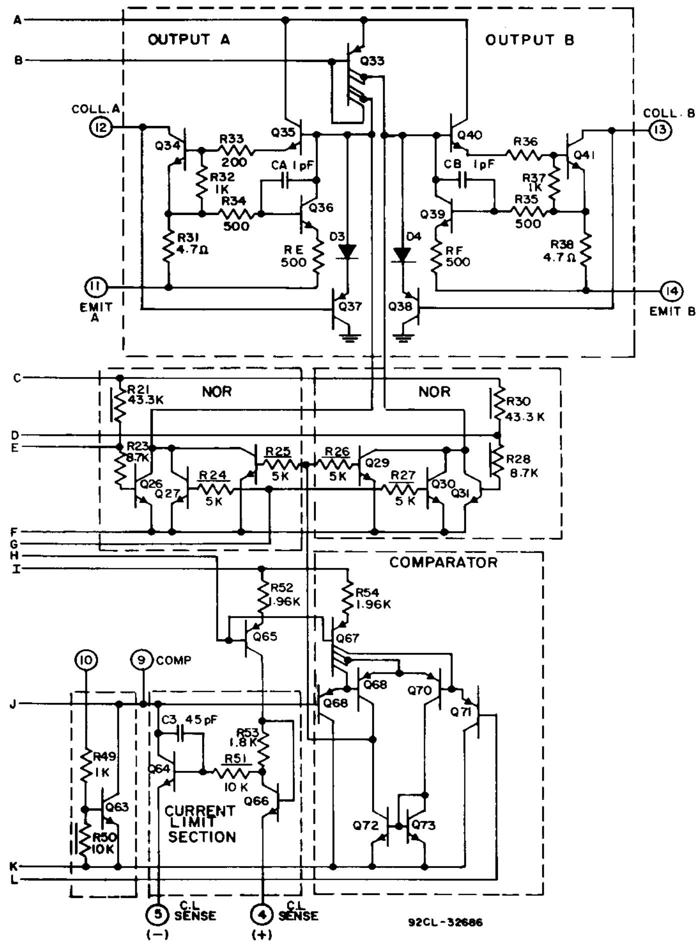

Fig. 3 - Schematic diagram (cont'd).

CIRCUIT DESCRIPTION

Voltage Reference Section

The CA1524 series contains an internal series voltage regulator employing a zener reference to provide a nominal 5-volt output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50-mA output current.

Fig. 4 shows the temperature variation of the reference voltage with supply voltages of 8 to 40 volts and load currents up to 20 mA. Load regulation and line regulation curves are shown in Figs. 5 and 6, respectively.

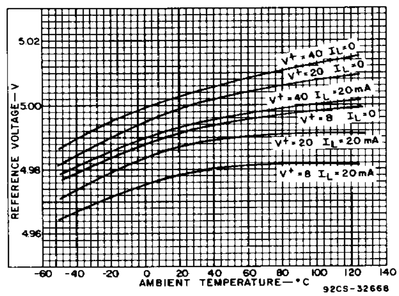

Fig. 4 - Typical reference voltage as a function of ambient temperature.

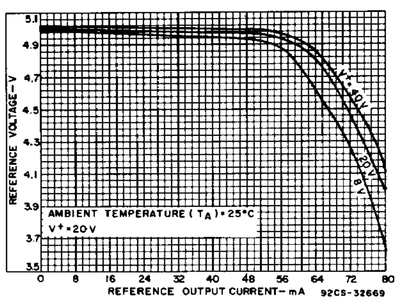

Fig. 5 - Typical reference voltage as a function of reference output current.

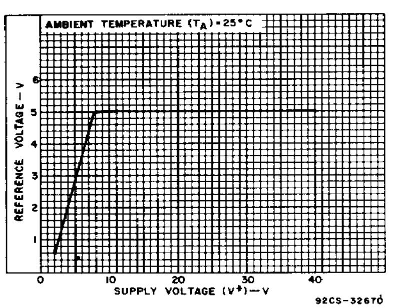

Fig. 6 - Typical reference voltage as a function of supply voltage.

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to $(5-2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30 μA to 2 mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5 μs to 5 μs for a capacitor range of 0.001 to 0.1 μF. The pulse has two internal uses: as a dead-time control of blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Fig. 7. Pulse widths less than 0.5 μs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

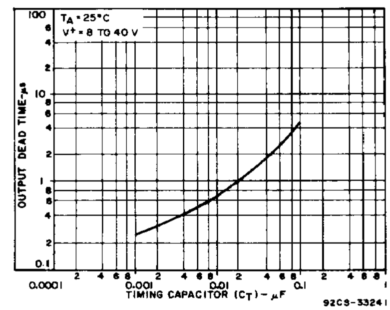

Fig. 7 - Typical output stage dead time as a function of timing capacitor value.

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100 pF but no greater than 1000 pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2-KΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable.

The oscillator period is determined by R_T and C_T, with an approximate value of $t=R_TC_T$, where R_T is in ohms, C_T is in μF, and t is in μs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals. Fig. 8 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Fig. 10. To synchronize two or more CA1524's, one must be designated as master, with

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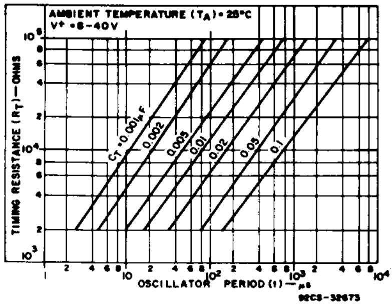

Fig. 8 - Typical oscillator period as a function of R_T and C_T.

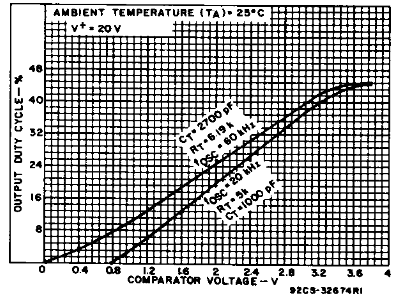

Fig. 10 - Typical duty cycle as a function of comparator voltage (at terminal 9).

R_TC_T set for the correct period. Each of the remaining units (slaves) must have a C_T of ½ the value used in the master and approximately a 10% longer R_TC_T period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

Error Amplifier Section

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{out}, terminal 9, is very high (≅ 5 MΩ).

The gain is:

$$A_V = g_mR = 8\ I_C\ R/2KT = 10^4,$$

$$\text{where } R = \frac{R_{out}\ R_L}{R_{out}+R_L},\ R_L=\infty,\ A_V \propto 10^4$$

Since R_{out} is extremely high, the gain can be easily reduced from a nominal 10^4 (80 dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Fig. 9.

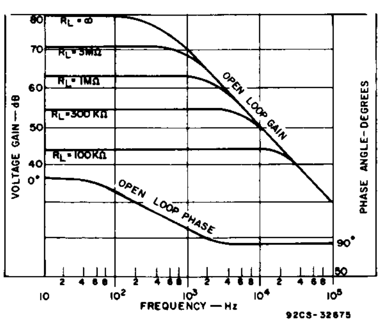

Fig. 9 - Open-loop error amplifier response characteristics.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Fig. 10. The uncompensated amplifier has a single pole at approximately 250 Hz and a unity gain cross-over at 3 MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000-pF capacitor and a variable series 50-KΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200 μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 11. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

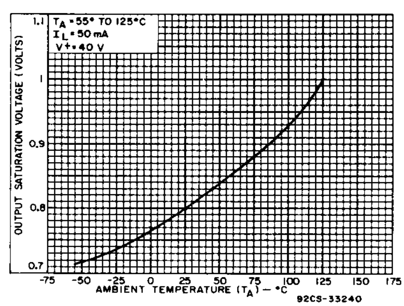

Fig. 11 - Typical output saturation voltage as a function of ambient temperature.

Output Section

The CA1524 series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100 mA for each output and 100 mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figs. 11 and 12, respectively.

There are a number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

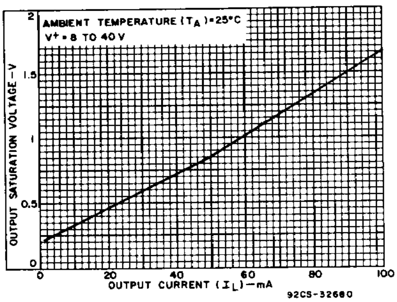

Fig. 12 - Typical output saturation voltage as a function of output current.

Device Application Suggestions

For higher currents, the circuit of Fig. 13 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5-volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

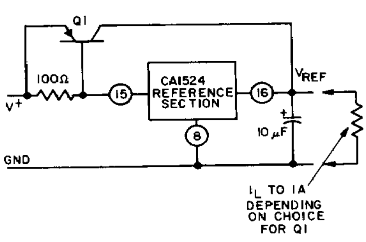

Fig. 13 - Circuit for expanding the reference current capability.

The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 14. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

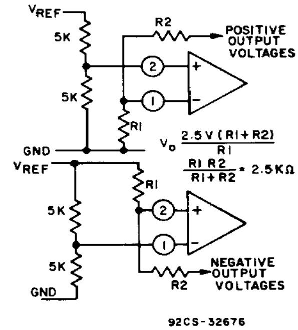

Fig. 14 - Error amplifier biasing circuits.

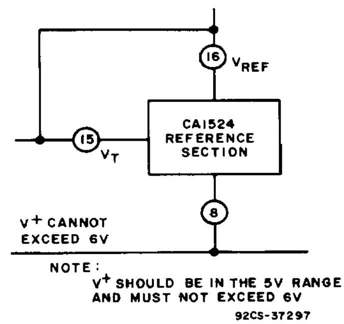

Fig. 15 - Circuit to allow external bypass of the reference regulation.

To provide an expansion of the dead time without loading the oscillator, the circuit of Fig. 16 may be used.

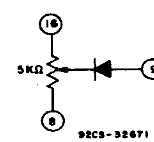

Fig. 16 - Circuit for expansion of dead time, without using a capacitor on pin 3 or when a low value oscillator capacitor is used.

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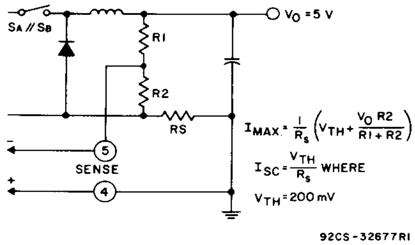

Fig. 17 - Foldback current-limiting circuit used to reduce power dissipation under shorted output conditions.

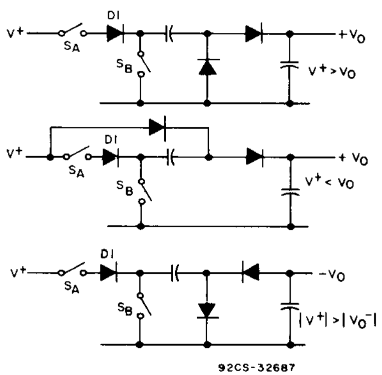

Fig. 18 - Capacitor-diode coupled voltage multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown of transistor switch S_A).

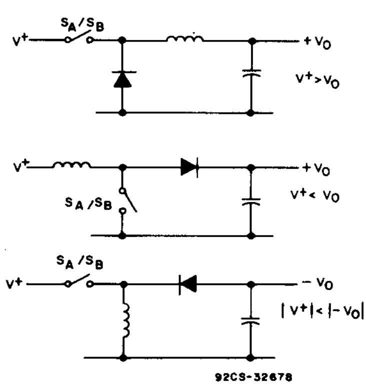

Fig. 19 - Single-ended inductor circuits where the two outputs of the 1524 are connected in parallel.

Table I - Input vs. Output voltage, and Feedback Resistor Values for I_L=40 mA (For capacitor-diode output circuit in Fig. 21)

V_O (V)	R2 (KΩ)	V+ (Min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

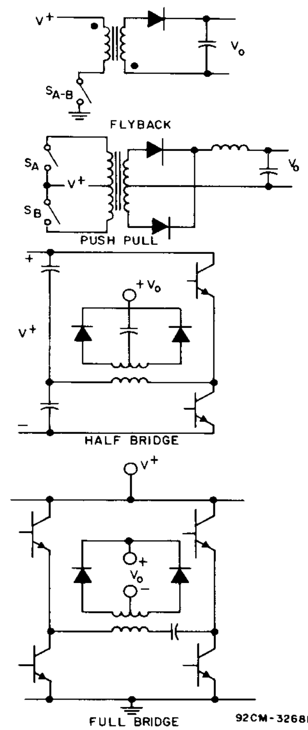

Fig. 20 - Transformer-coupled outputs.

APPLICATIONS*

A capacitor-diode output filter is used in Fig. 22 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage.

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Fig. 21 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5 V to -20 V with an output current of 40 mA.

Single-Ended Switching Regulator

The CA1524 in the circuit of Fig. 22 has both output stages connected in parallel to produce an effective 0-90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

*For additional information on the application of this device and a further explanation of the circuits below, see RCA Application Note ICAN-6915 "Application of the CA1524 series PWM IC".

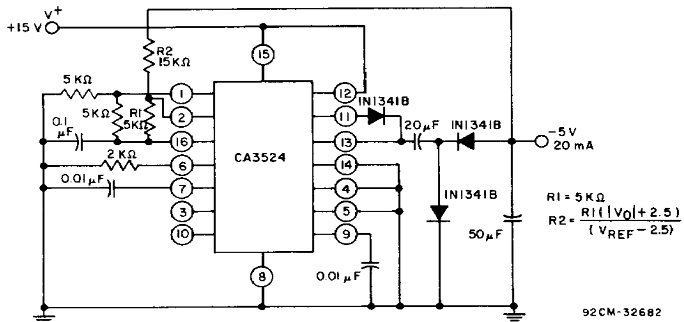

Fig. 21 - Capacitor-diode output circuit.

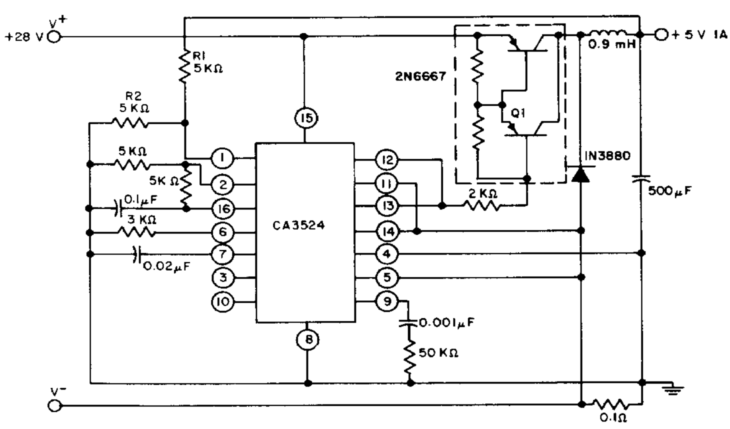

Fig. 22 - Single-ended LC switching regulator circuit.

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Flyback Converter

Fig. 23 shows a flyback converter circuit for generating a dual 15-volt output at 20 mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Fig. 24. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low-Frequency Pulse Generator

Fig. 25 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5-V (or 2.5-V) pulse of 0%-45% (or 0%-90%) on time is possible over a frequency range of 150 to 500 Hz. Switch S1 is used to go from a 5-V output pulse (S1 closed) to a 2.5-V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75 Hz to 250 Hz, respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500 Hz. The frequency is adjusted by R1; R2 controls duty cycle.

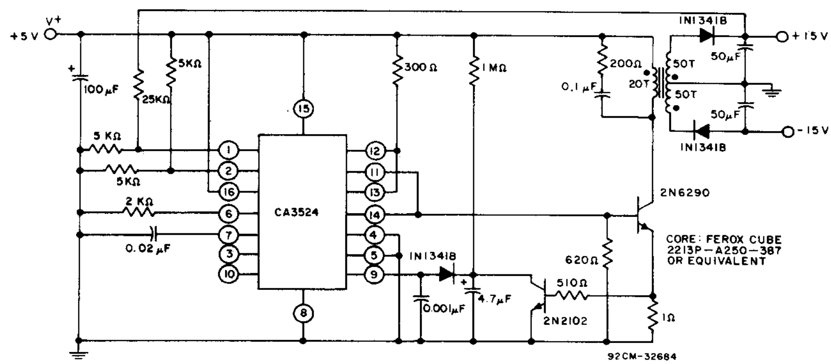


Fig. 23 - Flyback converter circuit.

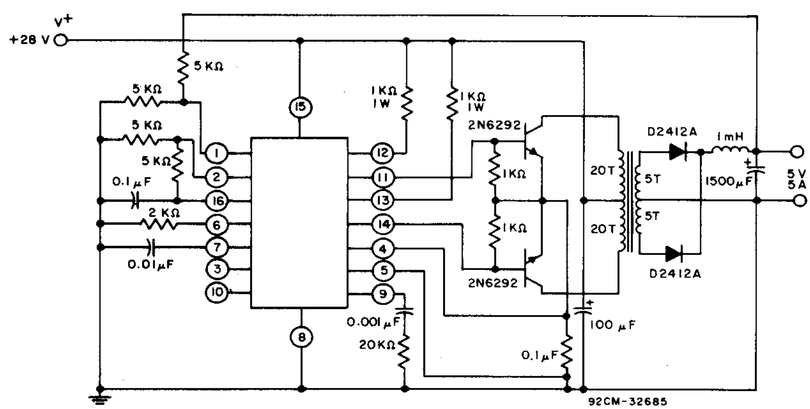
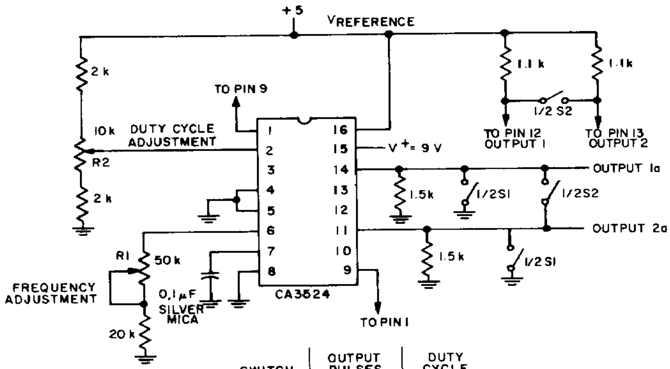


Fig. 24 - Push-pull transformer-coupled converter.



SWITCH	OUTPUT PULSES	DUTY CYCLE
S1	0 -5 V	0 - 45 %
S2	–	0 - 90 %

92CM-33244

Fig. 25 - Low-frequency pulse generator.

The Variable Switcher

The circuit diagram of the CA1524, used as a variable-output-voltage power supply is shown in Fig. 26. By connecting the two output transistors in parallel, the duty cycle is doubled, i.e., 0-90%.

As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage.

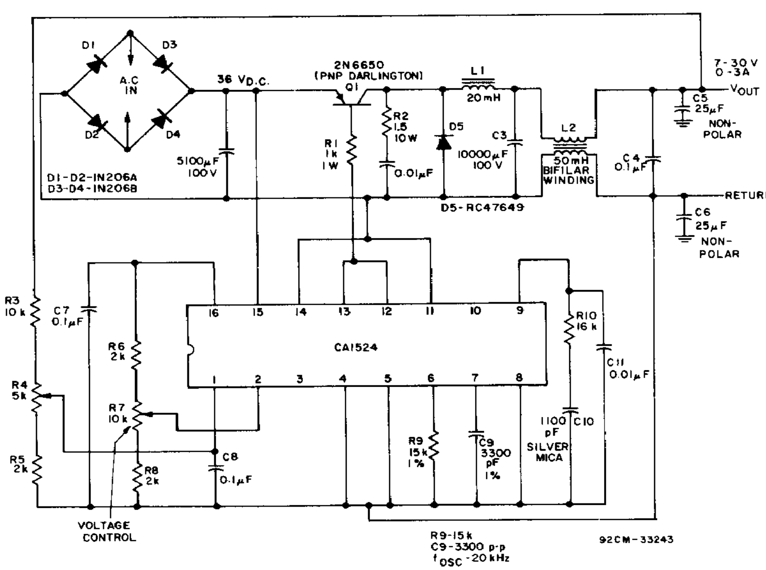


Fig. 26 - The CA1524 used as a 0-5 A, 7-30 V laboratory supply.

CA1524, CA2524, CA3524

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figs. 27 and 28 uses half (Q2) of the CA1524 output in a low-voltage switching regulator (2.2 V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

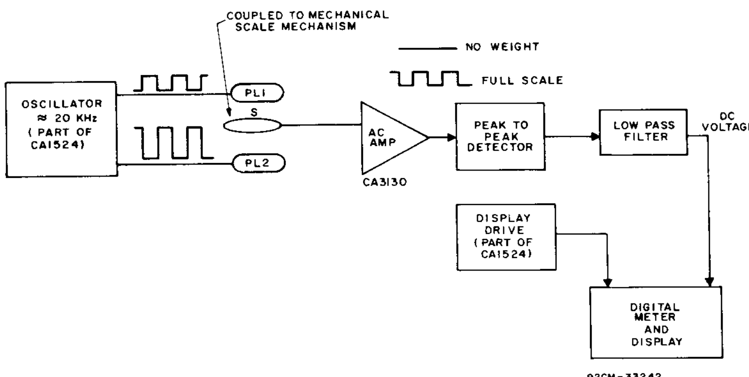


Fig. 27 - Basic digital readout scale.

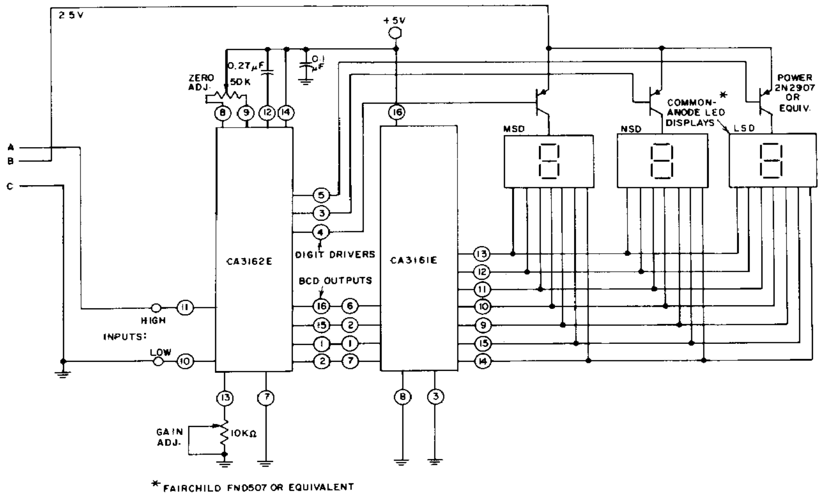


Fig. 28 - Schematic diagram of digital readout scale (cont'd).

CA1524, CA2524, CA3524

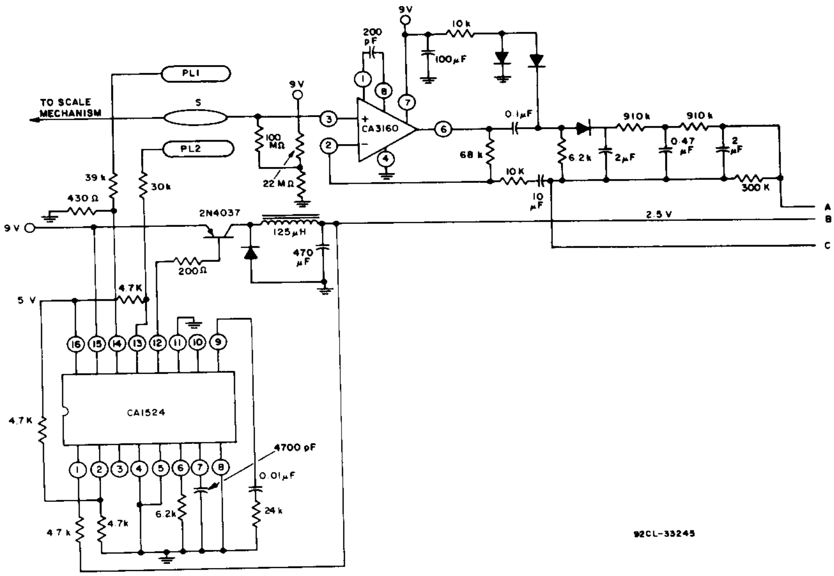
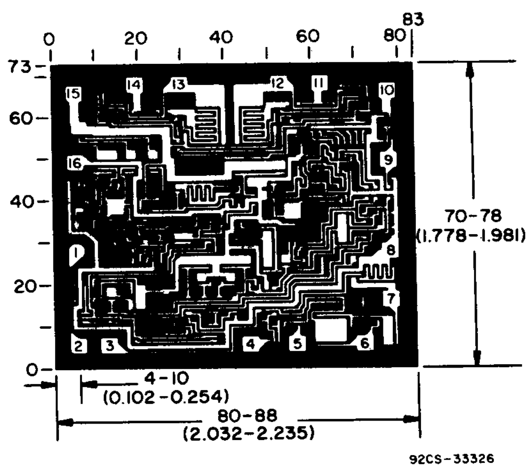


Fig. 28 - Schematic diagram of digital readout scale.



Dimensions and pad layout for CA3524H chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.