Features

- Utilizes the ARM7TDMI™ ARM® Thumb® Processor
  - High-performance 32-bit RISC architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In Circuit Emulation)
- 2/8K bytes Internal RAM
- Fully programmable External Bus Interface (EBI)
  - Maximum external address space of 64M bytes
  - Up to eight chip selects
  - Software programmable 8/16-bit external databus
- Multi-Processor Interface (MPI)
  - High-performance External Processor Interface
  - 512 x 16-bit SRAM
- Eight-channel Peripheral Data Controller
- Eight-level Priority, Individually Maskable, Vectored Interrupt Controller
  - Five External Interrupts, including a High-priority, Low-latency Interrupt Request
- 58 Programmable I/O Lines
- Six-channel 16-bit Timer/Counter
  - Six External Clock Inputs
  - Two Multi-purpose I/O Pins per Channel
- Three USARTs
  - Two Dedicated Peripheral Data Controller (PDC) Channels per USART
  - Support for up to 9-bit Data Transfers
- Master/Slave SPI Interface
  - Two Dedicated Peripheral Data Controller (PDC) Channels
  - 8- to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Power Management Controller (PMC)
  - CPU and Peripherals can be Deactivated Individually
- IEEE 1149.1 JTAG Boundary Scan on all pins
- Fully Static Operation: 0 Hz to 25 MHz
- 2.7V to 3.6V Operating Range
- Available in a 176-lead TQFP Package

Description

The M63200 and the M63800 are members of the Atmel AT91 16/32-bit Microcontroller family which is based on the ARM7TDMI embedded processor. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91 ARM-based MCU family also features Atmel's high-density, nonvolatile memory technology. The Flash memory is in-system programmable.

The M63X00 has a direct connection to off-chip memory, including Flash, through the External Bus Interface. A second parallel interface, the Multi-Processor Interface (MPI), provides a high-performance interface with an external coprocessor.

The device is manufactured using Atmel's high density CMOS technology. By combining the ARM7TDMI microcontroller core with an on-chip RAM and a wide range of peripheral functions on a monolithic chip, the Atmel M63X00 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many compute-intensive multi-processor applications.

AT91 ARM® Thumb® Microcontrollers

M63200
M63800
Summary

Rev. 1028AS–01/99

Pin Configuration

Table 1. M63X00 Pinout

Pin	M63X00
1	GND
2	GND
3	NCS0
4	NCS1
5	NCS2
6	NCS3
7	NLB/A0
8	A1
9	A2
10	A3
11	A4
12	A5
13	A6
14	A7
15	VDD
16	GND
17	A8
18	A9
19	A10
20	A11
21	A12
22	A13
23	A14
24	A15
25	A16
26	A17
27	A18
28	A19
29	VDD
30	GND
31	A20/CS7
32	A21/CS6
33	A22/CS5
34	A23/CS4
35	D0
36	D1
37	D2
38	D3
39	D4
40	D5
41	D6
42	D7
43	VDD
44	VDD

Pin	M63X00
45	GND
46	GND
47	D8
48	D9
49	D10
50	D11
51	D12
52	D13
53	D14
54	D15
55	PB19/TCLK0
56	PB20/TIOA0
57	PB21/TIOB0
58	PB22/TCLK1
59	VDD
60	GND
61	PB23/TIOA1
62	PB24/TIOB1
63	PB25/TCLK2
64	PB26/TIOA2
65	PB27/TIOB2
66	PA0/TCLK3
67	PA1/TIOA3
68	PA2/TIOB3
69	PA3/TCLK4
70	PA4/TIOA4
71	PA5/TIOB4
72	PA6/TCLK5
73	VDD
74	GND
75	PA7/TIOA5
76	PA8/TIOB5
77	PA9/IRQ0
78	PA10/IRQ1
79	PA11/IRQ2
80	PA12/IRQ3
81	PA13/FIQ
82	PA14/SCK0
83	PA15/TXD0
84	PA16/RXD0
85	PA17/SCK1
86	PA18/TXD1/NTRI
87	VDD
88	VDD

Pin	M63X00
89	GND
90	GND
91	PA19 / RXD1
92	PA20 / SCK2
93	PA21 / TXD2
94	PA22 / RXD2
95	PA23 / SPCK
96	PA24/MISO
97	PA25/MOSI
98	PA26/NPCS0/NSS
99	PA27/NPCS1
100	PA28/NPCS2
101	PA29/NPCS3
102	MPI_A1
103	VDD
104	GND
105	MPI_A2
106	MPI_A3
107	MPI_A4
108	MPI_A5
109	MPI_A6
110	MPI_A7
111	MPI_A8
112	MPI_A9
113	MPI_NCS
114	MPI_RNW
115	MPI_BR
116	MPI_BG
117	VDD
118	GND
119	MPI_D0
120	MPI_D1
121	MPI_D2
122	MPI_D3
123	MPI_D4
124	MPI_D5
125	MPI_D6
126	MPI_D7
127	MPI_D8
128	MPI_D9
129	MPI_D10
130	MPI_D11
131	VDD
132	VDD

Pin	M63X00
133	GND
134	GND
135	MPI_D12
136	MPI_D13
137	MPI_D14
138	MPI_D15
139	PB0/MPI_NOE
140	PB1/MPI_NLB
141	PB2/MPI_NUB
142	PB3
143	PB4
144	PB5
145	PB6
146	PB7
147	VDD
148	GND
149	PB8
150	PB9
151	PB10
152	PB11
153	PB12
154	PB13
155	PB14
156	PB15
157	PB16
158	PB17/MCKO
159	NWDOVF
160	MCKI
161	VDD
162	GND
163	PB18/BMS
164	JTAGSEL
165	TMS
166	TDI
167	TDO
168	TCK
169	NTRST
170	NRST
171	NWAIT
172	NOE/NRD
173	NWE/NWR0
174	NUB/NWR1
175	VDD
176	VDD

Pin Description

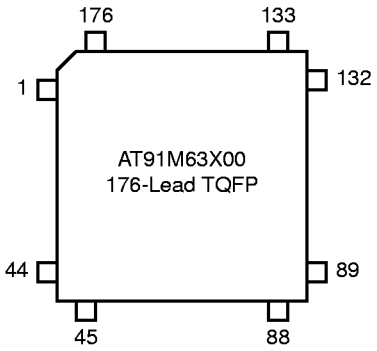
Table 2. M63X00 Pin Description

Module	Name	Function	Type	Active Level	Comments
EBI	A0 - A23	Address bus	Output	–	All valid after reset
	D0 - D15	Data bus	I/O	–	
	CS4 - CS7	Chip select	Output	high	A23 - A20 after reset
	NCS0 - NCS3	Chip select	Output	low	
	NWR0	Lower byte 0 write signal			
	NWR1	Lower byte 1 write signal			
	NRD	Read signal	Output	low	Used in Byte Write option
	NWE	Write enable	Output	low	Used in Byte Select option
	NOE	Output enable	Output	low	Used in Byte Select option
	NUB	Upper byte select (16-bit SRAM)	Output	low	Used in Byte Select option
	NLB	Lower byte select (16-bit SRAM)	Output	low	Used in Byte Select option
	NWAIT	Wait input	Input	low	
	BMS	Boot Mode Select	Input	low	Sampled during reset
MPI	MPI_NCS	Chip select	Input	low	
	MPI_RNW	Read not Write signal	Input	–	
	MPI_BR	Bus request from external processor	Input	high	
	MPI_BG	Bus Grant to external processor	Output	high	
	MPI_NOE	Output Enable	Input	low	
	MPI_NLB	Lower byte	Input	low	
	MPI_NUB	Upper byte	Input	low	
	MPI_A1 - MPI_A9	Address bus	Input		
	MPI_D0 - MPI_D15	Data bus	I/O		
AIC	IRQ0 - IRQ3	External interrupt request	Input	–	PIO controlled after reset
	FIQ	Fast external interrupt request	Input	–	PIO controlled after reset
Timer	TCLK0 - TCLK5	Timer external clock	Input	–	PIO controlled after reset
	TIOA0 - TIOA5	Multipurpose timer I/O pin A	I/O	–	PIO controlled after reset
	TIOB0 - TIOB5	Multipurpose timer I/O pin B	I/O	–	PIO controlled after reset
USART	SCK0 - SCK2	External Serial clock	I/O	–	PIO controlled after reset
	TXD0 - TXD2	Transmit data output	Output	–	PIO controlled after reset
	RXD0 - RXD2	Receive data input	Input	–	PIO controlled after reset
SPI	SPCK	SPI clock	I/O	–	PIO controlled after reset
	MISO	Master In Slave Out	I/O	–	PIO controlled after reset
	MOSI	Master Out Slave In	I/O	–	PIO controlled after reset
	NSS	Slave Select	Input	low	PIO controlled after reset
	NPCS0 - NPCS3	Peripheral chip select	Output	low	PIO controlled after reset
PIO	PA0 - PA29	Programmable I/O port A	I/O	–	Input after reset
	PB0 - PB27	Programmable I/O port B	I/O	–	Input after reset
WD	NWDOVF	Watchdog timer overflow	Output	low	Open drain
Clock	MCKI	Master clock input	Input	–	Schmidt trigger
	MCKO	Master clock output	Output	–	
Reset	NRST	Hardware reset input	Input	low	Schmidt trigger, internal pull-up

Table 2. M63X00 Pin Description (Continued)

Module	Name	Function	Type	Active Level	Comments
ICE/JTAG	JTAGSEL	Selects between JTAG and ICE mode	Input	high	
	TMS	Test mode select	Input	–	Schmidt trigger, internal pull-up
	TDI	Test data in	Input	–	Schmidt trigger, internal pull-up
	TDO	Test data out	Output	–	
	TCK	Test clock	Input	–	Schmidt trigger, internal pull-up
	NTRST	Test reset input	Input	low	Schmidt trigger, internal pull-up
Power	VDD	Power			
	GND	Ground			
Emulation	NTRI	Tristate Mode Enable	Input	low	Sampled during reset

Figure 1. Pin Configuration (Top View)



Architectural Overview

The M63X00 architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC) transfers data between the on-chip USARTs/SPI and the on and off-chip memories without processor intervention. Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64k contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The M63X00 peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16K byte address space allocated in the upper 3M bytes of the 4G byte address space. Except for the interrupt controller, the peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits and the third address reads the value stored in the register. A bit can be set or reset by writing a one to the corresponding position at the appropriate address. Writing a zero has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O controller. The PIO controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI processor operates in little-endian mode in the M63X00 microcontroller. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI Datasheet.

The ARM Standard In-Circuit-Emulation debug interface is supported via the ICE port of the M63X00.

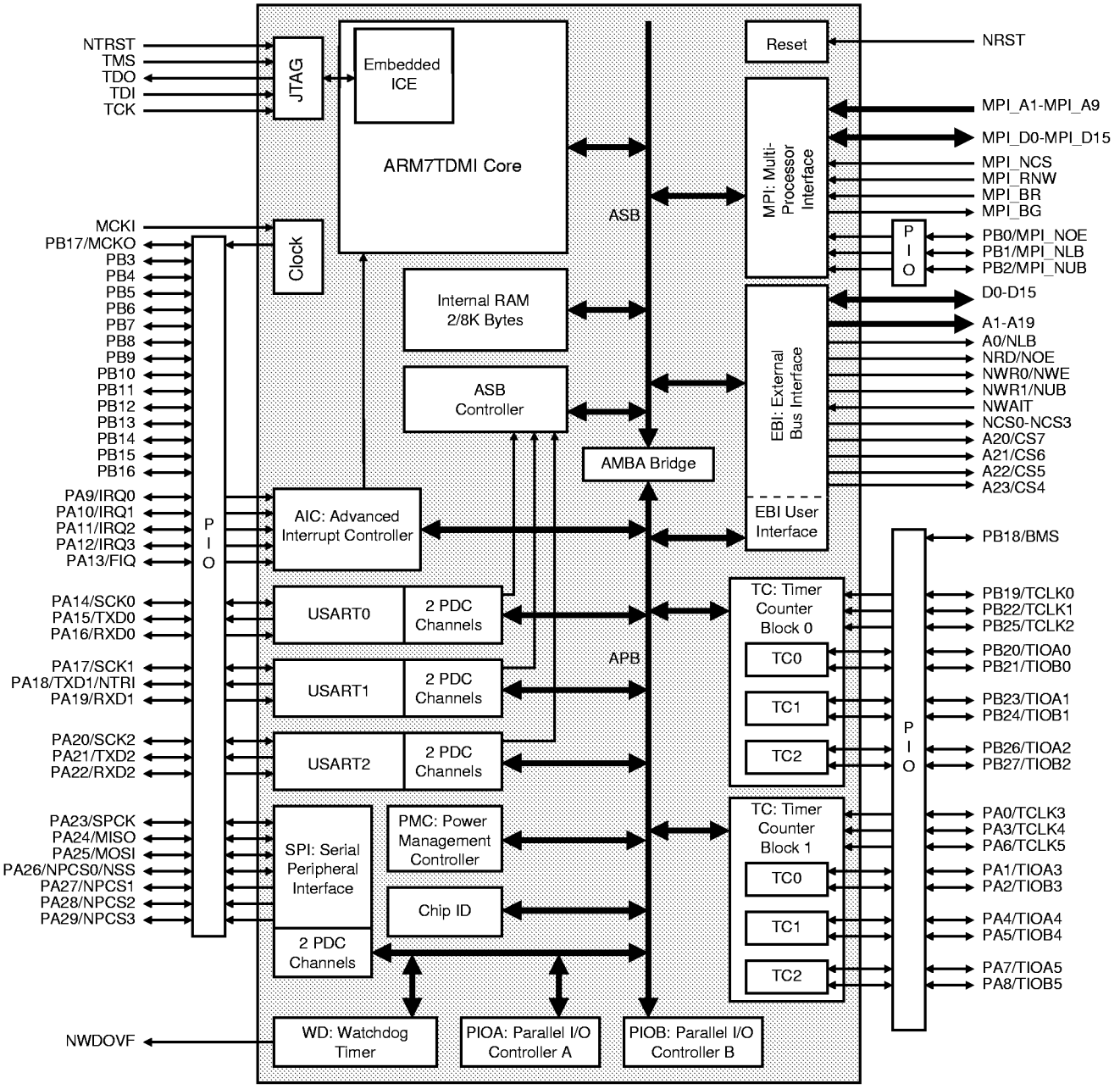
PDC: Peripheral Data Controller

The M63X00 has an 8-channel PDC dedicated to the three on-chip USARTs and to the SPI. One PDC channel is connected to the receiving channel and one to the transmitting channel of each USART and of the SPI.

The user interface of a PDC channel is integrated in the memory space of each USART channel and in the memory space of the SPI. It contains a 32-bit address pointer register (US_RPR/SP_RPR or US_TPR/SP_TRP) and a 16-bit count register (US_RCR/SP_RCR or US_TCR/SP_TCR). When the programmed data is transferred, an end of transfer interrupt is generated by the corresponding USART or the SPI.

Block Diagram

Figure 1. M63X00 Block Diagram



EBI: External Bus Interface

The EBI generates the signals which control the access to the external memory or peripheral devices. The EBI is fully programmable and can address up to 64M bytes. It has eight chip selects and a 24-bit address bus, the upper four bits of which are multiplexed with a chip select.

The 16-bit data bus can be configured to interface with 8- or 16-bit external devices. Separate read and write control signals allow for direct memory and peripheral interfacing.

The EBI supports different access protocols allowing single clock cycle memory accesses.

The main features are:

- External Memory Mapping
- Up to 8 chip select lines
- 8- or 16-bit data bus
- Byte write or byte select lines
- Remap of boot memory
- Two different read protocols
- Programmable wait state generation
- External wait request
- Programmable data float time

MPI: Multi-Processor Interface

The M63X00 family features a second bus interface which is dedicated to parallel data transfers with an external processing device. The MPI is based on a 1K byte SRAM and an arbiter. Both the ARM core and the external processor can read and write to any location in the SRAM.

AIC: Advanced Interrupt Controller

The M63X00 has an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The processor's NFIQ line can only be asserted by the external fast interrupt request input: FIQ. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ3.

An 8-level priority encoder allows the customer to define the priority between the different NIRQ interrupt sources.

Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high or low level sensitive.

PIO: Parallel I/O Controller

The M63X00 has 58 programmable I/O lines. 14 pins are dedicated as general purpose I/O pins. The other I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. The PIO lines are controlled by two separate and identical PIO Controllers called PIOA and PIOB. The PIO controller enables the generation of an interrupt on input change and insertion of a simple input glitch filter on any of the PIO pins.

USART: Universal Synchronous/Asynchronous Receiver/Transmitter

The M63X00 provides three identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:

- Programmable Baud Rate Generator
- Parity, Framing and Overrun Error Detection
- Line Break Generation and Detection
- Automatic Echo, Local Loopback and Remote Loopback channel modes
- Multi-drop Mode: Address Detection and Generation
- Interrupt Generation
- Two Dedicated Peripheral Data Controller channels
- 6-, 7-, 8- and 9-bit character length

SPI: Serial Peripheral Interface

The M63X00 includes an SPI which provides communication with external devices in master or slave mode.

The SPI has four external chip selects which can be connected to up to 15 devices. The data length is programmable, from 8 to 16-bit.

As for the USART, a 2-channel PDC can be used to move data between memory and the SPI without CPU intervention.

TC: Timer Counter

The M63X00 features two Timer Counter Blocks, each containing three identical 16-bit timer counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each Timer Counter channel has 3 external clock inputs, 5 internal clock inputs, and 2 multi-purpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts via the AIC (Advanced Interrupt Controller).

The Timer Counter block has two global registers which act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each Timer Counter channel, allowing them to be chained.

WD: Watchdog Timer

The M63X00 has an internal Watchdog Timer which can be used to prevent system lock-up if the software becomes trapped in a deadlock.

PMC: Power Management Controller

The M63X00 Power Management Controller allows optimization of power consumption. The PMC enables/disables the clock inputs of most of the peripherals and the ARM core.

When the ARM core clock is disabled, the current instruction is finished before the clock is stopped. The clock can be re-enabled by any enabled interrupt or by a hardware reset.

When a peripheral clock is disabled, the clock is immediately stopped. When the clock is re-enabled, the peripheral resumes action where it left off.

Due to the static nature of the design, the contents of the on-chip RAM and registers for which the clocks are disabled remain unchanged

SF: Special Function

The M63200 provides registers which implement the following special functions.

- Chip identification
- RESET status

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	RAM	Package	Operation Range
25	2.7V to 3.6V	AT91M63200-25AC	2K bytes	TQFP 176	Commercial (0°C to 70°C)
		AT91M63200-25AI	2K bytes	TQFP 176	Industrial (-40°C to 85°C)
25	2.7V to 3.6V	AT91M63800-25AC	8K bytes	TQFP 176	Commercial (0°C to 70°C)
		AT91M63800-25AI	8K bytes	TQFP 176	Industrial (-40°C to 85°C)