

# REALTEK

## ALC850(D)

### EIGHT CHANNEL AC'97 2.3 AUDIO CODEC

## DATASHEET

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## USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC850 Audio codec chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

## REVISION HISTORY

Revision	Release Date	Summary
0.40	2003/08/03	Preliminary version.
1.00	2003/11/6	Second preliminary version.
1.10	2004/04/05	The LQFP-48 ‘e’ dimension is typical 0.0196inch.
1.11	2004/09/19	Corrected typing error in S/PDIF output feature.
1.2	2004/11/15	First official release.
1.3	2005/03/11	Add lead (Pb)-free and version package identification information on page 4 and in Table 64, on page 48.

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## 1. General Description

Featuring four 16-bit two-channel DACs and a stereo 16-bit ADC, the ALC850 and ALC850D are AC'97 Rev 2.3 compatible eight-channel audio codecs designed for PC multimedia systems. The ALC850(D) incorporates proprietary converter technology and fully meets performance requirements for PC99/2001 systems.

Four pairs of stereo outputs, with 5-bit volume control and multiple stereo and mono inputs, along with flexible mixing, and gain and mute functions, provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC850(D) operates from a low-power-consumption 3.3V power supply.

Two integrated 50mW/20ohm headphone audio amplifiers provide high-quality personal audio listening. Utilizing Universal Audio Jack® technology, Line-In and Mic-In can also serve as an amplified stereo Headphone-Out. In addition, the ALC850(D) is embedded with an impedance sensing capability to detect when a device has been connected to input or output jacks.

The ALC850(D) integrates an on-board dual PLL clock generator (14.318MHz and 24.576MHz), saving the cost of a 24.576MHz crystal. A PCBEEP generator is built-in and can be programmed by the BIOS to generate POST beeps without a buzzer. S/PDIF input and output functions are also supported, offering easy connection of PCs to consumer electronic products such as AC3 decoders/speakers, and mini disk devices.

The ALC850(D) supports host/soft audio from Intel ICHx chipsets, as well as audio controller-based VIA/SiS/ALi/AMD/nVIDIA/ATI chipsets. Bundled Windows series (98/ME/NT/2000/XP) and Linux drivers, EAX/Direct Sound 3D/I3DL2/A3D compatible sound effect utilities (supporting Karaoke, 26 types of environment sound emulation, 10-band equalizer), HRTF 3D positional audio, and optional Dolby® Digital Live, providing an excellent entertainment package and game experience for PC users.

## 2. Features

- Meets performance requirements for audio on PC99/2001 systems
- Complies with AC'97 Rev 2.3 specifications:
  - ◆ Jack sensing on Front-Out, Surround-Out, Cen/LFE-Out, Surround-Back-Out, Mic-In, Line-In, and Front-Mic-In
  - ◆ Clock input support options:
    - 14.318MHz PLL (may be set to 24.576MHz) to eliminate crystal
    - 12.288MHz BITCLK input
  - ◆ Integrated PCBEEP generator
  - ◆ Interrupt capability
  - ◆ Page and analog Plug & Play registers
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- Eight-channel DA converter (48kHz)
- Stereo AD converter (48kHz)
- Three analog line-level stereo inputs with 5-bit volume control: Line-In, CD, Aux
- High-quality differential CD input
- Two analog line-level mono inputs: PCBEEP, Phone-In
- Dedicated stereo Front-Mic input for front panel applications
- Line-In, Aux, and Mic-In can be shared with Surround-Out, Surround-Back-Out, and Cen/LFE-Out (FlexJack<sup>®</sup>)
- +20dB boost preamplifier for Mic input
- Both Front-Out and Surround-Out integrate 50mW/20ohm amplifiers
- External Amplifier Power Down (EAPD)
- Power management and enhanced power saving features
- Stereo Mic record for AEC/BF application
- Supports Power-Off CD operation
- Adjustable VREFOUT control
- Supports 48kHz S/PDIF output
- Supports 32/44.1/48kHz S/PDIF input
- Three Universal Audio Jacks (UAJ<sup>®</sup>): Front-Out, Line-In, and Mic-In
- Six Jack Detect pins for automatic jack sensing
- Power support:
  - ◆ Digital: 3.3V
  - ◆ Analog: 3.3V/5V
- Standard 48-pin LQFP package
- EAX<sup>™</sup> 1.0 & 2.0 compatible
- Direct Sound 3D<sup>™</sup> compatible
- A3D<sup>™</sup> compatible
- I3DL2 compatible
- HRTF 3D positional audio
- 10-band Software Equalizer
- Optional Dolby<sup>®</sup> Digital Live
- Voice cancellation and key shifting in Karaoke mode
- AVRack<sup>®</sup> Media Player
- Configuration Panel for enhanced user experience

## 3. System Applications

- Multimedia PCs
- PC games
- Information appliances (IA)
- Voice recognition
- Audio conferencing

## 4. Analog Mixer Diagram

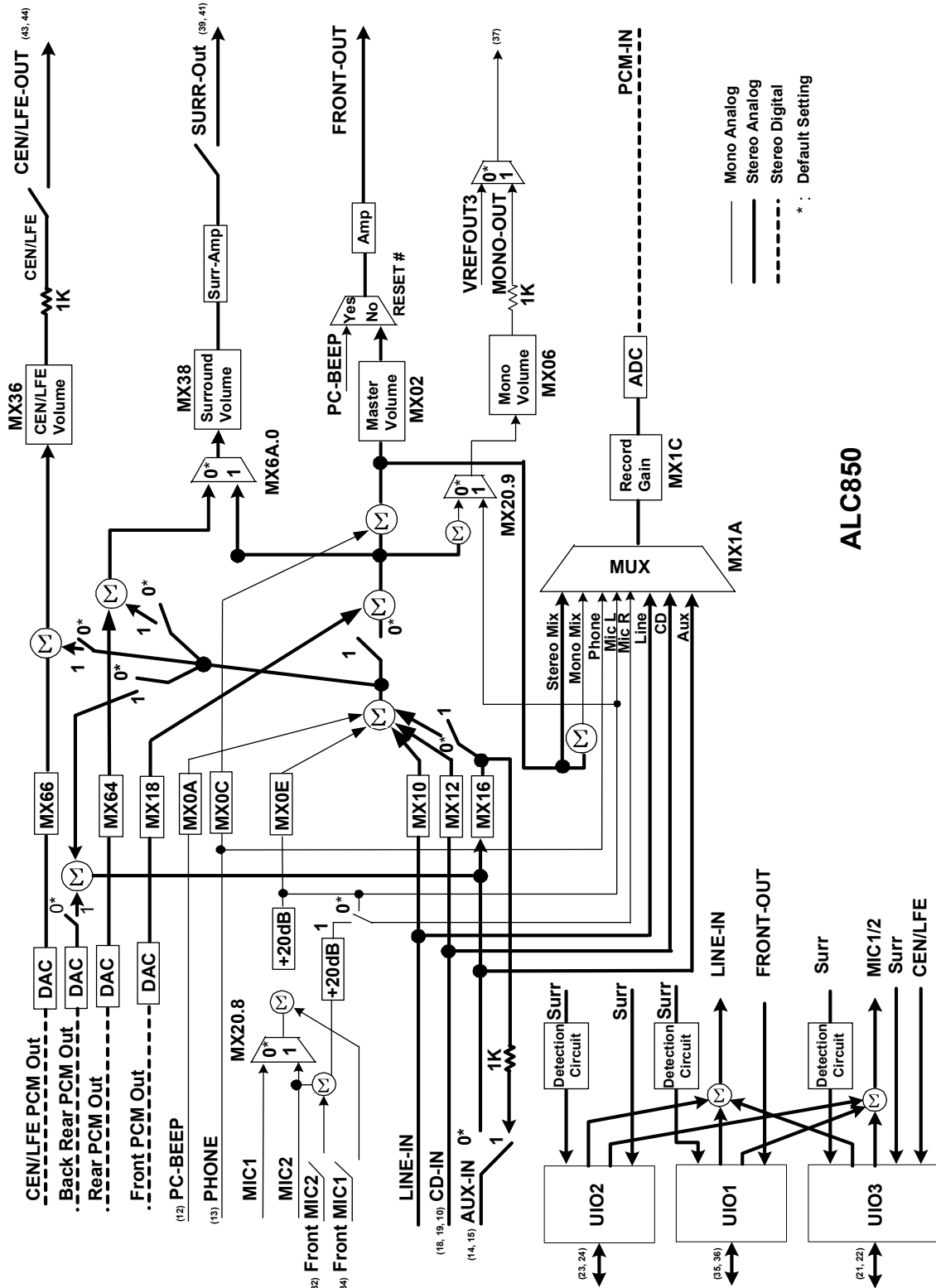


Figure 1. Analog Mixer

## 5. Pin Assignments

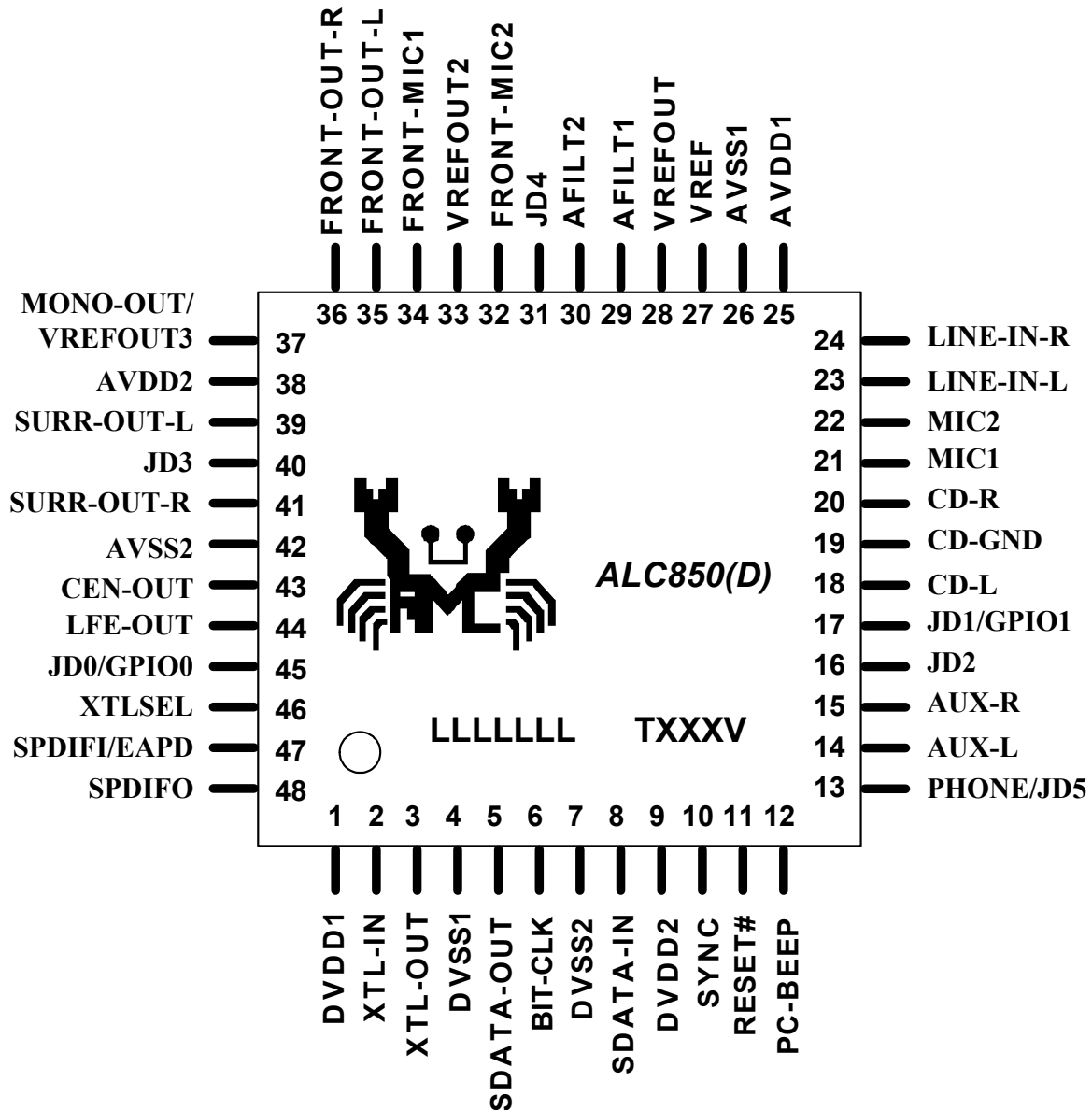


Figure 2. Pin Assignments

### 5.1. Lead (Pb)-Free Package and Version Identification

Lead (Pb)-free package is indicated by an “L” in the location marked “T” in Figure 2. The version number is shown in the location marked “V”.

## 6. Pin Description

### 6.1. Digital I/O Pins

**Table 1. Digital I/O Pins**

Name	Pin No	Type	Description	Characteristic Definition
XTL-IN	I	2	Crystal input	Crystal input pad
XTL-OUT	O	3	Crystal output	Crystal output pad
SDATA-OUT	I	5	Serial TDM AC'97 output	Schmitt input, $V_L=0.3V_{dd}$ , $V_H=0.4V_{dd}$
BIT-CLK	IO	6	Bit clock output (12.288MHz)	CMOS input/output, $V_t=0.35V_{dd}$ . This pin will be floating when RESET# is active
SDATA-IN	O	8	Serial TDM AC'97 input	CMOS output. Internally pulled low by a 100K resistor. This pin will be floating when RESET# is active.
SYNC	I	10	Sample Sync (48Khz)	Schmitt input, $V_L=0.3V_{dd}$ , $V_H=0.4V_{dd}$
RESET#	I	11	AC'97 master H/W reset	Schmitt input, $V_L=0.3V_{dd}$ , $V_H=0.4V_{dd}$
XTLSEL*	I	46	Crystal selection	Internally pulled high by a 100K resistor
SPDIFI/EAPD	I/O	47	S/PDIF input/External Amplifier power down control	Digital input with 0.4V Schmitt trigger biased at 1.65V/output
SPDIFO	O	48	S/PDIF output	Digital output
TOTAL: 10 Pins				

\*XTLSEL=floating, bypass 14.318MHz to 24.576MHz digital PLL. The clock source is 24.576MHz crystal or external clock.

XTLSEL=pull low, select 14.318MHz to 24.576MHz digital PLL

## 6.2. Analog I/O Pins

**Table 2. Analog I/O Pins**

Pin Name	Pin No	Type	Description	Characteristic Definition
PC-BEEP	I	12	PC speaker input	Analog input (1.6Vrms)
PHONE/JD5	I	13	Speaker phone input/Jack Detect 5	Analog input (1.6Vrms)/ Internally pulled high (5V) to AVDD by a 100K resistor. Trigger point of high is at 2.5V
AUX-L	I	14	AUX Left channel/Back Surround-Out-L	Analog input (1.6Vrms)/Analog output (1Vrms)
AUX-R	I	15	AUX Right channel/Back Surround-Out-L	Analog input (1.6Vrms)/Analog output (1Vrms)
CD-L	I	18	CD audio Left channel	Analog input (1.6Vrms)
CD-GND	I	19	CD audio analog GND	Analog input (1.6Vrms)
CD-R	I	20	CD audio Right channel	Analog input (1.6Vrms)
MIC1	IO	21	First Mic input/CEN-OUT/ Universal Jack3 left channel	Analog input (1.6Vrms)/Analog output (1Vrms)
MIC2	IO	22	Second Mic input/LFE-OUT/ Universal Jack3 right channel	Analog input (1.6Vrms)/Analog output (1Vrms)
LINE-L	IO	23	Line-In Left channel/S-OUT-L/ Universal Jack1 channel	Analog input (1.6Vrms)/Analog output (1Vrms)
LINE-R	IO	24	Line-In Right channel/S-OUT-R/ Universal Jack1 right channel	Analog input (1.6Vrms)/Analog output (1Vrms)
FRONT-MIC1	I	34	Dedicated Front MIC input	Analog input (1.6Vrms)
FRONT-MIC2	I	32	Dedicated Front MIC input	Analog input (1.6Vrms)
FRONT-OUT-L	O	35	Front output Left channel/ Universal Jack2 left channel	Analog output with amplifier
FRONT-OUT-R	O	36	Front output Right channel/ Universal Jack2 right channel	Analog output with amplifier
MONO-OUT/ VREFOUT3	O	37	Line-Out mixed mono output/ Third ref. Voltage out	Analog output
SURR-OUT-L	O	39	Surround Out Left channel	Analog output
SURR-OUT-R	O	41	Surround Out Right channel	Analog output
CEN-OUT	O	43	Center Out channel	Analog output
LFE-OUT	O	44	Low Frequency Effect Out channel	Analog output
GPIO0/JD0	IO	45	General purpose IO0/ Jack Detect 0	Internally pulled high (5V) to AVDD by a 100K resistor. Trigger point of high is at 4V
GPIO1/JD1	IO	17	General purpose IO1/ Jack Detect 1	Internally pulled high (5V) to AVDD by a 100K resistor. Trigger point of high is at 4V
JD2	I	16	Jack Detect 2	Internally pulled high (5V) to AVDD by a 100K resistor. Trigger point of high is at 4V
JD3	I	40	Jack Detect 3	Internally pulled high (5V) to AVDD by a 100K resistor. Trigger point of high is at 4V
JD4	I	31	Jack Detect 4	Internally pulled high (5V) to AVDD by a 100K resistor. Trigger point of high is at 4V
				TOTAL: 25 Pins

### 6.3. Filter/Reference Pins

**Table 3. Filter/Reference Pins**

Name	Pin No	Type	Description	Characteristic Definition
VREF	-	27	Reference voltage	+4.7uf and 0.1uf cap to AVSS
VREFOUT	O	28	Ref. Voltage out with 5mA drive	Analog output (2.25V – 2.75V)
AFILT1	-	29	ADC anti-aliasing filter capacitor	1nf cap to AVSS
AFILT2	-	30	ADC anti-aliasing filter capacitor	1nf cap to AVSS
VREFOUT2	O	33	Secondary reference voltage out	Analog output (2.25V – 2.75V)
				TOTAL: 5 Pins

### 6.4. Power/Ground Pins

**Table 4. Power/Ground Pins**

Name	Pin No	Type	Description	Characteristic Definition
AVDD1	25	I	Analog VDD (5.0V)	Minimum value is 3.0V Maximum value is 5.5V
AVDD2	38	I	Analog VDD (5.0V)	Minimum value is 3.0V Maximum value is 5.5V
AVSS1	26	I	Analog GND	
AVSS2	42	I	Analog GND	
DVDD1	1	I	Digital VDD (3.3V)	Minimum value is 3.0V (DVdd-0.3) Maximum value is 3.6V (DVdd+0.3)
DVDD2	9	I	Digital VDD (3.3V)	Minimum value is 3.0V (DVdd-0.3) Maximum value is 3.6V (DVdd+0.3)
DVSS1	4	I	Digital GND	
DVSS2	7	I	Digital GND	
				TOTAL: 8 Pins

## 7. Register Descriptions

### 7.1. Mixer Registers

Accessing odd numbered registers, or reading unimplemented registers, will return a 0.

**Table 5. Mixer Registers**

Reg. (hex)	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
02h	Master Vol	Mute	X	X	ML4	ML3	ML2	ML1	ML0	Mute*	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Vol	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	BEEP Vol	Mute	X	X	F7	F6	F5	F4	F3	F2	F1	F0	PB3	PB2	PB1	PB0	X	8000h
0Ch	Phone Vol	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Vol	Mute	X	X	X	X	X	X	X	X	20dB	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Vol	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Vol	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
16h	Aux Vol	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Vol	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Sel	X	X	X	X	X	LRS2	LRS1	LRS0	X	X	X	X	X	RRS2	RRS1	RRS0	0000h
1Ch	Rec. Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG0	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
20h	General	X	X	X	X	X	X	MIX	MS	LBK	X	X	X	X	X	X	X	0000h
24h	Audio Int. & Paging	14	I3	I2	I1	I0	X	X	X	X	X	X	X	PG3	PG2	PG1	PG0	0000h
26h	Power Down	EAPD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended	0	0	X	X	REV1	REV0	0	LDAC	SDAC	CDAC	X	X	X	SPDIF	X	VRA	09C4h
2Ah	Extended Status	X	PRL	PRK	PRJ	PRI	SPCV	SBDA C	LDAC	SDAC	CDAC	SPSA 1	SPSA 0	X	SPDIF	X	VRA	0040h
2Ch	PCM Out Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
2Eh	PCM Out Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
30h	PCM Out Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
32h	PCM In Rate	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	BB80h
36h	Center/LFE Volume	Mute	X	X	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	X	X	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Surround Volume	Mute	X	X	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	X	X	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	S/PDIF Ctl	V	0	SPSR 1	SPSR 0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	AUDIO	PRO	2000h
64h	Surr. DAC Volume	Mute	X	X	LSD4	LSD3	LSD2	LSD1	LSD0	X	X	X	RSD4	RSD3	RSD2	RSD1	RSD0	0808h
66h	CEN/LFE DAC Volume	Mute	X	X	LD4	LD3	LD2	LD1	LD0	X	X	X	CD4	CD3	CD2	CD1	CD0	0808h
6Ah	Multi-channel Ctl	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
7Ah	Extension Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	60A2h
7Ch	Vendor ID1	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	414Ch
7Eh	Vendor ID2	0	1	0	0	0	1	1	1	0	1	1	0	0	0	0	0	4760h

X = Reserved bit

\*: MX36 is the master volume control of CENTER/LFE output.

MX38 is the master volume control of surround output.



### 7.1.1. MX00 Reset

**Default: 0000H**

Writing any value to this register will start a register reset and causes all of the registers to revert to their default values. Reading this register returns the ID code of the specific part.

**Table 6. MX00 Reset**

Bit	Type	Function
15	R	Read as 0
14:10	R	Return 00000b (No 3D Stereo Enhancement)
9	R	Read as 0 (Not 20-bit ADC)
8	R	Read as 0 (Not 18-bit ADC)
7	R	Read as 0 (Not 20-bit DAC)
6	R	Read as 0 (Not 18-bit DAC)
5	R	Read as 0 (No Loudness)
4	R	Read as 0 (No True Line Level output)
3	R	Read as 0 (No simulated stereo for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	Read as 0 (No Modem Line support)

*Note: Writing any data into this register will reset all mixer registers to their default value. The written data is ignored.*

### 7.1.2. MX02 (Front) Master Volume

**Default: 8000H**

These registers control the volume level of Front-Out. Each step on the left and right channels corresponds to a 1.5dB increase/decrease in volume.

**Table 7. MX02 (Front) Master Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
12:8	R/W	Master Left Volume (ML[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	Master Right Volume (MR[4:0]) in 1.5dB steps

*For 00h 0dB attenuation*  
*MR/ML 1Fh 46.5dB attenuation*

### 7.1.3. MX06 Mono-Out Volume

**Default: 8000H**

These registers control the volume level of Mono-Out. Each step on the left and right channels corresponds to a 1.5dB increase/decrease in volume.

**Table 8. MX06 Mono-Out Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
4:0	R/W	Mono Master Volume (MM[4:0]) in 1.5dB steps

For 00h 0dB attenuation  
MR/ML: 1Fh 46.5dB attenuation

### 7.1.4. MX0A PC BEEP Volume

**Default: 0000H**

This register controls the input volume for the PC beep signal. Each step in bits 4:1 corresponds to a 3dB increase/decrease in volume. Sixteen levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the ALC850(D), eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the Front-Out. If the PC speaker/buzzer is eliminated it is recommended to connect the external speakers at all times so that the POST codes can be heard during reset.

**Table 9. MX0A PC BEEP Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13		Reserved
12:5	R/W	Internal PCBEEP Frequency, F[7:0] The internal PCBEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255*4)=47Hz. The highest tone is 48kHz/(1*4)=12kHz. A value of 00h in F[7:0] disables internal PCBEEP generator and allows external PCBEEP input
4:1	R/W	PC Beep Volume (PBV[3:0]) in 3dB steps
0		Reserved

For PB 00h 0dB attenuation  
0Fh 45dB attenuation



### 7.1.5. MX0C PHONE Volume

**Default: 8008H**

Register 0CH controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the codec can offer a speaker-out service. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

**Table 10. MX0C PHONE Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:5	-	Reserved
4:0	R/W	Phone Volume (PV[4:0]) in 1.5dB steps

For PV    00h    +12dB Gain  
          08h    0dB attenuation  
          1Fh    -34.5dB Gain

### 7.1.6. MX0E MIC Volume

**Default: 8008H**

Register 0EH controls the microphone input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Each step in bit 6 corresponds to a 20dB increase in volume.

**Table 11. MX0E MIC Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:7	-	Reserved
6	R/W	20dB Boost Control 0: Normal 1: 20dB boost
5	-	Reserved
4:0	R/W	Mic Volume (MV[4:0]) in 1.5dB steps

For MV    00h    +12dB Gain  
          08h    0dB attenuation  
          1Fh    -34.5dB Gain

### 7.1.7. MX10 LINE\_IN Volume

**Default: 8808H**

Register 10H controls the LINE\_IN input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

**Table 12. MX10 LINE\_IN Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
12:8	R/W	Line-In Left Volume (NL[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	Line-In Right Volume (NR[4:0]) in 1.5dB steps

*For*      00h    +12dB Gain  
*NL/NR*   08h    0dB attenuation  
            1Fh    -34.5dB Gain

### 7.1.8. MX12 CD Volume

**Default: 8808H**

Register 12H controls the CD input volume. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

**Table 13. MX12 CD Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
12:8	R/W	CD Left Volume (CL[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	CD Right Volume (CR[4:0]) in 1.5dB steps

*For*      00h    +12dB Gain  
*CL/CR*   08h    0dB attenuation  
            1Fh    -34.5dB Gain

### 7.1.9. MX16 AUX Input /Back-Surround Output Volume

**Default: 8808H**

Register 16H controls the volume of auxiliary input and back surround output. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

**Table 14. MX16 AUX Input /Back-Surround Output Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
12:8	R/W	AUX Left Volume (AL[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	AUX Right Volume (AR[4:0]) in 1.5dB steps

For 00h +12dB Gain  
 AL/AR 08h 0dB attenuation  
 1Fh -34.5dB Gain

### 7.1.10. MX18 PCM\_OUT Volume

**Default: 8808H**

Register 18H controls the PCM\_OUT output volume of front DAC. Each step in bits 4:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

**Table 15. MX18 PCM\_OUT Volume**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
12:8	R/W	PCM Left Volume (PL[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	PCM Right Volume (PR[4:0]) in 1.5dB steps

For 00h +12dB Gain  
 PL/PR 08h 0dB attenuation  
 1Fh -34.5dB Gain

### 7.1.11. MX1A Record Select

**Default: 0000H**

Register 1AH controls the record input volume. Each step in bits 2:0 corresponds to a 1.5dB increase/decrease in volume for the right channel, allowing 7 levels of volume, from 000 to 111. Each step in bits 10:8 corresponds to a 1.5dB increase/decrease in volume for the left channel, allowing 7 levels of volume, from 000 to 111.

**Table 16. MX1A Record Select**

Bit	Type	Function
15:11	-	Reserved
10:8	R/W	Left Record Source Select (LRS[2:0])
7:3	-	Reserved
2:0	R/W	Right Record Source Select (RRS[2:0])

*For LRS*

0	MIC
1	CD LEFT
2	Mute
3	AUX LEFT
4	LINE LEFT
5	STEREO MIXER OUTPUT LEFT
6	MONO MIXER OUTPUT
7	PHONE

*For RRS*

0	MIC
1	CD RIGHT
2	Mute
3	AUX RIGHT
4	LINE RIGHT
5	STEREO MIXER OUTPUT RIGHT
6	MONO MIXER OUTPUT
7	PHONE



### 7.1.12. MX1C Record Gain

**Default: 8000H**

Register 1CH controls the record gain. Each step in bits 3:0 corresponds to a 1.5dB increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 corresponds to a 1.5dB increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

**Table 17. MX1C Record Gain**

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:12	-	Reserved
11:8	R/W	Left Record Gain Select (LRG[3:0]) in 1.5dB steps
7:4	-	Reserved
3:0	R/W	Right Record Gain Select (RRG[3:0]) in 1.5dB steps

For 0Fh +22.5dB Gain  
 LRG/RRG 00h 0dB(No Gain)

### 7.1.13. MX20 General Purpose Register

**Default: 0000H**

This register is used to control several functions. Bit 13 enables or disables 3D control. Bit 9 allows selection of mono output. Bit 8 controls the MIC selector. Bit 7 enables loopback of the AD output to the DA input without involving the AC-Link, allowing for full system performance measurements.

**Table 18. MX20 General Purpose Register**

Bit	Type	Function
15:12	-	Reserved. Read as 0
11:10	R	DRSS[1:0], Double Rate Slot Select 01: PCM(n+1) data is on Slots 7/8 (Default) 00, 10, 11: Reserved
9	-	Reserved. Read as 0
8	R/W	MIC Select 0: MIC1 1: MIC2
7	R/W	AD to DA Loop-Back Control 0: Disable 1: Enable
6:0	-	Reserved

Note: Bit 7 enables ADC to front DAC loop-back.



### 7.1.14. MX24 Audio Interrupt and Paging

Default: 0000h

Table 19. MX24 Audio Interrupt and Paging

Bit	Type	Function
15		Interrupt Status, I4 0: Interrupt is clear 1: Interrupt was generated Interrupt event and status are clear by writing a 1 to this bit. The status will change regardless of interrupt enable (I0)
14	R	Interrupt Cause, I3 Reserved. Read as 0
13	R	Interrupt Cause, I2 I2=0: Sense value in page ID-01h MX6A[12:8] has not changed 1: Sense cycle completed or new sense value in page ID-01h MX6A[12:8] is available This bit reflects the cause of the first interrupt event generated. Software should read it after the interrupt status (I4) has been confirmed as interrupting. I2 will be zero when I4 is cleared
12	R/W	Sense Cycle, I1 0: Sense cycle not in progress 1: Sense cycle start Writing a '1' to this bit causes a sense cycle start. If a sense cycle is in progress, writing a '0' to this bit will abort the sense cycle Whether the data in the sense result register (page ID-01h MX6A) is valid or not is determined by the IV bit in MX6A, Page ID-1h
11	R/W	Interrupt Enable, I0 0: Interrupt is masked. Interrupt status (I4) will not be shown in bit 0 of Slot 12 in SDATA-IN 1: Interrupt is un-masked. Interrupt status (I4) will be shown in bit 0 of Slot 12 in SDATA-IN This bit controls the interrupt of the sense cycle
10:4	NA	Reserved. Read as 0
3:0	R/W	Page Selector, PG[3:0] 0000b: Vendor Specific 0001b: Page ID 01 (AC'97 2.3 Discovery Descriptor Definition) Others: Reserved This register is used to select a descriptor of 16 word pages between registers MX60 and MX6F. A value of 0 is used to select vendor specific space to maintain compatibility with the AC'97 2.2 vendor specific register. When PG[3:0] is not 0000b or 0001b, the ALC850(D) will return zero data for the ACLINK mixer read command



### 7.1.15. MX26 Power Down Control/Status

**Default: 0000H**

This read/write register is used to program power-down states and monitor subsystem readiness. The lower half of this register is read-only; a '1' indicating that the subsection is 'ready'. Ready is defined as the subsection's ability to perform in its nominal state. When the AC-Link 'Codec Ready' indicator bit (SDATA\_IN slot 0, bit 15) is 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this power down control/status register to determine exactly which subsections, if any, are ready.

**Table 20. MX26 Power Down Control/Status**

Bit	Type	Function
15	R/W	PR7 External Amplifier Power Down (EAPD) 0: EAPD output low (enable external amplifier) 1: EAPD output high (shut down external amplifier)
14	-	Reserved
13	R/W	PR5 0: Normal 1: Disable internal clock usage (BCLK remains output for modem codec)
12	R/W	PR4 0: Normal 1: Power down AC-Link
11	R/W	PR3 0: Normal 1: Power down Mixer (Vref off)
10	R/W	PR2 0: Normal 1: Power down Mixer (Vref still on)
9	R/W	PR1 0: Normal 1: Power down PCM DAC (front DAC)
8	R/W	PR0 0: Normal 1: Power down PCM ADCs and input MUX
7:4	-	Reserved. Read as 0
3	R	Vref Status 1: Vref is up to normal level 0: Not yet
2	R	Analog Mixer Status 1: Ready 0: Not yet
1	R	DAC Status 1: Ready 0: Not yet
0	R	ADC Status 1: Ready 0: Not yet

### 7.1.16. MX28 Extended Audio ID

**Default: 09C4H**

The Extended Audio ID register is a read-only register used to communicate information to the digital controller.

**Table 21. MX28 Extended Audio ID**

Bit	Type	Function
15:14	R	ID[1:0]. Always read as 0 (Only primary ID is supported)
13:12	-	Reserved. Read as 0
11:10	R	REV [1:0]=10 to indicate that the ALC850(D) is AC'97 rev. 2.3 compliant
9	R	AMAP. Read as 0
8	R	LDAC. Read as 1 (LFE DAC is supported, in compliance with AC'97 rev. 2.3)
7	R	SDAC. Read as 1 (Surround DAC is supported, in compliance with AC'97 rev. 2.3)
6	R	CDAC. Read as 1 (Center DAC is supported, in compliance with AC'97 rev. 2.3)
5:3	-	Reserved. Read as 0
2	R	S/PDIF. Read as 1 (S/PDIF output is supported)
1	R	DRA. Read as 0 (Double Rate Audio is not supported)
0	R	VRA. Read as 0 (Variable Rate Audio is not supported)

### 7.1.17. MX2A Extended Audio Status and Control Register

**Default: 05F0H**

This register contains two active bits for power-down and status of the surrounding DACs. Bits 1 & 2 are read/write bits that are used to enable or disable DRA and S/PDIF respectively. Bits 4 & 5 are read/write bits used to determine the AC-LINK slot assignment of the S/PDIF. Bits 6, 7, & 8 are read-only bits that tell the controller when the Center, Surround, and LFE DACs are ready to receive data. Bit 10 is a read-only bit that tells the controller if the S/PDIF configuration is valid. Bits 11, 12, & 13 are read/write bits that are used to power down the Center, Surround, and LFE DACs respectively.

**Table 22. MX2A Extended Audio Status and Control Register**

Bit	Type	Function
15	R/W	Validity Configuration of S/PDIF Output (VCFG) Combines with MX3A.15 to decide validity control in S/PDIF output signal
14	-	Reserved
13	R/W	Power Down LFE DAC (PRK) 0: Normal 1: Power down LFE DAC
12	R/W	Power Down Surround DAC (PRJ) 0: Normal 1: Power down Surround DAC
11	R/W	Power Down Center DAC (PRI) 0: Normal 1: Power down Center DAC
10	R	SPCV (S/PDIF Configuration Valid) 0: Current S/PDIF configuration (SPSA, SPSR, DAC/slot rate) is not valid 1: Current S/PDIF configuration (SPSA, SPSR, DAC/slot rate) is valid

Bit	Type	Function
9	-	Reserved
8	R	LFE DAC Status (LDAC) 0: Not yet 1: Ready
7	R	Surround DAC Status (SDAC) 0: Not yet 1: Ready
6	R	Center DAC Status (CDAC) 0: Not yet 1: Ready
5:4	R/W	S/PDIF-Out Slot Assignment (SPSA[1:0]) 00: S/PDIF-Out source is from AC-LINK slot 3/4 01: S/PDIF-Out source is from AC-LINK slot 7/8 10: S/PDIF-Out source is from AC-LINK slot 6/9 11: S/PDIF-Out source is from AC-LINK slot 10/11 (Default)
3	-	Reserved
2	R/W	S/PDIF Enable 1: Enable 0: Disable (Hi-Z)
1	R/W	DRA Enable 1: Enable 0: Disable
0	R/W	VRA Enable 1: Enable 0: Disable

Note: SPCV is a read-only bit that indicates whether the current S/PDIF-Out configuration is supported or not. If the configuration is supported, SPCV is set as 1 by H/W. The driver can check this bit to determine the status of the S/PDIF transmitter system. SPCV is always operating, independent of the S/PDIF enable bit (MX2A.2). The S/PDIF output is active if MX2A.2 is set, in spite of SPCV. If S/PDIF output is enabled, but SPCV is invalid (SPCV=0), channel status is still output, but the output data bits will be all zeros. The condition that allows S/PDIF output is S/PDIF(MX2A.2)=1 & SPACV=1, otherwise S/PDIF output will be all zeros when MX2A.2=1 and SPACV=0 (invalid).

### 7.1.18. MX2C PCM Front/Center Output Sample Rate

Default: BB80H

Table 23. MX2C PCM Front/Center Output Sample Rate

Bit	Type	Function
15:0	R	Front/Center Output Sample Rate (FOSR)

### 7.1.19. MX2E PCM Surround Output Sample Rate

Default: BB80H

Table 24. MX2E PCM Surround Output Sample Rate

Bit	Type	Function
15:0	R	Surround Output Sample Rate (SOSR)

### 7.1.20. MX30 PCM LFE Output Sample Rate

Default: BB80H

Table 25. MX30 PCM LFE Output Sample Rate

Bit	Type	Function
15:0	R	LFE Output Sample Rate (LOSR)

### 7.1.21. MX32 PCM Input Sample Rate

Default: BB80H

Table 26. MX32 PCM Input Sample Rate

Bit	Type	Function
15:0	R/W	ADC Input Sample Rate (AISR)

### 7.1.22. MX36 LFE/Center Master Volume

Default: 8080H

Table 27. MX36 LFE/Center Master Volume

Bit	Type	Function
15	R/W	LFE Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14	-	Reserved
13:8	R/W	LFE Master Volume (LFE[5:0]) in 1.5dB steps
7	R/W	Center Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
6	-	Reserved
5:0	R/W	Center Master Volume (CNT[5:0]) in 1.5dB steps

For LFE/CEN      00h      0dB  
                   3Fh      94.5dB attenuation

### 7.1.23. MX38 Surround Master Volume

Default: 8080H

**Table 28. MX38 Surround Master Volume**

Bit	Type	Function
15	R/W	Left Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14	-	Reserved
13:8	R/W	Surround Master Left Volume (LSR[5:0]) in 1.5dB steps
7	R/W	Right Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
6	-	Reserved
5:0	R/W	Surround Master Right Volume (RSR[5:0]) in 1.5dB steps

For 00h 0dB  
LSR/RSR 3Fh 94.5dB attenuation

### 7.1.24. MX3A S/PDIF Output Channel Status and Control

Default: 2000H

**Table 29. MX3A S/PDIF Output Channel Status and Control**

Bit	Type	Function
15	R/W	Validity Control (control V bit in Sub-Frame) 0: The V bit (valid flag) in the sub-frame depends on whether or not the S/PDIF FIFO has under-run 1: The V bit in the sub-frame is always sent as 1 to indicate the data is invalid
14		Reserved
13:12	R	S/PDIF Out Sample Rate (SPSR[1:0]) 00, 01, 11: Reserved 10: Sample rate is 48.0kHz, Fs[0:3]=0100 (default)
11	R/W	Generation Level (LEVEL)
10:4	R/W	Category Code (CC [6:0])
3	R/W	Pre-Emphasis (PRE) 0: None 1: Filter pre-emphasis is 50/15 $\mu$ sec
2	R/W	Copyright (COPY) 0: Asserted 1: Not asserted
1	R/W	Non-Audio Data type (/AUDIO) 0: PCM data 1: AC3 or other digital non-audio data
0	R	Professional or Consumer format (PRO) 0: Consumer format 1: Professional format The ALC850(D) only supports consumer channel status format. This bit is always 0

To ensure that control and status information is sent at the beginning of S/PDIF transmission (starting at bit31), MX3A.[14:0] should only be written to when the S/PDIF transmitter is disabled (MX2A.2=0). If validity control is set (MX3A.15=1), the data bits (bit8 ~ bit27) should be forced to 0 to get better compatibility with mini discs.

**Table 30. S/PDIF Channel Status**

<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>
PRO=0	/AUDIO	COPY	PRE	0	0	0	0
<b>8</b>	<b>9</b>	<b>10</b>	<b>11</b>	<b>12</b>	<b>13</b>	<b>14</b>	<b>15</b>
CC0	CC1	CC2	CC3	CC4	CC5	CC6	LEVEL
<b>16</b>	<b>17</b>	<b>18</b>	<b>19</b>	<b>20</b>	<b>21</b>	<b>22</b>	<b>23</b>
0	0	0	0	0	0	0	0
<b>24</b>	<b>25</b>	<b>26</b>	<b>27</b>	<b>28</b>	<b>29</b>	<b>30</b>	<b>31</b>
Fs0	Fs1	Fs2	Fs3	0	0	0	0

The 'V' bit in the sub-frame is determined by Validity control (MX3A.15) and VCFG (MX2A.15):

**Table 31. S/PDIF Validity Control**

<b>Validity</b>	<b>VCFG</b>	<b>Operation</b>
0	0	If S/PDIF FIFO is under-run, the 'V' bit in the sub-frame is set to indicate that the S/PDIF data is invalid
0	1	If S/PDIF FIFO is under-run, the 'V' bit in the sub-frame is always 0, and pads the data with zeros
1	0	The 'V' bit is always 1, and data bits (bit 8 ~ bit 27) should be forced to 0
1	1	The 'V' bit in the sub-frame is always '0', and the S/PDIF output data should be forced to 0

## 7.2. Vendor Defined Registers (Page ID-00h)

These registers are available to Realtek customers for specialized functions.

### 7.2.1. MX60 S/PDIF Input Channel Status [15:0]

**Default: 0000h**

The data in MX60 are captured from the channel status [15:0] of the S/PDIF-IN signal.

**Table 32. MX60 S/PDIF Input Channel Status [15:0]**

Bit	Type	Function
15	R	Generation Level (LEVEL)
14:8	R	Category Code (CC[6:0])
7:6	R	Mode[1:0]
5:3	R	Pre-Emphasis (PRE[2:0])
2	R	Copyright (COPY) 0: Asserted 1: Not Asserted
1	R	Non-Audio Data type (/AUDIO) 0: PCM data 1: AC3 or other digital non-audio data
0	R	Professional or Consumer Format (PRO) 0: Consumer Format 1: Professional Format The ALC850(D) only supports consumer channel status format. This bit is always 0

### 7.2.2. MX62 S/PDIF Input Channel Status [29:15]

**Default: 0000h**

The data in MX62 are captured from the channel status [29:16] of the S/PDIF-IN signal.

**Table 33. MX62 S/PDIF Input Channel Status [29:15]**

Bit	Type	Function
15	R	'V' bit in sub-frame of S/PDIFI, S/PDIFI_V 0: Data X and Y are valid 1: At least one of data X and Y is invalid This bit is real-time updated. It indicates that the ALC850(D) is ready to receive S/PDIF-IN data
14	R	S/PDIF-IN Input Signal Locked by hardware, S/PDIFI_LOCK 0: Unlocked 1: Locked
13:12	R	Clock Accuracy (Ca[1:0])
11:8	R	Sample Frequency in channel status (Fs[3:0]) 0000: 44.1kHz 0010: 48kHz 0011: 32kHz Others: Reserved
7:4	R	Channel Number (Cn[3:0])
3:0	R	Source Number (Sn[3:0])

*Note: Bits [13:0] are captured from the channel status [29:16] of S/PDIFI. The data from S/PDIF input is forced to 0 if the S/PDIF input signal is unlocked. Software must check this 'LOCK' bit before dealing with S/PDIF input operations.*



### 7.2.3. MX64 Surround DAC Volume

Default: 0808H (Unmuted)

Table 34. MX64 Surround DAC Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
12:8	R/W	Surround DAC Left Volume (SDL[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	Surround DAC Right Volume (SDR[4:0]) in 1.5dB steps

For 00h +12dB Gain  
 SDL/SDR 08h 0dB Gain  
 1Fh -34.5dB Gain

### 7.2.4. MX66 Center/LFE DAC Volume

Default: 0808H (Unmuted)

Table 35. MX66 Center/LFE DAC Volume

Bit	Type	Function
15	R/W	Mute Control 0: Normal 1: Mute ( $-\infty$ dB)
14:13	-	Reserved
12:8	R/W	LFE DAC Volume (LD[4:0]) in 1.5dB steps
7:5	-	Reserved
4:0	R/W	Center DAC Volume (CD[4:0]) in 1.5dB steps

For 00h +12dB Gain  
 LD/CD 08h 0dB Gain  
 1Fh -34.5dB Gain



### 7.2.5. MX6A Data Flow Control

This register is used to control various parts of the ALC850(D) multi-channel functions.

**Default: 0000h**

**Table 36. MX6A Data Flow Control**

Bit	Type	Function
15	RW	SPDIF Input Enable 0: Disable (Default) 1: Enable
14	R/W	SPDIF-In Monitoring Control 0: Disable. SPDIFI data is not added into PCM data to DAC (Default) 1: Enable. MSB 16-bit of SPDIFI data will be added into PCM data to DAC if SPDIFI is locked
13:12	R/W	S/PDIF Output Source 00: S/PDIF output data is from ACLINK (default) 01: S/PDIF output data is from ADC 10: Directly bypass S/PDIF-In signal to S/PDIF-Out 11: Reserved
11	R/W	PCM Data to AC-LINK 0: PCM Data are from ADC (default) 1: PCM Data are from S/PDIF input
10	R/W	AUX IN/Back Surround Output Control 0: Pin 14 is AUX-IN-L, pin-15 is AUX-IN-R (default) 1: Pin 14 is Back-Surround-Out-L, pin-15 is Back-Surround-Out-R
9	R/W	Analog Input Pass to Back Surround Control 0: Off (default) 1: On
8	R/W	Front-MIC/Mono-Out Control 0: Pin 37 is analog input (Front Microphone In) (default) 1: Pin 37 is duplicated output of Mono-Out
7:6		Reserved
5	R/W	Analog Input Pass to Center/LFE Control 0: Off (default) 1: On
4	R/W	Analog Input Pass to Surround Control 0: Off (default) 1: On
3:1		Reserved
0	R/W	Surround Output Source 0: S-OUT is the real surround output (default) 1: S-OUT is the duplicated output of LINE-OUT

### 7.3. Discovery Descriptor (Page ID-01h)

These registers are defined in AC'97 2.3 for sensing and analog plug and play functions.

#### 7.3.1. MX62 PCI Sub System ID

**Default: FFFFh**

**Table 37. MX62 PCI Sub System ID**

Bit	Type	Function
15:0	R/W	PCI Sub System Vendor ID This register can be written once only after power on, and is not affected by an AC'97 cold reset. The system manufacture's BIOS can set its own sub-system ID The default value 'FFFFh' means this register is implemented and data is not set by the BIOS

#### 7.3.2. MX64 PCI Sub Vendor ID

**Default: FFFFh**

**Table 38. MX64 PCI Sub Vendor ID**

Bit	Type	Function
15:0	R/W	PCI Vendor ID This register can be written once only after power on, and is not affected by an AC'97 cold reset. The system manufacture's BIOS can set its own sub-vendor ID The default value 'FFFFh' means this register is implemented and data is not set by the BIOS

#### 7.3.3. MX66 Sense Function Select

**Default: 0000h**

**Table 39. MX66 Sense Function Select**

Bit	Type	Function
15:5		Reserved
4:1	R/W	Function Code bits (FC[3:0]) These bits specify the type of audio function described in page ID 01h MX66, MX68, and MX6A. 0h: FRONT-OUT (pin-35/36) 1h: SURR-OUT (pin-39/41) 2h: CEN/LFE-Out (pin-43/44) 5h: MIC1 In (pin-21) 6h: MIC2 In (pin-22) 7h: LINE In (pin-23/24) Others: Reserved
0	R/W	Tip or Ring Selection (T/R) This bit sets which jack conductor the sense value is measured from. It is combined with FC[3:0] 0: Tip (Left channel) 1: Ring (Right channel)

### 7.3.4. MX68 Sense Function Information

Default: 0011h

**Table 40. MX68 Sense Function Information**

Bit	Type	Function
15:5	-	Reserved
4	R/W	Information Valid bit, IV 0: After a sense cycle is completed, indicates that no information is provided on the sensing method 1: After a sense cycle is completed, indicates that information is provided on the sensing method Clear this bit by writing '1'. Writing '0' to this bit has no effect
3:1	NA	Reserved
0	R	Function Information Present (FIP) When this bit is set to '0', indicates that the G[4:0], INV, DL[4:0] and ST[2:0] bits are not supported

### 7.3.5. MX6A Sense Detail

Default: 0000h

**Table 41. MX6A Sense Detail**

Bit	Type	Function
15:13	-	Reserved
12:8	R	Sense bits, S[4:0] (Default value depends on sensed result after Cold Reset) For output devices: (FC[3:0]= 0h, 1h, or 2h) 02h: Not specified or unknown 05h: Powered speaker 06h: Earphone or passive speaker Other: Not supported  For input devices: (FC[3:0]= 5h, 6h, or 7h) 12h: Not specified or unknown 13h: Mono Microphone 15h: Stereo Line-In Other: Not supported This field reports the type of output/input peripheral plugged into the jack after sensing
7:0	R	Always read as 0

## 7.4. Extension Registers

### 7.4.1. MX76 GPIO & Interrupt Control

Default: 0000h

**Table 42. MX76 GPIO & Interrupt Control**

Bit	Type	Function
15	R/W	Mute Control of Front-MIC1/2 0: Normal 1: Mute (Default)
14:12	R/W	Pin-23/24 UIO2 Function Selection 000: LINE IN-L/R (Default) 001: MIC1/MIC2 010: Surr 011: Detection circuit 100: NC (Floating)
11	R/W	Vrefout3 Disable 0: Vrefout3 is driven by the internal reference 1: Vrefout3 is in high-Z mode (Default)
10:8	R/W	Pin-35/36 UIO1 Function Selection 000: LINE IN-L/R 001: MIC1/MIC2 010: FRONT-OUT (Default) 011: Detection circuit 100: NC (Floating)
7	R/W	Vrefout2 Disable 0: Vrefout2 is driven by the internal reference 1: Vrefout2 is in high-Z mode (Default)
6:4	R/W	Pin-21/22 UIO3 Function Selection 000: LINE IN-L/R 001: MIC1/MIC2 (Default) 010: Surr 011: Detection circuit 100: NC (Floating) 101: Cen/LFE
3:2	R/W	Impedance Detect for Pad 23/24 (FO-control 2, 3, and 4) 01: Via 100ohm path 10: Via 2.2K path 11: Via 47K path 00: All path Floating (Default) Software must turn on Surround AMP and turn off SURR-OUT control before detecting
1:0	R/W	Impedance Detect for Pad 21/22 (FO-control 2, 3, and 4) 01: Via 100ohm path 10: Via 2.2K path 11: Via 47K path 00: All path Floating (Default) Software must turn on Surround AMP and turn off SURR-OUT control before detecting



## 7.4.2. MX78 GPIO & Interrupt Status

Default: 0000h

**Table 43. MX78 GPIO & Interrupt Status**

Bit	Type	Function
15:13		Reserved
12	R	JD5 Input Status 0: JD4 is driven low by external device (input) 1: JD4 is driven high by external device (input) Digital design need to tie the original control signal to low
11	R	JD4 Input Status 0: JD4 is driven low by external device (input) 1: JD4 is driven high by external device (input)
10	R	JD3 Input Status. 0: JD3 is driven low by external device (input) 1: JD3 is driven high by external device (input)
9	R/W	GPIO1 Primitiveness Control 0: Set GPIO1(JD1) as input pin 1: Set GPIO1(JD1) as output pin
8	R/W	GPIO0 Primitiveness Control 0: Set GPIO0(JD0) as input pin 1: Set GPIO0(JD0) as output pin
7	R/W	Pin 13 Function Selection 0: Phone In 1: Enable JD5 (default) If JD5 is enabled, recording from phone input is forbidden by software
6:4		Reserved
3	R/W	Pin 47 Function Selection 0: EAPD 1: SPDIF Input (Default)
2	R	JD2 Input Status 0: JD2 is driven low by external device (input) 1: JD2 is driven high by external device (input)
1	R/W	GPIO1(JD1) Input/Output Status 0: GPIO1 is driven low by/to external device 1: GPIO1 is driven high by/to external device
0	R/W	GPIO0(JD0) Input/Output Status 0: GPIO0 is driven low by/to external device 1: GPIO0 is driven high by/to external device



### 7.4.3. MX7A Miscellaneous Control

Default: 2092H

Table 44. MX7A Miscellaneous Control

Bit	Type	Function
15		Reserved
14	R/W	MIX Control 0: Add MIX and front DAC output (Default) 1: Turn off MIX, only DAC output
13	R/W	CEN/LFE-OUT 1K $\Omega$ Control (C/LF-Control) 0: 1K $\Omega$ path at pin 43 and 44 are off 1: 1K $\Omega$ path at pin 43 and 44 are on (Default)
12	R/W	Vrefout Disable 0: Vrefout is driven by the internal reference (Default) 1: Vrefout is in high-Z mode Software must set this bit to disable Vrefout output before MIC1 and MIC2 are shared as Center and LFE output
11:8		Reserved
7	R/W	FRONT-OUT Amplifier Control (FO-Control) 0: Amplifier at pin 35 and 36 are high impedance (Off) 1: Amplifier at pin 35 and 36 are turned on (Default)
6	R/W	FRONT-OUT 1K $\Omega$ Control (Front-Control) 0: 1K $\Omega$ path at pin 35 and 36 are off (Default) 1: 1K $\Omega$ path at pin 35 and 36 are on
5	R/W	SURR Amplifier Control (SO-Control) 0: Amplifier at pin 39 and 41 are high impedance (Off) (Default) 1: Amplifier at pin 39 and 41 are turned on
4	R/W	SURR-OUT 1K $\Omega$ Control (SURR-Control) 0: 1K $\Omega$ path at pin 39 and 41 are off 1: 1K $\Omega$ path at pin 39 and 41 are on (Default)
3:2		Reserved
1	R/W	SURR-OUT control 0: Off 1: On (Default)
0		Reserved

#### 7.4.4. MX7C Vendor ID1

The two registers (MX7C Vendor ID1 and MX7E Vendor ID2) contain four 8-bit ID codes. The first three codes have been assigned by Microsoft for Plug and Play definitions. The fourth code is a Realtek assigned code identifying the ALC850(D). The MX7C Vendor ID1 register contains the value 414Ch, which is the first and second characters of the Microsoft ID code. The MX7C Vendor ID2 register contains the value 4790h, which is the third character of the Microsoft ID code.

**Default: 414CH**

**Table 45. MX7C Vendor ID1**

Bit	Type	Function
15:0	R	Vendor ID - 'AL'

#### 7.4.5. MX7E Vendor ID2

**Default: 4790H**

**Table 46. MX7E Vendor ID2**

Bit	Type	Function
15:8	R	Vendor ID - 'G'
7:4	R	Chip ID - 1001b (ALC850(D))
3:0	R	Version number - 0000b

## 8. Electrical Characteristics

### 8.1. DC Characteristics

#### 8.1.1. Absolute Maximum Ratings

**Table 47. Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies:					
Digital	DVDD	3.0	3.3	3.6	V
Analog	AVDD	3.0	5.0	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts			+125	°C
<b>ESD (Electrostatic Discharge)</b>					
Susceptibility Voltage					
3000V					

#### 8.1.2. Threshold Voltage

DVDD= 3.3V±5%, T<sub>ambient</sub>=25 °C, with 50pF external load.

**Table 48. Threshold Voltage**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V <sub>in</sub>	-0.30	-	Dvdd+0.30	V
Low Level Input Voltage (SYNC, SDATA_OUT, RESET#)	V <sub>IL</sub>	-		0.5DVDD	V
Low Level Input Voltage (XTAL_IN,BIT_CLK)	V <sub>IL</sub>	-		0.5DVDD	V
Low Level Input Voltage (JDs, GPIOs)	V <sub>IL</sub>	-		2.0	V
High Level Input Voltage (SYNC, SDATA_OUT, RESET#)	V <sub>IH</sub>	0.5DVDD		-	V
High Level Input Voltage (XTAL_IN,BIT_CLK)	V <sub>IH</sub>	0.5DVDD		-	V
High Level Input Voltage (JDs, GPIOs)	V <sub>IH</sub>	2.0		-	V
High Level Output Voltage	V <sub>OH</sub>	0.9DVDD		-	V
Low Level Output Voltage	V <sub>OL</sub>	-	-	0.1DVDD	V
Input Leakage Current	-	-10	-	10	μA
Output Leakage Current (Hi-Z)	-	-10	-	10	μA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull up Resistance	-		100k	130k	Ω



### 8.1.3. Digital Filter Characteristics

**Table 49. Digital Filter Characteristics**

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	19.2	kHz
	Stopband	28.8			kHz
	Stopband Rejection		-76.0		dB
	Passband Frequency Response		+/- 0.20		dB

### 8.1.4. S/PDIF Output Characteristics

Dvdd= 3.3V, T<sub>ambient</sub>=25<sup>0</sup>C, with 75Ω external load.

**Table 50. S/PDIF Output Characteristics**

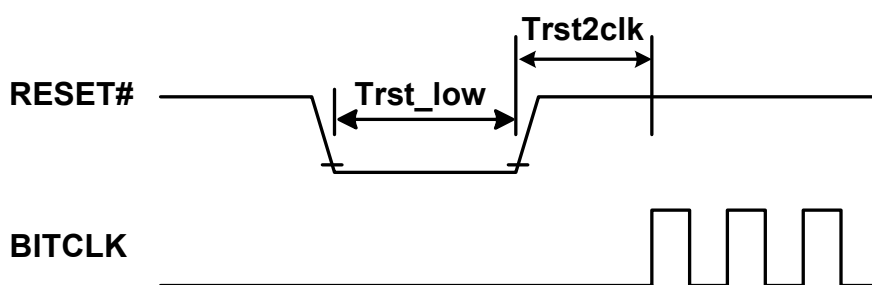
Parameter	Symbol	Minimum	Typical	Maximum	Units
High Level Output Voltage	V <sub>OH</sub>	3.0	3.3		V
Low Level Output Voltage	V <sub>OL</sub>	-	0	0.5	V

## 8.2. AC Timing Characteristics

### 8.2.1. Cold Reset

**Table 51. Cold Reset**

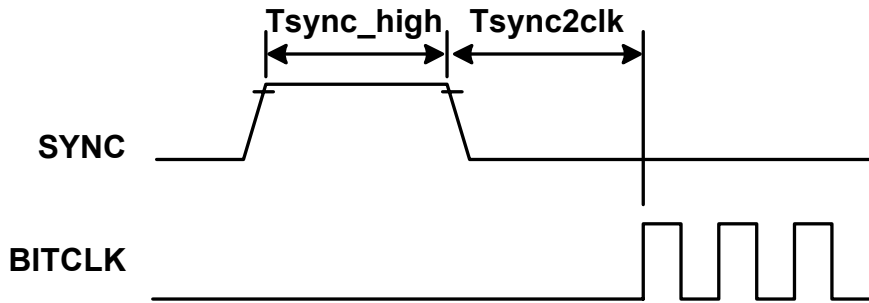
Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse width	T <sub>rst_low</sub>	1.0	-	-	μs
RESET# Inactive to BIT_CLK Startup Delay	T <sub>rst2clk</sub>	162.8	-	-	ns


**Figure 3. Cold Reset Timing**

### 8.2.2. Warm Reset

**Table 52. Warm Reset**

Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC Active High Pulse Width	$T_{sync\_high}$	1.0	-	-	$\mu$ s
SYNC Inactive to BIT_CLK Startup Delay	$T_{sync2clk}$	162.8	-	-	ns


**Figure 4. Warm Reset Timing**

### 8.2.3. AC-Link Clocks

**Table 53. AC-Link Clocks**

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK Frequency		-	12.288	-	MHz
BIT_CLK Period	$T_{clk\_period}$	-	81.4	-	ns
BIT_CLK Output Jitter		-	-	750	ps
BIT_CLK High Pulse Width	$T_{clk\_high}$		40.7		ns
BIT_CLK Low Pulse Width	$T_{clk\_low}$		40.7		ns
SYNC Frequency		-	48.0	-	kHz
SYNC Period	$T_{sync\_period}$	-	20.8	-	$\mu$ s
SYNC High Pulse Width	$T_{sync\_high}$	-	1.3	-	$\mu$ s
SYNC Low Pulse Width	$T_{sync\_low}$	-	19.5	-	$\mu$ s

## 8.2.4. Data Output and Input Timing

**Table 54. Data Output and Input Timing**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Valid Delay from rising edge of BIT_CLK	$t_{co}$	-	-	15	ns

Note 1: Timing is for SDATA and SYNC outputs with respect to BIT\_CLK at the device driving the output.

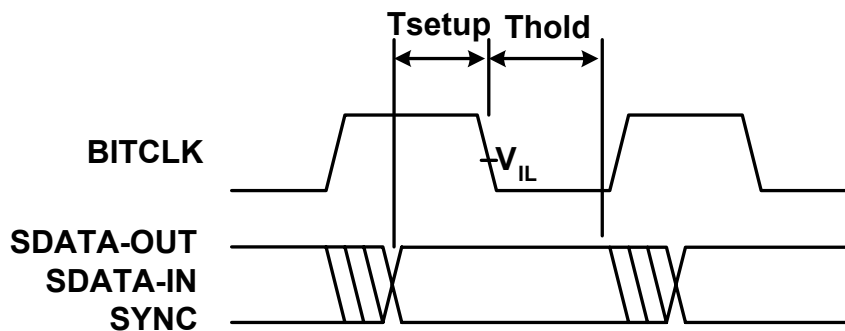
Note 2: 50pF external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	$t_{setup}$	10	-	-	ns
Input Hold from falling edge of BIT_CLK	$t_{hold}$	10	-	-	ns

Note: Timing is for SDATA and SYNC outputs with respect to BIT\_CLK at the device driving the output.

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns

Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.


**Figure 5. Data Output and Input Timing**

### 8.2.5. Signal Rise and Fall Timing

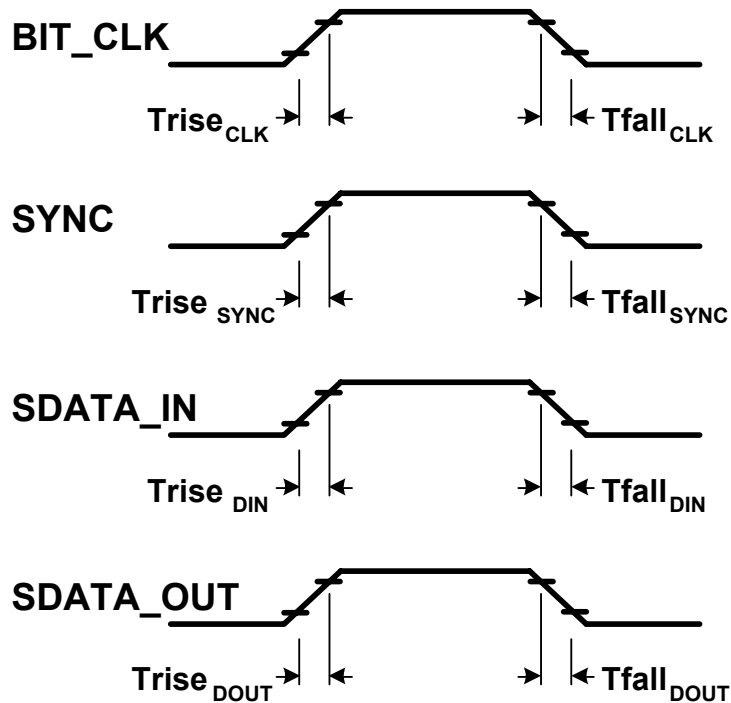
**Table 55. Signal Rise and Fall Timing**

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time	$T_{rise_{clk}}$	-	-	6	ns
BIT_CLK fall time	$T_{fall_{clk}}$	-	-	6	ns
SYNC rise time	$T_{rise_{sync}}$	-	-	6	ns
SYNC fall time	$T_{fall_{sync}}$	-	-	6	ns
SDATA_IN rise time	$T_{rise_{din}}$	-	-	6	ns
SDATA_IN fall time	$T_{fall_{din}}$	-	-	6	ns
SDATA_OUT rise time	$T_{rise_{dout}}$	-	-	6	ns
SDATA_OUT fall time	$T_{fall_{dout}}$	-	-	6	ns

Note1: 75pF external load (50 pF in AC'97 rev2.1)

Note2: Rise is from 10% to 90% of Vdd ( $V_{ol}$  to  $V_{oh}$ )

Note3: Fall is from 90% to 10% of Vdd ( $V_{oh}$  to  $V_{ol}$ )


**Figure 6. Signal Rise and Fall Timing**

8.2.6. AC-Link Low Power Mode Timing

Table 56. AC-Link Low Power Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T <sub>s2_pdown</sub>	-	-	1.0	μs

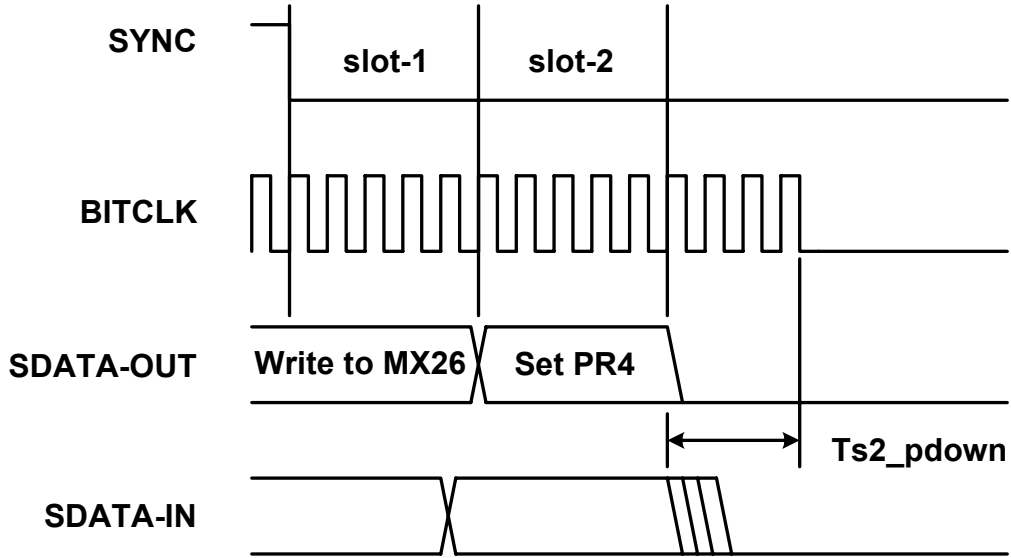


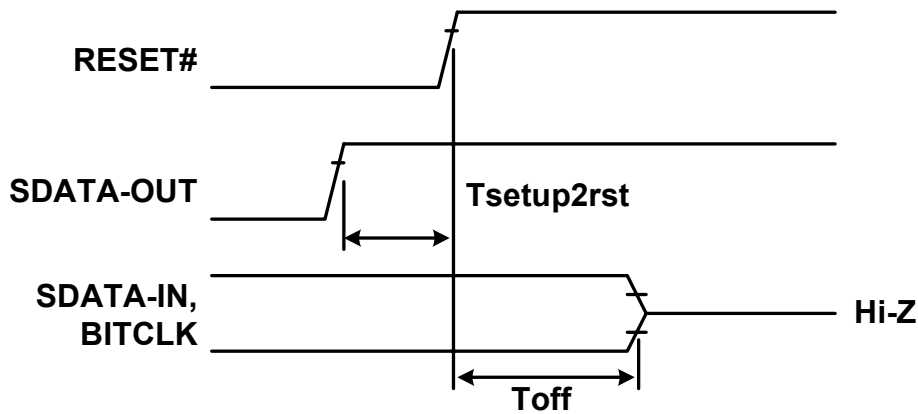
Figure 7. AC-Link Low Power Mode Timing

### 8.2.7. ATE Test Mode

To meet AC'97 rev. 2.3 specifications, EAPD, S/PDIFO, BIT\_CLK and SDATA\_IN should be floating in test mode.

**Table 57. ATE Test Mode**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{\text{setup2rst}}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	$T_{\text{off}}$	-	-	25.0	ns



**Figure 8. ATE Test Mode Timing**

### 8.2.8. AC-Link IO Pin Capacitance and Loading

**Table 58. AC-Link IO Pin Capacitance and Loading**

Output Pin	1 Codec	2 Codec	3 Codec	4 Codec
BIT_CLK (must support $\geq 2$ codecs)	55pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF



## 8.2.9. S/PDIF Output

Table 59. S/PDIF Output

S/PDIF_OUT	Minimum	Maximum	Units
Rise Time/Fall Time	0	10	%
Duty Cycle	45	55	%

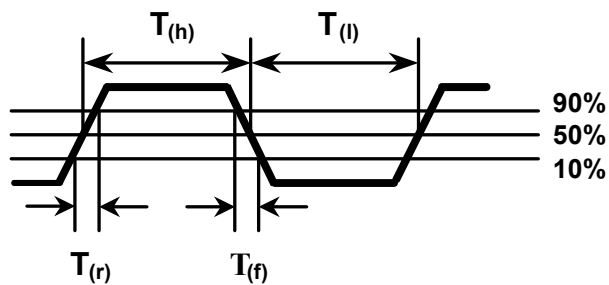


Figure 9. S/PDIF Output

Rise Time	$100 * T_{(r)} / (T_{(l)} + T_{(h)})\%$
Fall Time	$100 * T_{(f)} / (T_{(l)} + T_{(h)})\%$
Duty Cycle	$100 * T_{(h)} / (T_{(l)} + T_{(h)})\%$

## 9. Analog Performance Characteristics

Standard Test Conditions  $T_{\text{ambient}}=25^{\circ}\text{C}$ , DVDD= 3.3V $\pm$ 5%, AVDD=5.0V $\pm$ 5%  
 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms  
 10K $\Omega$ /50pF load; Test bench Characterization BW: 10Hz~22kHz  
 0dB attenuation: Tone and 3D disabled

**Table 60. Analog Performance Characteristics**

Parameter	Minimum	Typical	Maximum	Units
Full Scale Input Voltage:				
Line Inputs (Mixers)	-	1.6	-	Vrms
Line Inputs (A/D)	-	1.0	-	
Mic Input (0dB)	-	1.6	-	
Mic Input (20dB boost)	-	0.16	-	
Full Scale Voltage:				
DACs	-	1.10	-	Vrms
ADC	-	1.10	-	Vrms
Analog to Analog S/N:				
CD to LINE-OUT	-	95	-	dB
Other to LINE-OUT	-	95	-	
Analog Frequency Response	10	-	22,000	Hz
S/N (A-Weighted):				
D/A	-	86	-	dB
A/D	-	92	-	
Total Harmonic Distortion:				
D/A	-	-70	-	dB
A/D	-	-86	-	
D/A & A/D Frequency Response	16	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	$\infty$	Hz
Stop Band Rejection	-	-70	-	dB
Out-of-Band Rejection (28.8kHz~100kHz)	-	-60	-	dB
Power Supply Rejection Ratio	-	-40	-	dB
MIC Boost Gain	-	20	-	dB
Master Volume. 32 step:				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-46.5	dB
PC Beep Volume. 16 step:				
Step Size	-	3.0	-	dB
Attenuation Control Range	0	-	-45	dB
Analog Mixer Volume. 32 step:				
Step Size	-	1.5	-	dB
Gain Control Range	-34.5	-	+12	dB





Parameter	Minimum	Typical	Maximum	Units
Record Gain. 16 step:				
Step Size	-	1.5	-	dB
Gain Control Range	0	-	+22.5	dB
Input Impedance (gain=0dB, mixer=off):				
LINE-IN, CD-IN, AUX-IN, MIC1/MIC2	-	64	-	K $\Omega$
PCBEEP, PHONE	-	16	-	K $\Omega$
Output Impedance:				
Amplifier Outputs	-	5	-	$\Omega$
Outputs Without Amplifier	-	200	1000	$\Omega$
Amplifier Maximum Output Power:				
@20 $\Omega$ load	-	-	50	mW
Power Supply Current:				
VA=5.0V	-	59	-	mA
VA=3.3V	-	43	-	mA
VD=3.3V	-	15	-	mA
Power Down Current:				
VA=5.0V/3.3V	-	-	7.8/5.3	mA
VD=3.3V	-	-	9	mA
Vrefout/Vrefout2/Vrefout3	-	2.50	4.0	V
Vrefout Drive Current	-	5	-	mA

## 10. Design and Layout Guide

### 10.1. Clocking

The clock source is decided by XTLSEL latched from pin-46 after power-on reset. The clock source of different configurations is listed below:

**Table 61. Clocking**

Configuration	Operation & ID0		
	ID0	BIT-CLK	Clock Source
Pin-46 (XTLSEL)*			
NC	0 (Primary)	Output 12.288MHz	Crystal or ext. 24.576MHz is attached at XTL-IN
Low**	0 (Primary)	Output 12.288MHz	Crystal or ext. 14.318MHz is attached at XTL-IN
NC	0 (Primary)	Input	12.288M input at BIT-CLK***

\*Pin-46 is internally pulled high by a weak resistor.

\*\*Low: Pulled low by a 0 ohm resistor. NC: Not Connected or pulled high.

\*\*\*According to AC'97 ver 2.3, in Primary Mode, if a clock is present at BIT-CLK pin for at least 5 cycles before RESET# is de-asserted, the ALC850(D) is a consumer of BITCLK. The ALC850(D) uses external 12.288MHz BITCLK as its clock source.

### 10.2. AC-Link

When the ALC850(D) receives serial data from the AC'97 controller, it samples SDATA\_OUT on the falling edge of BIT\_CLK. When the ALC850(D) sends serial data to the AC'97 controller, it starts to drive SDATA\_IN on the rising edge of BIT\_CLK.

The ALC850(D) will return any uninstalled bits or registers with 0 for read operations. The ALC850(D) also stuffs the unimplemented slot or bit with 0's in SDATA\_IN. Note that AC-LINK is MSB-justified.

Refer to the AC'97 Component Specification, Revision 2.3, for details.

Slot#	0	1	2	3	4	5	6	7	8	9	10	11	12
SYNC	[Timing diagram showing SYNC signal across slots 0-12]												

SDATA-OUT	TAG	CMD	DATA	PCM L	PCMR		CEN	SURR L	SURR R	LFE	S/PDIFL	S/PDIFR	

SDATA-IN	TAG	ADD	DATA	PCM L	PCMR								

*Default ALC850(D) Slot Arrangement – Codec ID = 00 (the ALC850(D) supports primary mode only).*

### 10.3. Reset

There are three types of reset operations: Cold, Register, and Warm.

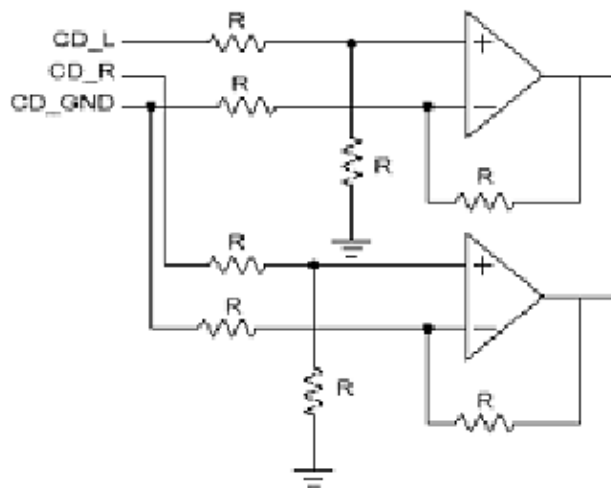
**Table 62. Reset**

Reset Type	Trigger Condition	Codec Response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to default values
Register	Write register indexed 00h	Reset all registers to default values
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK. No change to register values

The AC'97 controller should drive SYNC and SDATA\_OUT low during the period of RESET# assertion to guarantee that the ALC850(D) has reset successfully.

### 10.4. CD Input

For noise cancellation reasons, it is important to pay attention to differential CD input. Below is an example of differential CD input.



**Figure 10. Example of Differential CD Input**

## 10.5. Odd Addressed Register Access

The ALC850(D) will return '0000h' when odd-addressed and unimplemented registers are read.

## 10.6. Power Down Mode

For power saving reasons, it is important to pay attention to the power-down control register (index 26h), especially PR4 (power-down AC-link).

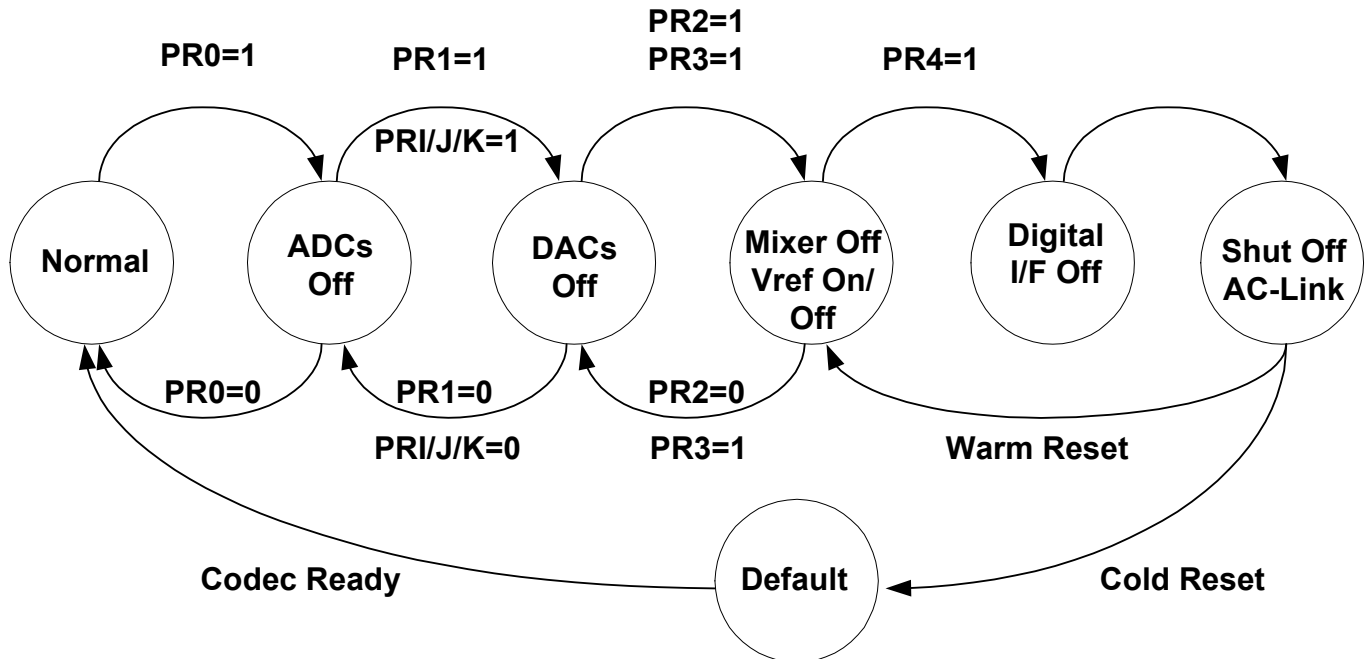


Figure 11. Power-Down Control

## 10.7. Test Mode

To provide compatibility with AC'97 Rev. 2.2, the ALC850(D) will float its digital output pins in ATE test mode. Please refer to AC'97 Rev. 2.2, section 9.2, for a detailed description of the test modes.

### 10.7.1. ATE in Circuit Test Mode

SDATA\_OUT is sampled high at the trailing edge of RESET#. In this mode, the ALC850(D) will drive BIT\_CLK, SDATA\_IN, EAPD, and S/PDIFO to high impedance.

### 10.7.2. Vendor Specific Test Mode

Vendor specific test mode is not supported.

## 10.8. Power-Off CD Function

The Power-Off CD function describes a state where the system has been shut down (digital power is off). When a +5V analog power is supplied the ALC850(D) will turn on the CD-IN op-amp and output amplifier. It is possible to design a system that can bypass op-amp circuitry and pass CD output directly to the speaker.

The figure below indicates the system application circuitry that supports the Power-Off CD function. The operating mode is determined by +3.3VCC and +5VA.

**Table 63. Power-Off CD Function Circuitry**

+3.3VCC	+5VA	+5Vstandby	Operation Mode
No (0)	No (0)	No (0)	Shut Down
No (0)	Yes (1)	-	Power-Off CD
No (0)	-	Yes (1)	Power-Off CD
Yes (1)	No (0)	No (0)	Digital on, Analog off
Yes (1)	Yes (1)	-	Normal

The AC'97 controller should drive SYNC and SDATA\_OUT low during the period of RESET# assertion to guarantee that the ALC850(D) has reset successfully.

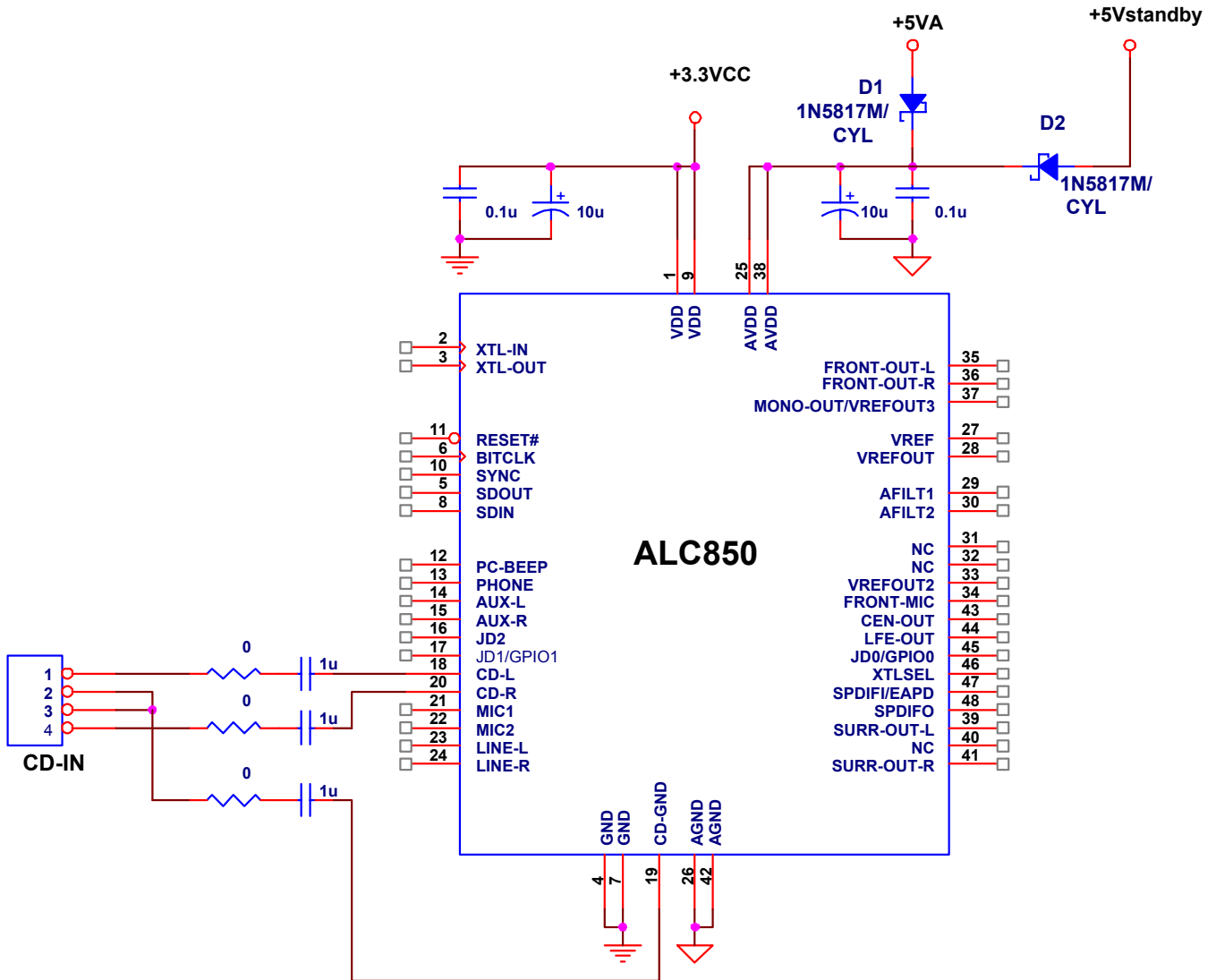


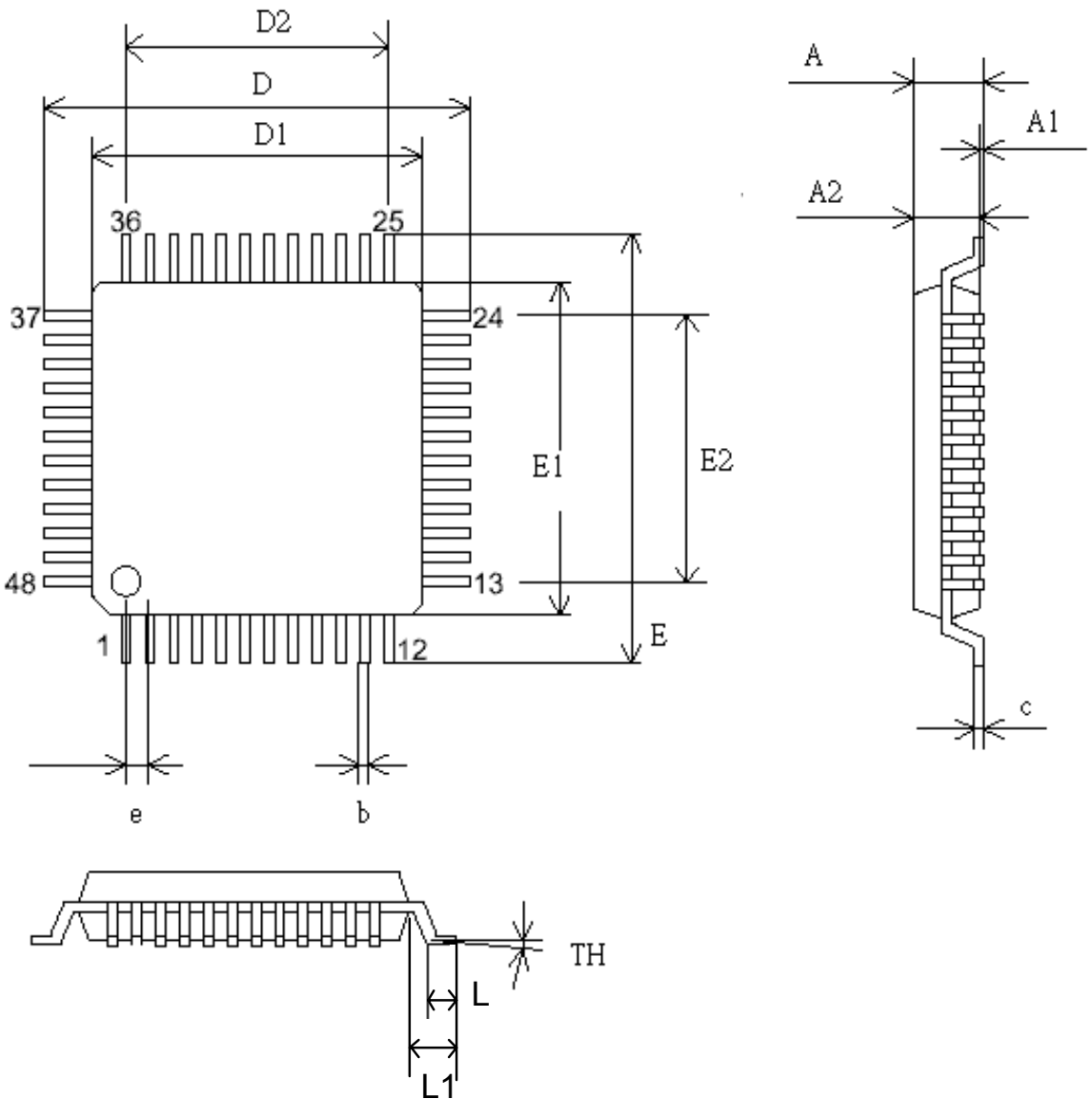
Figure 12. Power-Off CD Function Circuitry

## 11. Application Circuits

Application circuits are for design reference only. System designers are suggested to visit Realtek's web site to download the latest application circuits. To get the best compatibility in hardware design and software driver, Realtek should confirm modifications of application circuits.



## 12. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

## 12.1. Mechanical Dimensions Notes

SYMBOL	MILLIMETER			INCH		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
C	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm)		
PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKG-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

## 13. Ordering Information

**Table 64. Ordering Information**

Part Number	Package	Status
ALC850	48-pin LQFP. Standard product	
ALC850D	48-pin LQFP. ALC850 + Dolby Digital Live (software feature)	
ALC850-LF	48-pin LQFP. ALC850 + Lead (Pb)-Free package	
ALC850D-LF	48-pin LQFP. ALC880D + Lead (Pb)-Free package	

Note: See page 4 for lead (Pb)-free package and version identification.

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