

# DATA SHEET

## **TDA8768** 12-bit high-speed Analog-to-Digital Converter (ADC)

Preliminary specification  
Supersedes data of 1998 Feb 25  
File under Integrated Circuits, IC02

1998 Aug 26

# 12-bit high-speed Analog-to-Digital Converter (ADC)

## TDA8768

### FEATURES

- 12-bit resolution
- Sampling rate up to 55 MHz
- -3 dB bandwidth of 190 MHz
- 5 V power supplies
- Binary or twos-complement CMOS outputs
- In-range CMOS-compatible output
- TTL-CMOS compatible static digital inputs
- 3 to 5 V CMOS-compatible digital outputs
- Differential clock input; Positive Emitter Coupled Logic (PECL)-compatible
- Power dissipation 325 mW (typical)
- Low analog input capacitance (typical 2 pF), no buffer amplifier required
- Integrated sample-and-hold amplifier
- Differential analog input
- External amplitude range control
- Voltage controlled regulator included.

### APPLICATIONS

- High-speed analog-to-digital conversion for
  - Video signal digitizing
  - High Definition TV (HDTV)
  - Imaging (camera scanner)
  - Medical imaging
  - Telecommunication
  - Base-station receiver.

### GENERAL DESCRIPTION

The TDA8768 is a bipolar 12-bit Analog-to-Digital Converter (ADC) optimized for telecommunications and professional imaging. It converts the analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 55 MHz. All static digital inputs (SH,  $\overline{\text{CE}}$  and OTC) are TTL and CMOS compatible and all outputs are CMOS compatible. A sine wave clock input signal can also be used.

### QUICK REFERENCE DATA

| SYMBOL                | PARAMETER                  | CONDITIONS  | MIN. | TYP.      | MAX.      | UNIT |
|-----------------------|----------------------------|---|------|-----------|-----------|------|
| $V_{\text{CCA}}$      | analog supply voltage      |   | 4.75 | 5.0       | 5.25      | V    |
| $V_{\text{CCD}}$      | digital supply voltage     |   | 4.75 | 5.0       | 5.25      | V    |
| $V_{\text{CCO}}$      | output supply voltage      |   | 3.0  | 3.3       | 5.25      | V    |
| $I_{\text{CCA}}$      | analog supply current      |   | –    | 33        | tbf       | mA   |
| $I_{\text{CCD}}$      | digital supply current     |   | –    | 30        | tbf       | mA   |
| $I_{\text{CCO}}$      | output supply current      | $f_{\text{CLK}} = 4 \text{ MHz}; f_i = 400 \text{ kHz}$ | –    | 3.2       | tbf       | mA   |
| INL                   | integral non-linearity     | $f_{\text{CLK}} = 4 \text{ MHz}; f_i = 400 \text{ kHz}$ | –    | $\pm 2.0$ | $\pm 4.5$ | LSB  |
| DNL                   | differential non-linearity | $f_{\text{CLK}} = 4 \text{ MHz}; f_i = 400 \text{ kHz}$ | –    | $\pm 0.6$ | $\pm 1.0$ | LSB  |
| $f_{\text{CLK(max)}}$ | maximum clock frequency    |   |      |           |           |      |
|                       | TDA8768H/4                 |   | 40   | –         | –         | MHz  |
|                       | TDA8768H/5                 |   | 55   | –         | –         | MHz  |
| $P_{\text{tot}}$      | total power dissipation    |   | –    | 325       | tbf       | mW   |

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |   |          | SAMPLING FREQUENCY (MHz) |
|-------------|---------|---|----------|--------------------------|
|             | NAME    | DESCRIPTION   | VERSION  |                          |
| TDA8768H/4  | QFP44   | plastic quad flat package; 44 leads<br>(lead length 1.3 mm); body 10 × 10 × 1.75 mm | SOT307-2 | 40                       |
| TDA8768H/5  |         |   |          | 55                       |

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## BLOCK DIAGRAM

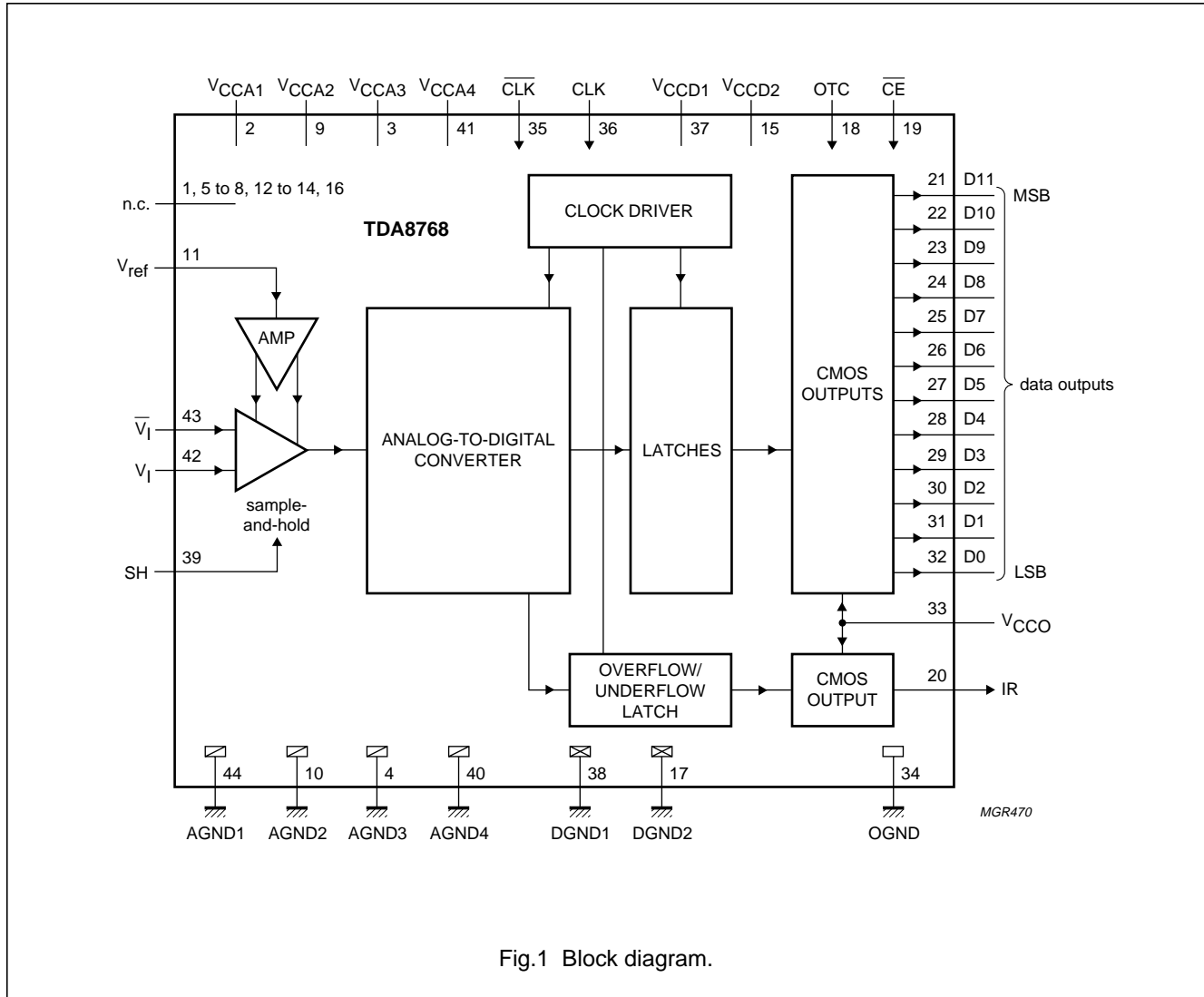


Fig.1 Block diagram.

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## PINNING

| SYMBOL                 | PIN | DESCRIPTION                                       |
|------------------------|-----|---|
| n.c.                   | 1   | not connected                                     |
| V <sub>CCA1</sub>      | 2   | analog supply voltage 1 (+5 V)                    |
| V <sub>CCA3</sub>      | 3   | analog supply voltage 3 (+5 V)                    |
| AGND3                  | 4   | analog ground 3                                   |
| n.c.                   | 5   | not connected                                     |
| n.c.                   | 6   | not connected                                     |
| n.c.                   | 7   | not connected                                     |
| n.c.                   | 8   | not connected                                     |
| V <sub>CCA2</sub>      | 9   | analog supply voltage 2 (+5 V)                    |
| AGND2                  | 10  | analog ground 2                                   |
| V <sub>ref</sub>       | 11  | reference voltage input                           |
| n.c.                   | 12  | not connected                                     |
| n.c.                   | 13  | not connected                                     |
| n.c.                   | 14  | not connected                                     |
| V <sub>CCD2</sub>      | 15  | digital supply voltage 2 (+5 V)                   |
| n.c.                   | 16  | not connected                                     |
| DGND2                  | 17  | digital ground 2                                  |
| OTC                    | 18  | control input twos complement output; active HIGH |
| $\overline{\text{CE}}$ | 19  | chip enable input (CMOS level; active LOW)        |
| IR                     | 20  | in-range output                                   |
| D11                    | 21  | data output; bit 11 (MSB)                         |
| D10                    | 22  | data output; bit 10                               |

| SYMBOL                  | PIN | DESCRIPTION  |
|-------------------------|-----|--|
| D9                      | 23  | data output; bit 9                                     |
| D8                      | 24  | data output; bit 8                                     |
| D7                      | 25  | data output; bit 7                                     |
| D6                      | 26  | data output; bit 6                                     |
| D5                      | 27  | data output; bit 5                                     |
| D4                      | 28  | data output; bit 4                                     |
| D3                      | 29  | data output; bit 3                                     |
| D2                      | 30  | data output; bit 2                                     |
| D1                      | 31  | data output; bit 1                                     |
| D0                      | 32  | data output; bit 0 (LSB)                               |
| V <sub>CCO</sub>        | 33  | output supply voltage (3 to 5.25 V)                    |
| OGND                    | 34  | output ground  |
| $\overline{\text{CLK}}$ | 35  | complementary clock input; active LOW                  |
| CLK                     | 36  | clock input  |
| V <sub>CCD1</sub>       | 37  | digital supply voltage 1 (+5 V)                        |
| DGND1                   | 38  | digital ground 1                                       |
| SH                      | 39  | sample-and-hold enable input (CMOS level; active HIGH) |
| AGND4                   | 40  | analog ground 4  |
| V <sub>CCA4</sub>       | 41  | analog supply voltage 4 (+5 V)                         |
| V <sub>I</sub>          | 42  | positive analog input voltage                          |
| $\overline{V}_I$        | 43  | negative analog input voltage                          |
| AGND1                   | 44  | analog ground 1  |

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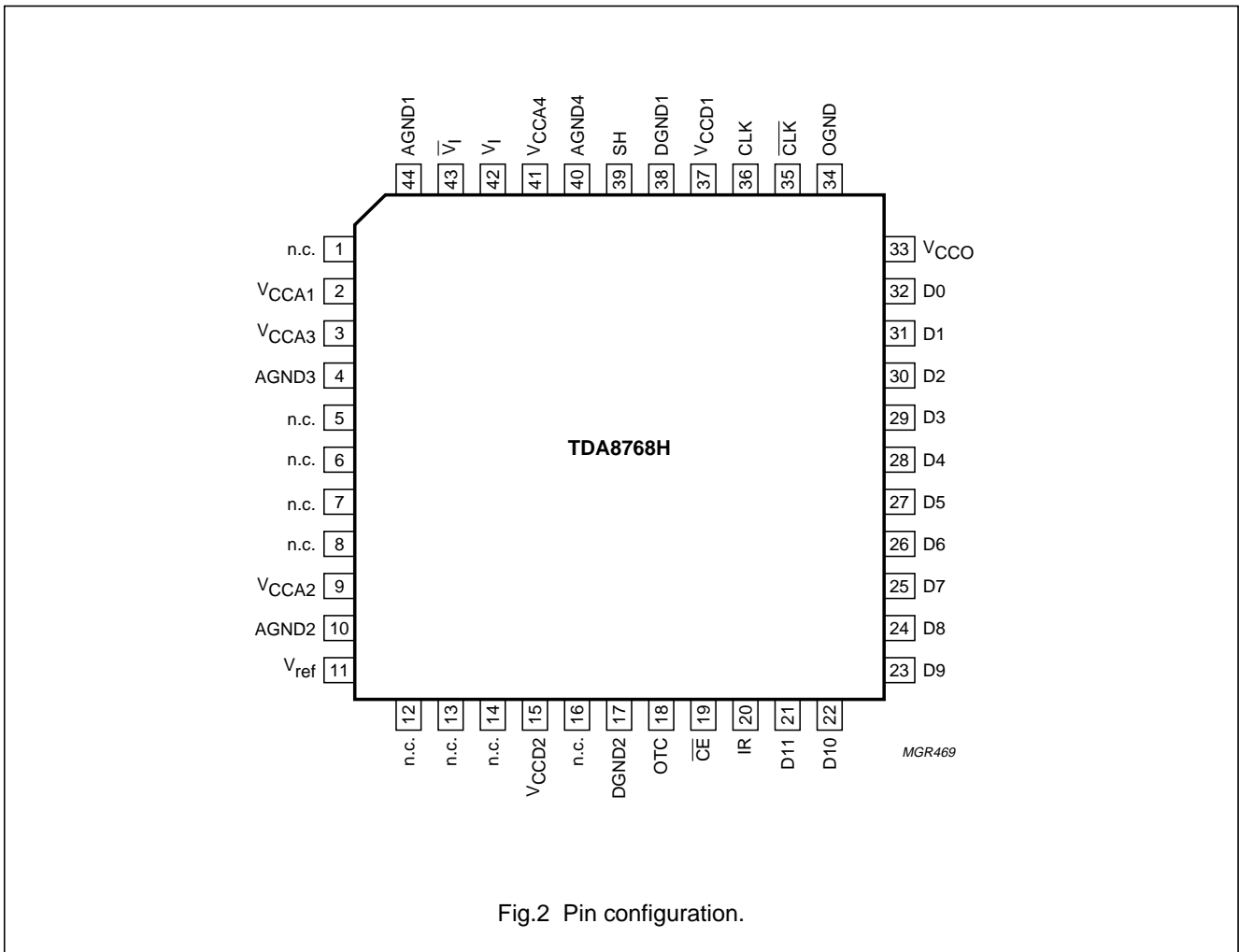


Fig.2 Pin configuration.

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL          | PARAMETER   | CONDITIONS         | MIN. | MAX.      | UNIT |
|-----------------|---|--------------------|------|-----------|------|
| $V_{CCA}$       | analog supply voltage   | note 1             | -0.3 | +7.0      | V    |
| $V_{CCD}$       | digital supply voltage  | note 1             | -0.3 | +7.0      | V    |
| $V_{CCO}$       | output supply voltage   | note 1             | -0.3 | +7.0      | V    |
| $\Delta V_{CC}$ | supply voltage difference   |                    |      |           |      |
|                 | $V_{CCA} - V_{CCD}$   |                    | -1.0 | +1.0      | V    |
|                 | $V_{CCD} - V_{CCO}$   |                    | -1.0 | +4.0      | V    |
|                 | $V_{CCA} - V_{CCO}$   |                    | -1.0 | +4.0      | V    |
| $V_I$           | input voltage at pins 42 and 43   | referenced to AGND | 0.3  | $V_{CCA}$ | V    |
| $V_{i(p-p)}$    | input voltage at pins 35 and 36 for differential clock drive (peak-to-peak value) |                    | -    | $V_{CCD}$ | V    |
| $I_O$           | output current  |                    | -    | 10        | mA   |
| $T_{stg}$       | storage temperature   |                    | -55  | +150      | °C   |
| $T_{amb}$       | operating ambient temperature   |                    | -10  | +85       | °C   |
| $T_j$           | junction temperature  |                    | -    | 150       | °C   |

### Note

- The supply voltages  $V_{CCA}$ ,  $V_{CCD}$  and  $V_{CCO}$  may have any value between -0.3 V and +7.0 V provided that the supply voltage differences  $\Delta V_{CC}$  are respected.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                   | CONDITION   | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 75    | K/W  |

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## CHARACTERISTICS

$V_{CCA} = V_2$  to  $V_{44}$ ,  $V_9$  to  $V_{10}$ ,  $V_3$  to  $V_4$  and  $V_{41}$  to  $V_{40} = 4.75$  to  $5.25$  V;  $V_{CCD} = V_{37}$  to  $V_{38}$  and  $V_{15}$  to  $V_{17} = 4.75$  to  $5.25$  V;  $V_{CCO} = V_{33}$  to  $V_{34} = 3.0$  to  $5.25$  V; AGND and DGND shorted together;  $T_{amb} = 0$  to  $70$  °C; typical values measured at  $V_{CCA} = V_{CCD} = 5$  V and  $V_{CCO} = 3.3$  V,  $T_{amb} = 25$  °C,  $V_{I(p-p)} - \bar{V}_{I(p-p)} = 2.0$  V and  $C_L = 10$  pF; unless otherwise specified.

| SYMBOL   | PARAMETER   | CONDITIONS  | MIN. | TYP. | MAX.      | UNIT       |
|--|---|---|------|------|-----------|------------|
| <b>Supply</b>  |   |   |      |      |           |            |
| $V_{CCA}$  | analog supply voltage   |   | 4.75 | 5.0  | 5.25      | V          |
| $V_{CCD}$  | digital supply voltage  |   | 4.75 | 5.0  | 5.25      | V          |
| $V_{CCO}$  | output supply voltage   |   | 3.0  | 3.3  | 5.25      | V          |
| $I_{CCA}$  | analog supply current   |   | –    | 33   | 45        | mA         |
| $I_{CCD}$  | digital supply current  |   | –    | 30   | 37        | mA         |
| $I_{CCO}$  | output supply current   | $f_{CLK} = 4$ MHz; $f_i = 400$ kHz                      | –    | 3.2  | tbf       | mA         |
|  |   | $f_{CLK} = 40$ MHz; $f_i = 4.43$ MHz                    | –    | 11   | tbf       | mA         |
| <b>Inputs</b>  |   |   |      |      |           |            |
| CLK and $\overline{CLK}$ (REFERENCED TO DGND)  |   |   |      |      |           |            |
| $V_{IL}$   | LOW-level input voltage   | $V_{CCD} = 5$ V; note 1                                 | 3.19 | –    | 3.52      | V          |
| $V_{IH}$   | HIGH-level input voltage  | $V_{CCD} = 5$ V; note 1                                 | 3.83 | –    | 4.12      | V          |
| $I_{IL}$   | LOW-level input current   | $V_{CLK}$ or $V_{\overline{CLK}} = 3.19$ V              | –10  | –    | –         | $\mu$ A    |
| $I_{IH}$   | HIGH-level input current  | $V_{CLK}$ or $V_{\overline{CLK}} = 3.83$ V              | –    | –    | 10        | $\mu$ A    |
| $Z_i$  | input impedance   | $f_{CLK} = 40$ MHz                                      | 2    | –    | –         | k $\Omega$ |
| $C_i$  | input capacitance   | $f_{CLK} = 40$ MHz                                      | –    | –    | 2         | pF         |
| $\Delta V_{CLK(p-p)}$  | differential AC input voltage (peak-to-peak value) for switching ( $V_{CLK} - V_{\overline{CLK}}$ ) | DC voltage level = 2.5 V                                | 0.5  | –    | 2.0       | V          |
| OTC, SH AND $\overline{CE}$ (REFERENCED TO DGND); see Tables 1 and 2                   |   |   |      |      |           |            |
| $V_{IL}$   | LOW-level input voltage   |   | 0    | –    | 0.8       | V          |
| $V_{IH}$   | HIGH-level input voltage  |   | 2.0  | –    | $V_{CCD}$ | V          |
| $I_{IL}$   | LOW-level input current   | $V_{IL} = 0.8$ V  | –20  | –    | –         | $\mu$ A    |
| $I_{IH}$   | HIGH-level input current  | $V_{IH} = 2.0$ V  | –    | –    | +20       | $\mu$ A    |
| $V_I$ AND $\bar{V}_I$ (REFERENCED TO AGND); $V_{REF} = V_{CCA} - 1.825$ V; see Table 1 |   |   |      |      |           |            |
| $I_{IL}$   | LOW-level input current   |   | –    | 10   | –         | $\mu$ A    |
| $I_{IH}$   | HIGH-level input current  |   | –    | 10   | –         | $\mu$ A    |
| $R_i$  | input resistance  | $f_i = 4.43$ MHz  | 100  | –    | –         | k $\Omega$ |
| $C_i$  | input capacitance   | $f_i = 4.43$ MHz  | –    | –    | 2         | pF         |
| $V_{I(CM)}$  | common mode input voltage   | $V_I = \bar{V}_I$ ; output code 2047<br>$V_{CCA} = 5$ V | tbf  | 3.6  | tbf       | V          |
|  |   | $V_{CCA} = 4.75$ V                                      | tbf  | 3.35 | tbf       | V          |
|  |   | $V_{CCA} = 5.25$ V                                      | tbf  | 3.85 | tbf       | V          |

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| SYMBOL  | PARAMETER  | CONDITIONS   | MIN.            | TYP.      | MAX.      | UNIT          |
|---|--|--|-----------------|-----------|-----------|---------------|
| <b>Voltage controlled regulator input <math>V_{ref}</math> (referenced to AGND); note 2</b>   |  |  |                 |           |           |               |
| $V_{ref(FS)}$   | full-scale fixed voltage   | $V_{CCA} = 5\text{ V}$   | –               | 3.175     | –         | V             |
| $I_{ref}$   | input current  |  | –               | 0.5       | 10        | $\mu\text{A}$ |
| $V_{I(p-p)} - \bar{V}_{I(p-p)}$   | input voltage amplitude (peak-to-peak value)                                   | $V_{ref} = V_{CCA} - 1.825\text{ V}$   | –               | 2.0       | –         | V             |
| <b>Outputs (referenced to OGND)</b>   |  |  |                 |           |           |               |
| DIGITAL OUTPUTS D11 TO D0 AND IR (REFERENCED TO OGND)   |  |  |                 |           |           |               |
| $V_{OL}$  | LOW-level output voltage   | $I_{OL} = 2\text{ mA}$   | 0               | –         | 0.5       | V             |
| $V_{OH}$  | HIGH-level output voltage  | $I_{OH} = -0.4\text{ mA}$  | $V_{CCO} - 0.5$ | –         | $V_{CCO}$ | V             |
| $I_o$   | output current in 3-state  | output level between 0.5 V and $V_{CCO}$   | –20             | –         | +20       | $\mu\text{A}$ |
| <b>Switching characteristics</b>  |  |  |                 |           |           |               |
| CLOCK FREQUENCY $f_{CLK}$ ; see Fig.3   |  |  |                 |           |           |               |
| $f_{CLK(min)}$  | minimum clock frequency  | SH = HIGH  | –               | –         | 2         | MHz           |
| $f_{CLK(max)}$  | maximum clock frequency<br>TDA8768H/4<br>TDA8768H/5                            |  | 40              | –         | –         | MHz           |
|   |  |  | 55              | –         | –         | MHz           |
| $t_{CLKH}$  | clock pulse width HIGH   |  | 8.5             | –         | –         | ns            |
| $t_{CLKL}$  | clock pulse width LOW  |  | 8.5             | –         | –         | ns            |
| <b>Analog signal processing; 50% clock duty factor; <math>V_I - \bar{V}_I = 2.0\text{ V}</math>; <math>V_{ref} = V_{CCA} - 1.825\text{ V}</math>; see Table 1</b> |  |  |                 |           |           |               |
| LINEARITY   |  |  |                 |           |           |               |
| INL   | integral non-linearity   | $f_{CLK} = 4\text{ MHz}$ ; $f_i = 400\text{ kHz}$  | –               | $\pm 2.0$ | $\pm 4.5$ | LSB           |
| DNL   | differential non-linearity   | $f_{CLK} = 4\text{ MHz}$ ; $f_i = 400\text{ kHz}$ ;<br>no missing code   | –               | $\pm 0.6$ | $\pm 1.0$ | LSB           |
| $E_{offset}$  | offset error   | $V_{CCA} = V_{CCD} = V_{CCO} = 5\text{ V}$ ;<br>$T_{amb} = 25\text{ }^\circ\text{C}$ ; $V_I = \bar{V}_I$ ;<br>output code = 2047         | tbf             | –11       | tbf       | mV            |
| $E_{G(FS)}$   | gain error amplitude (full scale); spread from device to device                | $V_{CCA} = V_{CCD} = V_{CCO} = 5\text{ V}$ ;<br>$T_{amb} = 25\text{ }^\circ\text{C}$ ;<br>$V_{I(p-p)} - \bar{V}_{I(p-p)} = 2.0\text{ V}$ | –5              | –         | +5        | %             |
| BANDWIDTH ( $f_{CLK} = 55\text{ MHz}$ ); note 3   |  |  |                 |           |           |               |
| B   | analog bandwidth   | –3 dB; full scale input  | tbf             | 190       | –         | MHz           |
| HARMONICS ( $f_{CLK} = 40\text{ MHz}$ )   |  |  |                 |           |           |               |
| $h_{fund(FS)}$  | fundamental harmonics (full scale)   | $f_i = 4.43\text{ MHz}$  | –               | –         | 0         | dB            |
| $h_{tot(FS)}$   | harmonics (full scale);<br>all components<br>second harmonic<br>third harmonic |  | –               | –75       | –         | dB            |
|   |  |  | –               | –70       | –         | dB            |
|   |  |  | –               | –66       | –         | dB            |
| THD   | total harmonic distortion  | $f_i = 4.43\text{ MHz}$ ; note 4   | –               | –66       | –         | dB            |



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| SYMBOL   | PARAMETER  | CONDITIONS  | MIN. | TYP.       | MAX. | UNIT             |
|--|--|---|------|------------|------|------------------|
| <b>THERMAL NOISE</b>   |  |   |      |            |      |                  |
| $N_{th(rms)}$  | thermal noise (RMS value)                                    | grounded input;<br>$f_{CLK} = 40$ MHz                                       | –    | 0.25       | tbf  | LSB              |
| <b>SPURIOUS FREE DYNAMIC RANGE</b>                             |  |   |      |            |      |                  |
| $DR_{sf}$  | spurious free dynamic range                                  | $f_i = 4.43$ MHz  | tbf  | 69         | –    | dB               |
|  |  | $f_i = 10$ MHz  | tbf  | tbf        | –    | dB               |
|  |  | $f_i = 20$ MHz  | tbf  | tbf        | –    | dB               |
| <b>SIGNAL-TO-NOISE RATIO; note 5</b>                           |  |   |      |            |      |                  |
| S/N  | signal-to-noise ratio  | without harmonics;<br>$f_{CLK} = 40$ MHz; $f_i = 4.43$ MHz                  | –    | 67         | –    | dB               |
| <b>EFFECTIVE NUMBER OF BITS; note 5</b>                        |  |   |      |            |      |                  |
| $N_{bit}$  | effective number of bits<br>TDA8768H/4 ( $f_{CLK} = 40$ MHz) | $f_i = 4.43$ MHz  | –    | 10.3       | –    | bits             |
|  |  | $f_i = 10$ MHz  | –    | tbf        | –    | bits             |
|  |  | $f_i = 15$ MHz  | –    | tbf        | –    | bits             |
|  | effective number of bits<br>TDA8768H/5 ( $f_{CLK} = 55$ MHz) | $f_i = 4.43$ MHz  | –    | 9.9        | –    | bits             |
|  |  | $f_i = 10$ MHz  | –    | tbf        | –    | bits             |
|  |  | $f_i = 15$ MHz  | –    | tbf        | –    | bits             |
|  |  | $f_i = 20$ MHz  | –    | tbf        | –    | bits             |
| <b>INTERMODULATION; note 6</b>                                 |  |   |      |            |      |                  |
| TTIR   | two-tone intermodulation rejection                           | $f_{CLK} = 40$ MHz  | tbf  | 66         | –    | dB               |
| $d_3$  | third order intermodulation distortion                       | $f_{CLK} = 40$ MHz  | tbf  | 67         | –    | dB               |
| <b>BIT ERROR RATE</b>  |  |   |      |            |      |                  |
| BER  | bit error rate   | $f_{CLK} = 40$ MHz;<br>$f_i = 4.43$ MHz;<br>$V_1 = \pm 16$ LSB at code 2047 | –    | $10^{-15}$ | tbf  | times/<br>sample |
| <b>Timing (<math>C_L = 10</math> pF); see Fig.3 and note 7</b> |  |   |      |            |      |                  |
| $t_{d(s)}$   | sampling delay time  |   | –    | –          | 2    | ns               |
| $t_h$  | output hold time   |   | 4    | –          | –    | ns               |
| $t_d$  | output delay time  | $V_{CCO} = 5.25$ V  | –    | 10         | 15   | ns               |
|  |  | $V_{CCO} = 3.0$ V   |      | 13         | 18   | ns               |
| <b>3-state output delay times; see Fig.4</b>                   |  |   |      |            |      |                  |
| $t_{dZH}$  | enable HIGH  |   | –    | 14         | 18   | ns               |
| $t_{dZL}$  | enable LOW   |   | –    | 16         | 20   | ns               |
| $t_{dHZ}$  | disable HIGH   |   | –    | 16         | 20   | ns               |
| $t_{dLZ}$  | disable LOW  |   | –    | 14         | 18   | ns               |

# 12-bit high-speed Analog-to-Digital Converter (ADC)

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## Notes

- The circuit has two clock inputs: CLK and  $\overline{\text{CLK}}$ . There are four modes of operation:
  - PECL mode 1: (DC level varies 1 : 1 with  $V_{\text{CCD}}$ ) CLK and  $\overline{\text{CLK}}$  inputs are at differential PECL levels.
  - PECL mode 2: (DC level varies 1 : 1 with  $V_{\text{CCD}}$ ) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on  $\overline{\text{CLK}}$  decoupled to GND via a 100 nF capacitor.
  - PECL mode 3: (DC level varies 1 : 1 with  $V_{\text{CCD}}$ )  $\overline{\text{CLK}}$  input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.
  - AC driving mode 4: when driving the CLK input directly and with any AC signal of minimum 0.5 V (peak-to-peak value) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal. When driving the  $\overline{\text{CLK}}$  input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the  $\overline{\text{CLK}}$  or CLK input to DGND via a 100 nF capacitor.
- It is possible with an external reference connected to pin  $V_{\text{ref}}$  to adjust the ADC input range. This voltage has to be referenced to  $V_{\text{CCA}}$ . For  $V_{\text{CCA}} - 1.825$  V, the differential input voltage amplitude is 2 V (peak-to-peak value).
- The -3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.
- THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$\text{THD} = 20 \log \frac{F}{\sqrt{(2\text{nd})^2 + (3\text{rd})^2 + (4\text{th})^2 + (5\text{th})^2 + (6\text{th})^2}}$$

where F is the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.

- Effective number of bits are obtained via a Fast Fourier Transform (FFT). The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to SNR:  
 $\text{SNR} = N_{\text{bit}} \times 6.02 + 1.76$  dB.
- Intermodulation measured relative to either tone with analog input frequencies of 4.43 and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (-6 dB below full-scale for each input signal).  
 $d_3$  is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product.
- Output data acquisition: the output data is available after the maximum delay of  $t_d$ .

# 12-bit high-speed Analog-to-Digital Converter (ADC)

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**Table 1** Output coding with differential inputs (typical values to AGND);  $V_{I(p-p)} - \bar{V}_{I(p-p)} = 2.0\text{ V}$ ;  $V_{ref} = V_{CCA} - 1.825\text{ V}$

| CODE      | $V_{I(p-p)}$ | $\bar{V}_{I(p-p)}$ | IR | BINARY OUTPUTS | TWOS COMPLEMENT OUTPUTS |
|-----------|--------------|--------------------|----|----------------|-------------------------|
|           |              |                    |    | D11 TO D0      | D11 TO D0               |
| Underflow | <3.1         | >4.1               | 0  | 000000000000   | 100000000000            |
| 0         | 3.1          | 4.1                | 1  | 000000000000   | 100000000000            |
| 1         | –            | –                  | 1  | 000000000001   | 100000000001            |
| ↓         | –            | –                  | ↓  | ↓              | ↓                       |
| 2047      | 3.6          | 3.6                | 1  | 011111111111   | 111111111111            |
| ↓         | –            | –                  | ↓  | ↓              | ↓                       |
| 4094      | –            | –                  | 1  | 111111111110   | 011111111110            |
| 4095      | 4.1          | 3.1                | 1  | 111111111111   | 011111111111            |
| Overflow  | >4.1         | <3.1               | 0  | 111111111111   | 011111111111            |

**Table 2** Mode selection

| OTC              | $\bar{CE}$ | D0 TO D11 AND IR        |
|------------------|------------|-------------------------|
| 0                | 0          | binary; active          |
| 1                | 0          | twos complement; active |
| X <sup>(1)</sup> | 1          | high impedance          |

**Note**

1. X = don't care.

**Table 3** Sample-and-hold selection

| SH | SAMPLE-AND-HOLD         |
|----|-------------------------|
| 1  | active                  |
| 0  | inactive; tracking mode |

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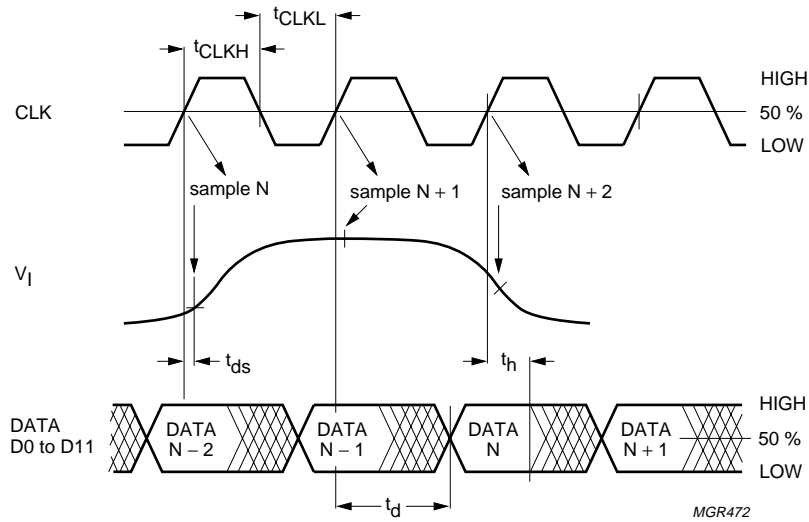
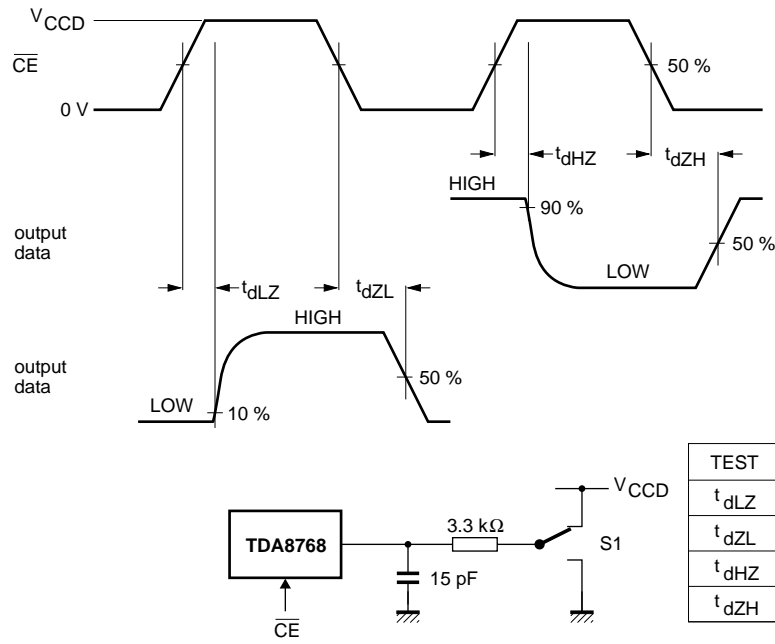


Fig.3 Timing diagram.



$f_{\overline{CE}} = 100 \text{ kHz}$ .

Fig.4 Timing diagram and test conditions of 3-state output delay time.

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## APPLICATION INFORMATION

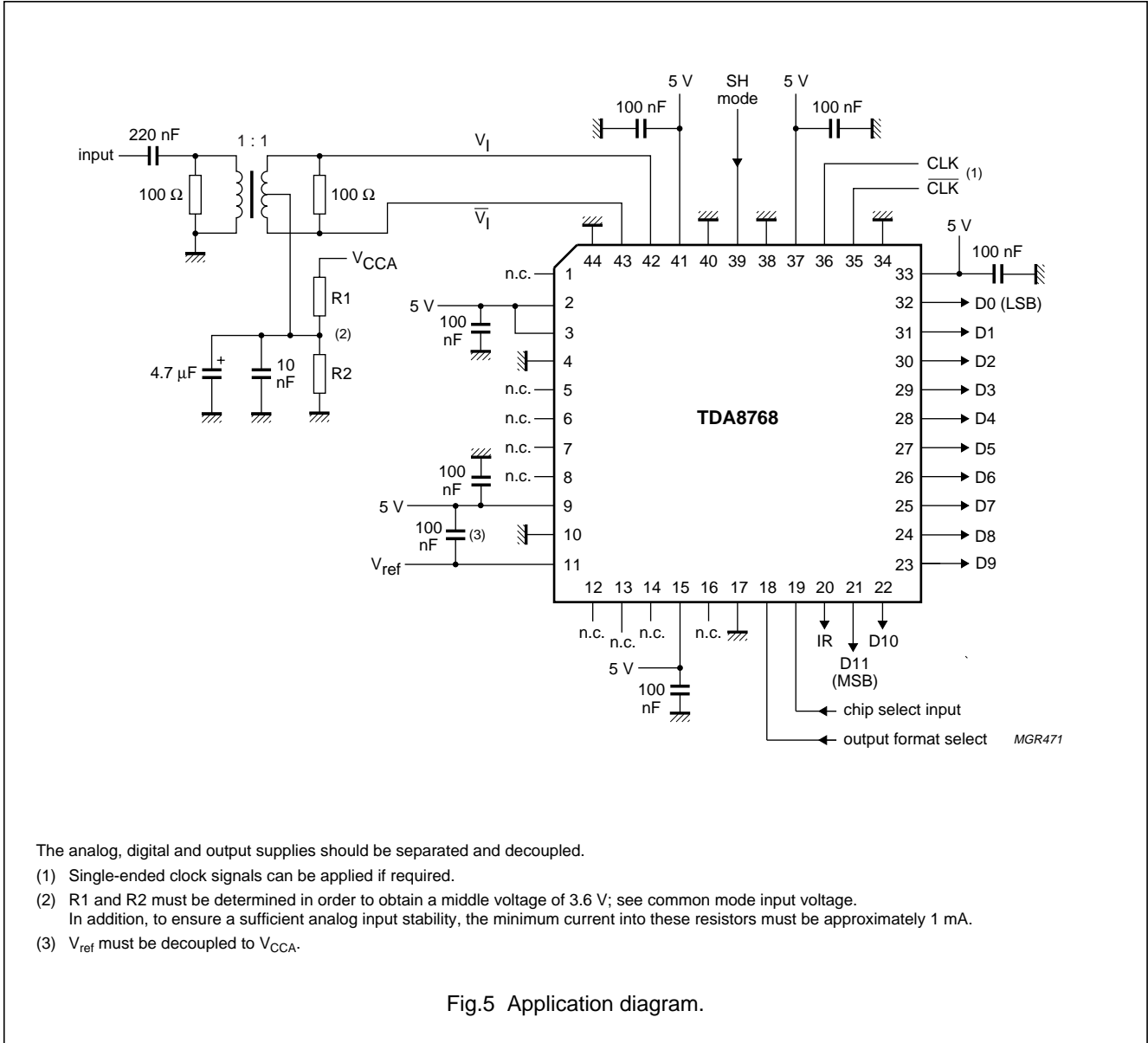
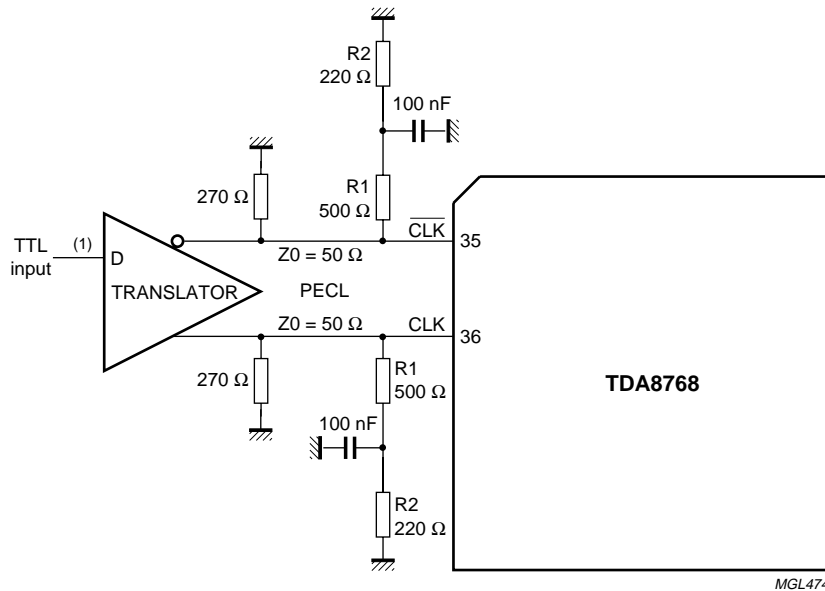


Fig.5 Application diagram.

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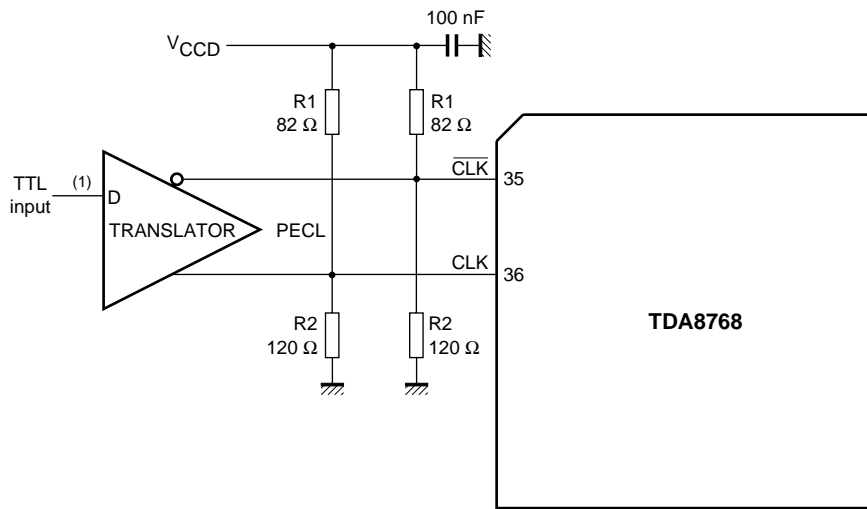


MGL474

If the clock lines are more than 1 inch long they must be matched. In fact, the 27 Ω resistor will be changed by the series connection of R1 and R2, with R1 = Z<sub>0</sub> placed close to pins CLK and CLK.

(1) 50 Ω matched line (Z<sub>0</sub>, L).

Fig.6 Application diagram for differential clock input (PECL-compatible) using a TTL to PECL translator.



MGL473

The value of R1 and R2 must be chosen in order to meet the following relations:

$$3\text{ V} = \frac{V_{\text{CCD}} \times R2}{R1 + R2} \text{ and } Z0 = \frac{R1 \times R2}{R1 + R2}$$

(1) 50 Ω matched line (Z<sub>0</sub>, L).

Fig.7 Application diagram for differential clock input (PECL-compatible) using a TTL to PECL translator and Thevenin parallel terminations.

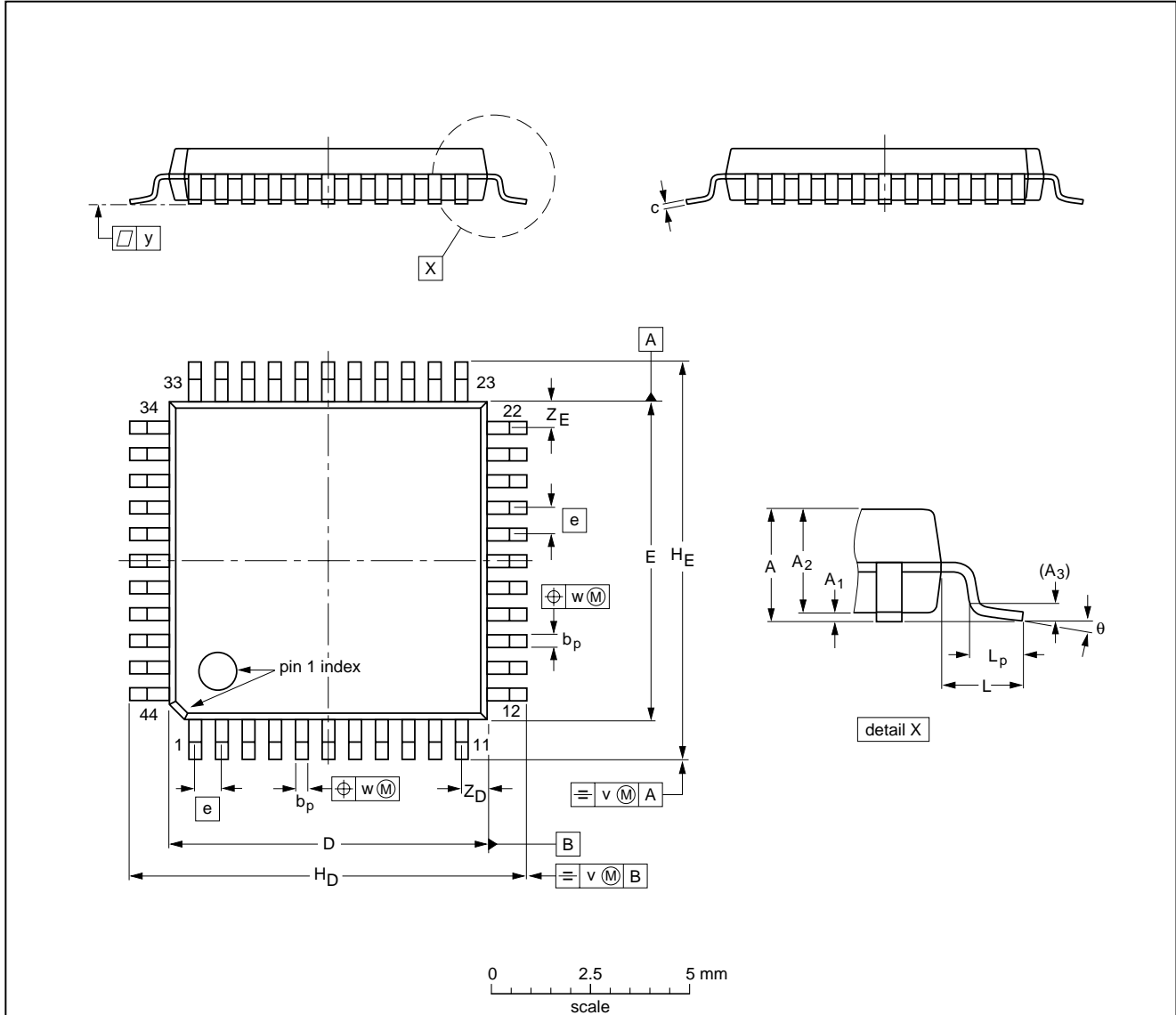
# 12-bit high-speed Analog-to-Digital Converter (ADC)

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## PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e   | H <sub>D</sub> | H <sub>E</sub> | L   | L <sub>p</sub> | v    | w    | y   | Z <sub>D</sub> <sup>(1)</sup> | Z <sub>E</sub> <sup>(1)</sup> | θ         |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|------|------|-----|-------------------------------|-------------------------------|-----------|
| mm   | 2.10   | 0.25<br>0.05   | 1.85<br>1.65   | 0.25           | 0.40<br>0.20   | 0.25<br>0.14 | 10.1<br>9.9      | 10.1<br>9.9      | 0.8 | 12.9<br>12.3   | 12.9<br>12.3   | 1.3 | 0.95<br>0.55   | 0.15 | 0.15 | 0.1 | 1.2<br>0.8                    | 1.2<br>0.8                    | 10°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |       |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|-------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC | EIAJ |  |                     |                      |
| SOT307-2        |            |       |      |  |                     | 95-02-04<br>97-08-01 |

# 12-bit high-speed Analog-to-Digital Converter (ADC)

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## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

### Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

|  |
|--|
| <b>CAUTION</b>   |
| <b>Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.</b> |



# 12-bit high-speed Analog-to-Digital Converter (ADC)

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## DEFINITIONS

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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**NOTES**

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**NOTES**

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