μPD71641
Cache Memory Controller

Description

The μPD71641 is an LSI cache controller chip offering advanced features, unequaled flexibility, and built-in reliability to system designers. The μPD71641 makes it practical and economical to use sophisticated caches in microprocessor-based systems.

The implementation of μPD71641 is transparent to the application program. The μPD71641 is configurable from direct-mapped to 4-way set-associative mapping. The μPD71641 allows up to 128K bytes of cache memory. Cache updating is made efficient with sub-block partition and burst mode features.

The μPD71641 can be easily used with many general-purpose, high-performance 32-bit or 16-bit microprocessors. Its architecture is suitable for multiprocessors and multimaster environments. Cache data consistency is ensured by bus monitoring and dual comparator techniques. The μPD71641 uses a write-through strategy to update main memory, which guarantees the best cache consistency in a multiprocessor and multimaster system. External data storage is flexible in size and organization. The μPD71641 will work with any word width.

The μPD71641 is unique in offering features to implement a highly reliable cache memory subsystem. The μPD71641 provides built-in reliability checks, such as address tag parity check, multiple hit detection, and self-diagnosis for directory faults. Upon detection of an erroneous condition, the μPD71641 can either be disabled, or continue to operate in a functionally degraded mode.

Features

- General-purpose interface supports high-performance microprocessors
- Transparent to application programs
- Flexible placement algorithm: direct 2-, 4-way set-associative
- Large tag memory configuration:
  - 1024 sets x 1 way x 2 sub-blocks
  - 512 sets x 2 ways x 2 sub-blocks
  - 256 sets x 4 ways x 2 sub-blocks
- Programmable sub-block size up to 64 bytes
- Bus replacement cycle variable from 1 to 16 words
- Supports large cache memory up to 128K bytes
- Supports up to 4G bytes of main memory
- LRU replacement algorithm
- Write-through strategy
- Data consistency check by bus monitoring
- External PURGE input to flush tag store
- Increased reliability through internal error detection
  - Parity check on tag store
  - Incorrect match check
  - Multiple hit check
  - LRU output check
- Unique level degradation feature to maximize cache system up time
- 16- and 20-MHz operation
- 132-pin PGA package

Ordering Information

Part Number	Max Clockout Frequency	Package
μPD71641R	20 MHz	132-pin Ceramic PGA

Block Diagram