SSD0859

Advance Information

128 x 80 STN
LCD Segment / Common 4 G/S Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SOLOMON SYSTECH

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1. GENERAL DESCRIPTION

SSD0859 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. SSD0859 consists of 210 high voltage driving output pins for driving 128 Segments and 80 Commons and 1 icon line.

SSD0859 display data directly from its internal 128x81x2 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through I^2C interface.

SSD0859 embeds a DC-DC Converter, a LCD Voltage Regulator, an On-Chip Bias Divider, integrated bias capacitors, integrated booster capacitors and an On-Chip Oscillator, which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD0859 is suitable for any portable battery-driven applications requiring long operation period and compact size.

2. FEATURES

128x80 + 1 icon line, 4 gray-levels Graphic Display
Programmable Multiplex ratio [16Mux - 81Mux]
Single Supply Operation, 1.8 V - 3.3V
Low Current Sleep Mode
On-Chip Voltage Generator / External Power Supply
Software selectable 3X / 4X / 5X / 6X On-Chip DC-DC Converter
On-Chip Oscillator
On-Chip Bias Dividers
Programmable 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 and 1/10 bias ratio
Maximum +15.0V LCD Driving Output Voltage
I^2C interface
On-Chip 128x81x2 Graphic Display Data RAM
Re-mapping of Row and Column Drivers
Vertical Scrolling
Display Offset Control
Maximum 1MHz I^2C interface
64 Level Internal Contrast Control
External Contrast Control
Selectable LCD Driving Voltage Temperature Coefficients (2 settings)
Available in Gold Bump Die

3. ORDERING INFORMATION

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD0859Z	128	80 + 1	Gold Bump Die	Figure 2 on Page 7	-

Table 1 - Ordering Information

4. BLOCK DIAGRAM

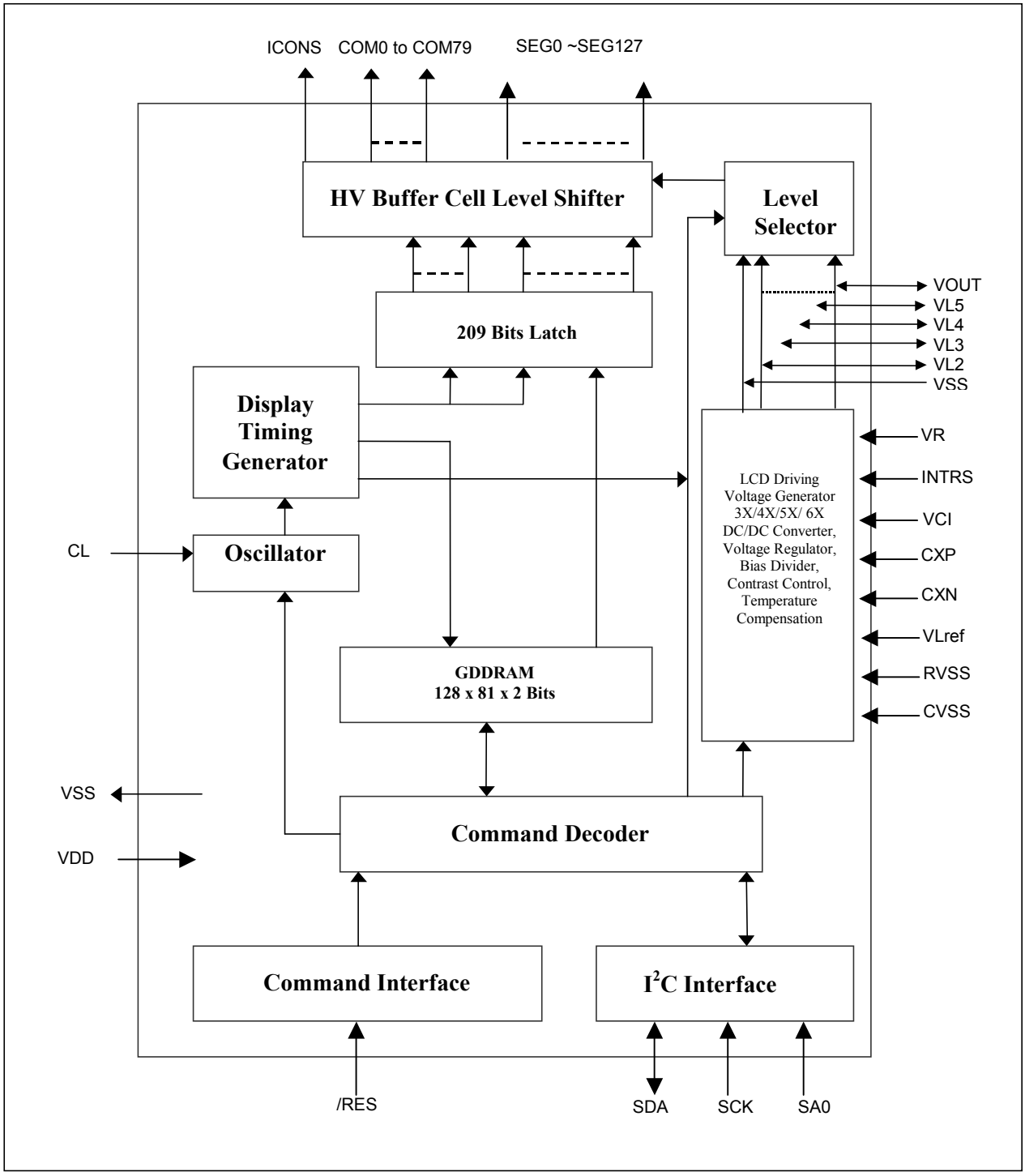
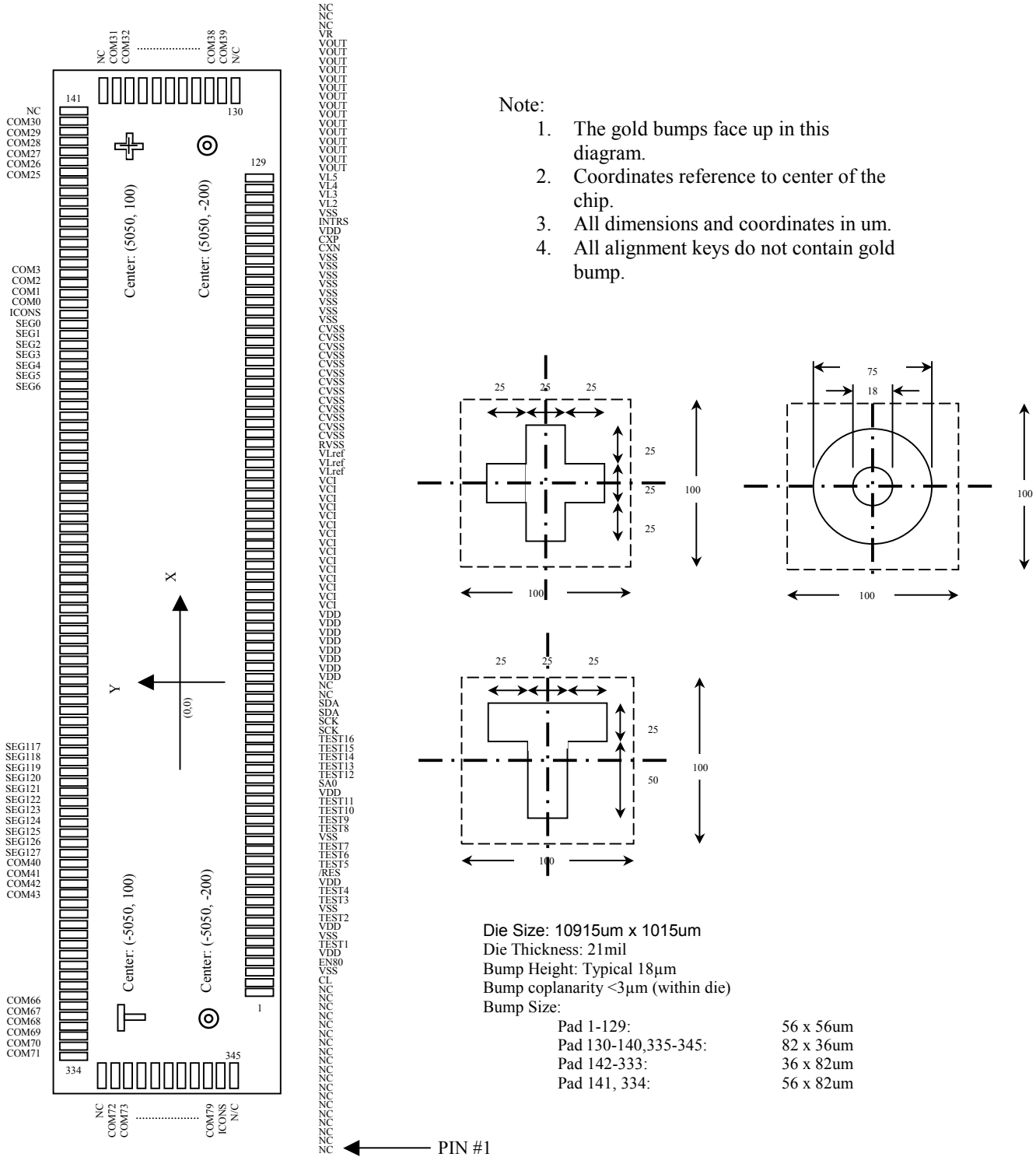


Figure 1 - SSD0859 Block Diagram

5. DIE PAD ARRANGEMENT (SSD0859Z DIE PIN ASSIGNMENT)



Note:

1. The gold bumps face up in this diagram.
2. Coordinates reference to center of the chip.
3. All dimensions and coordinates in um.
4. All alignment keys do not contain gold bump.

Die Size: 10915um x 1015um
Die Thickness: 21mil
Bump Height: Typical 18µm
Bump coplanarity <3µm (within die)
Bump Size:

Pad 1-129:	56 x 56um
Pad 130-140,335-345:	82 x 36um
Pad 142-333:	36 x 82um
Pad 141, 334:	56 x 82um

Figure 2 - SSD0859 Die Pad Floor Plan

Table 2 - SSD0859 Die Pad Coordinates

Pad#	Signal	X-pos	Y-pos
1	NC	-4883.2	-353.5
2	NC	-4806.9	-353.5
3	NC	-4730.6	-353.5
4	NC	-4654.3	-353.5
5	NC	-4578.0	-353.5
6	NC	-4501.7	-353.5
7	NC	-4425.4	-353.5
8	NC	-4349.1	-353.5
9	NC	-4272.8	-353.5
10	NC	-4196.5	-353.5
11	NC	-4120.2	-353.5
12	NC	-4043.9	-353.5
13	NC	-3967.6	-353.5
14	NC	-3891.3	-353.5
15	NC	-3815.0	-353.5
16	NC	-3738.7	-353.5
17	NC	-3662.4	-353.5
18	NC	-3586.1	-353.5
19	NC	-3509.8	-353.5
20	CL	-3433.5	-353.5
21	VSS	-3357.2	-353.5
22	EN80	-3280.9	-353.5
23	VDD	-3204.6	-353.5
24	TEST1	-3128.3	-353.5
25	VSS	-3052.0	-353.5
26	VDD	-2975.7	-353.5
27	TEST2	-2899.4	-353.5
28	VSS	-2823.1	-353.5
29	TEST3	-2746.8	-353.5
30	TEST4	-2670.5	-353.5
31	VDD	-2594.2	-353.5
32	/RES	-2517.9	-353.5
33	TEST5	-2441.6	-353.5
34	TEST6	-2365.3	-353.5
35	TEST7	-2289.0	-353.5
36	VSS	-2212.7	-353.5
37	TEST8	-2136.4	-353.5
38	TEST9	-2060.1	-353.5
39	TEST10	-1983.8	-353.5
40	TEST11	-1907.5	-353.5
41	VDD	-1831.2	-353.5
42	SA0	-1754.9	-353.5
43	TEST12	-1678.6	-353.5
44	TEST13	-1602.3	-353.5
45	TEST14	-1526.0	-353.5
46	TEST15	-1449.7	-353.5
47	TEST16	-1373.4	-353.5
48	SCK	-1297.1	-353.5
49	SCK	-1220.8	-353.5
50	SDA	-1144.5	-353.5
51	SDA	-1068.2	-353.5
52	NC	-991.9	-353.5
53	NC	-915.6	-353.5
54	VDD	-839.3	-353.5
55	VDD	-763.0	-353.5
56	VDD	-686.7	-353.5
57	VDD	-610.4	-353.5
58	VDD	-534.1	-353.5
59	VDD	-457.8	-353.5
60	VDD	-381.5	-353.5
61	VDD	-305.2	-353.5
62	VCI	-228.9	-353.5
63	VCI	-152.6	-353.5
64	VCI	-76.3	-353.5
65	VCI	0.0	-353.5
66	VCI	76.3	-353.5
67	VCI	152.6	-353.5
68	VCI	228.9	-353.5
69	VCI	305.2	-353.5
70	VCI	381.5	-353.5
71	VCI	457.8	-353.5
72	VCI	534.1	-353.5
73	VCI	610.4	-353.5
74	VCI	686.7	-353.5
75	VCI	763.0	-353.5
76	VCI	839.3	-353.5
77	VLref	915.6	-353.5
78	VLref	991.9	-353.5
79	VLref	1068.2	-353.5
80	RVSS	1144.5	-353.5
81	CVSS	1220.8	-353.5
82	CVSS	1297.1	-353.5
83	CVSS	1373.4	-353.5
84	CVSS	1449.7	-353.5
85	CVSS	1526.0	-353.5
86	CVSS	1602.3	-353.5
87	CVSS	1678.6	-353.5
88	CVSS	1754.9	-353.5
89	CVSS	1831.2	-353.5
90	CVSS	1907.5	-353.5
91	CVSS	1983.8	-353.5
92	CVSS	2060.1	-353.5
93	CVSS	2136.4	-353.5
94	VSS	2212.7	-353.5
95	VSS	2289.0	-353.5
96	VSS	2365.3	-353.5
97	VSS	2441.6	-353.5
98	VSS	2517.9	-353.5
99	VSS	2594.2	-353.5
100	VSS	2670.5	-353.5
101	VSS	2746.8	-353.5
102	CXN	2823.1	-353.5
103	CXP	2899.4	-353.5
104	VDD	2975.7	-353.5
105	INTRS	3052.0	-353.5
106	VSS	3128.3	-353.5
107	VL2	3204.6	-353.5
108	VL3	3280.9	-353.5
109	VL4	3357.2	-353.5
110	VL5	3433.5	-353.5
111	VOUT	3509.8	-353.5
112	VOUT	3586.1	-353.5
113	VOUT	3662.4	-353.5
114	VOUT	3738.7	-353.5
115	VOUT	3815.0	-353.5
116	VOUT	3891.3	-353.5
117	VOUT	3967.6	-353.5
118	VOUT	4043.9	-353.5
119	VOUT	4120.2	-353.5
120	VOUT	4196.5	-353.5
121	VOUT	4272.8	-353.5
122	VOUT	4349.1	-353.5
123	VOUT	4425.4	-353.5
124	VOUT	4501.7	-353.5
125	VOUT	4578.0	-353.5
126	VR	4654.3	-353.5
127	NC	4730.6	-353.5
128	NC	4806.9	-353.5
129	NC	4883.2	-353.5
130	NC	5290.5	-364.3
131	COM39	5290.5	-309.7

Pad#	Signal	X-pos	Y-pos
132	COM38	5290.5	-255.1
133	COM37	5290.5	-200.5
134	COM36	5290.5	-145.9
135	COM35	5290.5	-91.3
136	COM34	5290.5	-36.7
137	COM33	5290.5	17.9
138	COM32	5290.5	72.5
139	COM31	5290.5	127.1
140	NC	5290.5	181.7
141	NC	5275.9	341.5
142	COM30	5214.3	341.5
143	COM29	5159.7	341.5
144	COM28	5105.1	341.5
145	COM27	5050.5	341.5
146	COM26	4995.9	341.5
147	COM25	4941.3	341.5
148	COM24	4886.7	341.5
149	COM23	4832.1	341.5
150	COM22	4777.5	341.5
151	COM21	4722.9	341.5
152	COM20	4668.3	341.5
153	COM19	4613.7	341.5
154	COM18	4559.1	341.5
155	COM17	4504.5	341.5
156	COM16	4449.9	341.5
157	COM15	4395.3	341.5
158	COM14	4340.7	341.5
159	COM13	4286.1	341.5
160	COM12	4231.5	341.5
161	COM11	4176.9	341.5
162	COM10	4122.3	341.5
163	COM9	4067.7	341.5
164	COM8	4013.1	341.5
165	COM7	3958.5	341.5
166	COM6	3903.9	341.5
167	COM5	3849.3	341.5
168	COM4	3794.7	341.5
169	COM3	3740.1	341.5
170	COM2	3685.5	341.5
171	COM1	3630.9	341.5
172	COM0	3576.3	341.5
173	ICONS	3521.7	341.5
174	SEG0	3467.1	341.5
175	SEG1	3412.5	341.5
176	SEG2	3357.9	341.5
177	SEG3	3303.3	341.5
178	SEG4	3248.7	341.5
179	SEG5	3194.1	341.5
180	SEG6	3139.5	341.5
181	SEG7	3084.9	341.5
182	SEG8	3030.3	341.5
183	SEG9	2975.7	341.5
184	SEG10	2921.1	341.5
185	SEG11	2866.5	341.5
186	SEG12	2811.9	341.5
187	SEG13	2757.3	341.5
188	SEG14	2702.7	341.5
189	SEG15	2648.1	341.5
190	SEG16	2593.5	341.5
191	SEG17	2538.9	341.5
192	SEG18	2484.3	341.5
193	SEG19	2429.7	341.5
194	SEG20	2375.1	341.5
195	SEG21	2320.5	341.5
196	SEG22	2265.9	341.5
197	SEG23	2211.3	341.5
198	SEG24	2156.7	341.5
199	SEG25	2102.1	341.5
200	SEG26	2047.5	341.5
201	SEG27	1992.9	341.5
202	SEG28	1938.3	341.5
203	SEG29	1883.7	341.5
204	SEG30	1829.1	341.5
205	SEG31	1774.5	341.5
206	SEG32	1719.9	341.5
207	SEG33	1665.3	341.5
208	SEG34	1610.7	341.5
209	SEG35	1556.1	341.5
210	SEG36	1501.5	341.5
211	SEG37	1446.9	341.5
212	SEG38	1392.3	341.5
213	SEG39	1337.7	341.5
214	SEG40	1283.1	341.5
215	SEG41	1228.5	341.5
216	SEG42	1173.9	341.5
217	SEG43	1119.3	341.5
218	SEG44	1064.7	341.5
219	SEG45	1010.1	341.5
220	SEG46	955.5	341.5
221	SEG47	900.9	341.5
222	SEG48	846.3	341.5
223	SEG49	791.7	341.5
224	SEG50	737.1	341.5
225	SEG51	682.5	341.5
226	SEG52	627.9	341.5
227	SEG53	573.3	341.5
228	SEG54	518.7	341.5
229	SEG55	464.1	341.5
230	SEG56	409.5	341.5
231	SEG57	354.9	341.5
232	SEG58	300.3	341.5
233	SEG59	245.7	341.5
234	SEG60	191.1	341.5
235	SEG61	136.5	341.5
236	SEG62	81.9	341.5
237	SEG63	27.3	341.5
238	SEG64	-27.3	341.5
239	SEG65	-81.9	341.5
240	SEG66	-136.5	341.5
241	SEG67	-191.1	341.5
242	SEG68	-245.7	341.5
243	SEG69	-300.3	341.5
244	SEG70	-354.9	341.5
245	SEG71	-409.5	341.5
246	SEG72	-464.1	341.5
247	SEG73	-518.7	341.5
248	SEG74	-573.3	341.5
249	SEG75	-627.9	341.5
250	SEG76	-682.5	341.5
251	SEG77	-737.1	341.5
252	SEG78	-791.7	341.5
253	SEG79	-846.3	341.5
254	SEG80	-900.9	341.5
255	SEG81	-955.5	341.5
256	SEG82	-1010.1	341.5
257	SEG83	-1064.7	341.5
258	SEG84	-1119.3	341.5
259	SEG85	-1173.9	341.5
260	SEG86	-1228.5	341.5
261	SEG87	-1283.1	341.5
262	SEG88	-1337.7	341.5
263	SEG89	-1392.3	341.5
264	SEG90	-1446.9	341.5
265	SEG91	-1501.5	341.5

Pad#	Signal	X-pos	Y-pos
266	SEG92	-1556.1	341.5
267	SEG93	-1610.7	341.5
268	SEG94	-1665.3	341.5
269	SEG95	-1719.9	341.5
270	SEG96	-1774.5	341.5
271	SEG97	-1829.1	341.5
272	SEG98	-1883.7	341.5
273	SEG99	-1938.3	341.5
274	SEG100	-1992.9	341.5
275	SEG101	-2047.5	341.5
276	SEG102	-2102.1	341.5
277	SEG103	-2156.7	341.5
278	SEG104	-2211.3	341.5
279	SEG105	-2265.9	341.5
280	SEG106	-2320.5	341.5
281	SEG107	-2375.1	341.5
282	SEG108	-2429.7	341.5
283	SEG109	-2484.3	341.5
284	SEG110	-2538.9	341.5
285	SEG111	-2593.5	341.5
286	SEG112	-2648.1	341.5
287	SEG113	-2702.7	341.5
288	SEG114	-2757.3	341.5
289	SEG115	-2811.9	341.5
290	SEG116	-2866.5	341.5
291	SEG117	-2921.1	341.5
292	SEG118	-2975.7	341.5
293	SEG119	-3030.3	341.5
294	SEG120	-3084.9	341.5
295	SEG121	-3139.5	341.5
296	SEG122	-3194.1	341.5
297	SEG123	-3248.7	341.5
298	SEG124	-3303.3	341.5
299	SEG125	-3357.9	341.5
300	SEG126	-3412.5	341.5
301	SEG127	-3467.1	341.5
302	COM40	-3521.7	341.5
303	COM41	-3576.3	341.5
304	COM42	-3630.9	341.5
305	COM43	-3685.5	341.5
306	COM44	-3740.1	341.5
307	COM45	-3794.7	341.5
308	COM46	-3849.3	341.5
309	COM47	-3903.9	341.5
310	COM48	-3958.5	341.5

Pad#	Signal	X-pos	Y-pos
311	COM49	-4013.1	341.5
312	COM50	-4067.7	341.5
313	COM51	-4122.3	341.5
314	COM52	-4176.9	341.5
315	COM53	-4231.5	341.5
316	COM54	-4286.1	341.5
317	COM55	-4340.7	341.5
318	COM56	-4395.3	341.5
319	COM57	-4449.9	341.5
320	COM58	-4504.5	341.5
321	COM59	-4559.1	341.5
322	COM60	-4613.7	341.5
323	COM61	-4668.3	341.5
324	COM62	-4722.9	341.5
325	COM63	-4777.5	341.5
326	COM64	-4832.1	341.5
327	COM65	-4886.7	341.5
328	COM66	-4941.3	341.5
329	COM67	-4995.9	341.5
330	COM68	-5050.5	341.5
331	COM69	-5105.1	341.5
332	COM70	-5159.7	341.5
333	COM71	-5214.3	341.5
334	NC	-5275.9	341.5
335	NC	-5290.5	181.7
336	COM72	-5290.5	127.1
337	COM73	-5290.5	72.5
338	COM74	-5290.5	17.9
339	COM75	-5290.5	-36.7
340	COM76	-5290.5	-91.3
341	COM77	-5290.5	-145.9
342	COM78	-5290.5	-200.5
343	COM79	-5290.5	-255.1
344	ICONS	-5290.5	-309.7
345	NC	-5290.5	-364.3

6. PIN DESCRIPTIONS

$\overline{\text{RES}}$
This pin is reset signal input. When the pin is low, initialization of the chip is executed.

SDA, SCK & SA0
These pins are bi-directional data bus to be connected to the MCU in I^2C-bus interface. Please refer to the section: IIC Communication interface on page 13 for detail pin descriptions.

INTRS
This pin is an input pin to enable the internal resistor network for the voltage regulator when INTRS is high. When external regulator is used, this pin must be connected to VSS, and external resistor R1/R2 should be connected to VOUT, VR and VSS.

VDD
This pin is power supply.

VSS
This is a logic ground pin. It must connect to GND from external supply.

RVSS
This pin is the ground for internal voltage regulator. It must connect to same external GND of CVSS.

CVSS
This is an analog ground pin. It must connect to GND from external supply.

VLref
This pin is the reference voltage for internal operational amplifiers. It must connect to VDD / VSS depends on the panel loading. Connect to VSS for small panel, while connect to VDD for large panel.

VCI
Reference voltage input for internal DC-DC converter. The voltage of generated VOUT equals to the multiple factor (3X, 4X, 5X or 6X) times VCI with respect to VSS.
Note: voltage at this input pin must be larger than or equal to VDD.

CXP, CXN
Connect an external capacitor to these pins when 6X DC-DC Converter Factor is set.

VOUT
This pin is the most positive LCD driving voltage. It can be supplied externally or generated by the internal regulator.

VR
This pin is an input of the internal voltage regulator. When the internal resistors network for the voltage regulator is disabled (INTRS is pulled low), external resistors should be connected between VSS and VR, and VR and VOUT, respectively (Please refer to application circuit).

VL5, VL4, VL3 and VL2
These are LCD driving voltages. These pins should NOT be connected to any signal pins nor shorted together. They should be left open. They have the following relationship:
VOUT > VL5 > VL4 > VL3 > VL2 > VSS

	1:a bias
VL5	(a-1)/a*VOUT
VL4	(a-2)/a*VOUT
VL3	2/a*VOUT
VL2	1/a*VOUT

COM0 - COM79
These pins provide the row driving signal COM0 - COM79 to the LCD panel.

ICONS
This pin is the special icon line COM signal output.

SEG0 - SEG127
These pins provide the LCD column driving signal. Their voltage level is VSS during sleep mode and standby mode.

CL
This pin is the external clock input for the device if external clock mode is selected by software command. Under POR operation, this pin should be left opened and internal oscillator will be used after power on reset.

EN80
This pin must be connected to VDD.

TEST1, TEST3-TEST11
These pins should be connected to VSS.

TEST2, TEST12-TEST16
These pins can be either connected to VSS or VDD.

NC
These No Connection pins should NOT be connected to any signal pins nor shorted together. They should be left open.

7. FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder

Input is directed to the command decoder based on the input of control byte, which consists of a D/C bit and a R/W bit. For further information about the control byte, please refer to the section "I²C-bus Write data and read register status" on page 38. If both the D/C bit and the R/W bit are low, the input signal is interpreted as a Command. It will be decoded and written to the corresponding command register. If the D/C bit is high and the R/W bit is low, input signal is written to Graphic Display Data RAM (GDDRAM).

I²C communication Interface

The IIC communication interface consists of slave address bit (SA0), I²C-bus data signal (SDA) and I²C-bus clock signal (SCK). Both the SDA and the SCK must be connected to pull-up resistors. There is also an input signal $\overline{RES}$, which is used for the initialization of device.

a) Slave address bit (SA0)
   SSD0859 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W" bit) with the following byte format,
   b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
   0 1 1 1 1 0 SA0 R/W
   "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101" can be selected as the slave address of SSD0859.
   "R/W" bit determines the I²C-bus interface is operating at either write mode or read status mode.
b) I²C-bus data signal (SDA)
   SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
   It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
c) I²C-bus clock signal (SCK)
   The transmission of information in the I²C-bus is following a clock signal, SCK. Each transmission of data bit is taken place during a single clock period of SCK.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 81 x 2 = 20736bits. Figure 3 is a description of the GDDRAM address map. For mechanical flexibility, remapping on both Segment and Common outputs are provided respectively. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 3 shows the cases in which the display start line register are set at 48H.

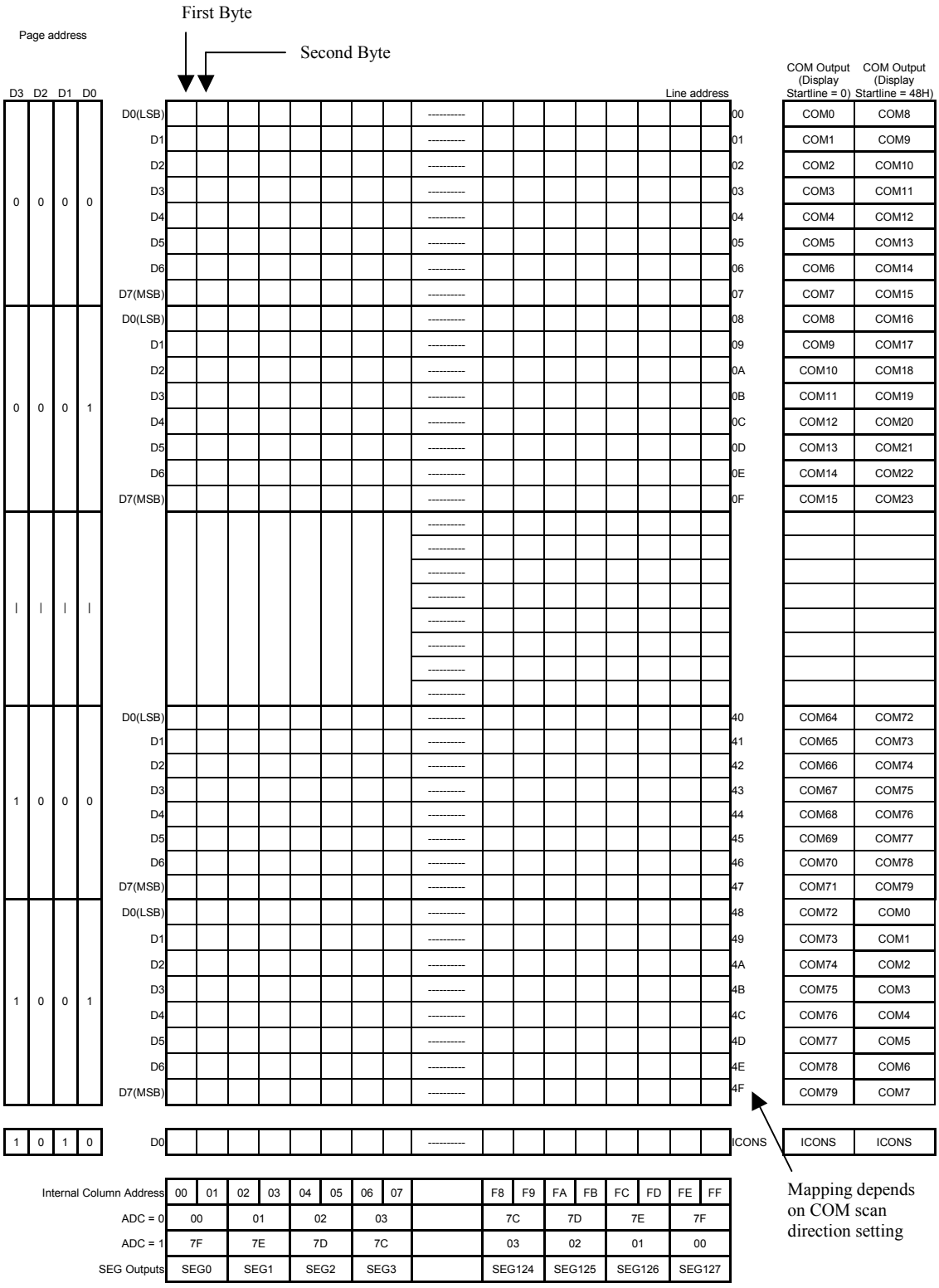


Figure 3 - Graphic Display Data RAM (GDDRAM) Address Map for SSD0859 (with vertical scroll value 48H)

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

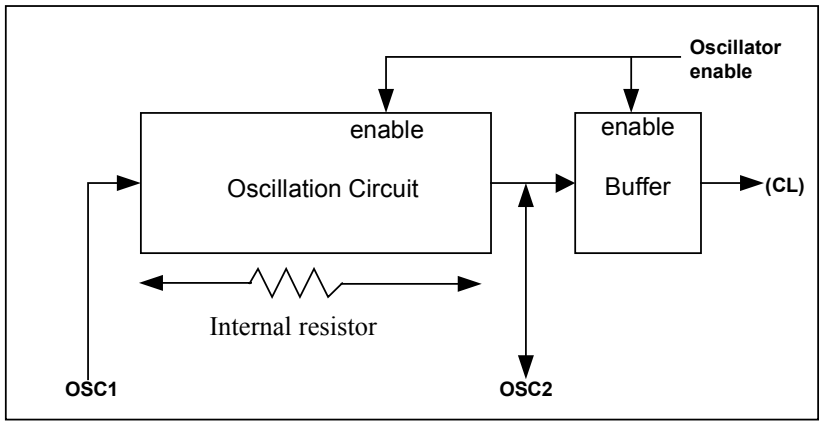


Figure 4 - Oscillator Circuitry

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

It consists of:

1. 3X, 4X, 5X and 6X DC-DC voltage converter
2. Bias Divider
   If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{out}) to give the LCD driving levels (V_{L2} - V_{L5}).
   The divider does not require external capacitors to reduce the external hardware and pin counts.
3. Contrast Control
   Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry
   Software control of 1/4 to 1/10 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry
   Provide 2 compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is -0.05%/°C.

209 Bit Latch

A register carries the display signal information. In 128X81 display mode, data will be fed to the HV-buffer Cell and level-shifted to the required level.

Level Selector

Level Selector is a control of the display synchronization.
Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

Reset Circuit

When $\overline{RES}$ input is low, the chip is initialized to the following:
1. Page address is set to 0
2. Column address is set to 0
3. Display is OFF
4. Display Start Line is set to 0 (GDDRAM page 0, D0)
5. Display Offset is set to 0 (COM0 is mapped to ROW0)
6. 128x80 display mode
7. Normal/Reverse Display is Normal
8. N-line Inversion Register is 0
9. Entire Display is OFF
10. Power Control Register (VC, VR, VF) is set to (0,0,0)
11. 3X Booster is selected
12. Internal Resistor Ratio register is set to 0H
13. Software Contrast is set to 32
14. LCD Bias Ratio is set to 1/10
15. Normal scan direction of COM outputs
16. Segment remap is disabled (SEG0 display column address 0)
17. Internal oscillator is OFF
18. Test mode is OFF
19. Temperature coefficient is set to PTC0 (-0.05%)
20. Icon display line is OFF

When RESET command is issued, the following parameters are initialized only:
1. Page address is set to 0
2. Column address is set to 0
3. Initial Display Line is set to 0 (point to display RAM page 0, D0)
4. Internal Resistor Ratio register is set to 0H
5. Software Contrast is set to 32

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 5 and 6 illustrate the desired multiplex scheme with N-line Inversion feature is disabled (default).

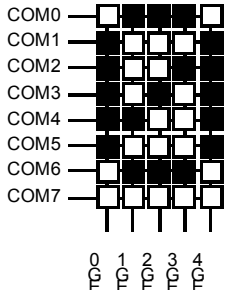
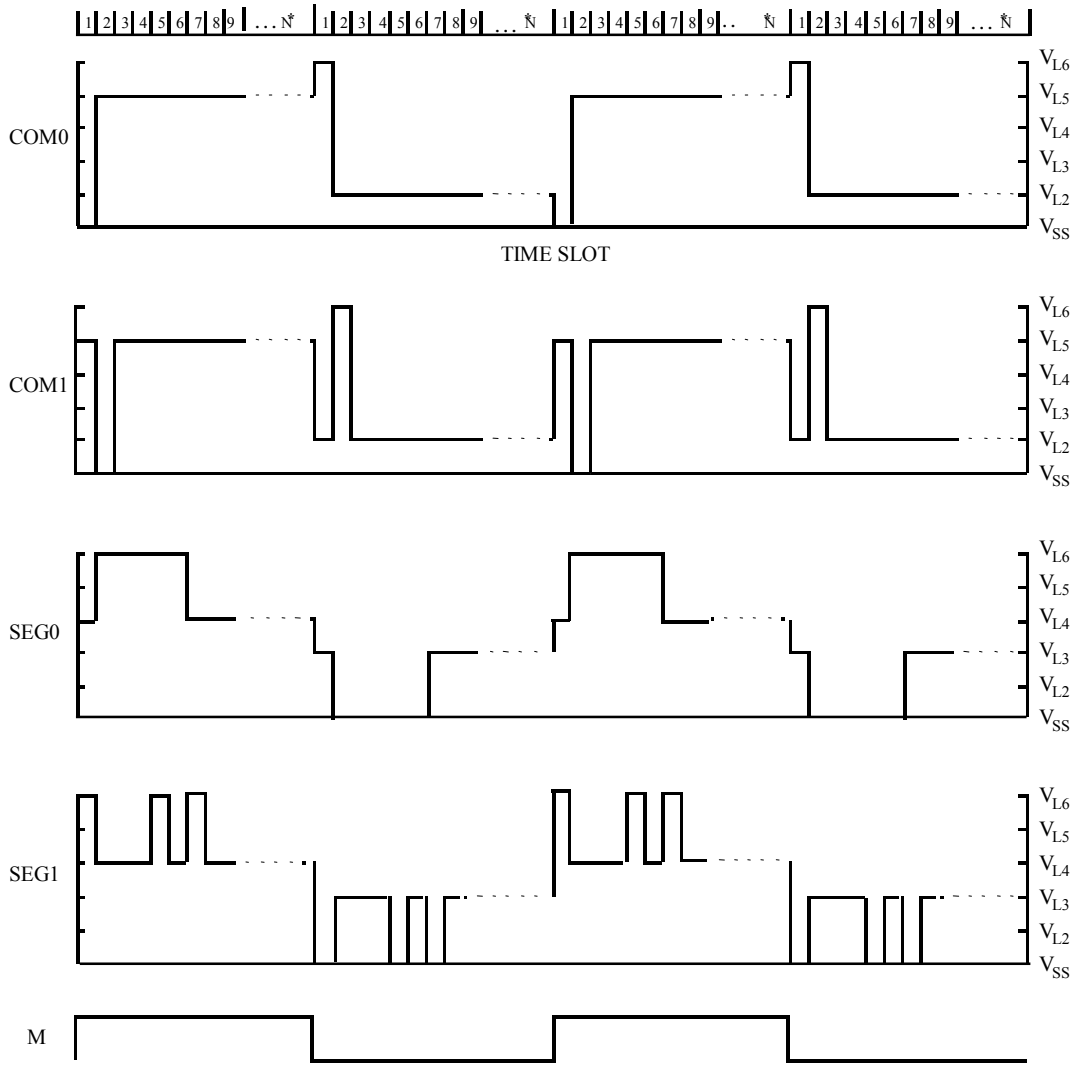


Figure 5 - LCD Display Example "0"



* Note: N is the number of multiplex ratio including Icon line. If it is enabled, N is equal to 80 on POR

Figure 6 - LCD Driving Signal From SSD0859

8. COMMAND TABLE

Table 3 - Command Table

Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
00~0F	0	0	0	0	C3	C2	C1	C0	Set Lower Column Address	Set the lower nibble of the column address pointer for RAM access. The pointer is reset to 0 after rest.
10~17	0	0	0	1	0	C6	C5	C4	Set Upper Column Address	Set the upper nibble of the column address pointer for RAM access. The pointer is reset to 0 after rest.
18~1F									Reserved	Reserved
20~27	0	0	1	0	0	R2	R1	R0	Set Internal Regulator Resistor Ratio	The internal regulator gain (1+R2/R1)Vout increases as R2R1R0 is increased from 000b to 111b. The factor, 1+R2/R1, is given by: R2R1R0 = 000: 2.84 (POR) R2R1R0 = 001: 3.71 R2R1R0 = 010: 4.57 R2R1R0 = 011: 5.44 R2R1R0 = 100: 6.30 R2R1R0 = 101: 7.16 R2R1R0 = 110: 8.03 R2R1R0 = 111: 8.89
28~2F	0	0	1	0	1	VC	VR	VF	Set Power Control Register	VC=0: turns OFF the internal voltage booster (POR) VC=1: turns ON the internal voltage booster VR=0: turns OFF the internal regulator (POR) VR=1: turns ON the internal regulator VF=0: turns OFF the output op-amp buffer (POR) VF=1: turns ON the output op-amp buffer
30~3F									Reserved	Reserved
40~43	0 X	1 L6	0 L5	0 L4	0 L3	0 L2	X L1	X L0	Set Display Start Line	The second command specifies the row address pointer (0-79) of the RAM data to be displayed in COM0. This command has no effect on ICONS. The pointer is set to 0 after reset.
44~47	0 X	1 C6	0 C5	0 C4	0 C3	1 C2	X C1	X C0	Set Display Offset	The second command specifies the mapping of first display line (COM0) to one of ROW0~79. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.
48~4B	0 X	1 D6	0 D5	0 D4	1 D3	0 D2	X D1	X D0	Set Multiplex Ratio	The second command specifies the number of lines, excluding ICONS, to be displayed. With Icon is disabled (POR), duties 1/16~1/80 could be selected. With Icon enabled, the available duty ratios are 1/17~ 1/81.

Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
4C~4F	0 X	1 X	0 X	0 N4	1 N3	1 N2	X N1	X N0	Set N-line Inversion	The second command sets the n-line inversion register from 3 to 33 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 3 lines to 33 lines respectively. Value 00000b disables the N-line inversion, which is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux (including the icon line) should NOT be a multiple of the lines of inversion (n).
50~56	0	1	0	1	0	B2	B1	B0	Set LCD Bias	Sets the LCD bias from 1/4 ~ 1/10 according to B2B1B0: 000: 1/4 bias 001: 1/5 bias 010: 1/6 bias 011: 1/7bias 100: 1/8 bias 101: 1/9 bias 110: 1/10 bias (POR)
57~63									Reserved	Reserved
64~67	0	1	1	0	0	1	B1	B0	Set DC-DC Converter Factor	Sets the DC-DC multiplying factor from 3X to 6X B1B0: 00: 3X (POR) 01: 4X 10: 5X 11: 6X
68~80									Reserved	Reserved
81	1 X	0 X	0 C5	0 C4	0 C3	0 C2	0 C1	1 C0	Set Contrast Control Register	The second command sets one of the 64 contrast levels. The darkness increase as the contrast level increase. The level is set to 32 after POR.
82	1 1	0 1	0 1	0 1	0 X3	0 X2	1 X1	0 X0	OTP Setting	Set the desired VOUT voltage value: 0000: original contrast 0001: original contrast +1 step 0010: original contrast +2 steps 0011: original contrast +3 steps 0100: original contrast +4 steps 0101: original contrast +5 steps 0110: original contrast +6 steps 0111: original contrast +7 steps 1000: original contrast -8 steps 1001: original contrast -7 steps 1010: original contrast -6 steps 1011: original contrast -5 steps 1100: original contrast -4 steps 1101: original contrast -3 steps 1110: original contrast -2 steps 1111: original contrast -1 step
83	1	0	0	0	0	0	1	1	OTP Programming	Please refer the sequence of OTP programming
84~87									Reserved	Reserved

Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
88	1 WB3	0 WB2	0 WB1	0 WB0	1 WA3	0 WA2	0 WA1	0 WA0	Set White mode, Frame 2nd & 1st	Set gray scale mode and register. These are two-byte commands used to specify the contrast levels for the gray scale, 4 levels available. After power on reset, WA0~3 = WB0~3 = WC0~3 = WD0~3 = 0000 LA0~3 = LB0~3 = LC0~3 = LD0~3 = 0000 DA0~3 = DB0~3 = DC0~3 = DD0~3 = 1111 BA0~3 = BB0~3 = BC0~3 = BD0~3 = 1111
89	1 WD3	0 WD2	0 WD1	0 WD0	1 WC3	0 WC2	0 WC1	1 WC0	Set White mode, Frame 4th & 3rd	
8A	1 LB3	0 LB2	0 LB1	0 LB0	1 LA3	0 LA2	1 LA1	0 LA0	Set Light Gray mode, Frame 2nd & 1st	
8B	1 LD3	0 LD2	0 LD1	0 LD0	1 LC3	0 LC2	1 LC1	1 LC0	Set Light Gray mode, Frame 4th & 3rd	
8C	1 DB3	0 DB2	0 DB1	0 DB0	1 DA3	1 DA2	0 DA1	0 DA0	Set Dark Gray mode, Frame 2nd & 1st	
8D	1 DD3	0 DD2	0 DD1	0 DD0	1 DC3	1 DC2	0 DC1	1 DC0	Set Dark Gray mode, Frame 4th & 3rd	
8E	1 BB3	0 BB2	0 BB1	0 BB0	1 BA3	1 BA2	1 BA1	0 BA0	Set Black mode, Frame 2nd & 1st	
8F	1 BD3	0 BD2	0 BD1	0 BD0	1 BC3	1 BC2	1 BC1	1 BC0	Set Black mode, Frame 4th & 3rd	
90~97	1	0	0	1	0	FRC	PWM1	PWM0	Set PWM and FRC	Sets PWM and FRC for gray-scale operation. FRC = 0 : 4-frame (POR) FRC = 1 : 3-frame PWM1 PWM0 = 00 & 01 : 9-levels (POR) PWM1 PWM0 = 10 : 12-levels PWM1 PWM0 = 11 : 15-levels
98~9F									Reserved	Reserved
A0~A1	1	0	1	0	0	0	0	S0	Set Segment Re-map	S0=0: column address 00H is mapped to SEG0 (POR) S0=1: column address 7FH is mapped to SEG0
A2~A3	1	0	1	0	0	0	1	C0	Set Icon Enable	C0=0: Disable icon row (Mux = 16 to 80, POR) C0=1: Enable icon row (Mux = 17 to 81)
A4~A5	1	0	1	0	0	1	0	E0	Set Entire Display On/Off	E0=0: Normal display (display according to RAM contents, POR) E0=1: All pixels are ON regardless of the RAM contents *Note: This command will override the effect of “Set Normal/Inverse Display”
A6~A7	1	0	1	0	0	1	1	R0	Set Normal/Inverse Display	R0=0: Normal display (display according to RAM contents, POR) R0=1: Inverse display (ON and OFF pixels are inverted) *Note: This command will not affect the display of the icon line
A8~A9	1	0	1	0	1	0	0	S0	Set Power Save Mode	S0=0: Standby mode (POR) S0=1: Sleep mode

Memory Content		Gray Mode
1st Byte	2nd Byte	
0	0	White
0	1	Light Gray
1	0	Dark Gray
1	1	Black

Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
AA									Reserved	Reserved
AB	1	0	1	0	1	0	1	1	Start Internal Oscillator	This command starts the internal oscillator. Note that the oscillator is OFF after reset, so this instruction must be executed for initialization.
AC~AD									Reserved	Reserved
AE~AF	1	0	1	0	1	1	1	D0	Set Display On/Off	D0=0: Display OFF (POR) D0=1: Display ON
B0~BF	1	0	1	1	P3	P2	P1	P0	Set Page Address	Set GDDRAM page address (0~10) using P3P2P1P0 for RAM access. The page address is sets to 0 after reset.
C0~CF	1	1	0	0	S0	X	X	X	Set COM Output Scan Direction	S0=0: Normal mode (POR) S0=1: Remapped mode. COM0 to COM[N-1] becomes COM[N-1] to COM0 when the duty is set to N. See Figure 3 as an example for N equals to 80. *Note: This command will not affect the display of the icon lines
D0~E0									Reserved	Reserved
E1	1	1	1	0	0	0	0	1	Exit Power-save Mode	DC-DC converter, regulator and divider status before entering the power-save mode is restored. At POR, Power-save Mode is released.
E2	1	1	1	0	0	0	1	0	Software Reset	Initialize some internal registers
E3									Reserved	Reserved
E4	1	1	1	0	0	1	0	0	Exit N-line Inversion	The frame will be inverted once per frame
E5~E7									Reserved	Reserved
E9~EF									Reserved	Reserved
F0~FF	1	1	1	1	X	X	X	X	Extended Features	Test mode commands and Extended features, see Extended Command Table.

9. Extended Command Table

Table 4 - Extended Command Table

Bit Pattern	Command	Description
11110001 00001 $X_2X_1X_0$	$X_2X_1X_0$: Set TC Value	$X_2X_1X_0$ = 000: -0.05%/°C (POR) $X_2X_1X_0$ = 001: -0.07%/°C
11110111 0000000 X_0	Select Oscillator Source	X_0 = 0: Internal RC oscillator is selected (POR) X_0 = 1: External oscillator from CL pin is selected
11110010 00000 $X_2X_1X_0$	Oscillator Adjustment	$X_2X_1X_0$ = 000: -14.5% $X_2X_1X_0$ = 001: -10% $X_2X_1X_0$ = 011: 0 (POR) $X_2X_1X_0$ = 000: +7.5% $X_2X_1X_0$ = 000: +15.5% $X_2X_1X_0$ = 000: +26% $X_2X_1X_0$ = 000: +36%

Bit Pattern	Command	Description
11111101 xxxx0 $X_2$10	Lock / Unlock Interface	X_2 = 0 : Unlock the IC. The driver accepts any command and data written. X_2 = 1 : Lock the IC. The driver ignores all command and data written, except the unlock command or pin reset.
11110110 000 $X_4X_3X_2X_1X_0$	Frame Frequency Adjust (Please find the default setting in the following table)	**FRAMEFQ** $X_2X_1X_0$ = 000: 0 $X_2X_1X_0$ = 001: 1 $X_2X_1X_0$ = 010: 2 $X_2X_1X_0$ = 011: 3 $X_2X_1X_0$ = 100: 4 $X_2X_1X_0$ = 101: 5 $X_2X_1X_0$ = 110: 6 $X_2X_1X_0$ = 111: 7 **Fosc** X_4X_3 = 00: 58kHz X_4X_3 = 01: 77kHz X_4X_3 = 10: 92kHz X_4X_3 = 11: 115kHz
11110101 1000 $X_3$010	Low Power mode	X_3 = 1: Disable Low Power mode (POR) X_3 = 0: Enable Low Power mode
11111100 $X_7X_6X_5X_4X_3X_2X_1X_0$	Crosstalk Compensation	**Upper bits Adjustment** $X_7X_6X_5X_4$ = 0000: No adjustment (POR) $X_7X_6X_5X_4$ = 0001: + 1 step $X_7X_6X_5X_4$ = 0010: + 2 steps $X_7X_6X_5X_4$ = 0011: + 3 steps $X_7X_6X_5X_4$ = 0100: + 4 steps $X_7X_6X_5X_4$ = 0101: + 5 steps $X_7X_6X_5X_4$ = 0110: + 6 steps $X_7X_6X_5X_4$ = 0111: + 7 steps $X_7X_6X_5X_4$ = 1000: - 7 steps $X_7X_6X_5X_4$ = 1001: - 7 steps $X_7X_6X_5X_4$ = 1010: - 6 steps $X_7X_6X_5X_4$ = 1011: - 5 steps $X_7X_6X_5X_4$ = 1100: - 4 steps $X_7X_6X_5X_4$ = 1101: - 3 steps $X_7X_6X_5X_4$ = 1110: - 2 steps $X_7X_6X_5X_4$ = 1111: - 1 step **Lower bits Adjustment** $X_3X_2X_1X_0$ = 0000: No adjustment (P0R) $X_3X_2X_1X_0$ = 0001: + 1 step $X_3X_2X_1X_0$ = 0010: + 2 steps $X_3X_2X_1X_0$ = 0011: + 3 steps $X_3X_2X_1X_0$ = 0100: + 4 steps $X_3X_2X_1X_0$ = 0101: + 5 steps $X_3X_2X_1X_0$ = 0110: + 6 steps $X_3X_2X_1X_0$ = 0111: + 7 steps $X_3X_2X_1X_0$ = 1000: - 7 steps $X_3X_2X_1X_0$ = 1001: - 7 steps $X_3X_2X_1X_0$ = 1010: - 6 steps $X_3X_2X_1X_0$ = 1011: - 5 steps $X_3X_2X_1X_0$ = 1100: - 4 steps $X_3X_2X_1X_0$ = 1101: - 3 steps $X_3X_2X_1X_0$ = 1110: - 2 steps $X_3X_2X_1X_0$ = 1111: - 1 step The result for upper 4 bits & lower 4 bits are additive.
Other than the above	Set Test Mode	Reserved

Frame Frequency Default Setting

Frame Frequency = Fosc / [Mux x (FRAMEFQ + 1) x PWM]

Mux (Icon Enable)	FRAMEFQ	PWM	Fosc
Mux<=17	2	15	58kHz
	5	12	92kHz
	4	9	58kHz
18<=MUX<=33	1	15	77kHz
	1	12	58kHz
	2	9	77kHz
34<=MUX<=49	0	15	58kHz
	1	12	92kHz
	1	9	77kHz
50<=MUX<=65	0	15	77kHz
	0	12	58kHz
	1	9	92kHz
66<=MUX<=81	0	15	92kHz
	0	12	77kHz
	0	9	58kHz

PWM is defined in command Set PWM and FRC.

Read Status Byte

A 8 bits status byte will be placed onto the data bus when a read operation is performed if D/$\overline{C}$ is low. The status byte is defined as following:

D7	D6	D5	D4	D3	D2	D1	D0	Comment
BUSY	ON	$\overline{RES}$	0	1	0	DS1	DS0	BUSY=0 : Chip is idle BUSY=1 : Chip is executing instruction ON=0 : Display is OFF ON=1 : Display is ON $\overline{RES}$ =0: Chip is idle $\overline{RES}$ =1: Chip is executing reset DS1, DS0 = 01: SSD0859

* No need to resend the command again if it is set previously.
The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

10. COMMAND DESCRIPTIONS

Set Display On/Off
This command turns the display on/off, by the value of the LSB.

Set Display Start Line
This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 79. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 9 are assigned to Page 0 to 9.

Set Page Address
This command positions the page address to 0 to 8/10 possible positions in GDDRAM. Refer to Figure 3.
Set Higher Column Address This command specifies the higher nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>127).

Set Lower Column Address
This command specifies the lower nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>127).

Set Segment Re-map
This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to Figure 3.

Set Normal/Inverse Display
This command sets the display to be either normal/inverse. In normal display, a RAM data of 1 indicates an “ON” pixel. While in reverse display, a RAM data of 0 indicates an “ON” pixel. The icon line is not affected by this command.

Set Entire Display On/Off
This command forces the entire display, including the icon row, to be “ON” regardless of the contents of the display data RAM. This command has priority over normal/inverse display.
To execute this command, Set Display On command must be sent in advance.

Set LCD Bias
This command is used to select a suitable bias ratio (1/4 to 1/10) required for driving the particular LCD panel in use. The POR default is set to 1/10 bias.

Software Reset
This command causes some of the internal status of the chip to be initialized:
1. Page address is set to 0
2. Column address is set to 0
3. Initial Display Line is set to 0 (point to display RAM page 0, D0)
4. Internal Resistor Ratio register is set to (0,0,0)
5. Software Contrast is set to 32

Set COM Output Scan Direction
This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

Set Power Control Register
This command turns on/off the various power circuits associated with the chip.

Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network (INTRS pin pulled high). The Contrast Control Voltage Range curves below is referred to the following formula:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) * V_{con}$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref} \qquad ,where\ Vref = 1.7V$$

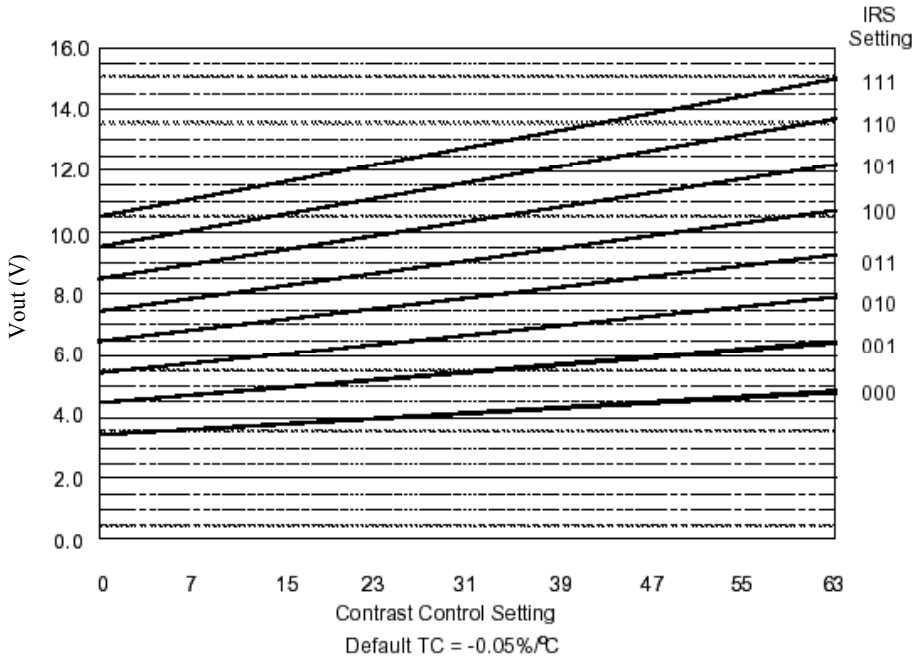


Figure 7 - Contrast Control Voltage Range Curve

Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing VOUT of the LCD drive voltage provided by the On-Chip power circuits. VOUT is set with 64 steps (6-bit) contrast control register. It is a compound commands:

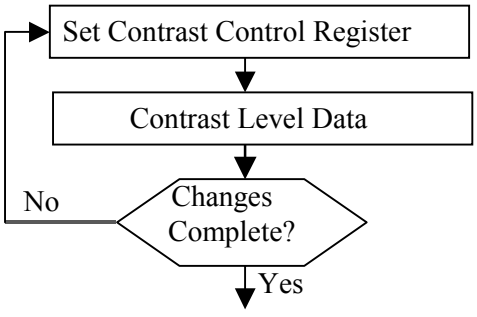


Figure 8 - Contrast Control Flow

Set Display Offset
The second command specifies the mapping of display start line (COM0 if display start line register equals to 0) to one of ROW0-79. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

Set Multiplex Ratio
This command switches default 80 multiplex mode to any multiplex from 16 to 80, if Icon is disabled (POR). When Icon is set enable, the corresponding multiplex ratio setting will be mapped to 17 to 81. The chip pads ROW0-ROW79 will be switched to corresponding COM signal output.

Set Power Save Mode
This command forces the chip to enter Standby or Sleep Mode. LSB of the command will define which mode will be entered.

Exit Power Save Mode
This command releases the chip from either Standby or Sleep Mode and return to normal operation.

Set N-line Inversion
Number of line inversion is set by this command for reducing crosstalk. 3 to 33-line inversion operations could be selected. At POR, this operation is disabled.
It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (N). Or else, some lines will not be changed their polarity during frame change.

Exit N-line Inversion
This command releases the chip from N-line inversion mode. The driving waveform will be inverted once per frame after issuing this command.

Set DC-DC Converter Factor
Internal DC-DC converter factor is set by this command. 3X to 6X multiplying factors could be selected using this command. Hardware configuration is used for 6X setup.

Set Icon Enable
This command enable/disable the Icon display.

Start Internal Oscillator
After POR, the internal oscillator is OFF. It should be turned ON by sending this command to the chip.

Set Gray Scale Mode (White/Light Gray/Dark Gray/Black)
Command 88(hex) to 8F(hex) are used to specify the four gray levels' pulse width at the four possible frames. The four gray levels are called white, light gray, dark gray and black. Each level is defined by 4 registers for 4 consecutive frames. For example, WA is a 4-bit register to define the pulse width of the 1st frame in White mode. WB is a register for 2nd frame in White mode etc. Each command specifies two registers.

For 4 FRC,

Memory Content		Gray Mode	FRAME			
1st Byte	2nd Byte		1st	2nd	3rd	4th
0	0	White	WA	WB	WC	WD
0	1	Light Gray	LA	LB	LC	LD
1	0	Dark Gray	DA	DB	DC	DD
1	1	Black	BA	BB	BC	BD

For 3 FRC,

Memory Content		Gray Mode	FRAME			
1st Byte	2nd Byte		1st	2nd	3rd	4th (No use)
0	0	White	WA	WB	WC	WD (XX)
0	1	Light Gray	LA	LB	LC	LD (XX)
1	0	Dark Gray	DA	DB	DC	DC (XX)
1	1	Black	BA	BB	BC	BC (XX)

Set PWM and FRC
This command selects the number of frames in frame rate control, or the number of levels in the pulse width modulation.

Set Test Mode
This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

EXTENDED COMMANDS
These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip. These features are on top of general ones.

Set Temperature Coefficient (TC) Value
This command is to set 1 out of 2 different temperature coefficients in order to match various liquid crystal temperature grades.

Select Oscillator Source
This command enables the external clock input from CL pin.

Oscillator adjustment
This command is used to adjust the oscillator frequency to desired frame frequency.

Lock/Unlock Interface
After sending the lock command, the interface will be disabled until the unlock command is received. The lock command is suggested whenever the LCD driver will not be accessed for some period. This can minimize incorrect data or command written due to noisy interface.

Low Power mode
The current consumption will be reduced when enter the Low Power Mode. However, crosstalk compensation may be required after entered the low power mode.

Crosstalk Compensation
By using these double commands, 0xFC, 0xNN, to adjust the upper 4 bits and/or lower 4 bits, it can compensate the crosstalk.

11. MAXIMUM RATINGS

Table 5 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 4.0	V
V_{OUT}		VSS-0.3 to VSS+18.0	V
V_{CI}	Booster Supply Voltage	VDD to 4.0	V
V_{in}	Input Voltage	VSS-0.3 to VDD+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	^oC
T_{stg}	Storage Temperature Range	-65 to +150	^oC

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range V_{SS} < or = (Vin or V_{OUT}) < or = V_{DD}. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12. ELECTRICAL CHARACTERISTICS

Table 6 - DC Characteristics (Voltages Referenced to V_{SS}, V_{DD}=1.8 to 3.3V, T_A=-40 to 85°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ (at 25°C)	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	1.8	2.7	3.3	V
V_{CI}	Voltage Generator Circuit Supply Voltage Range		V_{DD}	2.7	3.3	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} + V_{CI} Pins)	V_{DD} = V_{CI} = 2.7V, Voltage Generator On, 4X Converter Enabled, Write accessing, Tcyc = 3.3MHz, Frame Freq.= 80Hz, Display On.	-	456	550	µA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} + V_{CI} Pins)	V_{DD} = V_{CI} = 2.7V, VOUT=9V, Voltage Generator Off, Divider Enabled, Read/Write Halt, Frame Freq.=80Hz, Display On,	-	27	30	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD}+ V_{CI} Pins)	V_{DD} = V_{CI} = 2.7V, Vout=9V, Voltage Generator On, 4x DC-DC Converter Enabled Divider Enabled, Read/Write Halt, Frame Freq.=80Hz, Display On.	200	270	340	µA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} + V_{CI} Pins)	V_{DD} = V_{CI} = 2.7V, LCD Driving Waveform Off, Oscillator On, Read/Write halt. (@ 25°C)	11	20	40	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} + V_{CI} Pins)	V_{DD} = V_{CI} = 2.7V, LCD Driving Waveform Off, Oscillator Off, Read/Write halt. (@ 25°C)	0.9	2	5	µA
V_{OUT}	LCD Driving Voltage Generator Output (VOUT Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Frame Freq.=80Hz, Divider Enabled.	VDD	-	15.0	V
	DC-DC Converter Efficiency	I_{CC} < 20uA, 3X booster I_{CC} < 20uA, 4X booster I_{CC} < 20uA, 5X booster I_{CC} < 20uA, 6X booster	- - - -	93 91 90 88	- - - -	% % % %
V_{LCD}	LCD Driving Voltage Input (VOUT Pin)	Voltage Generator Disabled.	4.0	-	15.0	V
V_{OH1}	Output High voltage (D_0-D_7)	Iout = +500µA	0.8*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (D_0-D_7)	Iout = -500µA	0.0	-	0.2*V_{DD}	V
VOUT	LCD Driving Voltage Source (VOUT Pin)	Regulator Enabled (VOUT voltage depends on Int/Ext Contrast Control)	V_{DD}	-	VOUT - 0.5	V
VOUT	LCD Driving Voltage Source (VOUT Pin)	Regulator Disable	-	Floating	-	V
VOUT V_{L5} V_{L4} V_{L3} V_{L2}	LCD Display Voltage Output (VOUT, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	Divider Enabled, 1:a bias ratio, a=4~10.	- - - - -	VOUT (a-1)/a*VOUT (a-2)/a*VOUT 2/a*VOUT 1/a*VOUT	- - - - -	V V V V V
VOUT V_{L5} V_{L4} V_{L3} V_{L2}	LCD Display Voltage Input (VOUT, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	Voltage reference to V_{SS}, External Voltage Generator, Divider Disabled	V_{L5} V_{L4} V_{L3} V_{L2} V_{SS}	- - - - -	VOUT VOUT V_{L5} V_{L4} V_{L3}	V V V V V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{OH}	Output High Current Source(D_0-D_7)	Vout=V_{DD}-0.4V	50	-	-	μA
I_{OL}	Output Low Current Drain (D_0-D_7)	Vout=0.4V	-	-	-50	μA
I_{OZ}	Output Tri-state Current Drain Source (D_0-D_7)		-1	-	1	μA
C_{IN}	Input Capacitance (all logic pins)			5	7.5	pF
ΔVOUT	Variation of VOUT Output (1.8V < V_{DD} < 3.3V)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	± 2	-	%
	Temperature Coefficient Compensation					
PTC0	Temperature Coefficient [POR]	Voltage Regulator Enabled	-0.04	-0.05	-0.06	%
PTC1	Temperature Coefficient	Voltage Regulator Enabled	-0.06	-0.07	-0.08	%

*The formula for the temperature coefficient is:

$$TC(\%/^0C) = \frac{V_{out}at50^0C - V_{out}at0^0C}{50^0C - 0^0C} * \frac{1}{V_{out}at25^0C} * 100\%$$

13.AC ELECTRICAL CHARACTERISTICS

Table 7 - AC Characteristics (T_A=-40 to 85°C, Voltages referenced to V_{SS}, V_{DD}=V_{CI}=2.7V, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ (at 25°C)	Max	Unit
F_{FRM}	Frame Frequency Fosc / [Mux x (FRAMEFQ+1) x PWM]	Display ON, Set 128 x 81 Graphic Display Mode, Icon Line Enabled, 15PWM, Default frame frequency setting	70	80	100	Hz

Table 8 - I²C-bus timing Characteristics (T_A = -40 to 85°C, V_{DD} = 1.8 to 3.3V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCK}	I²C-bus Clock frequency, SCK	0	-	1	MHz
T_{CLKL}	I²C-bus Clock Low period, SCK	1.3	-	-	µs
T_{CLKH}	I²C-bus Clock high period, SCK	0.6	-	-	µs
T_{DSW}	I²C-bus Data Setup time, SDA	100	-	-	µs
T_{DHW}	I²C-bus Data Hold time, SDA	0.3	-	0.9	µs
T_R	Rise time between SDA & SCK	$20+0.1C_{BUS}$	-	300	ns
T_F	Fall time between SDA & SCK	$20+0.1C_{BUS}$	-	300	ns
C_{BUS}	Capacitive loadings at each I²C-bus channel	-	-	400	pF
$T_{DH, START}$	I²C-bus Hold time, START condition	0.6	-	-	µs
$T_{DS, STOP}$	I²C-bus Setup time, STOP condition	0.6	-	-	µs

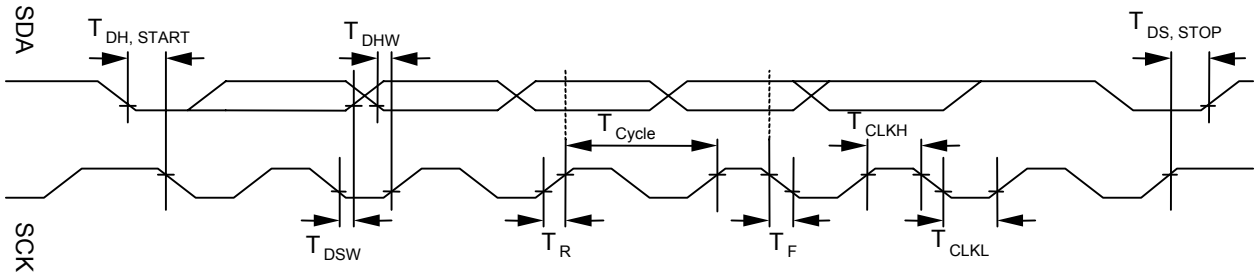


Figure 9 - I²C data bus Interface driving waveform

14. APPLICATION CIRCUIT

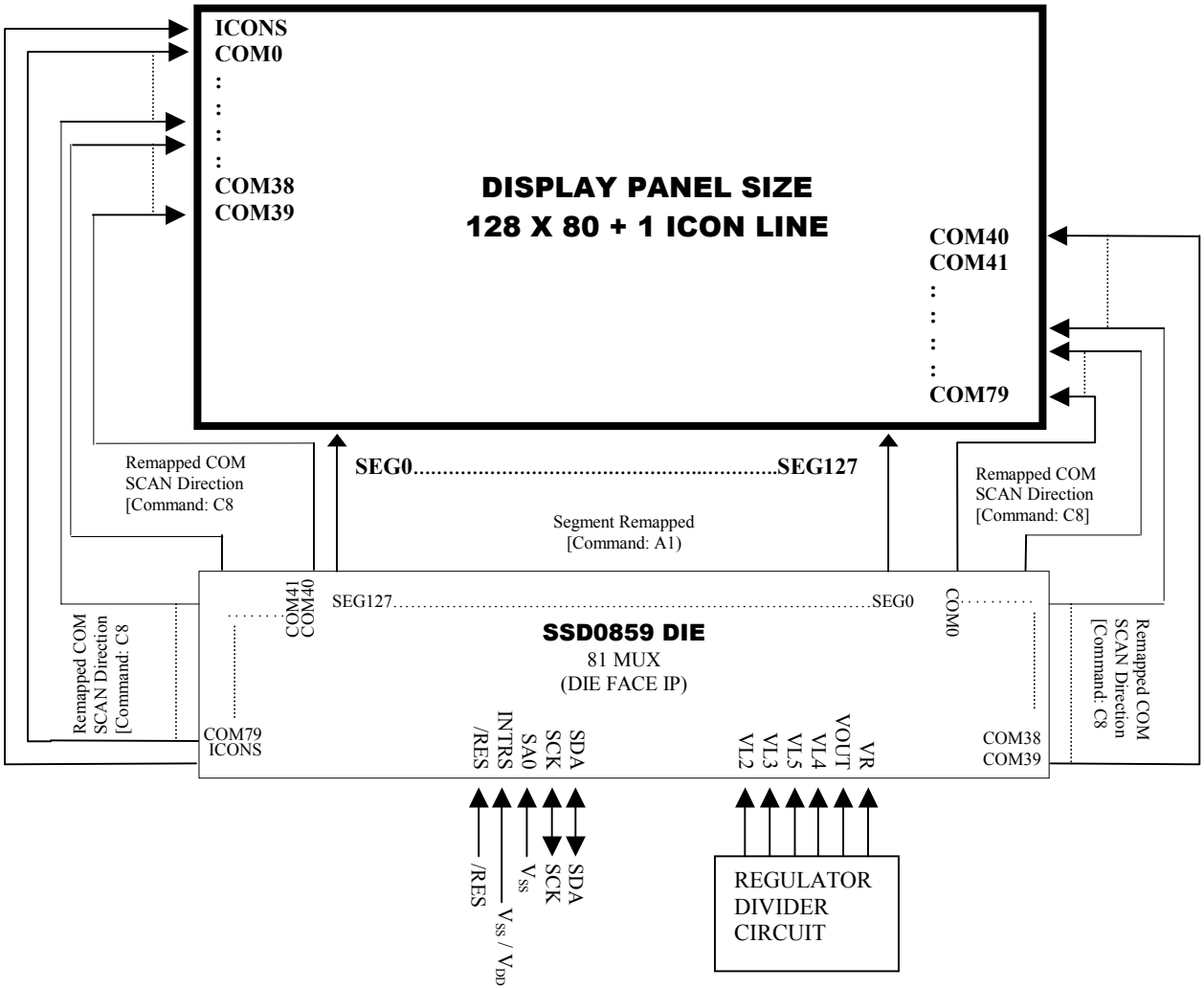
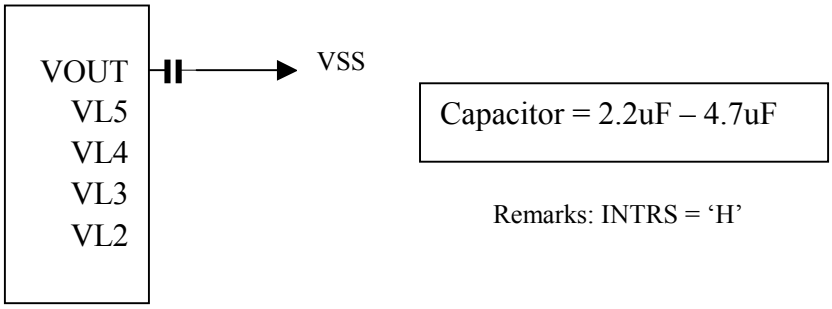
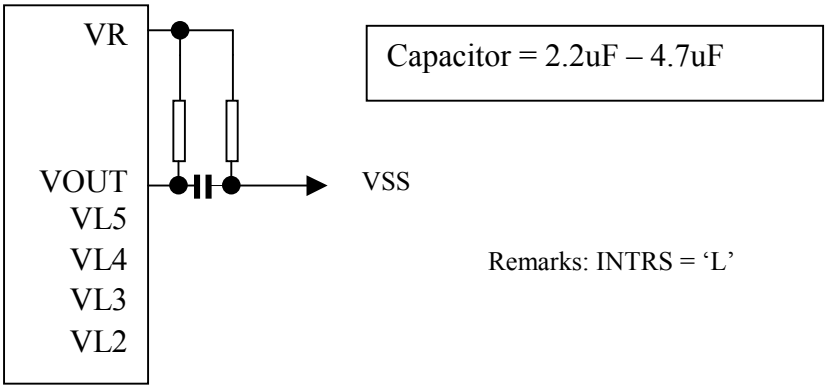


Figure 10 - Application Circuit

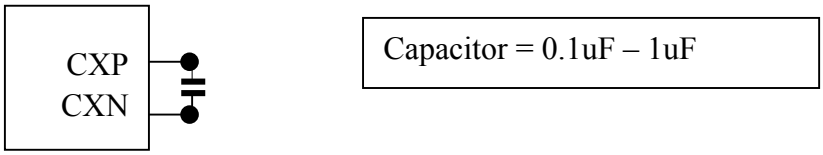
Internal Regulator and Bias Divider
[COMMAND: 2F]



External Regulator and Internal Bias Divider
[COMMAND: 2D]



6X DC-DC Converter Factor
[COMMAND: 67]



OTP Programming Circuit and Sequence

OTP (One Time Programming) is a method to adjust the VOUT. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules.

OTP setting and programming should include two major steps of (1) Find the OTP offset and (2) OTP programming as following,

Step 1. Find the OTP offset

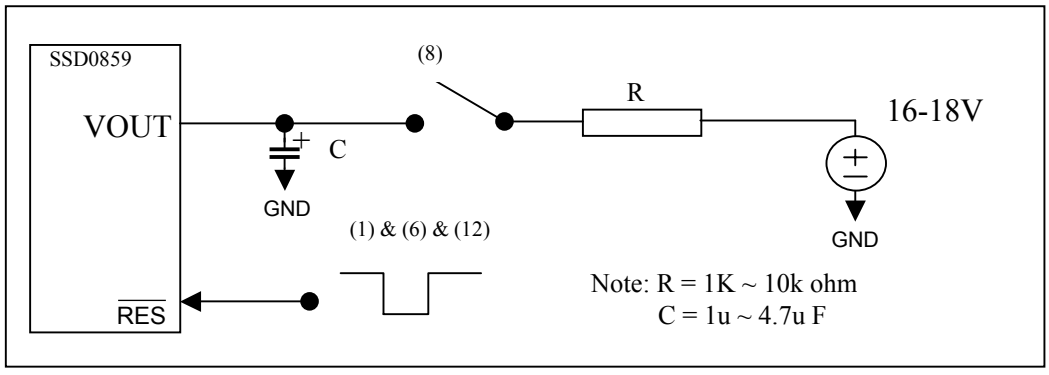
(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value (0x81, 0x00~0x3F) until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:
Contrast value of original initialization = 0x20
Contrast value of the best visual contrast = 0x24
OTP setting steps = 0x24 - 0x20 = +4
OTP setting commands should be (0x82, 0xF4)

Example 2:
Contrast value of original initialization = 0x20
Contrast value of the best visual contrast = 0x1B
OTP setting steps = 0x1B - 0x20 = -5
OTP setting commands should be (0x82, 0xFB)

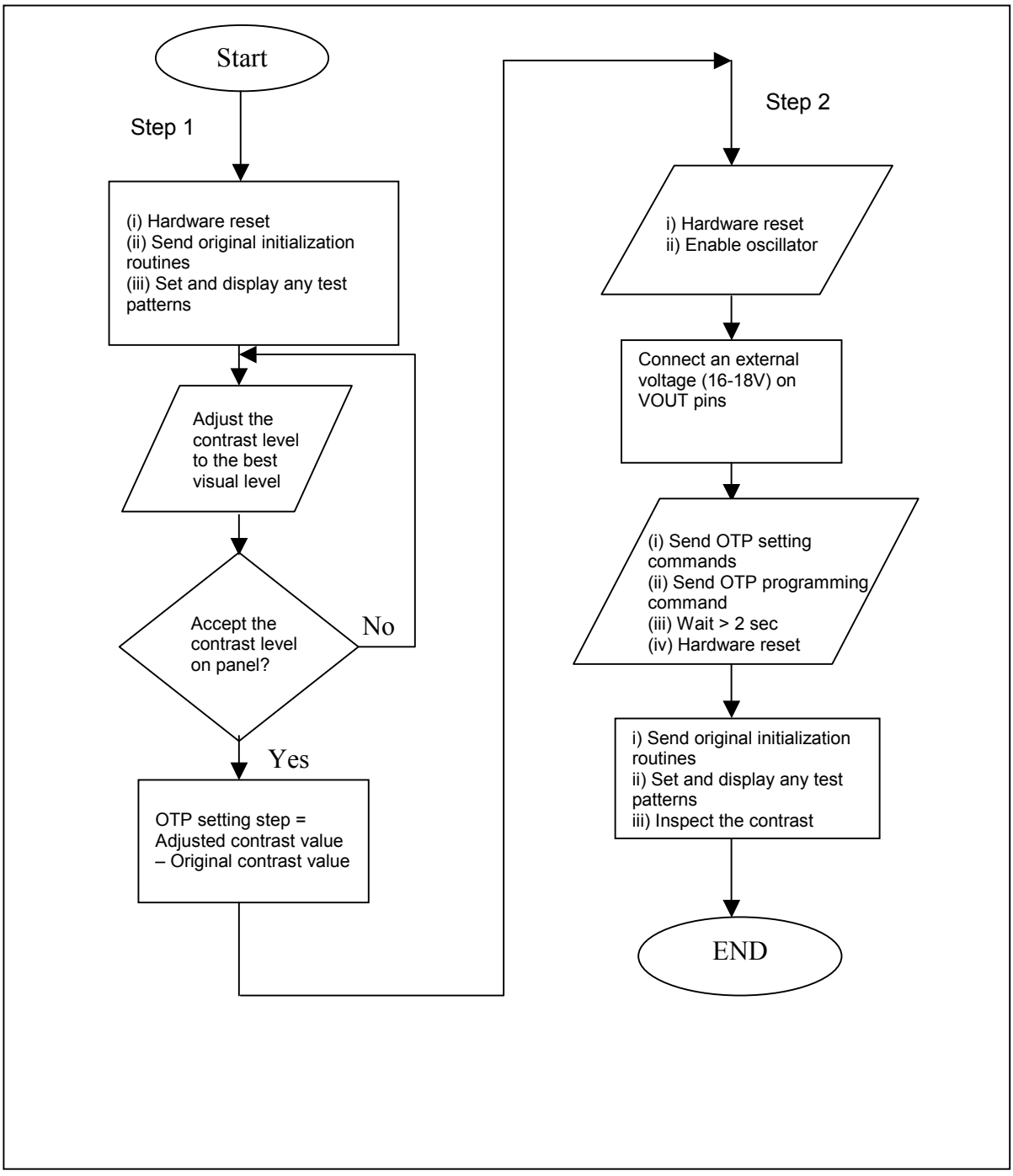
Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(7) Enable Oscillator (0xAB)
(8) Connect an external VCC (see diagram below)
(9) Send OTP setting commands that we find in step 1 (0x82, 0xF0~0xFF)
(10) Send OTP programming command (0x83)
(11) Wait at least 2 seconds
(12) Hardware Reset
Verify the result by repeating step 1. (2) – (3)



OTP Programming Circuit

Flow Chart of OTP Program



OTP Example program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
2. COMMAND(0XAB) \\Enable oscillator
   COMMAND(0X2F) \\ turn on the internal voltage booster, internal regulator and output op-amp buffer; Select booster level
3. COMMAND(0X48) \\ Set Duty ratio
   COMMAND(0X40) \\ 64Mux
   COMMAND(0X55) \\ Set Biasing ratio (1/9 BIAS)
4. COMMAND(0X81) \\ Set target gain and contrast.
   COMMAND(0X2D) \\ contrast = 45
   COMMAND(0X24) \\ gain = 5.1
5. \\ Set target display contents
   COMMAND(0XB0) \\ set page address
   COMMAND(0x00) \\ set lower nibble column address
   COMMAND(0X10) \\ set higher nibble column address
   DATA(…) \\ write target content to GDDRAM
   COMMAND(0XAF) \\ Set Display On
6. OTP offset calculation… target OTP offset value is +3

OTP programming:

7. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
8. COMMAND(0XAB) \\ Enable Oscillator
9. Connect an external VOUT (16V-18V)
10. COMMAND(0X82) \\ Set OTP offset value to +3 (0011)
    COMMAND(0XF3) \\ 0001 $X_3X_2X_1X_0$, where $X_3X_2X_1X_0$ is the OTP offset value
11. COMMAND(0X83) \\ Send the OTP programming command
12. Wait at least 2 seconds for programming wait time
13. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

Verify the result:

14. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel

I²C-bus Write data and read register status

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 11 for the write mode of I²C-bus in chronological order.

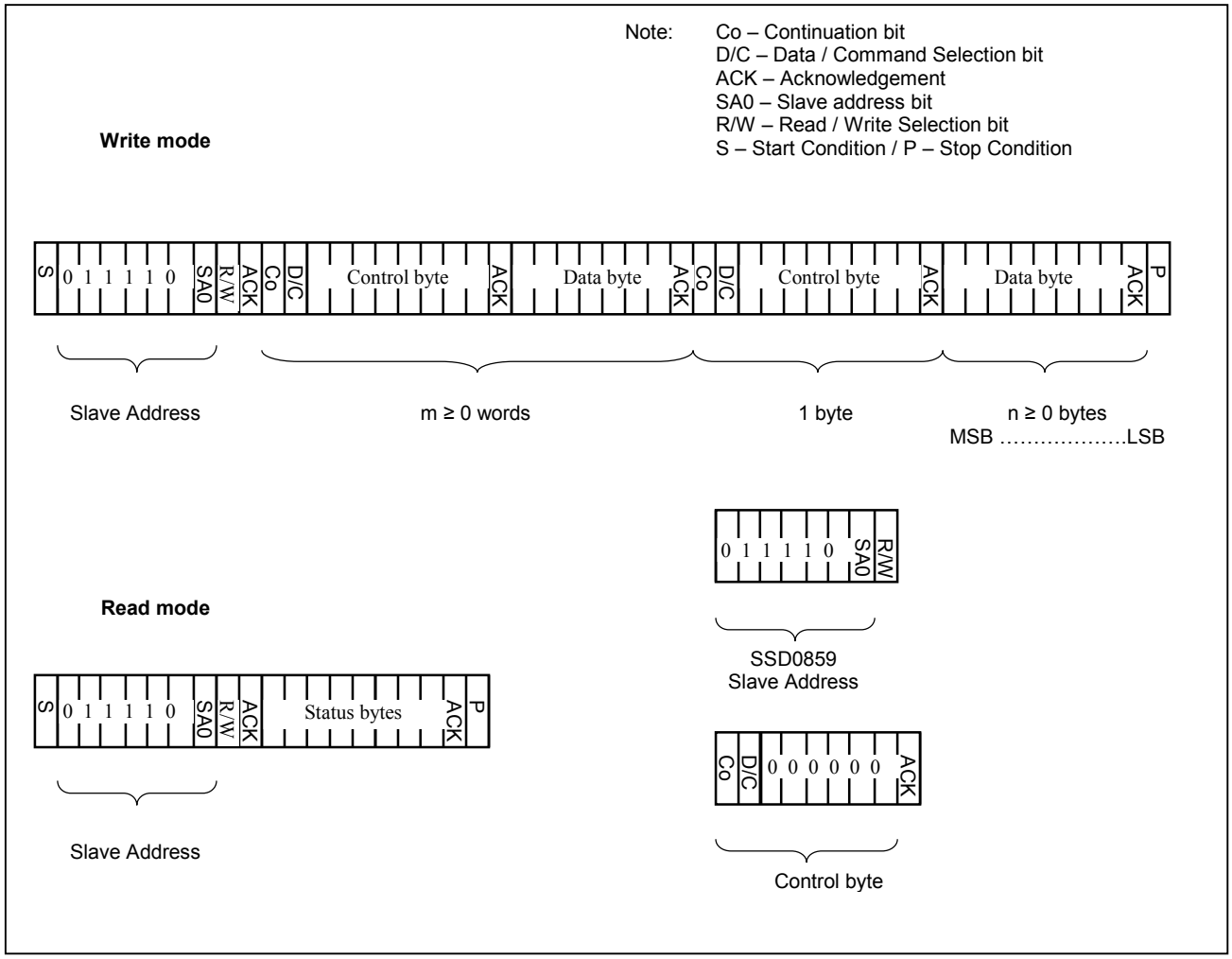


Figure 11 - I²C-bus data format

Write mode

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 12. The start condition is established by pulling the SDA from high to low while the SCK stays high.
2) The slave address is following the start condition for recognition use. For the SSD0859, the slave address is either “b0111100” or “b0111101” by changing the SA0 to high or low.
3) The write mode is established by setting the R/W bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W bit. Please refer to the Figure 13 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as that the SDA line is pulled down during the high period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C bit determines the next data byte is acted as a command or a data. If the D/C bit is set to logic “0”, it defines the following data byte as a command. If the D/C bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.

7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 12. The stop condition is established by pulling the “SDA in” from low to high while the “SCK” stays high.

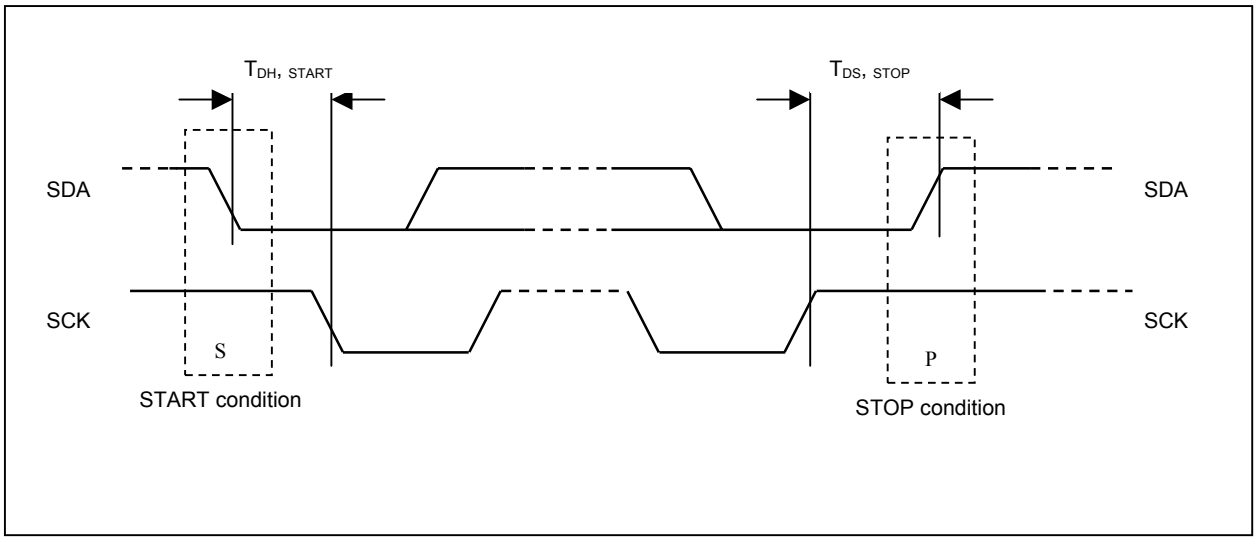


Figure 12 - Definition of the start and stop condition

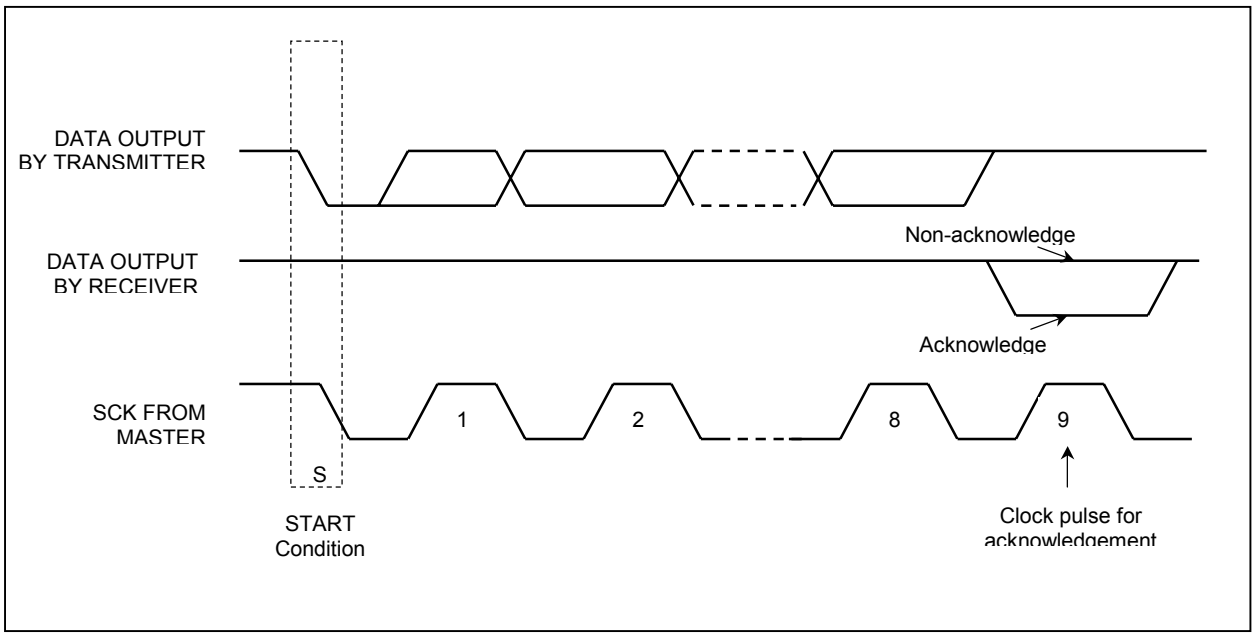


Figure 13 - Definition of the acknowledgement condition

Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCK pulse, must be kept at a stable state within the “high” period of the clock pulse. Please refer to the Figure 14 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCK is low.
2. Both the data line (SDA) and the clock line (SCK) should be pulled up by external resistors.

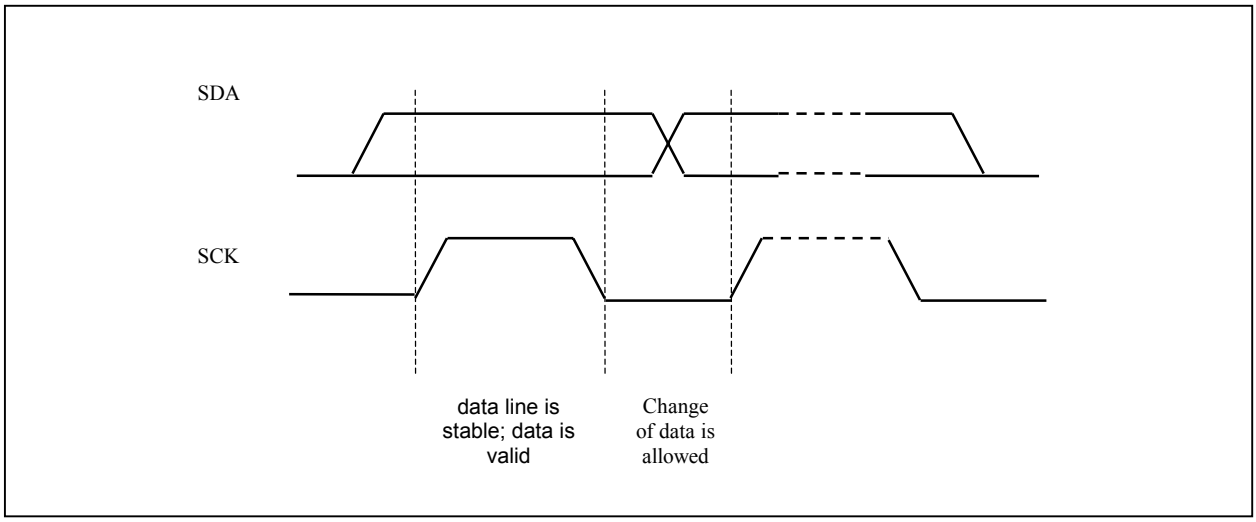


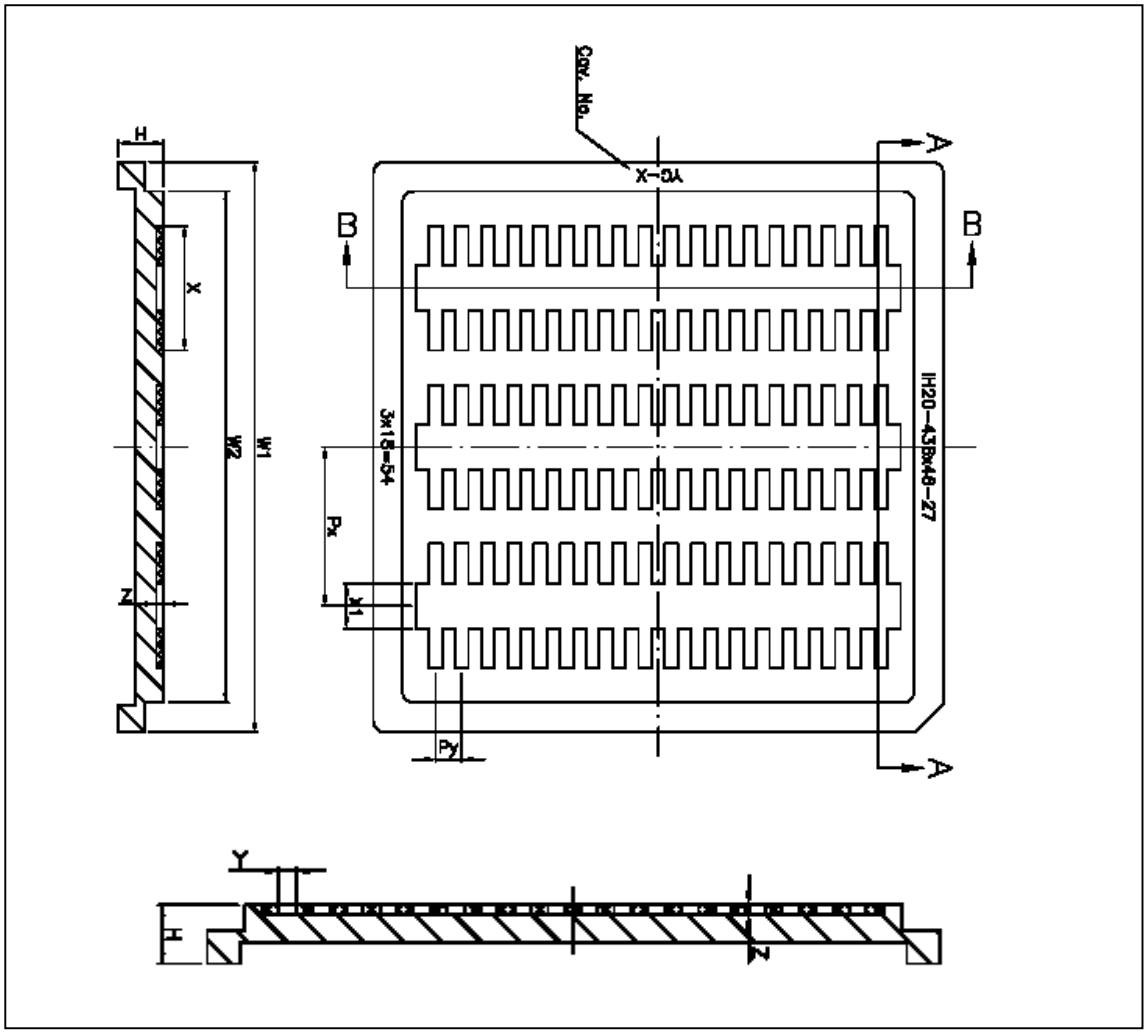
Figure 14 - Definition of the data transfer condition

Read mode (Read status register)

1) No Read mode in SSD0859 device

15. PACKAGE INFORMATION

DIE TRAY DIMENSIONS



Spec	mm	(mil)
W1	50.70 ± 0.2	(1996)
W2	45.50 ± 0.2	(1791)
H	4.05 ± 0.2	(160)
Px	14.14 ± 0.1	(557)
Py	2.33 ± 0.1	(92)
X	11.07 + 0.1/-0	(436)
Y	1.17 + 0.1/-0	(46)
Z	0.68 +0.1/-0	(27)
X1	4.00 ± 0.10	(157)
N	54	

http://www.solomon-systech.com