SIEMENS

SIMATIC

S7-300 Programmable Controller Hardware and Installation

Manual

This manual is part of the documentation package with order no.: **6ES7 398-8AA03-8BA0**

EWA 4NEB 710 6084-02

Edition 1

Safety Guidelines

This manual contains notices which you should observe to ensure your own personal safety, as well as to protect the product and connected equipment. These notices are highlighted in the manual by a warning triangle and are marked as follows according to the level of danger:

Danger

indicates that death, severe personal injury or substantial property damage **will** result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage **can** result if proper precautions are not taken.

Caution

indicates that minor personal injury or property damage can result if proper precautions are not taken.

Note

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground, and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical descriptions, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

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Automation and Drives (A&D)
Industrial Automation Systems (AS)
Postfach 4848, D- 90327 Nürnberg

Disclaimer of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Important Information

Purpose of the Manual

The information contained in this manual enables you to:

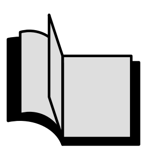
- Install and wire an S7-300 programmable controller.
- Look up operator entries, functional descriptions and the technical specifications relevant to the S7-300's CPUs.

  You will find the function descriptions and technical specifications for the signal modules, power supply modules and interface modules in the *Module Specifications* Reference Manual.

Delivery Package

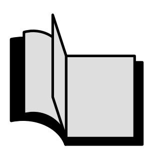
This documentation package (order number 6ES7 398-8AA03-8BA0) comprises two manuals and an instruction list with the following contents:

S7-300 Programmable Controller, Hardware and Installation



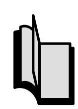
- Mechanical and electrical configuration
- Installation and wiring
- Preparing the S7-300 for operation
- Characteristics and technical data for the S7-300 CPUs

S7-300, M7-300 Programmable Controllers, Module Specifications



- General technical data
- Power supply modules
- Digital modules
- Analog modules
- Order numbers for the S7-300

Instruction List



- Instruction set for all CPUs
- Brief description of instructions and execution times in relation to the individual CPUs

A detailed description of all instructions with examples can be found in the *STEP 7 manuals* (see Appendix H).

You can also order the instruction list separately: 6ES7 398-8AA03-8BN0

Scope of the Manual

This manual applies for the following CPUs:

CPU	Order No.	As of Version	
		Firmware	Hardware
CPU 312 IFM	6ES7 312-5AC02-0AB0	1.0.0	01
CPU 313	6ES7 313-1AD03-0AB0	1.0.0	01
CPU 314	6ES7 314-1AE04-0AB0	1.0.0	01
CPU 314 IFM	6ES7 314-5AE03-0AB0	1.0.0	01
CPU 315	6ES7 315-1AF03-0AB0	1.0.0	01
CPU 315-2 DP	6ES7 315-2AF03-0AB0	1.0.0	01
CPU 316-2 DP	6ES7 316-2AG00-0AB0	1.0.0	01
CPU 318-2	6ES7 318-2AJ00-0AB0	1.0.0	01

This manual describes all modules that are valid at the time the manual is released. For new modules or newer versions of modules, we reserve the option to add to the manual a product information containing the current information on this module.

Changes Since the Previous Version

The following changes have been made since the previous version (*S7-300 Programmable Controller, Hardware and Installation Manual* (order no. 6ES7 398-8AA02-8BA0), Edition 2):

- New CPUs:
  - CPU 316-2 DP
  - CPU 318-2
    (Refer to Section11.1! It describes important differences between the CPU 318-2 and other CPUs).
- The CPU 316 is no longer included in the scope of delivery for the S7-300 and therefore not described in this manual.
- Separate versions for CPU firmware and hardware:
  - You can find the firmware version of the CPU (V 1.0.0) under the front cover, on the left next to the power supply connections.
  - You can find the hardware version of the CPU on the front cover.
- You can save the firmware of the CPU on the memory card (not 318-2).
- New for the CPU 315-2 DP
  - Routing
  - Direct communication
  - Equidistance

Standards, Certificates and Approvals

The S7-300 programmable controller meets the requirements and criteria of standard IEC 1131, Part 2. The S7-300 meets the requirements for the CE mark. Approvals for CSA, UL and FM have been granted for the S7-300.

See Appendix A for detailed information on standards and approvals.

Recycling and Disposal

The SIMATIC S7-300 can be recycled thanks to the low level of pollutants in its equipment.

Please contact the following address for environmentally-friendly recycling and disposal of your old SIMATIC equipment:

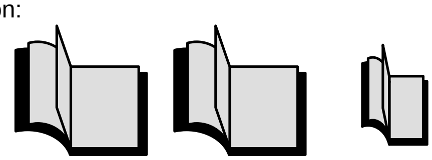
Siemens Aktiengesellschaft
Anlagenbau und Technische Dienstleistungen
ATD ERC Essen Recycling/Remarketing
Fronhauser Str. 69
D-45127 Essen

Phone: +49 201/816 1540 (hotline)
Fax: +49 201/816 1504

Documentation Required

Depending on the CPU, you require the following documentation for installing your S7-300:

The following documentation is required for installing the S7-300 and for preparing it for operation:



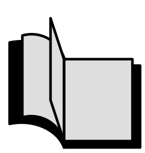
Hardware and Installation, Manual

Reference Manual *Module Specifications*

Instruction List

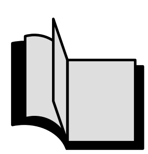
Documentation package
Order number
6ES7 398-8AA03-8BA0

For CPUs 312 IFM and 314 IFM, you will also require the description of the integrated functions and the control functions in STEP 7:



Integrated Functions Manual

Order No. 6ES7 398-8CA00-8BA0



System and Standard Functions *Reference Manual*

(You can find this in *STEP 7* as an electronic manual)

Documentation for Programming

In Appendix H you will find a list of the documentation required to program and commission the S7-300. In addition, you will find a list of specialist books on programmable controllers.

CD-ROM

Furthermore, the complete SIMATIC S7 documentation is available on CD-ROM.

Guide

To help you find special information quickly, the manual contains the following access aids:

- At the start of the manual you will find a complete table of contents and a list of the diagrams and tables that appear in the manual.
- An overview of the contents of each section is provided in the left-hand column on each page of each chapter.
- You will find a glossary in the appendix at the end of the manual. The glossary contains definitions of the main technical terms used in the manual.
- At the end of the manual you will find a comprehensive index which gives you rapid access to the information you need.

Additional Support

Please contact your local Siemens representative if you have any queries about the products described in this manual. A list of Siemens representatives worldwide is contained in the appendix to this manual.

If you have any questions or suggestions concerning this manual, please fill in the form at the end of this manual and return it to the specified address. Please feel free to enter your personal assessment of the manual in the form provided.

We offer a range of courses to help get you started with the SIMATIC S7 programmable controller. Please contact your local training center or the central training center in Nuremberg, D-90327 Germany (tel. +49 (911) 895-3154)

Constantly Updated Information

You can receive up-to-date information on SIMATIC products from the following sources:

- On the Internet at http://www.ad.siemens.de/
- On the fax polling number +49-8765-93 00-55 00

In addition, the SIMATIC Customer Support provides up-to-date information and downloads for users of SIMATIC products:

- On the Internet at http://www.ad.siemens.de/simatic-cs
- Via the SIMATIC Customer Support mailbox on the following number: +49 (911) 895-7100

  To access the mailbox, use a modem with up to V.34 (28.8 kbps), and set the parameters as follows: 8, N, 1, ANSI. Alternatively, access it using ISDN (x.75, 64 kbps).

You can reach the SIMATIC Customer Support by telephone at +49 (911) 895-7000 and by fax at +49 (911) 895-7002. Queries can also be addressed to us by Internet mail or by mail to the mailbox specified above.

Contents

Figures

Tables

Product Overview

1

Modular Design

The S7-300 has a modular design. You can set up your own individual system by combining components from a comprehensive range of S7-300 modules.

The range of modules includes the following components:

- CPUs for various performance ranges
- Signal modules for digital and analog input/output (see *Module Specifications* Reference Manual)
- Function modules for technological functions (see the function module manual for a description).
- CP communication processors (see the communication processor manual for a description)
- Load power supply modules for connecting the S7-300 to 120/230V AC power supplies (see *Module Specifications* Reference Manual)
- Interface modules for the interconnection of racks in multi-rack installations (see *Module Specifications* Reference Manual)

All of the S7-300 modules are contained in housings protected to IP 20, i.e. they are encapsulated and can be operated without a fan.

In This Chapter

In this chapter, we will introduce you to the most important components that go to make up an S7-300.

Structure of an S7-300

An S7-300 programmable controller is made up of the following components:

- Power supply (PS)
- CPU
- Signal modules (SM)
- Function modules (FM)
- Communication processor (CP).

Several S7-300s can communicate together and with other SIMATIC S7 PLCs via PROFIBUS bus cables.

You require a programming device (PG) to program the S7-300. You hook the programming device up to the S7-300 with a special programming device cable.

Figure 1-1 shows a possible configuration with two S7-300 programmable controllers. The components in the shaded area are described in this manual.

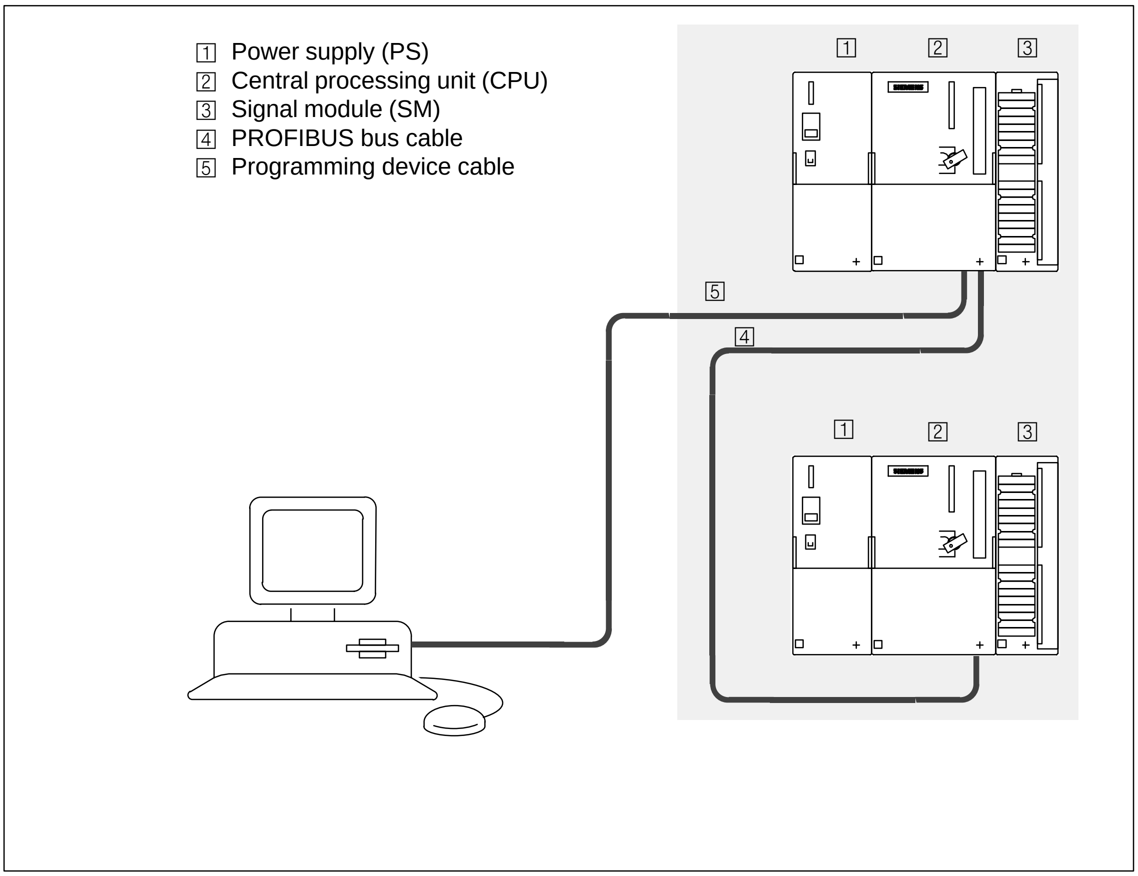


Figure 1-1 Components of an S7-300

Components of an S7-300

You have a number of components at your disposal for installing and starting up an S7-300 programmable controller. Table 1-1 lists the major components and their functions:

Table 1-1 Components of an S7-300

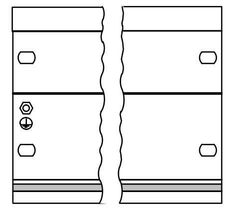
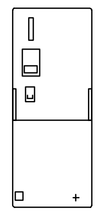
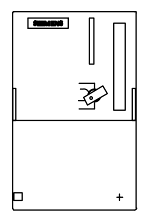
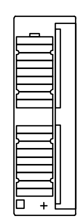
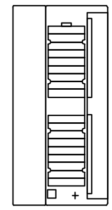
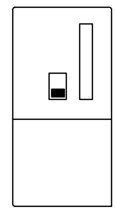
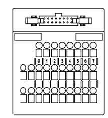
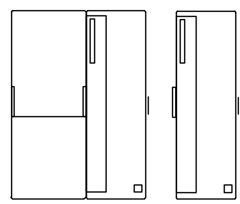
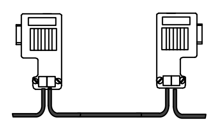
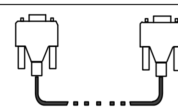
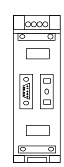
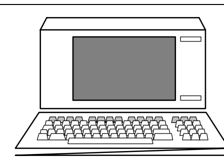
Components	Function	Illustration
Rail Accessory: Shield contact element	... accommodates the S7-300 modules	
Power supply (PS)	... converts the power system voltage (120/230V AC) into 24V DC for the S7-300 and load power supply for 24V DC load circuits	
CPU Accessory: • CPU 313/314/315/315-2 DP/ 316-2 DP/318-2 – Memory card – Backup battery (or accumulator for real-time clock) except for CPU 313) • CPU 314 IFM – Backup battery (or accumulator for real-time clock) – Front connector • CPU 312 IFM – Front connector	... executes the user program; supplies the S7-300 backplane bus with 5 V; communicates with other nodes in an MPI network via the MPI interface. You can also use the CPU 31x-2 DP/318-2 in a PROFIBUS subnet: • as a DP master • as a DP slave on an S7/M7 DP master or another DP master.	
Signal modules (SM) (digital input modules, digital output modules, digital input/output modules) analog input module analog output module analog input/output modules) Accessory: Front connector	... match different process signal levels to the S7-300	

Table 1-1 Components of an S7-300, continued

Components	Function	Illustration
Function modules (FM) Accessories: Front connector	... for time-critical and memory-intensive process signal processing tasks, for example, positioning or closed-loop control	
Communication processor (CP). Accessory: Connecting cable	... relieves the CPU of communication tasks, for example, CP 342-5 DP for connection to PROFIBUS-DP.	
SIMATIC TOP connect Accessories: Front connector module with ribbon cable connection	... for wiring of the digital modules	
Interface module (IM) Accessories: Connecting cables	... interconnects the individual tiers of an S7-300	
PROFIBUS bus cable with bus connector	... interconnects stations on an MPI or PROFIBUS subnet	
Programming device cable	... connects a CPU to a programming device/PC	
RS 485 repeaters	... for amplifying the signals in an MPI or PROFIBUS subnet and for connecting segments in these systems	
Programming device (PG) or PC with the STEP 7 software package	... configures, initializes, programs and tests the S7-300	

Installation 2

Introduction

In this chapter we will show you how to carry out the mechanical configuration, and prepare and install the S7-300 components.

To set up a S7-300, you must take into account the configuration of the electrical setup. Make sure you also read Chapter 3, “Wiring”.

Contents

Open Modules

The modules of an S7-300 are open components. That means you can only install the S7-300 in housings, cabinets or electrical operating areas that are only accessible by key or a special tool. Only trained or authorized personnel should have access to the housings, cabinets or electrical operating areas.

2.1 Configuring an S7-300 Installation

2.1.1 Horizontal and Vertical Installation

Installation

You can install your S7-300 in either a horizontal or vertical position.

Permissible Ambient Temperature

- Horizontal installation from 0 to 60 °C
- Vertical installation from 0 to 40 °C

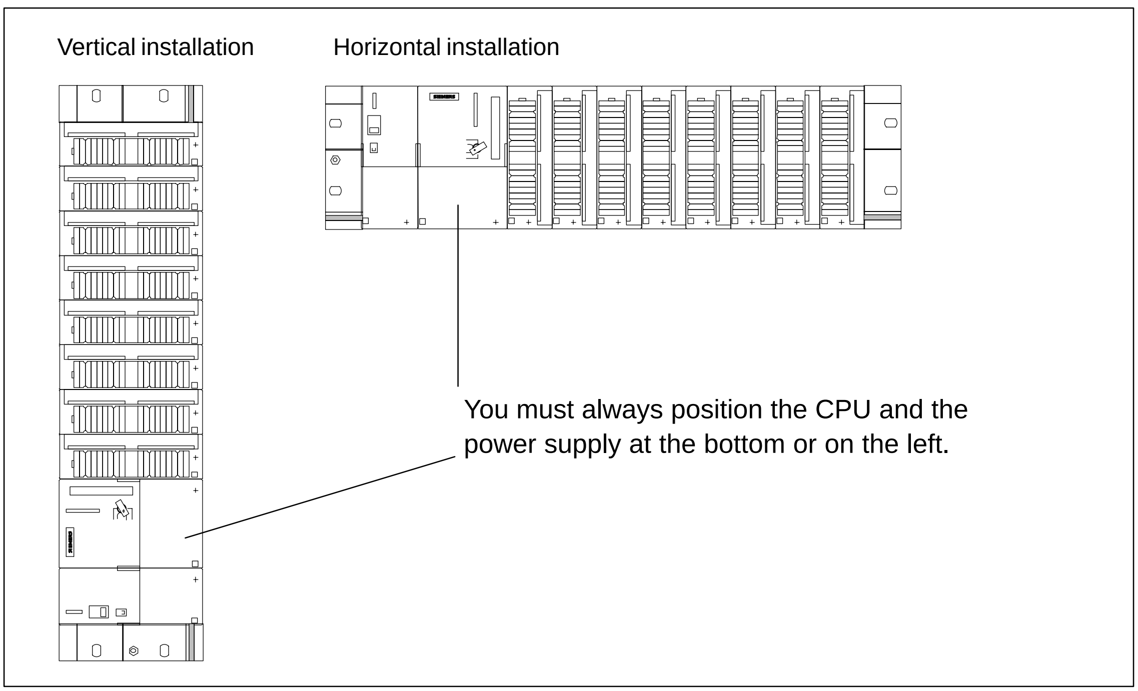


Figure 2-1 Horizontal and Vertical Installation of an S7-300

2.1.2 Clearance Measurements

Rules

If you adhere to the minimum clearance measurements:

- You will ensure that the S7-300 modules do not get too hot.
- You will have adequate space for inserting and removing the S7-300 modules.
- You will have sufficient space for running cables.
- The height of the S7-300 mounting rack increases to 185 mm.
  Despite this, you must maintain a clearance of 40 mm (1.56 in.).

Note

If you use a shield contact element (see Section 4.3.4), the dimension specifications apply from the lower edge of the shield contact element.

Clearance Measurements

Figure 2-2 shows the necessary clearances between the individual racks and to the adjacent equipment, cable ducts, cabinet walls etc. for standard S7-300 configurations on several racks.

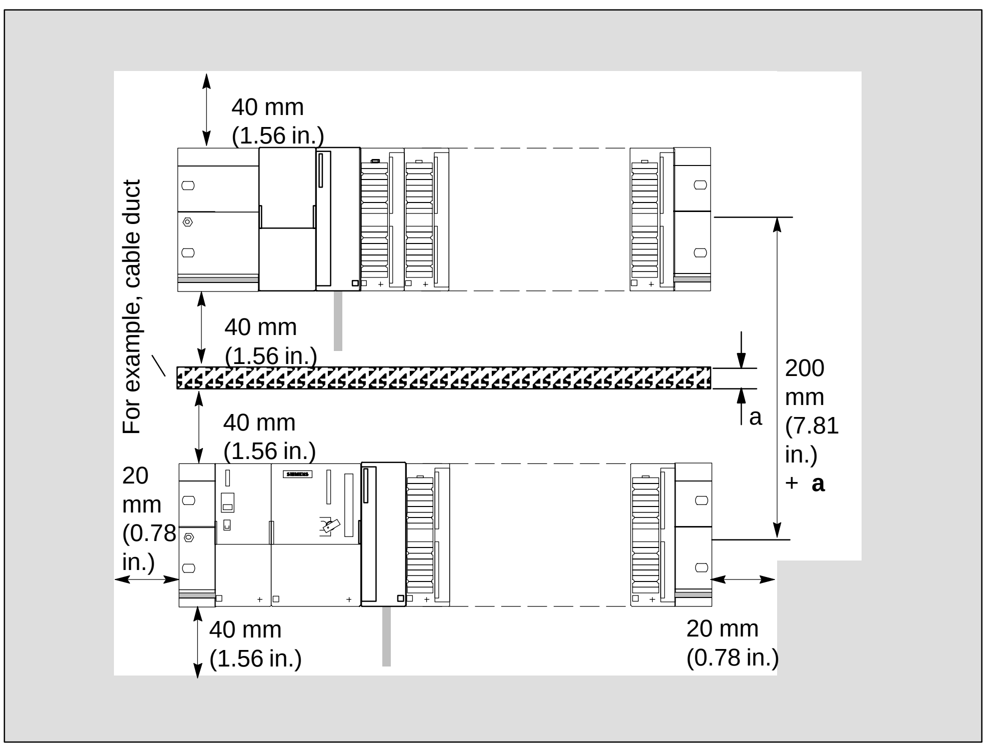


Figure 2-2 Clearance Measurements for an S7-300 Installation

2.1.3 Installation dimensions of the Modules

Table 2-1 shows the installation dimensions of the S7-300 modules.

Table 2-1 Installation Dimensions of the S7-300 Modules

Modules	Module Width	Module Height	Max. Installa-tion Depth
Power supply PS 307, 2 A Power supply PS 307, 5 A Power supply PS 307, 10 A	50 mm (1.95 in.) 80 mm (3.12 in.) 200 mm (7.8 in)	125 mm, 185 mm with shield contact element	130 mm or 180 mm (7.02 in.) with front cover of CPU and IM 361 open (195 mm (8.00 in.) for CPU 312 IFM)
CPU 31x/312 IFM, CPU 314 IFM/CPU 318-2	80 mm (3.12 in.) 160 mm (6.24 in.)		
Digital input module SM 321 Digital output module SM 322 Relay output module SM 322 Digital input/output module SM 323 Simulator module SM 374	40 mm (1.56 in.)		
Analog input module SM 331 Analog output module SM 332 Analog input/output module SM 334	40 mm (1.56 in.)		
Interface module IM 360 Interface module IM 361 Interface module IM 365	40 mm (1.56 in.) 80 mm (3.12 in.) 40 mm (1.56 in.)		

Rail Length

Depending on your S7-300 configuration, you can use rails of the following lengths:

Rail	Usable Lengths for Modules	Remarks
160 mm (6.24 in.)	120 mm (4.68 in.)	Comes with fixing holes
482.6 mm (18.82 in.)	450 mm (17.55 in.)	
530 mm (20.67 in.)	480 mm (18.72 in.)	
830 mm (32.37 in.)	780 mm (30.42 in.)	
2000 mm (1.56 in.)	Cut to length required	Fixing holes must be drilled

2.1.4 Arranging the Modules on a Single Rack

Rules

The following rules apply to the arrangement of the modules on a single rack:

- No more than eight modules(SM, FM, CP) may be installed to the right of the CPU.
- The number of modules (SM, FM, CP) that can be plugged in is limited by the amount of power they draw from the S7-300's backplane bus (see the table containing the technical specifications of the various modules).

  The power input from the S7-300 backplane bus to all the modules installed on a mounting rack must not exceed the following:

  – For the CPUs 313/314/314 IFM/315/315-2 DP/ 316-2 DP/318-2 1.2 A

  – For the CPU 312 IFM 0.8 A

Figure 2-3 shows the arrangement of the modules in an S7-300 configuration with 8 signal modules.

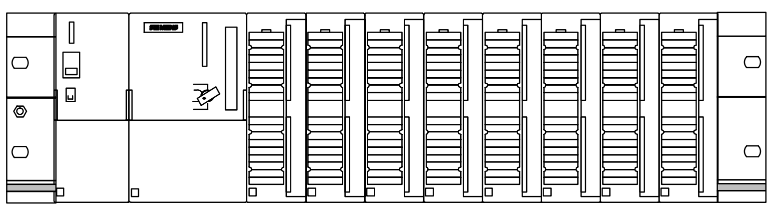


Figure 2-3 Module Arrangement for an S7-300 Programmable Controller Mounted on One Rack

2.1.5 Arranging the Modules on Multiple Racks (Not CPU 312 IFM/313)

Exception

The CPU 312 IFM and CPU 313 can only be used for a configuration on **one** rack.

Rules

The following rules apply to the arrangement of modules on more than one rack:

- The interface module is always be installed in slot 3, to the left of the first signal module.
- No more than 8 modules (SM, FM, CP) are permitted per rack. These modules are always located to the right of the interface modules.
  Exception: In the case of the CPU 314 IFM, a module cannot be inserted in slot 11 on rack 3 (see Chapter 3).
- The number of modules (SM, FM, CP) that can be installed is limited by the maximum permissible current that can be drawn from the S7-300 backplane bus. The power consumption must not exceed 1.2 A per line (see technical specifications of the modules).

Prerequisite: Interface modules

Interface modules that relay the S7-300 backplane bus from one rack to the next are required in multi-rack configurations. The CPU is always located on rack 0.

Interface Module	To Be Used for ...	Order No.
IM 360	Rack 0	6ES7 360-3AA01-0AA0
IM 361	Rack 1 to 3	6ES7 361-3CA01-0AA0
Two-Line Configuration Only..		
IM 365 S	Rack 0	6ES7 365-0BA00-0AA0
IM 365 R	Rack 1	

Connecting Cables for the IM 360/361 Interface Module

The following connecting cables are available for the interface modules:

Table 2-2 Connecting Cables for Interface Modules

Length	Order No. of the Connecting Cable
1 m	6ES7 368-3BB01-0AA0
2.5 m (8.2 ft.)	6ES7 368-3BC51-0AA0
5 m	6ES7 368-3BF01-0AA0
10 m	6ES7 368-3CB01-0AA0

IM 365 Interface Module

The S7-300 offers the IM 365 interface module for a configuration on 2 racks. The two IM 365 interface modules are connected by a 1 m long cable (fixed wiring).

If you use the IM 365 interface modules, you can use only signal modules on rack 1.

The total current drawn by the inserted signal modules from both mounting racks must not exceed 1.2 A ; the current drawn by mounting rack 1 is limited to 800 mA.

Maximum Configuration of an Installation

Figure 2-4 shows the module arrangement in an S7-300 configuration on 4 mounting racks (not CPU 312 IFM/313).

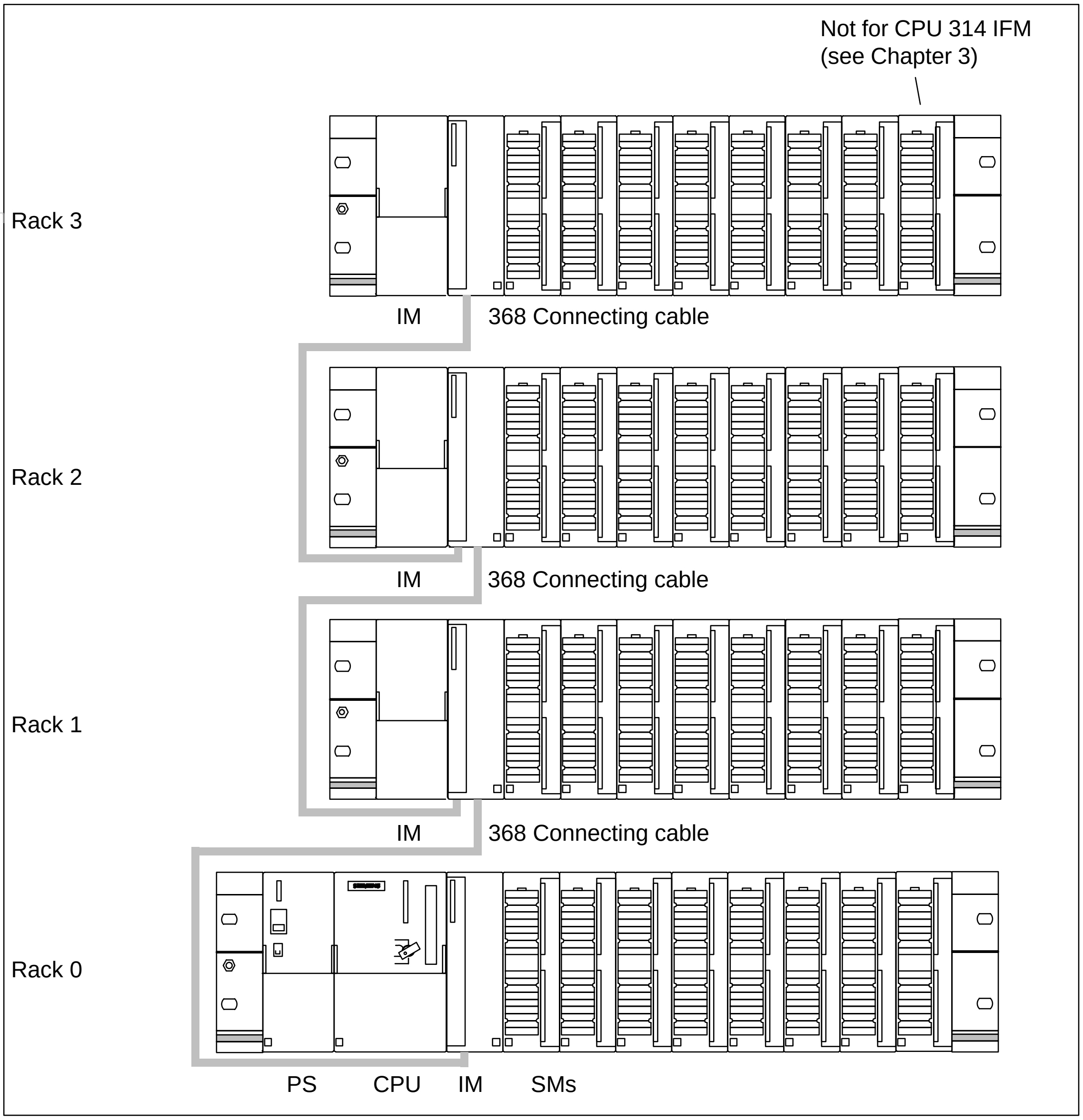


Figure 2-4 Arrangement of Modules in a Four-Rack S7-300 Configuration

2.2 Installation

Section	Contents	Page
2.2.1	Installing the Rail	2-9
2.2.2	Installing Modules on the Rail	2-13
2.2.3	After Installation	2-15

2.2.1 Installing the Rail

Are you Installing a 2-Meter Rail?

If not, you can skip this section and read on from the section entitled **Dimensioned Drawing for Fixing Holes**.

If so, the 2-meter rail has to be prepared for installation. Proceed as follows:

1. Shorten the rail to the required length.
2. Mark out:
   - Four holes for the fixing screws (dimensions: see Table 2-3)
   - A hole to take the fixing screw for the protective conductor.
3. Is the rail longer than 830 mm/32.37 in.?

   If so: You must make additional holes for more fixing screws to ensure the rail is secure. Mark out these holes along the groove in the middle section of the rail (see Figure 2-5). These additional holes should be at 500 mm (19.5 in) intervals.

   If not: No further steps must be taken.

4. Drill the marked holes to a diameter of $6.5^{+0.2}$ mm for M6 screws.
5. Tighten the M6 screw to fix the protective conductor.

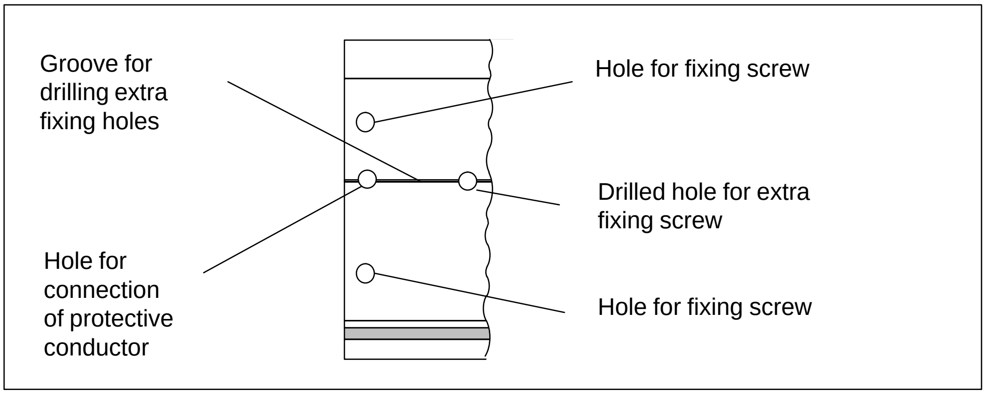
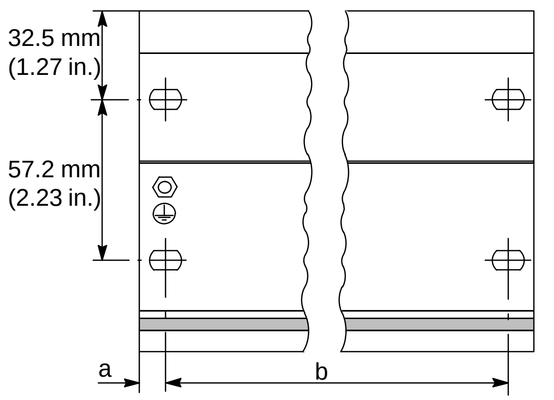
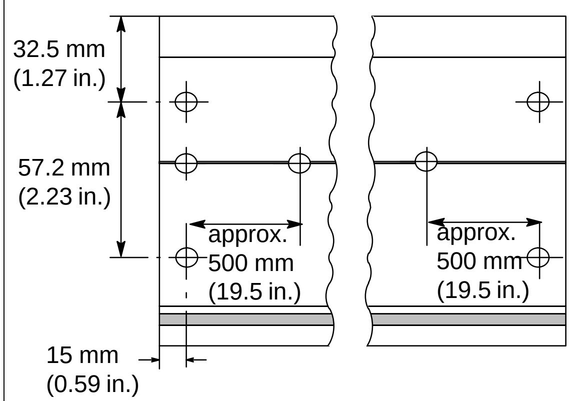


Figure 2-5 Fixing Holes of the 2 m/6.56 ft. Rail

Dimensioned Drawing for Fixing Holes

The fixing-hole dimensions for the rail are shown in Table 2-3.

Table 2-3 Fixing Holes for Rails

<table>
<tr><th colspan="3">“Standard” Rail</th><th>2 m Rail</th></tr>
<tr><td colspan="3">
</td><td>
</td></tr>
<tr><th>Length of Rail</th><th>Dimension a</th><th>Dimension b</th><td rowspan="5">–</td></tr>
<tr><td>160 mm
(6.24 in.)</td><td>10 mm
(0.39 in.)</td><td>140 mm
(5.46 in.)</td></tr>
<tr><td>482.6 mm
(18.82 in.)</td><td>8.3 mm
(0.32 in.)</td><td>466 mm
(18.17 in.)</td></tr>
<tr><td>530 mm
(20.67 in.)</td><td>15 mm
(0.59 in.)</td><td>500 mm
(19.5 in.)</td></tr>
<tr><td>830 mm
(32.37 in.)</td><td>15 mm
(0.59 in.)</td><td>800 mm
(31.2 in.)</td></tr>
</table>

Fixing Screws

You have a choice of the following screw types for fixing the rail.

<table>
<tr><th>for</th><th>Type of Screw</th><th>Description</th></tr>
<tr><td rowspan="2">Lateral fixing screws</td><td>M6 cheese-head screw M6 to ISO 1207/ ISO 1580 (DIN 84/DIN 85)</td><td rowspan="3">Choose a suitable screw length to for your configuration.
You will also require 6,4 washers to ISO 7092 (DIN 433)</td></tr>
<tr><td>M6 hexagon-head screw to ISO 4017 (DIN 4017)</td></tr>
<tr><td>Extra fixing screw (only for 2 m rail)</td><td>M6 cheese-head screw to ISO 1207/ ISO 1580 (DIN 84/DIN 85)</td></tr>
</table>

Installing the Rail

To install rails, proceed as follows:

1. Choose a position for the rail that leaves enough room to install it properly and enough space to cope with the temperature rise of the modules (leave at least 40 mm /1.56 in. free above and below the rail; see page 2-3).
2. Screw the rail to its base (size: M6). Is this base a metallic plate or a grounded supporting plate?

   If so: Make sure there is a low-impedance connection between the rail and the base. In the case of painted or anodized metals, for instance, use a suitable contacting agent or contact washers.

   If not: No particular steps are required.
3. Connect the rail to the protective conductor. An M6 screw is provided for this purpose on the rail.

   Minimum cross-section from the conductor to the protective conductor: 10 mm^2.

Note

Make absolutely sure that your connection to the protective conductor is low-impedance (see Figure 2-6). If the S7-300 is mounted on a hinged rail, you must use a flexible cable to establish the connection to the protective conductor.

Protective Conductor Connection

Figure 2-6 shows you how to connect the protective conductor to the rail.

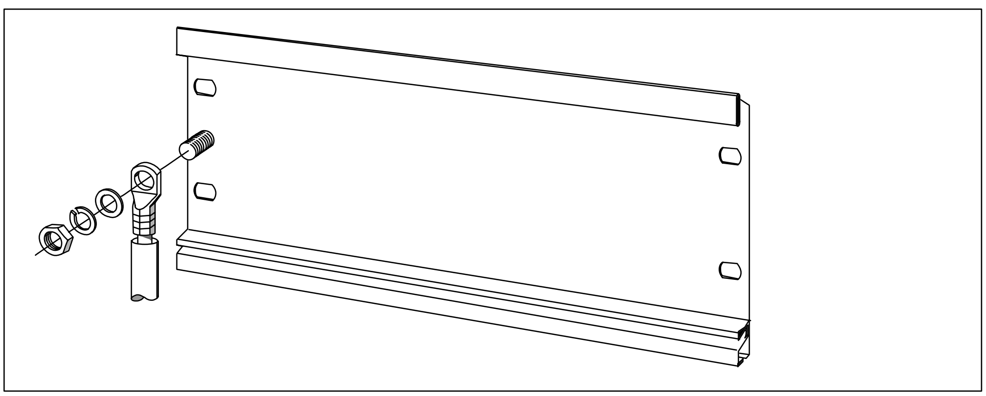


Figure 2-6 Connecting the Protective Conductor to the Rail

2.2.2 Installing Modules on the Rail

Accessories

The accessories you need for installation are included with the modules. Appendix G contains a list of accessories and spare parts with the corresponding order numbers.

Table 2-4 Module Accessories

Module	Accessories Included	Description
CPU	1 × slot number label	For assigning slot numbers
	2 keys	The key is used for actuating the CPU's mode selector
	Labeling strip (CPU 312 IFM/314 IFM only)	For labeling the integrated input and output points of the CPU
Signal module (SM)	1 bus connector	For establishing the electrical connections between the modules
	1 labeling strip	For labeling the input and output points on the module
Interface module (IM)	1 × slot number label (IM 361 and IM 365 only)	For assigning slot numbers on racks 1 to 3

Sequence for Installing the Modules on the Rail

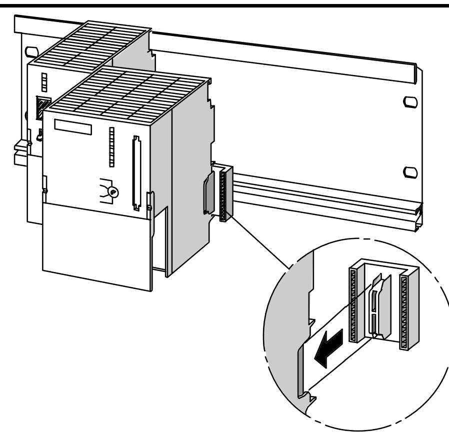
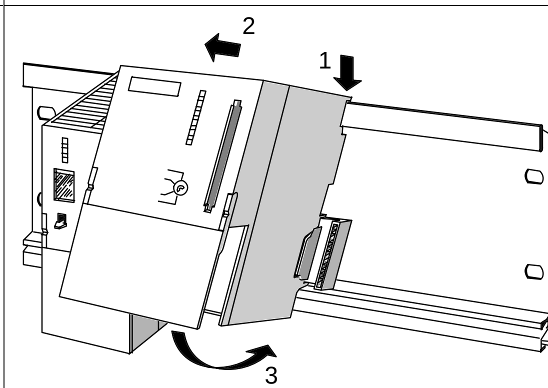
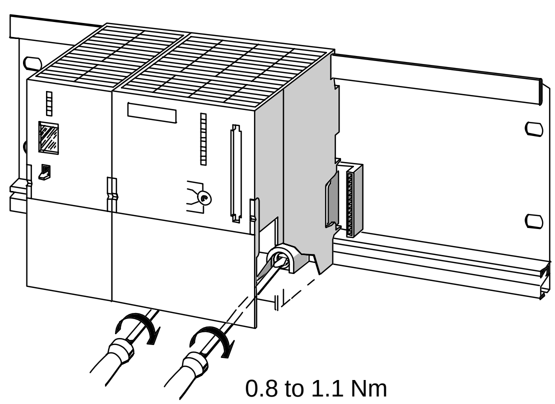
1. Power supply module
2. CPU
3. Signal module(s)

   Note: If you are installing SM 331 analog input modules, please check **before** installation whether you have to move the measuring range submodules on the side of the module. (see Chapter 4 on analog modules in the *Module Specifications* Reference Manual).

Sequence for Installation

The individual steps to be followed when installing the modules are described below.

Table 2-5 Installing the Modules on the Rail

Each signal module comes with a bus connector, but not the CPU. When attaching the bus connectors, always start with the CPU: • Remove the bus connector from the last module and plug it into the CPU. • You must not plug a bus connector into the "last" module.	
Hook the modules onto the rail (1), slide them along as far as the module on the left (2), and swing them down into place (3).	
Bolt the modules tight, applying a torque of between 0.8 and 1.1 Nm (7 to 10 in. lb.).	

2.2.3 After Installation

Inserting the Key

After installing the CPU on the rail, you can insert the key into the CPU in the STOP or RUN switch position.

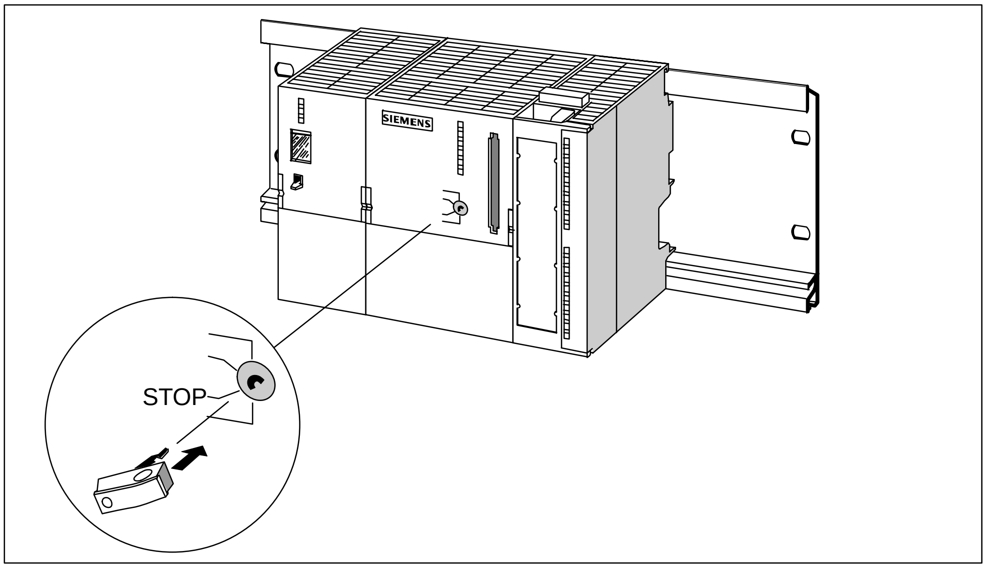


Figure 2-7 Inserting the Key in the CPU

Assigning Slot Numbers

After installation you can assign a slot number to each module. This makes it easier to assign the modules in the configuration table in *STEP 7*. Table 2-6 shows the slot number assignment.

Table 2-6 Slot Numbers for S7 Modules

Slot Number	Module	Remarks
1	Power supply (PS)	–
2	CPU	–
3	Interface module (IM)	To the right of the CPU
4	1st signal module	To the right of the CPU or IM
5	2nd signal module	–
6	3rd signal module	–
7	4th signal module	–
8	5th signal module	–
9	6th signal module	–
10	7th signal module	–
11	8th signal module	–

Applying Slot Numbers

Figure 2-8 shows you how to apply the slot numbers.The slot number labels are included with the CPU.

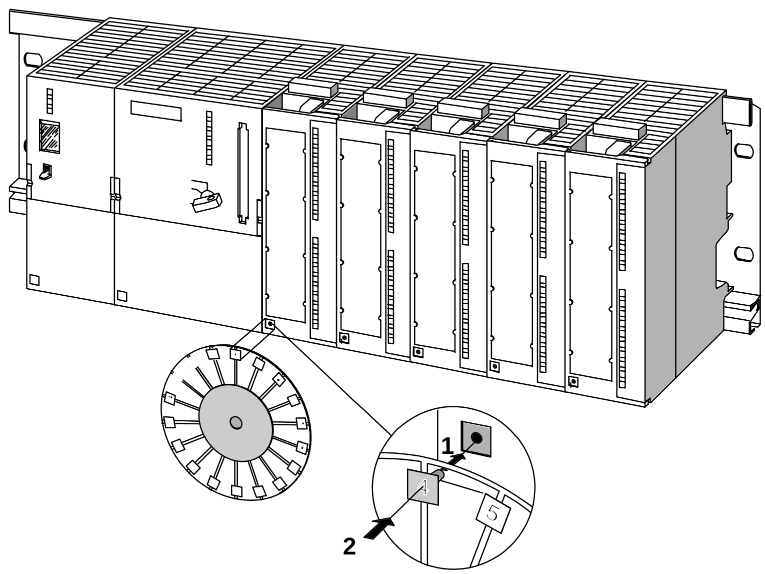


Figure 2-8 Applying Slot Numbers to the Modules

Addressing

3

In This Chapter

In this chapter, you will learn about the different ways of addressing the individual channels of the signal modules.

Slot-Based Address Allocation

Slot-based address allocation is the default addressing method on the *S7*, i.e. a defined module start address is allocated to each slot number.

User-Defined Address Allocation

In user-defined address allocation, you can allocate any address within the available CPU address area to any module. User-oriented address allocation on the S7-300 is only possible with the CPU 315-2 DP.

In This Chapter

3.1 Slot-Based Addressing for Modules (Default Addressing)

Introduction

In slot-based addressing (default addressing), a module start address is allocated to each slot number (see Table 3-1). This section shows you which module start address is allocated to which slot number. You need this information to determine the module start addresses on the installed modules.

Maximum Configuration

Figure 3-1 shows a configuration of the S7-300 on four racks and all of the available module slots. Please note that with the CPUs 312 IFM and 313, only one configuration is possible on rack 0.

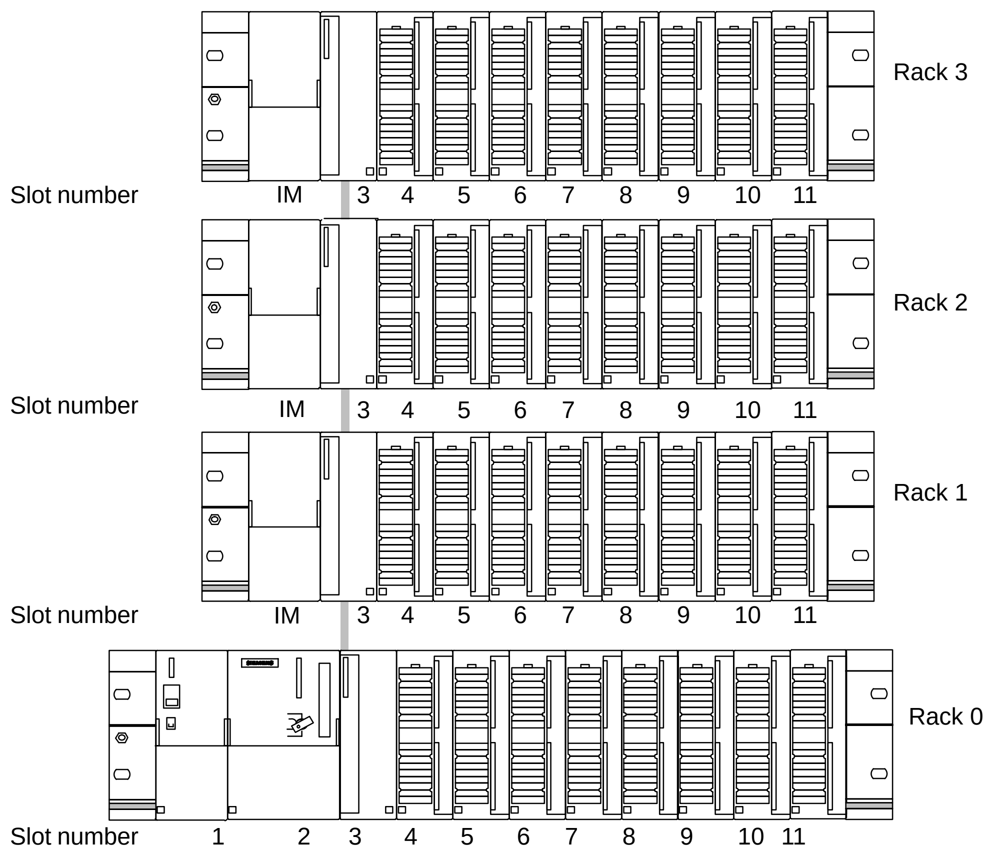


Figure 3-1 Slots of the S7-300

Module Start Addresses

Table 3-1 shows the allocation of the module start addresses to the slot numbers and racks.

The input and output addresses for I/O modules start from the same module start address.

Note

In the case of the CPU 314 IFM, a module cannot be plugged into slot 11 on rack 3. The address space is occupied by the integrated inputs and outputs.

Table 3-1 Start Addresses for the Signal Modules

Rack	Module Start Addresses	Slot Number										
		1	2	3	4	5	6	7	8	9	10	11
0	Digital Analog	PS	CPU	IM	0 256	4 272	8 288	12 304	16 320	20 336	24 352	28 368
1[1]	Digital Analog	– –		IM	32 384	36 400	40 416	44 432	48 448	52 464	56 480	60 496
2[1]	Digital Analog	– –		IM	64 512	68 528	72 544	76 560	80 576	84 592	88 608	92 624
3[1]	Digital Analog	– –		IM	96 640	100 656	104 672	108 688	112 704	116 720	120 736	124[2] 752[2]

1 Not with the CPU 312 IFM/313
2 Not with the CPU 314 IFM

3.2 User-Defined Address Allocation with the CPU 31x-2 DP

Only the 315-2 DP, 316-2 DP and 318-2 CPUs

... support user-defined address allocation.

User-Defined Address Allocation

User-defined address allocation means that you are free to allocate any module (SM/FM/CP) an address of your choice. The addresses are allocated in *STEP 7*. You define the start address of the module, and all other addresses of this module are based on this start address.

Advantages

Advantages of user-defined address allocation:

- Optimum utilization of the address areas available, since between the modules, address “gaps” will not occur.
- When generating standard software, you can program addresses which are independent of the S7-300 configuration.

Addresses of the Distributed I/Os

To address the distributed I/Os of the CPUs 31x-2 DP, please read Section 9.1.

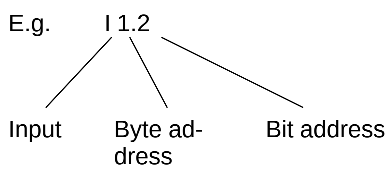
3.3 Addressing the Signal Modules

Introduction

This section shows you how signal modules are addressed. You need this information in order to be able to address the channels of the signal modules in your user program.

Addresses of the Digital Modules

The address of an input or output of a digital module consists of a byte address and a bit address.



The byte address depends on the module start address.

The bit address is the number printed on the module.

Figure 3-2 shows you how the addresses of the individual channels of a digital module are obtained.

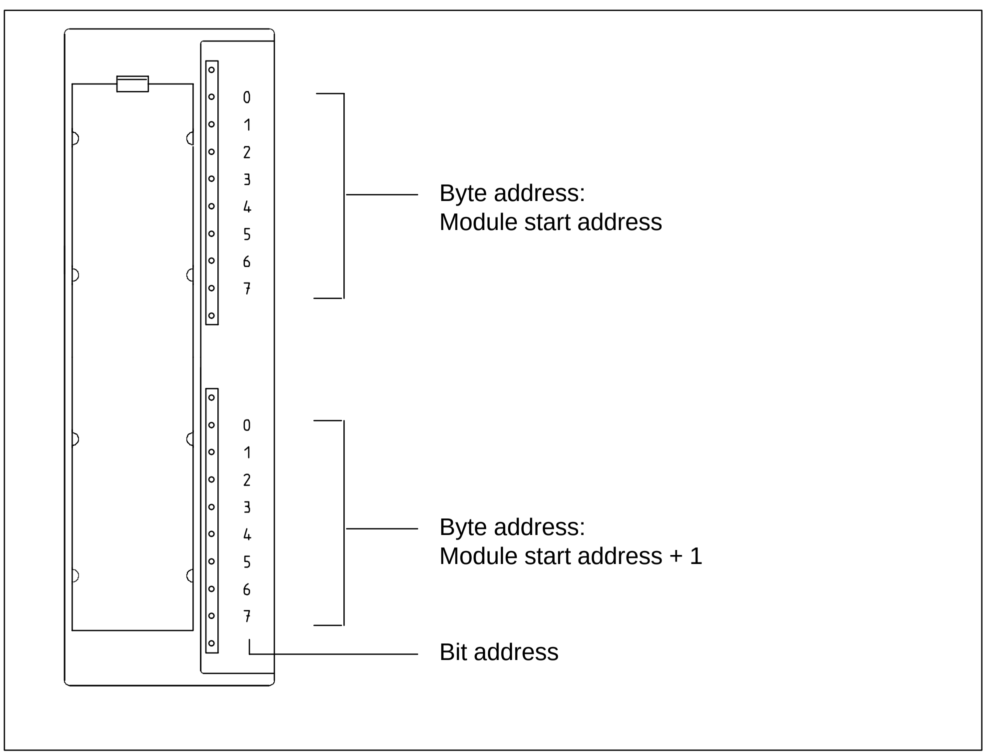


Figure 3-2 Addresses of the Inputs and Outputs of Digital Modules

An Example for Digital Modules

The example in Figure 3-3 shows which default addresses are obtained if a digital module is plugged into slot 4 (i.e. when the module start address is 0).

Slot number 3 has not been assigned since there is no interface module in the example.

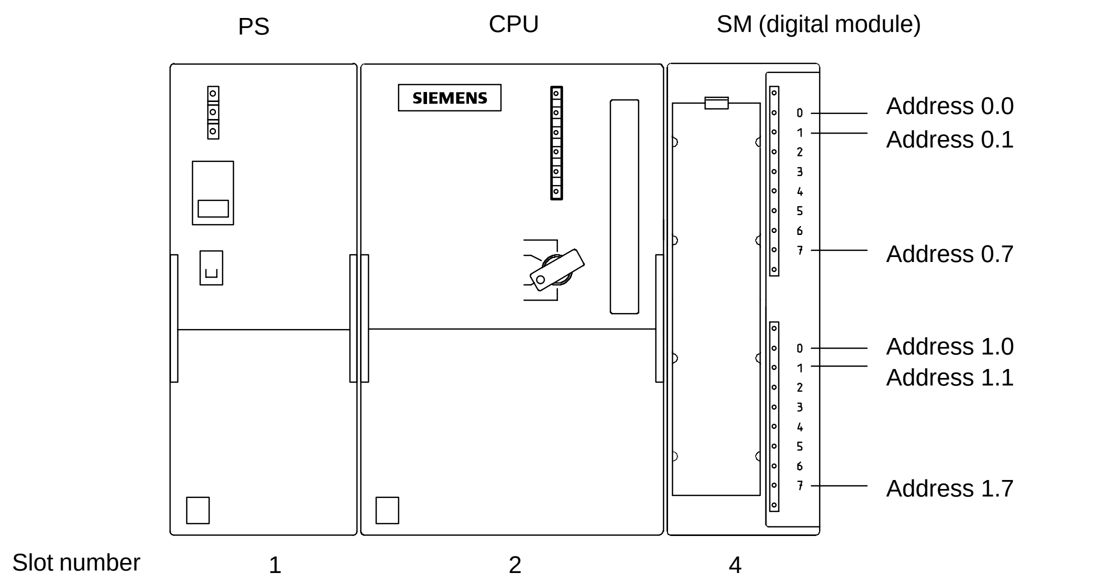


Figure 3-3 Addresses of the Inputs and Outputs of the Digital Module in Slot 4

Addresses of the Analog Modules

The address of an analog input or output channel is always a word address.

The channel address depends on the module start address.

If the first analog module is plugged into slot 4, it has the default start address 256. The start address of each further analog module increases by 16 per slot (see Table 3-1).

An analog input/output module has the same start addresses for its input and output channels.

An Example for Analog Modules

The example in Figure 3-4 shows you which default channel addresses are obtained for an analog module plugged into slot 4. As you can see, the input and output channels of an analog input/output module are addressed as of the same address (the module start address).

Slot number 3 has not been assigned since there is no interface module in the example.

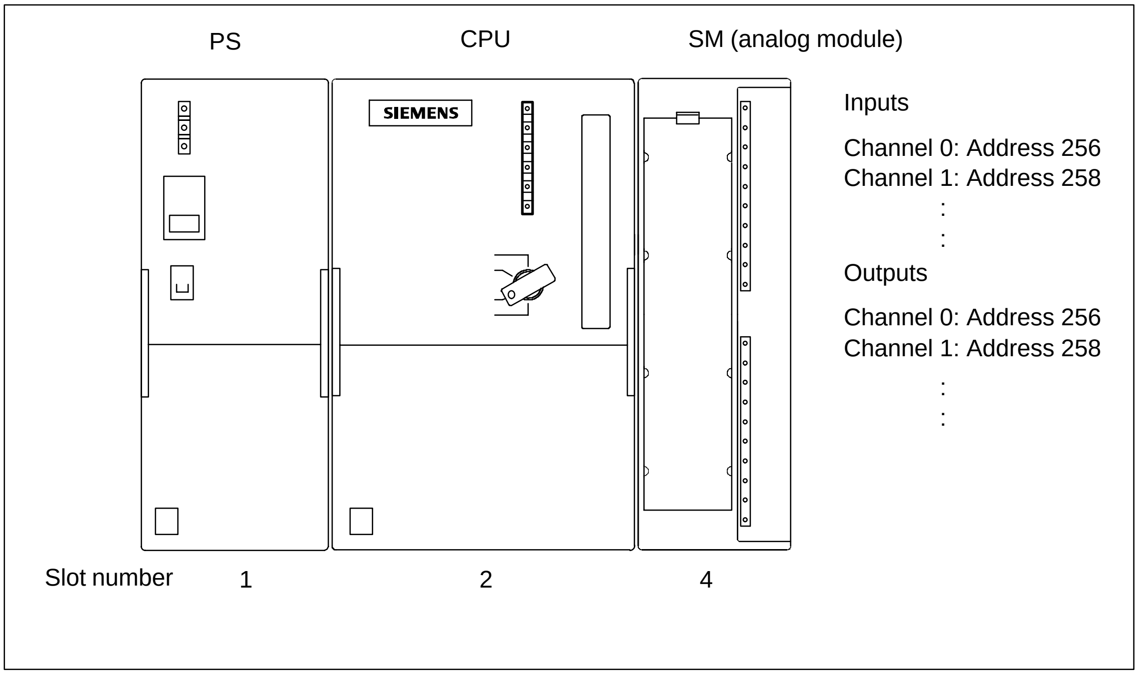


Figure 3-4 Addresses of the Inputs and Outputs of the Analog Module in Slot 4

3.4 Addressing the Integrated Inputs and Outputs of the CPU 312 IFM and CPU 314 IFM

CPU 312 IFM

The integrated inputs and outputs of the CPU 312 IFM have the following addresses:

Table 3-2 Integrated Inputs and Outputs of the CPU 312 IFM

Inputs/Outputs	Addresses	Remarks
10 digital inputs	124.0 to 125.1 Of these, **4 are special channels:** 124.6 to 125.1	You can assign these special channels the counter and frequency functions (see the *Integrated Functions*) manual), or you can use them as interrupt inputs.
6 digital outputs	124.0 to 124.5	–

CPU 314 IFM

The integrated inputs and outputs of the CPU 314 IFM have the following addresses:

Table 3-3 Integrated Inputs and Outputs of the CPU 314 IFM

Inputs/Outputs	Addresses	Remarks
20 digital inputs	124.0 to 126.3 Of these, **4 are special channels:** 126.0 to 126.3	You can assign these special channels the functions “Counter”, “Frequency meter”, “Counter A/B” or “Positioning” (see the *Integrated Functions*) manual), or you can use them as interrupt inputs.
16 digital outputs	124.0 to 125.7	–
4 analog inputs	128 to 135	–
1 analog output	128 to 129	–

Wiring

4

Introduction

In this chapter we will show you how to configure the electrical installation and how to wire an S7-300.

To configure an S7-300 you must take into account the mechanical configuration. Make sure you also read Section 2.1.

Basic Rules

In view of the many and varied applications an S7-300, this chapter can only describe a few basic rules on its electrical configuration. You must observe at least these basic rules if you want your S7-300 to operate faultlessly and satisfactorily.

Contents

4.1 Electrical Configuration

Section	Contents	Page
4.1.1	General Rules and Guidelines for Operating an S7-300 Programmable Controller	4-2
4.1.2	Configuring the S7-300 Process Peripherals	4-5
4.1.3	S7-300 Configuration with Grounded Reference Potential	4-9
4.1.4	S7-300 Configuration with Ungrounded Reference Potential (not CPU 312 IFM)	4-9
4.1.5	S7-300 Configuration with Isolated Modules	4-11
4.1.6	Configuration of an S7-300 with Non-Isolated Modules	4-13
4.1.7	Cabling Inside Buildings	4-13
4.1.8	Cabling Outside Buildings	4-17
4.1.9	Protecting Digital Output Modules Against Inductive Overvoltage	4-17

4.1.1 General Rules and Guidelines for Operating an S7-300 Programmable Controller

As part of a plant or system, and depending on its particular area of application, the S7-300 programmable controller requires that you observe a number of specific rules and guidelines.

Observe the safety and accident prevention regulations applying to particular applications or situations, for example the relevant machine protection guidelines.

This section outlines the most important rules you must observe when integrating your S7-300 in an existing plant or system.

Emergency Stop Systems

Emergency stop systems to IEC 204 (corresponds to VDE 113) must remain effective in all operating modes of the plant or system.

Starting Up a Plant Again Following Specific Events

The following table shows you what you have to observe when starting up a plant again following certain events.

If There Is...	What Must Not Happen ...
A restart following a voltage dip or power failure	No dangerous operating states may occur. If necessary, force an emergency stop.
A restart following resetting of the emergency stop system	An uncontrolled or undefined start-up must be avoided.

Mains Voltage

The following table shows you what to watch with respect to the mains voltage.

In the Case of ...	The Following Must Apply
Permanently installed plants or systems without all-pole mains disconnect switches	There must be a mains disconnect switch or a fuse in the building installation system
Load power supplies, power supply modules	The system voltage range set must correspond to the local system voltage
All circuits of the S7-300	Any fluctuations in, or deviations from, the rated mains voltage must be within the permissible tolerances (see the technical specifications of the S7-300 modules)

24V DC Power Supply

The following table shows you what you must observe in connection with the 24V DC power supply.

<table>
<tr><th>Function</th><th colspan="2">Measures to Take</th></tr>
<tr><td>Buildings</td><td>External lightning protection</td><td rowspan="2">Install lightning protection
(e.g. lightning conductors).</td></tr>
<tr><td>24V DC power supply cables,
signal cables</td><td>Internal lightning protection</td></tr>
<tr><td>24 V power supply</td><td colspan="2">Safe (electrical) extra-low voltage isolation</td></tr>
</table>

Protection Against the Effects of External Electrical Interference

The following table will show you what you must do to protect your programmable controller against electrical interference or faults.

Function	Make Sure That ...
All plants and systems in which the S7-300 is installed	A protective conductor is connected to the plant or system to divert electromagnetic interference.
Supply, signal and bus cables	The conductor routing and installation is correct. (see Section 4.1.7 and 4.1.8)
Signal and bus cables	A cable break or conductor break cannot result in undefined plant or system states.

Rules Relating to S7-300 Power Consumption and Power Loss

The S7-300 modules draw the power they need from the backplane bus and, if required, from an external load power supply.

- The power consumption of all the signal modules from the backplane bus must **not** exceed the current the CPU can deliver to the backplane bus.
- The PS 307 power supply is dependent on the power consumption from the 24V load power supply; this is made up of the total power consumption of the signal modules and all other connected loads.
- The power loss of **all** the components in a cabinet must not exceed the maximum thermal rating of the cabinet.

  Tip: When establishing the required dimensions of the cabinet, ensure that the temperature inside the cabinet does not exceed the permissible 60 °C even where external temperatures are high.

You will find the values for the power consumption and power loss of a module under the technical specifications of the relevant modules.

4.1.2 Configuring the S7-300 Process I/Os

This section contains information concerning the overall configuration of an S7-300 system with a grounded incoming supply (TN-S system). The following aspects are covered:

- Circuit-breaking devices, short-circuit and overload protection to VDE 0100 and VDE 0113
- Load power supplies and load circuits

Definition: Grounded Supply

In a grounded incoming supply system, the neutral is grounded. A single fault to ground or a grounded part of the plant causes the protective devices to trip.

Components and Protective Measures

A number of components and protective measures are prescribed for a plant. The type of components and the degree of compulsion pertaining to the protective measures will depend on the VDE specification applicable to your particular plant. The following table refers to Figure 4-1 on page 4-5.

Table 4-1 VDE Specifications for Configuring a PLC System

Compare ...	Refer to Figure 4-1	VDE 0100	VDE 0113
Disconnecting devices for control systems, sensors and actuators	1	... Part 460: Main switch	... Part 1: Disconnector
Short-circuit and overload protection: In groups for sensors and actuators	2	... Part 725: Single-pole fusing of circuits	... Part 1: • In the case of a grounded secondary circuit: provide **single-pole** protection • Otherwise: provide **all-pole** protection
Load power supply for AC load circuits with more than five electromagnetic devices	3	Galvanic isolation by transformer **recommended**	Galvanic isolation by transformer **mandatory**

Features of Load Power Supplies

The load power supply feeds input and output circuits (load circuits), as well as sensors and actuators. The characteristic features of load power supplies required in specific applications are listed in the following table.

Characteristics of the Load Power Supply	Mandatory for ...	Remarks
Protective separation	Modules that have to be supplied with $\leq$60V DC or $\leq$25V AC	The PS 307 power supplies and the Siemens load power supplies of the 6EP1 series have these characteristics
	24V DC load circuits	
Output voltage tolerances: 20.4 V to 28.8 V 40.8 V to 57.6 V 51 V to 72 V	 24V DC load circuits 48V DC load circuits 60V DC load circuits	If the output voltage tolerances are exceeded, we recommend you fit a back-up capacitor Rating: 200 µF per 1A load current (in the case of full-wave rectification).

Rule: Ground Load Circuits

Load circuits should be grounded.

The common reference potential (ground) guarantees full functionality. Provide a detachable connection to the protective conductor on the load power supply (terminal L- or M) or on the isolating transformer (Figure 4-1, [4]). In the event of power distribution faults, this makes it easier to localize ground faults.

S7-300 Grounding Concept

In the S7-300 grounding concept, a distinction is drawn between the CPU 312 IFM and the other CPUs.

- **CPU 312 IFM**: With the CPU 312 IFM, you can only implement a grounded configuration. The functional ground is connected to the chassis ground internally in CPU 312 IFM (see Section 8.4.1).
- **CPU 313/314/314 IFM/315/315-2 DP/316-2 DP/318-2:** If you use the S7-300 with one of these CPUs on a grounded supply, you should also ground the reference potential of the S7-300. The reference potential is grounded if the connection between the M terminal and the functional ground terminal on the CPUs is in place (factory setting of the CPU).

S7-300 in the Overall Configuration

Figure 4-1 shows the S7-300 in the overall configuration (load power supply and grounding concept) supplied from a TN-S system.

Note: The arrangement of the power supply connections shown does not reflect the actual physical arrangement; this has been done to improve clarity.

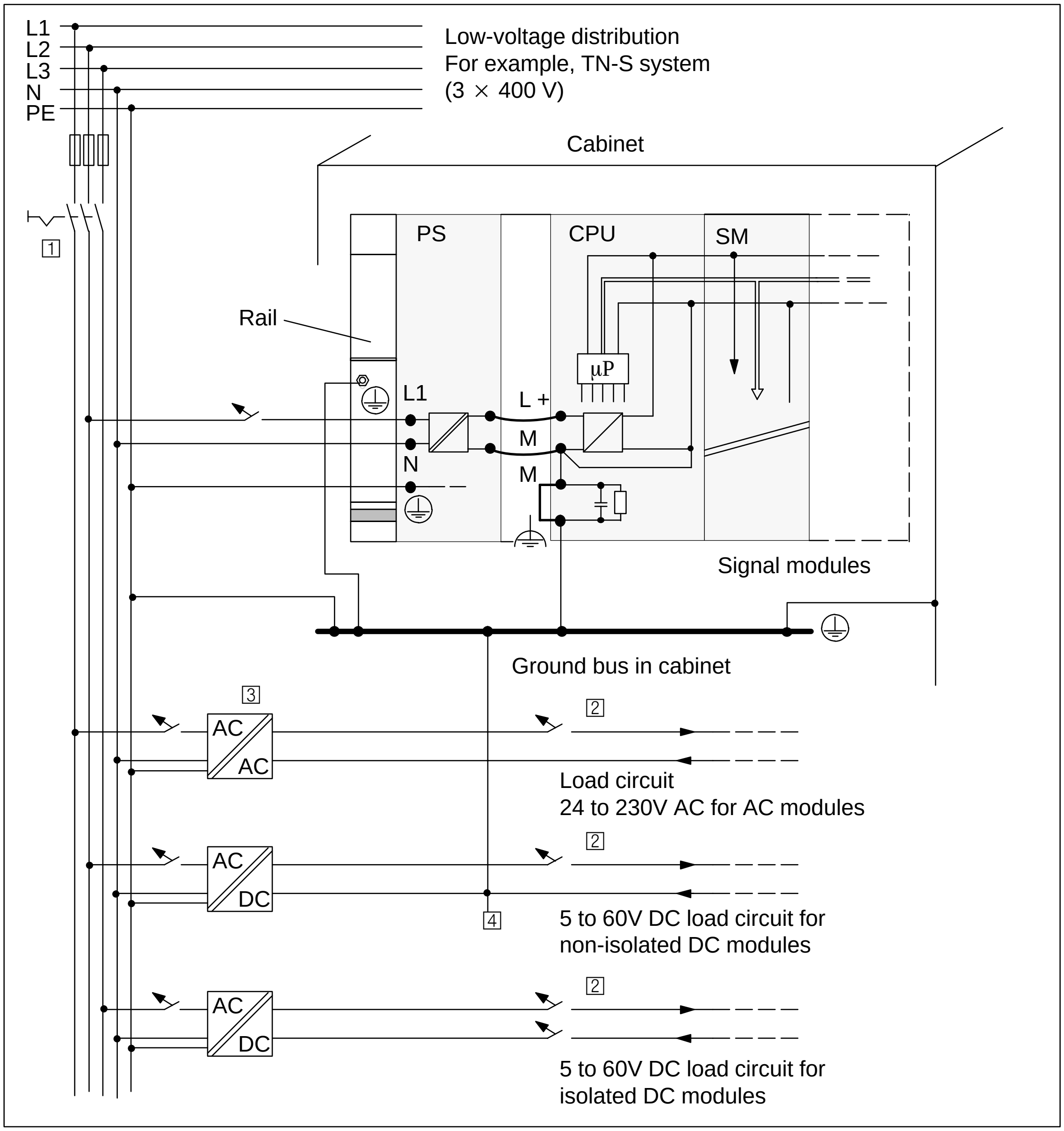


Figure 4-1 Signal Modules Operated on a Grounded Incoming Supply

S7-300 with Load Power Supply from the PS 307

Figure 4-2 shows the S7-300 in the overall configuration (load power supply and grounding concept) in a TN-S power system environment.

Apart from powering the CPU, the PS 307 also supplies the load current for the 24V DC modules.

Note: The arrangement of the power supply connections does not reflect the actual physical arrangement; this has been done to improve clarity.

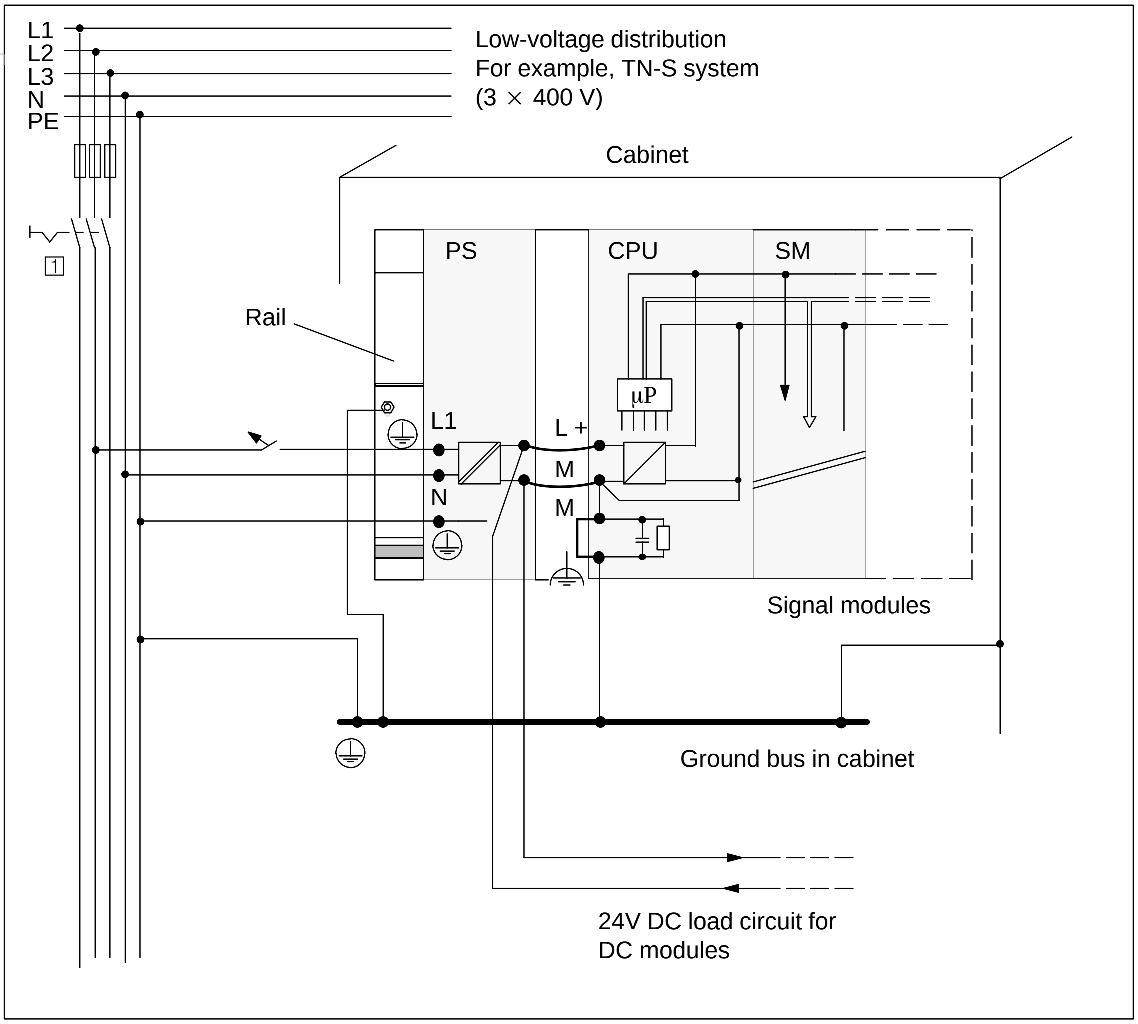


Figure 4-2 Signal Modules Powered from the PS 307

4.1.3 S7-300 Configuration with Grounded Reference Potential

If you install the S7-300 with grounded reference potential, interference currents that might occur are discharged to the protective conductor.

- In the case of CPUs 313/314/314 IFM/315/315-2 DP/316-2DP/318-2, via a jumper inserted between terminal M and functional ground (see Figure 4-3)
- In the case of the CPU 312 IFM, these terminals are connected internally (see Section 8.4.1).

Terminal Connection Model

Figure 4-3 shows the configuration of an S7-300 with CPU 313/314/314 IFM/315/ 315-2 DP/316-2 DP/318-2 with grounded reference potential. If you want to ground the reference potential, you **must not** remove the jumper on the CPU between the M terminal and functional ground**.**

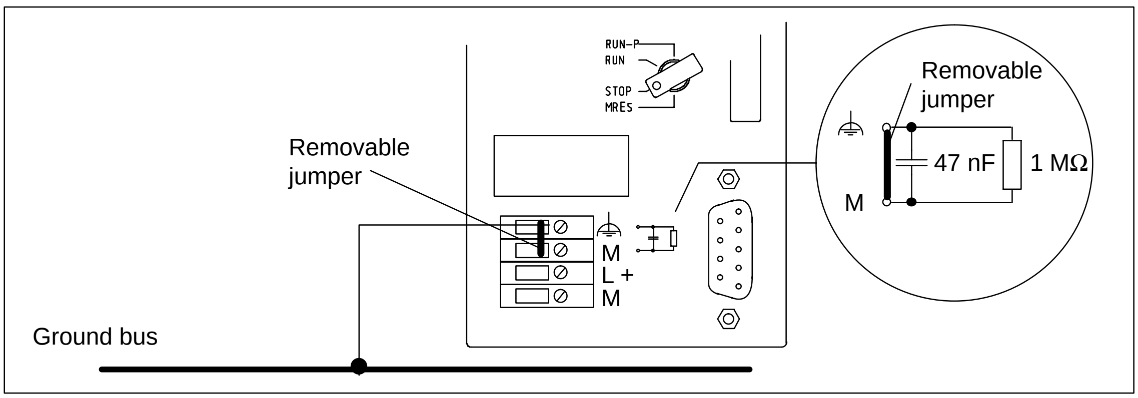


Figure 4-3 S7-300 Configuration with Grounded Reference Potential

4.1.4 S7-300 Configuration with Ungrounded Reference Potential (Not CPU 312 IFM)

If you install the S7-300 with ungrounded reference potential, any interference current is discharged to the protective conductor via an RC network integrated in CPUs 313/314/314 IFM/315/315-2 DP/ 316-2 DP/318-2 (see Figure 4-4).

Application

In plants covering large areas, it may be necessary to configure the S7-300 with ungrounded reference potential for ground fault monitoring purposes, for example. This is the case, for example, in the chemical industry and in power stations.

Terminal Connection Model

Figure 4-4 shows the configuration of an S7-300 (not with CPU 312 IFM) with ungrounded reference potential. If you do not want to ground the reference potential, you must remove the jumper **on the CPU between the M terminal and functional ground**. If the jumper is not in place, the S7-300's reference potential is connected internally to the protective conductor over an RC network and the rail. This discharges radio-frequency interference current and precludes static charges.

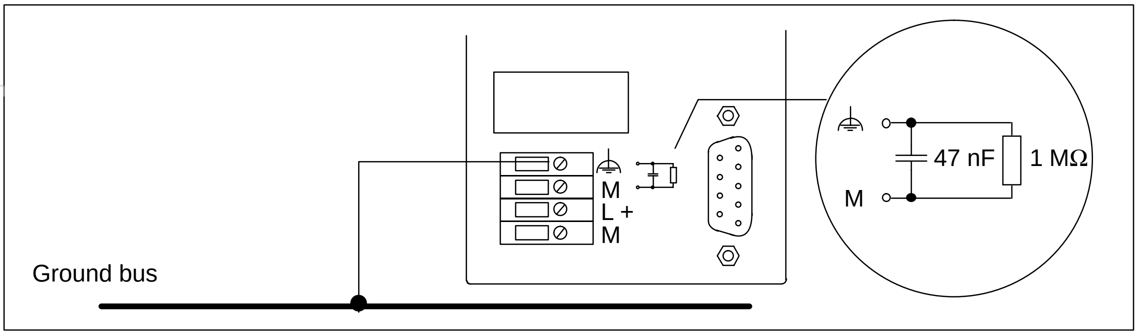


Figure 4-4 S7-300 Configuration with Ungrounded Reference Potential

Power Supply Units

In the case of power supply units, make sure that the secondary winding has no connection to the protective conductor. We recommend the use of the PS 307 power supply module.

Filtering the 24V DC Supply

If you supply the CPU from a battery without grounding the reference potential, you must filter the 24 V DC supply. Use an interference suppression device from Siemens, for example, B84102-K40.

Insulation Monitoring

If dangerous plant conditions can arise as a result of double faults, you must provide some form of insulation monitoring.

4.1.5 S7-300 Configuration with Isolated Modules

Isolation Between...

In configurations with isolated modules, the reference potentials of the control circuit ($M_{internal}$) and load circuit ($M_{external}$) are electrically isolated (see Figure 4-5).

Application

You use isolated modules for the following:

- All AC load circuits
- DC load circuits with separate reference potential

  Examples of load circuits with separate reference potential:

  – DC load circuits whose sensors have different reference potentials (for example if grounded sensors are located at some considerable distance from the control system and no equipotential bonding is possible)

  – DC load circuits whose positive pole (L+) is grounded (battery circuits).

Isolated Modules and Grounding Concept

You can use isolated modules irrespective of whether the reference potential of the control system is grounded or not.

Potentials in a Configuration with Isolated Modules

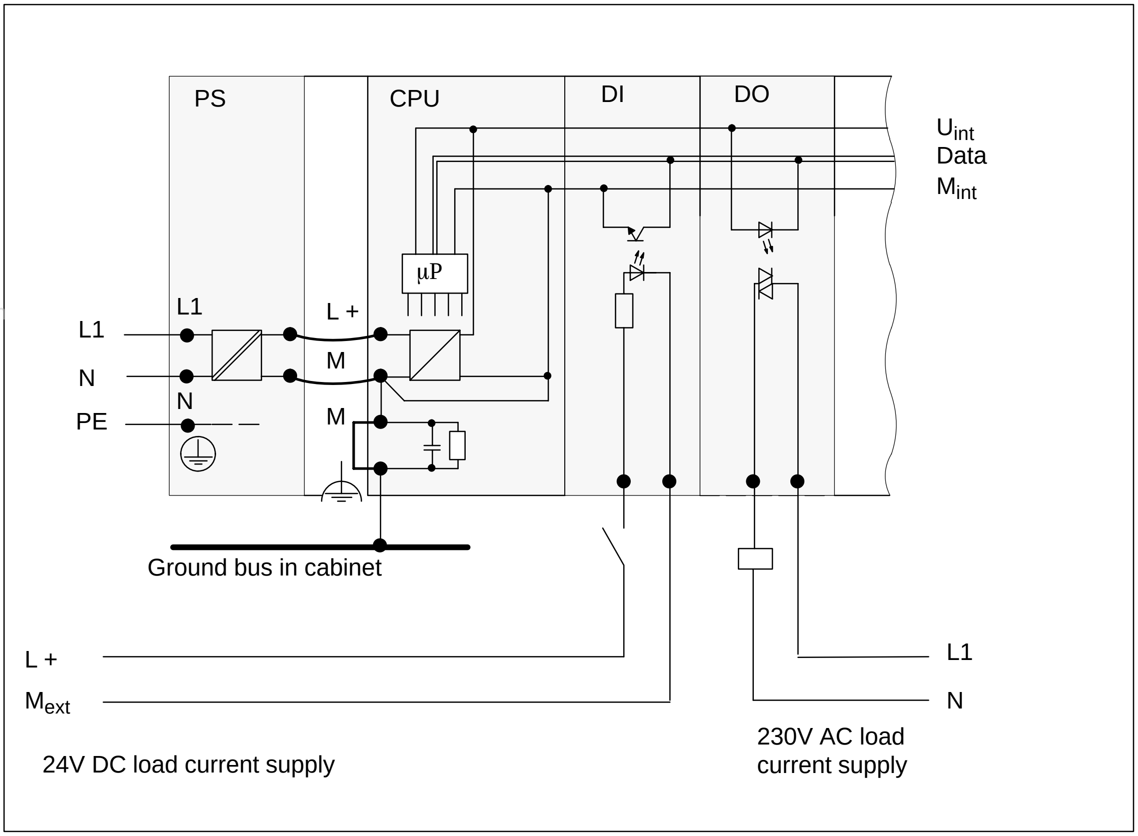


Figure 4-5 Potentials in a Configuration with Isolated Modules

4.1.6 Configuration of an S7-300 with Non-Isolated Modules

Potentials in a Configuration with Non-Isolated Modules

Figure 4-6 shows the potentials of an S7-300 configuration with grounded reference potential with the non-isolated analog input/output module SM 334; AI 4/AO 2 × 8/8Bit. For this analog input/output module, you must connect one of the M_{ANA} grounds with the chassis ground of the CPU.

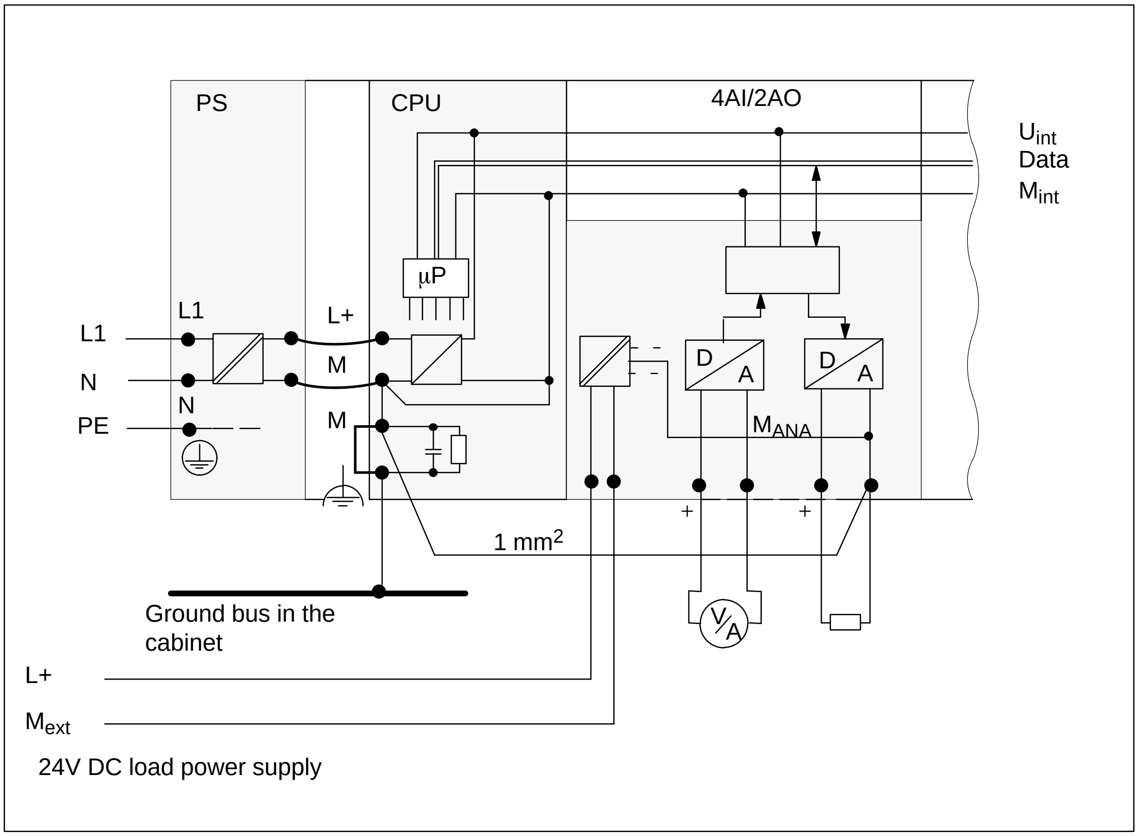


Figure 4-6 Potentials in a Configuration with the Non-Isolated SM 334 Analog Input/Output Module; AI 4/AO 2 × 8/8Bit

4.1.7 Cable/Wiring Routing Inside Buildings

Rules for EMC Cable/Wiring Routing

Inside buildings (inside and outside cabinets), clearances must be observed between groups of different cables to achieve the necessary electromagnetic compatibility (EMC). Table 4-2 provides you with information on the general rules governing clearances to enable you to choose the right cables.

How to Read the Table

To find out how to run two cables of different types, proceed as follows:

1. Look up the type of the first cable in column 1 (Cables for ...).
2. Look up the type of the second cable in the corresponding field in column 2 (and Cables for ...).
3. Read off the guidelines to be observed from column 3 (Run ...).

Table 4-2 Cabling Inside Buildings

Cables for ...	and Cables for ...	Run ...
Bus signals, shielded (SINEC L1, PROFIBUS) Data signals, shielded (programming devices, operator panels, printers, counter inputs, etc.) Analog signals, shielded Direct voltage (≤ 60 V), unshielded Process signals (≤ 25 V), shielded Alternating voltage (≤ 25 V), unshielded Monitors (coaxial cable)	Bus signals, shielded (SINEC L1, PROFIBUS) Data signals, shielded (programming devices, operator panels, printers, counter inputs, etc.) Analog signals, shielded Direct voltage (≤ 60 V), unshielded Process signals (≤ 25 V), shielded Alternating voltage (≤ 25 V), unshielded Monitors (coaxial cable)	In common bundles or cable ducts
	Direct voltage (> 60 V and ≤ 400 V), unshielded Alternating voltage (> 25 V and ≤ 400 V), unshielded	In separate bundles or cable ducts (no minimum clearance necessary)
	Direct and alternating voltages (> 400 V), unshielded	**Inside cabinets:** In separate bundles or cable ducts (no minimum clearance necessary) **Outside cabinets:** On separate cable racks with a clearance of at least 10 cm (3.93 in.)

Table 4-2 Cable/Wiring Routing Inside Buildings, continued

Cables for ...	and Cables for ...	Run ...
Direct voltage (> 60 V and ≤ 400 V), unshielded Alternating voltage (> 25 V and ≤ 400 V), unshielded	Bus signals, shielded (SINEC L1, PROFIBUS) Data signals, shielded (programming devices, OPs, printers, count signals, etc.) Analog signals, shielded Direct voltage (≤ 60 V), unshielded Process (≤ 25 V), shielded Alternating voltage (≤ 25 V), unshielded Monitors (coaxial cable)	In separate bundles or cable ducts (no minimum clearance necessary)
	Direct voltage (> 60 V and ≤ 400 V), unshielded Alternating voltage (> 25 V and ≤ 400 V), unshielded	In common bundles or cable ducts
	Direct and alternating voltages (> 400 V), unshielded	**Inside cabinets:** In separate bundles or cable ducts (no minimum clearance necessary) **Outside cabinets:** On separate cable racks with a clearance of at least 10 cm (3.93 in.)

Table 4-2 Cable/Wiring Routing Inside Buildings, continued

Cables for ...	and Cables for ...	Run ...
Direct and alternating voltages ($>$ 400 V), unshielded	Bus signals, shielded (SINEC L1, PROFIBUS) Data signals, shielded (programming devices, OPs, printers, count signals, etc.) Analog signals, shielded Direct voltage ($\le$ 60 V), unshielded Process ($\le$ 25 V), shielded Alternating voltage ($\le$ 25 V), unshielded Monitors (coaxial cable)	**Inside cabinets:** In separate bundles or cable ducts (no minimum clearance necessary) **Outside cabinets:** On separate cable racks with a clearance of at least 10 cm (3.93 in.)
	Direct voltage ($>$ 60 V and $\le$ 400 V), unshielded Alternating voltage ($>$ 25 V and $\le$ 400 V), unshielded	
Direct and alternating voltages ($>$ 400 V), unshielded	Direct and alternating voltages ($>$ 400 V), unshielded	In common bundles or cable ducts
SINEC H1	SINEC H1	In common bundles or cable ducts
	Others	In separate bundles or cable ducts with a clearance of at least 50 cm (19.65 in.)

4.1.8 Cable/Wiring Routing Outside Buildings

Rules for EMC Cable/Wiring Routing

When installing cables outside buildings, the same EMC rules apply as for inside buildings. The following also applies:

- Run cables on metal cable supports.
- Establish an electrical connection between the joints in the cable supports.
- Ground the cable supports.
- If necessary, provide adequate equipotential bonding between the various items of equipment connected.
- Take the necessary (internal and external) lightning protection and grounding measures in as far as they are applicable to your particular application (see below).

Rules for Lightning Protection Outside Buildings

Run your cables either:

- in metal conduits grounded at both ends, or
- in concrete cable ducts with continuous end-to-end armoring.

Overvoltage Protection Equipment

An individual appraisal of the entire plant is necessary before any lightning protection measures are taken (see Section 4.2).

4.1.9 Protecting Digital Output Modules from Inductive Overvoltage

Integrated Overvoltage Protection

The digital output modules of the S7-300 have integral surge protectors. Surge voltages occur when inductive loads (for example, relay coils and contactors) are switched off.

Additional Overvoltage Protection

Inductive loads should only be fitted with supplementary surge protectors in the following cases:

- If SIMATIC output circuits can be switched off by means of additionally installed contacts (e.g. relay emergency stop contacts)
- If the inductive loads are not driven by SIMATIC modules

Note: Ask the supplier of the inductances how the various overvoltage protection devices should be rated.

Example:

Figure 4-7 shows an output circuit that makes supplementary overvoltage protection necessary.

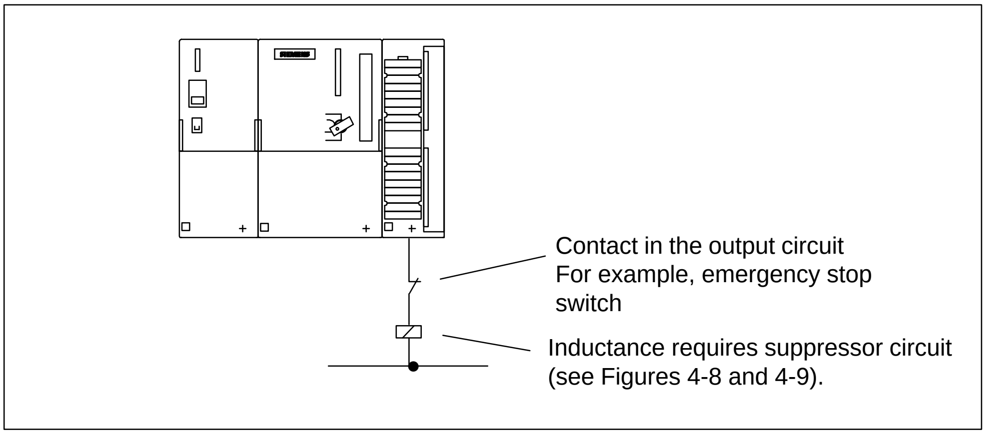


Figure 4-7 Relay Contact for Emergency Stop in the Output Circuit

Suppressor Circuit with DC-Operated Coils with Diodes and Zener Diodes

DC-operated coils are connected with diodes or Zener diodes.

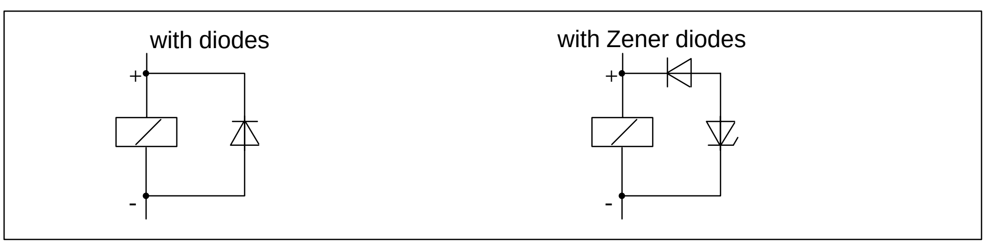


Figure 4-8 Suppressor Circuit with DC-Operated Coils with Diodes and Zener Diodes

Suppressor Circuit with Diodes/Zener Diodes

Diode/Zener diode circuits have the following characteristics:

- The overvoltages induced on circuit interruption are completely suppressed/Zener diode has a higher cut-off voltage.
- They have a high time delay (six to nine times higher than without a diode circuit)/Zener diode interrupts switch faster than a diode circuit.

Suppressor Circuit with AC-Operated Coils

AC-operated coils are connected with varistors or RC elements.

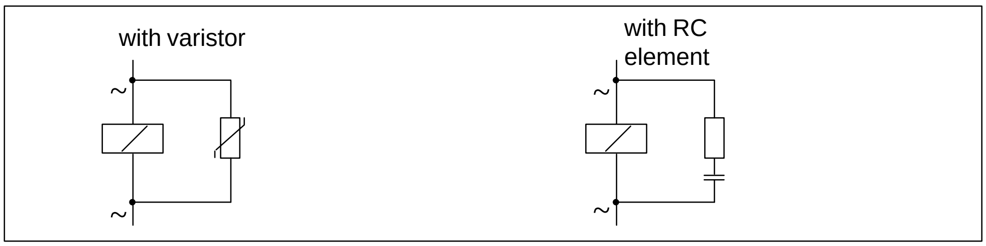


Figure 4-9 Suppressor Circuit with AC-Operated Coils

Suppressor Circuit with Varistors

Suppressor circuits with varistors have the following characteristics:

- The amplitude of the switching overvoltage is limited, but not damped
- The wavefront steepness remains the same
- Very short time delay

Suppressor Circuit with RC Elements

Suppressor circuits with RC elements have the following characteristics:

- The amplitude and wavefront steepness of the switching overvoltage are reduced
- Short time delay.

4.2 Lightning Protection

Section	Contents	Page
4.2.1	Lightning Protection Zone Concept	4-21
4.2.2	Rules for the Transition Between Lightning Protection Zones 0↔1	4-23
4.2.3	Rules for the Transition Between Lightning Protection Zones 1↔2 and Greater	4-25
4.2.4	Sample Circuit for Overvoltage Protection of Networked S7-300s	4-28

Reference Literature

The solutions given are based on the lightning protection zone concept described in the IEC 1312-1 “Protection against LEMP”.

Overview

Failures are very often the result of overvoltages caused by:

- Atmospheric discharge or
- Electrostatic discharge.

We will begin by showing you what the theory of overvoltage protection is based on: the lightning protection zones concept.

At the end of this section, you will find rules for the transitions between the individual lightning protection zones.

Note

This section can only provide information on the protection of a **programmable controller** against overvoltages.

However, complete protection against overvoltage is guaranteed only if the whole surrounding building is designed to provide protection against overvoltages. This applies especially to constructional measures for the building at the planning stage.

If you wish to obtain detailed information on overvoltage protection, we therefore recommend you to address your Siemens contact or a company specialized in lightning protection.

4.2.1 Lightning Protection Zone Concept

The Principle of the Lightning Protection Zone Concept

The principle of the lightning protection zone concept states that the volume to be protected, for example, a manufacturing hall, is subdivided into lightning protection zones in accordance with EMC guidelines (see Figure 4-10).

The individual lightning protection zones are made up of:

The outer lightning protection of the building (field side)	Lightning protection zone 0
Shielding	
• Buildings	Lightning protection zone 1
• Rooms and/or	Lightning protection zone 2
• Devices	Lightning protection zone 3

Effects of the Lightning Strike

Direct lightning strikes occur in lightning protection zone 0. The lightning strike creates high-energy electromagnetic fields which can be reduced or removed from one lightning protection zone to the next by suitable lightning protection elements/measures.

Overvoltage

In lightning protection zones 1 and higher, surges can result from switching operations and interference.

Schematic of the Lightning Protection Zones

Figure 4-10 shows a schematic of the lightning protection zone concept for a free-standing building.

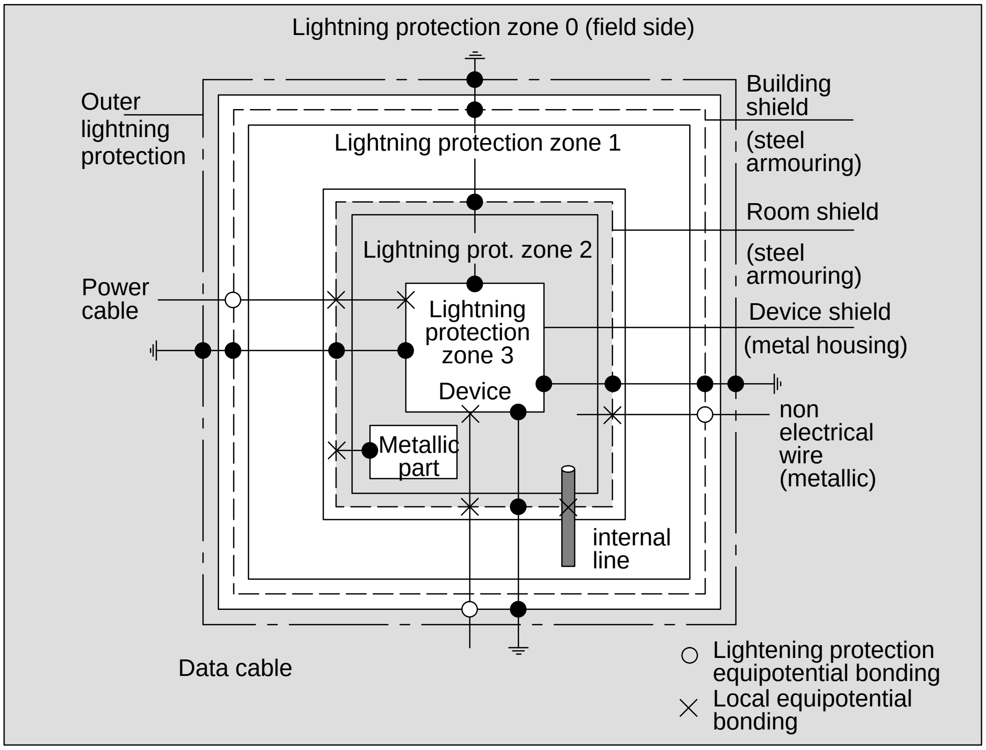


Figure 4-10 Lightning Protection Zones of a Building

Principle of the Transitions between Lightning Protection Zones

At the transitions between the lightning protection zones, you must take measures to prevent surges being conducted further.

The lightning protection zone concept also states that all cables at the transitions between the lightning protection zones that can carry lightning stroke current (!) must be included in the lightning protection equipotential bonding.

Lines that can carry lightning stroke current include:

- Metal pipelines (for example, water, gas and heat)
- Power cables (for example, line voltage, 24 V supply)

  and
- Data cables (for example, bus cable).

4.2.2 Rules for the Transition Between Lightning Protection Zones 0 ↔ 1

Rule for the Transition 0 ↔ 1 (Lightning Protection Equipotential Bonding)

The following measures are suitable for lightning protection equipotential bonding at the transition between lightning protection zones 0 ↔ 1:

- Use grounded, spiraled, current-conducting metal strips or metal braiding, for example, NYCY or A2Y(K)Y, as a cable shield at the start and end,

  and

- lay cable
  - in continuous metal pipes that are grounded at the start and end, or
  - in ducts of armored concrete with continuous armoring or
  - on closed metal cable racks grounded at the start and end,

  or

- use fiber optic cables instead of lightning stroke current-carrying cables.

Additional Measures

If you cannot take the measures listed above, you must install a high-voltage protector at the 0 ↔ 1 transition with a corresponding lightning conductor.
Table 4-3 contains the components you can use for high-voltage protection of your plant.

Table 4-3 High-Voltage Protection of Cables Using Surge Protection Components

No.	Cables for ...	... with the Following at Transition 0 ↔ 1		Order No.
1	• 3-phase TN-C system	3	DEHNport lightning conductors Phase L1/L2/L3 to PEN	5 SD 7 028*
	• 3-phase TN-S and TT system	4	DEHNport lightning conductors Phase L1/L2/L3/N to PE	5 SD 7 028*
	• AC TN-L, TN-S, TT system	2	DEHNport lightning conductors Phase L1 + N to PE	5 SD 7 028*
2	24V DC power supply	1	KT lightning conductor Type A D 24 V	DSN: 919 253

Table 4-3 High-Voltage Protection of Cables Using Surge Protection Components, continued

No.	Cables for ...	... with the Following at Transition 0 ↔ 1	Order No.
3	Bus cable • MPI, RS 485	• up to 500 kbps 1 KT lightning conductor Type ARE 8 V -	DSN: 919 232
		• over 500 kbps 1 KT lightning conductor Type AHFD 5 V -	DSN: 919 270
	• RS 232 (V.24)	• per core pair 1 KT lightning conductor Type ARE 15 V -	DSN: 919 231
4	Inputs/outputs of digital modules and power supply • 24V DC	1 KT lightning conductor Type AD 24 V -	DSN: 919 253
	• 120/230V AC	2 DEHNguard 150 surge arresters	900 603*
5	Inputs/outputs of analog modules • Up to 12 V +/–	1 KT lightning conductor Type ALE 15 V -	DSN: 919 220
	• Up to 24 V +/–	1 KT lightning conductor Type ALE 48 V -	DSN: 919 227
	• Up to 48 V +/–	1 KT lightning conductor Type ALE 60 V -	DSN: 919 222

* You can order these components direct from DEHN + SÖHNE
GmbH + Co. KG
Elektrotechnische Fabrik
Hans-Dehn-Str. 1
D-92318 Neumarkt
Federal Republic of Germany

4.2.3 Rules for the Transitions Between 1 ↔ 2 and Greater Lightning Protection Zones

Rules for 1 ↔ 2 and Greater Transitions (Local Equipotential Bonding)

The following applies to all 1 ↔ 2 and greater lightning protection zone transitions:

- Set up local equipotential bonding at each subsequent lightning protection zone transition.
- Include all cables (also metal conduits, for example) in the local equipotential bonding at all subsequent lightning protection zone transitions.
- Include all metal installations located within the lightning protection zone in the local equipotential bonding (for example, metal part within lightning protection zone 2 at transition 1 ↔ 2).

Additional Measures

We recommend low-voltage protection:

- For all 1 ↔ 2 and greater lightning protection zone transitions

  and

- For all cables that run within a lightning protection zone and are longer than 100 m

Lightning Protection Element for the 24V DC Power Supply

You must use only the KT lightning conductor, Type AD 24 V SIMATIC for the 24V DC power supply of the S7-300. All other surge protection components do not meet the required tolerance range of 20.4 V to 28.8 V of the S7-300's power supply.

Lightning Conductor for Signal Modules

You can use standard surge protection components for the digital input/output modules. However, please note that these only permit a maximum of 1.15 × V_{Nom} = 27.6 V for a rated voltage of 24V DC. If the tolerance of your 24V DC power supply is higher, use the surge protection components for 48V DC nominal voltage.

You can also use the KT lightning conductor, Type AD 24 V SIMATIC. However, this can result in the following restrictions:

- Digital inputs: An increased input current can flow in the case of negative input voltages.
- Digital outputs: The release time of contactors can increase significantly.

Low-Voltage Protection Elements for 1 ↔ 2

We recommend the surge protection components listed in Table 4-4 for the interfaces between lightning protection zones 1 ↔ 2. You must use these low-voltage protection elements for the S7-300 in order to meet the conditions for the CE mark.

Table 4-4 Low-Voltage Protection for Lightning Protection Zone 1 ↔ 2

No.	Cables for ...	... with the Following at Transition 1 ↔ 2	Order No.
1	• 3-phase TN-C system	3 DEHNguard 275 surge arresters	900 600* 5 SD 7 030
	• 3-phase TN-S and TT system	4 DEHNguard 275 surge arresters	900 600* 5 SD 7 030
	• AC TN-L, TN-S, TT system	2 DEHNguard 275 surge arresters	900 600* 5 SD 7 030
2	24V DC power supply	1 KT lightning conductor Type A D 24 V	DSN: 919 253
3	Bus cable • MPI, RS 485	• up to 500 kbps 1 KT lightning conductor Type ARE 8 V -	DSN: 919 232
		• over 500 kbps 1 KT lightning conductor Type AHFD 5 V -	DSN: 919 270
	• RS 232 (V.24)	• per core pair 1 KT lightning conductor Type ARE 15 V -	DSN: 919 231
4	Inputs/outputs of digital modules • 24V DC	1 KT lightning conductor Type AD 24 V -	DSN: 919 253
	• 120/230V AC	2 DEHNguard 150 surge arresters	900 603*
5	Inputs of analog modules • Up to 12 V +/–	1 KT ALD 12 V terminal block on insulated rail	DSN: 919 216

* You can order these components direct from DEHN + SÖHNE
GmbH + Co. KG
Elektrotechnische Fabrik
Hans-Dehn-Str. 1
D-92318 Neumarkt
Federal Republic of Germany

Low-Voltage Protection Elements for 2 ↔ 3

We recommend the surge protection components listed in Table 4-5 for the transitions between lightning protection zones 2 ↔ 3. You must use these low-voltage protection elements for the S7-300 in order to meet the conditions for the CE mark.

Table 4-5 Low-Voltage Protection for Lightning Protection Zone 2 ↔ 3

No.	Cables for ...	... with the Following at Transition 2 ↔ 3	Order No.
1	• 3-phase TN-C system	3 DEHNguard 275 surge arresters	900 600* 5 SD 7 030
	• 3-phase TN-S and TT system	4 DEHNguard 275 surge arresters	900 600* 5 SD 7 030
	• AC TN-L, TN-S, TT system	2 DEHNguard 275 surge arresters	900 600* 5 SD 7 030
2	24V DC power supply	1 KT lightning conductor Type A D 24 V	DSN: 919 253
3	Bus cable • MPI, RS 485	• up to 500 kbps 1 KT lightning conductor Type ARE 8 V -	DSN: 919 232
		• over 500 kbps 1 KT lightning conductor Type AHFD 5 V -	DSN: 919 270
	• RS 232 (V.24)	• per core pair 1 KT lightning conductor Type ARE 15 V -	DSN: 919 231
4	Inputs of digital modules • 24V DC	1 Terminal block FDK 60 V on insulated rail	DSN: 919 997
	• 120/230V AC	2 DEHNguard 150 surge arresters	900 603*
5	Outputs of analog modules • Up to 12 V +/–	1 Terminal block Type FDK 12 V on an insulated rail, which is connected to M – of the module supply	DSN: 919 999

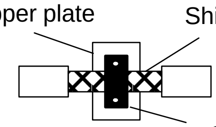
* You can order these components direct from DEHN + SÖHNE
GmbH + Co. KG
Elektrotechnische Fabrik
Hans-Dehn-Str. 1
D-92318 Neumarkt
Federal Republic of Germany

4.2.4 Sample Circuit for Overvoltage Protection of Networked S7-300s

Components in Figure 4-11

Table 4-6 explains the consecutive numbers in Figure 4-11:

Table 4-6 Example of a Configuration Fulfilling Lightning Protection Requirements (Legend for Figure 4-11)

No. from Figure 4-11	Components	Description
1	DEHNport lightning conductors, 2 - 4 depending on mains system Order no.: 900 100*	High-voltage protection against direct lightning strikes and surges as of transition 0 ↔ 1
2	2 DEHNguard 275 surge arresters, Order no.: 900 600*	High-voltage surge protection at transition 1 ↔ 2
3	• In the spur line 1 intermediate adapter Type FS 9E-PB Order no.: DSN 924 017 • In the spur line 1 standard rail 35 mm with connecting cable Type ÜSD-9-PB/S-KB Order no.: DSN 924 064	Low-voltage surge protection for RS 485 interfaces at transition 1 ↔ 2
4	Digital modules: KT lightning conductor, type AD 24 V SIMATIC Analog modules: KT lightning conductor, type ARE 12 V–	Low-voltage surge protection at inputs and outputs of the signal modules at transition 1 ↔ 2
5	Shielding the bus cable:  	–
6	Equipotential bonding cable 16 mm^2	–
7	KT lightning conductor, type AHFD, for building entry point Order No.: DSN 919 270	Low-voltage surge protection for RS 485 interfaces at transition 0 ↔ 1

Interconnection Example

Figure 4-11 gives an example of how to wire connect networked S7-300s in order to achieve effective protection against surges:

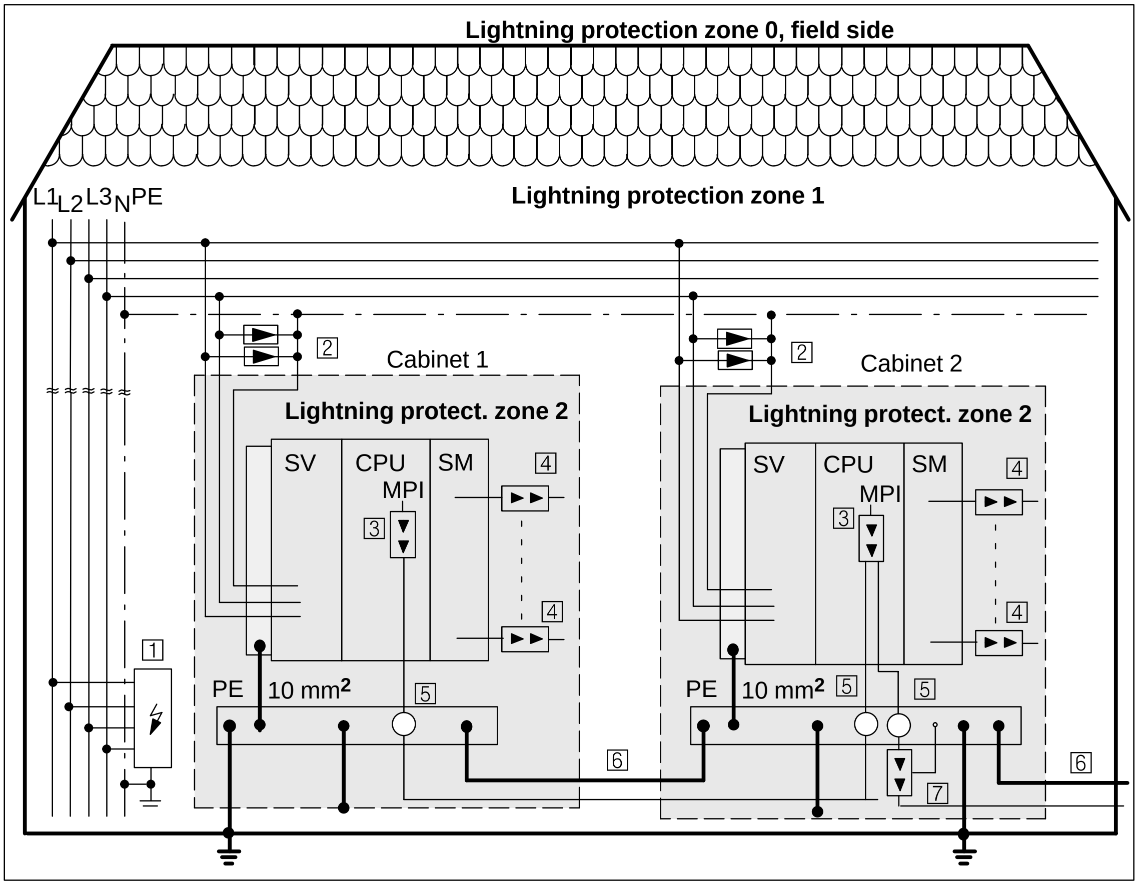


Figure 4-11 Example of the Interconnection of Networked S7-300s

4.3 Wiring

Prerequisite

You have already installed the S7-300 as described in Chapter 2.

4.3.1 Wiring Rules

Table 4-7 Wiring Rules for the Power Supply and CPU

Wiring Rules for...		Power Supply and CPU
Connectable cable cross-sections for rigid cables		No
Connectable cable cross-sections for flexible cables	Without wire end ferrule	0.25 to 2.5 mm^2
	With wire end ferrule	0.25 to 1.5 mm^2
Number of cables per terminal connection		1 or combination of 2 conductors up to 1.5 mm^2 (total) in a common wire end ferrule
Maximum outside diameter of the insulation		∅ 3.8 mm
Length of stripped lines	Without insulating collar	11 mm
	With insulating collar	11 mm
Wire end ferrules to DIN 46228	Without insulating collar	Version A, 10 to 12 mm long
	With insulating collar	Version E, up to 12 mm long

Table 4-8 Wiring Rules for Module Front Connectors

Wiring Rules for...		Module Front Connectors (Spring Terminal and Screw-Type Terminal)	
		20-pin	40-pin
Connectable cable cross-sections for rigid cables		No	No
Connectable cable cross-sections for flexible cables	Without wire end ferrule	0.25 to 1.5 mm^2	0.25 to 0.75 mm^2
	With wire end ferrule	0.25 to 1.5 mm^2	0.25 to 0.75 mm^2 Potential infeed: 1.5 mm^2
Number of cables per terminal connection		1 or combination of 2 conductors up to 1.5 mm^2 (total) in a common wire end ferrule	1 or combination of 2 conductors up to 0.75 mm^2 (total) in a common wire end ferrule
Maximum outside diameter of the insulation		∅ 3.1 mm Max. qty. 20	∅ 2.0 mm Max. qty. 40
			∅ 3.1 mm Max. qty. 20
Length of stripped lines	Without insulating collar	6 mm	6 mm
	With insulating collar	6 mm	6 mm
Wire end ferrules to DIN 46228	Without insulating collar	Version A, 5 to 7 mm long	Version A, 5 to 7 mm long
	With insulating collar	Version E, up to 6 mm long	Version E, up to 6 mm long

4.3.2 Wiring the Power Supply Module and CPU

Power Cables

Use flexible cables with a cross-section of between 0.25 and 2.5 mm^2 to wire the power supply.

If you use only one cable per connection, you don't need an end ferrule.

Power Connector (not for CPU 312 IFM)

Use the power connector when wiring the PS 307 power supply module to the CPU. The power connector comes with the power supply module.

Wiring the CPU 312 IFM

The PS 307 power supply module and the CPU 312 IFM are wired via the front connector of the integrated inputs/outputs of the CPU 312 IFM (see Section 8.4.1). You therefore cannot use the power connector for the CPU 312 IFM.

Other 24V Connections

Above the power connector on the PS 307 power supply there are still a number of free 24V connections for powering the I/O modules.

Wiring with the Power Connector

To wire the PS 307 power supply module and CPU, proceed as follows (see Figure 4-12).

Warning

Accidental contact with live conductors is possible, if the power supply module and any additional load power supplies are switched on.

Make sure the S7-300 is absolutely dead before doing any wiring!

1. Open the front doors of the PS 307 power supply and CPU.
2. Undo the strain-relief assembly on the PS 307.
3. Strip the insulation from the power cable (230V/120V), and connect it to the PS 307.
4. Screw the strain-relief assembly tight.
5. **CPU 312 IFM:** Strip the insulation off the power cable of the CPU 312 IFM, and connect it to the PS 307 an.

   CPU 313/314/314 IFM/315/315-2 DP/316-2 DP/318-2: Insert the power connector, and screw it in tightly.
6. Close the front doors.

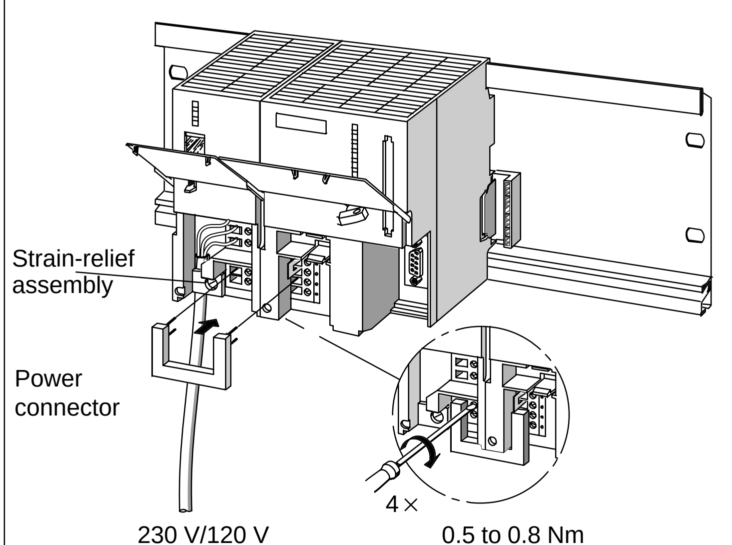


Figure 4-12 Wiring the Power Supply Module and CPU to the Power Connector

Setting the Power Supply to the Required Mains Voltage

Check to see that the voltage selector switch on the power supply module is set to your local mains voltage. This switch is always factory-set to 230 V on the PS 307. To select another mains voltage, do the following:

1. Pry the cover off with a screwdriver.
2. Set the selector to your mains voltage.
3. Replace the cover.

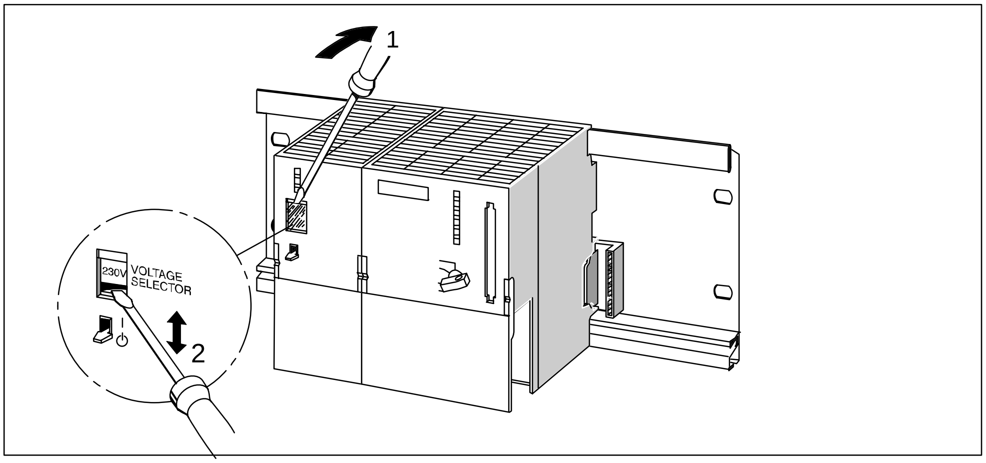


Figure 4-13 Setting the Mains Voltage for the PS 307

4.3.3 Wiring the Front Connectors of the Signal Modules

Cables

You can use flexible cables with cross-sections as in Table 4-8 on page 4-31.

You do not need wire end ferrules. If you use wire end ferrules, only use those listed in Table 4-8 on page 4-31.

Integrated Inputs/Outputs

You wire the integrated inputs/outputs of the CPU 312 IFM and 314 IFM also via the front connector as described in this section.

If you use the possible digital inputs of the CPUs for the special functions, you wire these inputs with shielded cables via a shield contact element (see Section 4.3.4). This also applies when wiring the analog inputs/outputs of the CPU 314 IFM.

Types of Front Connector

You can order the 20- and 40-pin front connectors with spring or screw-type terminals. You will find the order numbers in Appendix F.

Spring Terminals

To wire the front connector using spring terminals, simply insert the screwdriver vertically into the opening with the red opening mechanism, put the cable into the correct terminal, and remove the screwdriver.

Tip: There is a separate opening for test probes up to 2 mm in diameter to the left of the opening for the screwdriver.

Wiring the Front Connector

Wire the screw-type front connector as follows:

1. Prepare the connector for wiring.
2. Wire the connector.
3. Prepare the module for operation.

These three steps are described on the following pages.

Preparing the Connector for Wiring.

Warning

Accidental contact with live conductors is possible if the power supply module and any additional load power supplies are switched on.

Make sure the S7-300 is absolutely dead before doing any wiring!

1. Open the front door.
2. Place the front connector in the wiring position.

   To do this, push the front connector into the signal module until it snaps into place. The front connector still protrudes from the module in this position.

   An advantage of the wiring position is that it makes wiring easier; in the wiring position a wired front connector has no contact with the module.

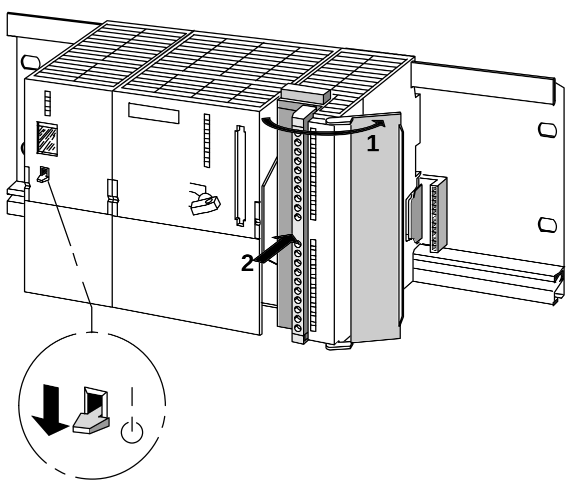


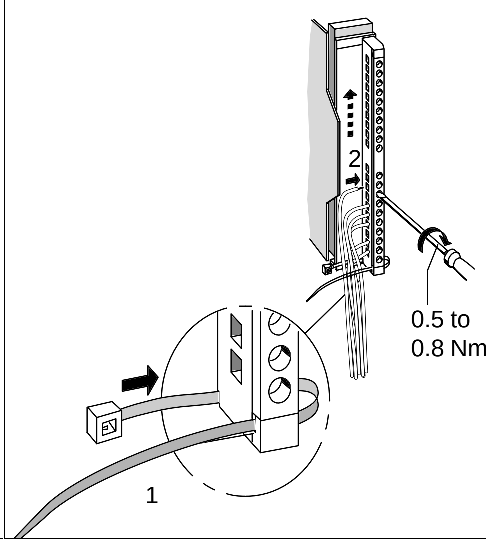
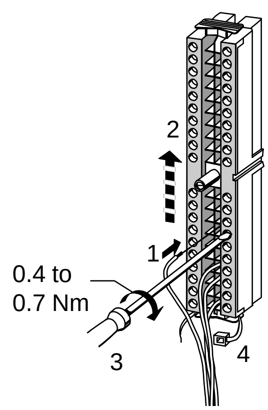
Figure 4-14 Bringing the Front Connector into the Wiring Position

3. Strip the insulation off the cables (see Table 4-8 on page 4-31)
4. Do you want to use end ferrules?

   If so: Press the end ferrules and the cables together

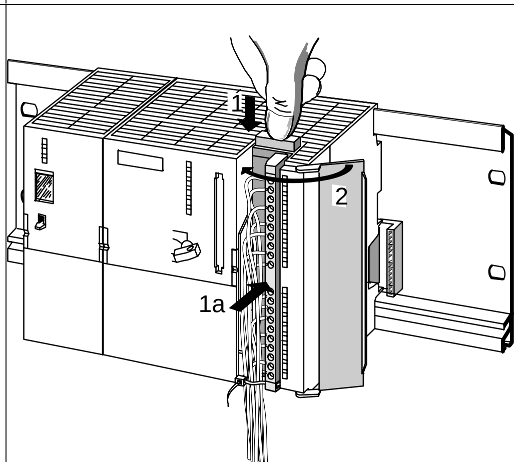
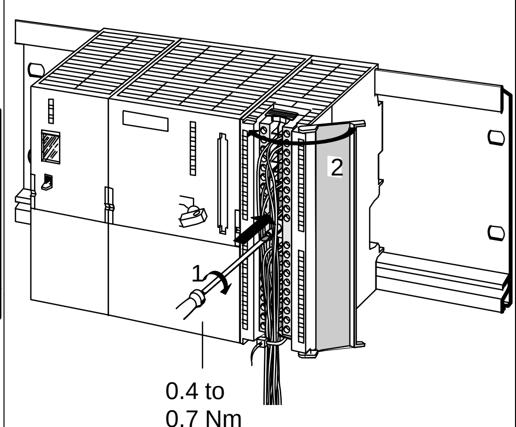
Wiring the Front Connector

Table 4-9 Wiring the Front Connector

Step	20-Pin Front Connector	40-Pin Front Connector
1.	Thread the cable strain-relief assembly into the front connector.	–
2.	Do you want to bring the cables out at the bottom of the module?	
	If so:	
	Start with terminal 20, and wire the terminals in the following order: terminal 20, 19, ... 1.	Starting at terminal 40 or 20, connect up the terminals in alternating order, that is terminals 39, 19, 38, 18 etc., down to terminals 21 and 1.
	If not:	
	Start with terminal 1, and wire the terminals in the following order: terminal 1, 2, ... 20.	Starting at terminal 1 or 21, connect up the terminals in alternating order, that is terminals 2, 22, 3, 23 etc., up to terminals 20 and 40.
3.	**With screw-type terminals:** Also tighten the screws of any terminals that are not wired.	
4.	–	Attach the cable strain-relief assembly around the cable and the front connector.
5.	Pull the cable strain-relief assembly tight. Push the retainer on the strain-relief assembly in to the left; this will improve utilization of the available space.	
–		

Preparing the Signal Module for Operation

Table 4-10 Preparing the Signal Module for Operation

Step	20-Pin Front Connector	40-Pin Front Connector
1.	Press down the unlocking button on the top of the module and, at the same time, push the front connector into its operating position on the module. When the front connector reaches its operating position, the unlocking button will snap back into the locking position.	Tighten screws to bring front connector to its operating position.
	Note: When the front connector is put in its operating position, a front connector encoding device engages in the front connector. The front connector then only fits this type of module (see Section 7.2).	
2.	Close the front door.	
3.	Enter the addresses for identifying the individual channels on the labeling strip.	
4.	Slide the labeling strip into the guides on the front door.	
–		

4.3.4 Connecting Shielded Cables via a Shield Contact Element

Application

Using the shield contact element you can easily connect all the shielded cables of S7 modules to ground by directly connecting the shield contact element to the rail.

Also for the CPU 312 IFM and 314 IFM

You can also use the shield contact element for wiring the integral inputs/outputs of the CPU 312 IFM and 314 IFM, when using inputs for the special functions or when wiring the analog inputs/outputs for the CPU 314 IFM.

Design of the Shield Contact Element

The shield contact element consists of the following parts:

- A fixing bracket with two bolts for attaching the element to the rail (Order No.: 6ES5 390-5AA00-0AA0) and
- The shield terminals

Depending on the cable cross-sections used, you must use the following shield terminal:

Table 4-11 Assignment of Cable Cross-Sections and Terminal Elements

Cable with Shield Diameter	Shield Terminal Order No.:
2 cables with a shield diameter of 2 to 6 mm (0.08 to 0.23 in.) each	6ES7 390-5AB00-0AA0
1 cable with a shield diameter of 3 to 8 mm (0.12 to 0.31 in.)	6ES7 390-5BA00-0AA0
1 cable with a shield diameter of 4 to 13 mm (0.16 to 0.51 in.)	6ES7 390-5CA00-0AA0

The shield contact element is 80 mm (3.15 in.) wide with space for two rows each with 4 shield terminals.

Installing the Shield Contact Element

Install the shield contact element as follows:

1. Push the two bolts of the fixing bracket into the guide on the underside of the rail. Position the fixing bracket under the modules to be wired.
2. Bolt the fixing bracket tight to the rail.
3. A slotted web is arranged at the bottom side of the terminal element. Place the shield terminal at this position onto edge a of the fixing bracket (see Figure 4-15). Press the shield terminals down and swing them into the desired position.

   You can attach up to four terminal elements on each of the two rows of the shield contact element.

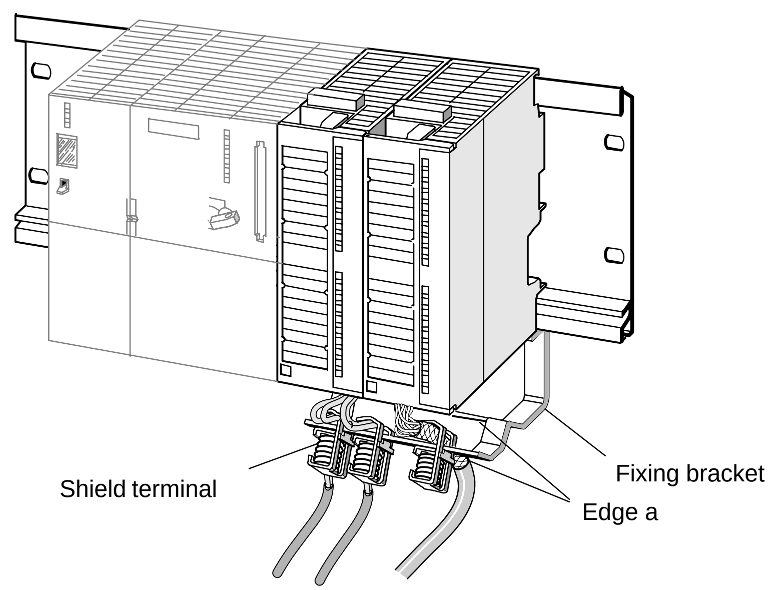


Figure 4-15 Configuration of Two Signal Modules With Shield Contact Element

Attaching Cables

You can only attach one or two shielded cables per shield terminal (see Figure 4-16 and Table 4-11). The cable is connected by its bare cable shield. There must be at least 20 mm (0.78 in.) of bare cable shield. If you need more than 4 shield terminals, start wiring at the rear row of the shield contact element.

Tip: Use a sufficiently long cable between the shield terminal and the front connector. You can thus remove the front connector without the need to also remove the shield terminal.

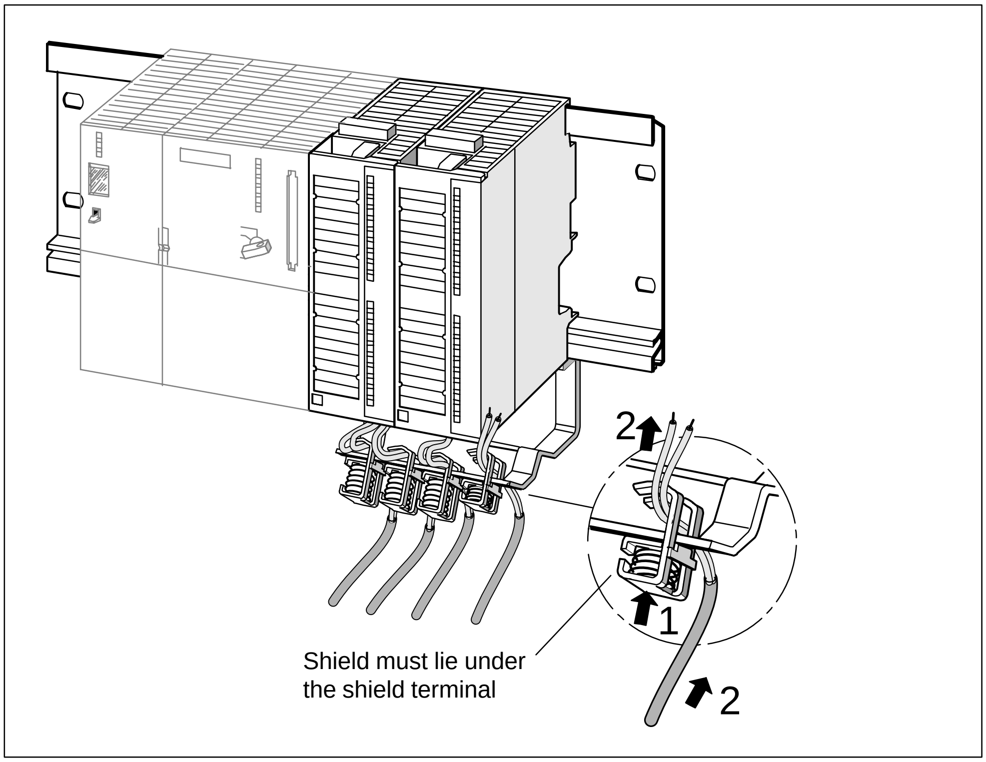


Figure 4-16 Attaching Shielded 2-Wire Cables to a Shield Contact Element

Networking

5

Similar Structure

The structure of an MPI subnet is basically the same as a PROFIBUS subnet. That means the same rules and the same components are used to set up the subnet. The only exception arises if you set a transmission rate > 1.5 Mbps in a PROFIBUS subnet. In this case, you will need other components. Special reference is made to these components where relevant in this documentation.

Since the structure of an MPI subnet does not differ from that of a PROFIBUS subnet, general reference is made in the following sections to configuring a subnet.

In This Chapter

5.1 Configuring a Subnet

In This Chapter

Device = Node

Declaration: In the following, all devices that you connect in an MPI subnet are called nodes.

5.1.1 Prerequisites

MPI/PROFIBUS Addresses

To ensure that all nodes can communicate with one another, you must allocate them an address **before** networking:

- An “MPI address” and a “highest MPI address” in the MPI subnet
- A “PROFIBUS address” and a “highest PROFIBUS address” in a PROFIBUS subnet.

Set these MPI/PROFIBUS addresses individually for each node using the programming device (also on the slave switch in the case of some PROFIBUS-DP slaves).

Note

The RS 485 repeater is not allocated an “MPI address” or a “PROFIBUS address”.

Table 5-1 Permissible MPI/PROFIBUS Addresses

MPI Addresses	PROFIBUS Addresses
0 to 126	0 to 125
Of these, the following are reserved: 0 for the PG 1 for the OP 2 for the CPU	Of these, the following are reserved: 0 for the PG

Rules for the MPI/PROFIBUS Addresses

Observe the following rules before assigning MPI/PROFIBUS addresses:

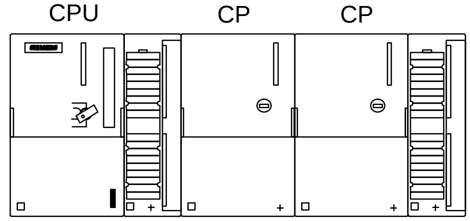
- All MPI/PROFIBUS addresses in a subnet must be different.
- The highest MPI/PROFIBUS address must be ≥ the largest actual MPI/PROFIBUS address and be identical for each node. (Exception: If the programming device is connected to several nodes; see Section 6.3.2).

Differences in the Case of MPI Addresses of CPs/FMs in an S7-300

Please note the following peculiarities and differences when using CPs/FMs with a separate MPI address dependent on the CPU being used.

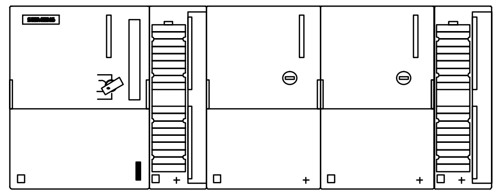
CPU 312 IFM to 316-2 DP:

Table 5-2 MPI Addresses of CPs/FMs in an S7-300 (with the CPU 312 IFM to 316-2 DP)

Options	Example
Example: S7-300 with a CPU and 2 CPs in a configuration. The following 2 possibilities exist for the assignment of MPI addresses of the CP/FM in one configuration:	CPU CP CP 
Option 1 The CPU accepts the MPI addresses of the CPs you set in *STEP 7*. As of *STEP 7 V 4.02* (see Section 11.2)	MPI addr. — MPI addr. "x" — MPI addr. "z"
Option 2 The CPU automatically establishes the MPI addresses of the CPs in their configuration in accordance with the MPI addr. pattern. CPU MPI addr.+1 MPI addr.+2	MPI addr. — MPI addr.+1 — MPI addr.+2

CPU 318-2

An S7-300 with the CPU 318-2 only occupies **one** MPI address in the MPI subnet.



Recommendation for MPI Addresses

Reserve the MPI address “0” for a service programming device and “1” for a service OP that will be connected temporarily to the MPI if required. This means, that you must assign different addresses to programming devices/OPs that are integrated in the MPI subnet.

Recommendation for the MPI address of the CPU in the event of replacement or servicing:

Reserve the MPI address “2” for a CPU. You thus prevent double MPI addresses occurring after connection of a CPU with default settings to the MPI subnet (for example, when replacing a CPU). This means that you must assign an MPI address greater than “2” to the CPUs in the MPI subnet.

Recommendation for PROFIBUS Addresses

Reserve the PROFIBUS address “0” for a service programming device that may subsequently be temporarily connected to the PROFIBUS subnet if required. Allocate other PROFIBUS addresses to the programming devices integrated in the PROFIBUS subnet.

5.1.2 Rules for Configuring a Subnet

In This Section

This chapter describes how to configure a subnet and provides examples.

Segment

A segment is a bus cable between two terminating resistors. A segment can contain up to 32 nodes. A segment is further limited by the permissible cable length, which depends on the transmission rate (see Section 5.1.3).

Rules on Connecting the Nodes of a Subnet

- **Before** you interconnect the individual nodes of the subnet you must assign the MPI address and the highest MPI address or the “PROFIBUS address” and the “highest PROFIBUS address” to each node (except for RS 485 repeater).

  Mark all the nodes in a subnet by putting their address on their housings. In this way, you can always see which node has been assigned which address in your system. For this purpose, each CPU comes with an enclosed sheet of address labels.

- Connect all nodes in the subnet “in a row”; that is, integrate the stationary programming devices and OPs direct in the subnet.

  Connect only those programming devices/OPs that are required for commissioning or maintenance via spur lines to the subnet.

Note

As of 3 Mbps, use only bus connectors with the order no. 6ES7 972-0B.**1**0-0XA0 or 6ES7 972-0B.**4**0-0XA0 to connect the nodes. (see Section 5.2)

As of 3 Mbps, use only the programming device connecting cable with the order no. 6ES7 901-4BD00-0XA0 to connect the programming device. (see Section 5.2)

Rules (Continued)

- If you operate more than 32 nodes on a network, you must connect the bus segments via RS 485 repeaters.

  All bus segments in a PROFIBUS subnet must have at least one DP master and one DP slave between them.
- You connect non-grounded bus segments and grounded bus segments via RS 485 repeaters (see the description of the RS 485 repeater in the *Module Specifications* Reference Manual).

- Each RS 485 repeater that you use reduces the maximum number of nodes on each bus segment. That means if a RS 485 repeater is installed in one of the bus segments, only a further 31 nodes can be installed in that segment. The number of RS 485 repeaters has **no** impact on the maximum number of nodes on the bus, however.

  Up to 10 segments can be installed in a row.
- Switch the terminating resistor on at the first and last node of a segment.
- **Before** you integrate a new node in the subnet, you must switch off its supply voltage.

Components

You connect the individual nodes via bus connectors and the PROFIBUS bus cable (see also Section 5.2). Make sure that the bus connector is provided with a programming device socket so that a programming device can be connected if required.

Use RS 485 repeaters to connect segments or extend the cable.

Terminating Resistor

A cable must be terminated with its surge impedance. To do this, switch on the terminating resistor on the first and last node of a subnet or a segment.

The nodes with a terminating resistor switched on must have their power supply switched on during power up and operation.

The Terminating Resistor on the Bus Connector

Figure 5-1 shows you how to switch on the terminating resistor on the bus connector.

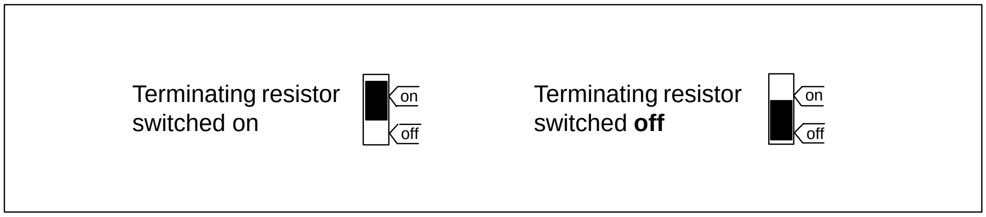


Figure 5-1 Terminating Resistor on the Bus Connector Switched On and Off

The Terminating Resistor on the RS 485 Repeater

Figure 5-2 shows you where to switch on the terminating resistor on the RS 485 repeater.

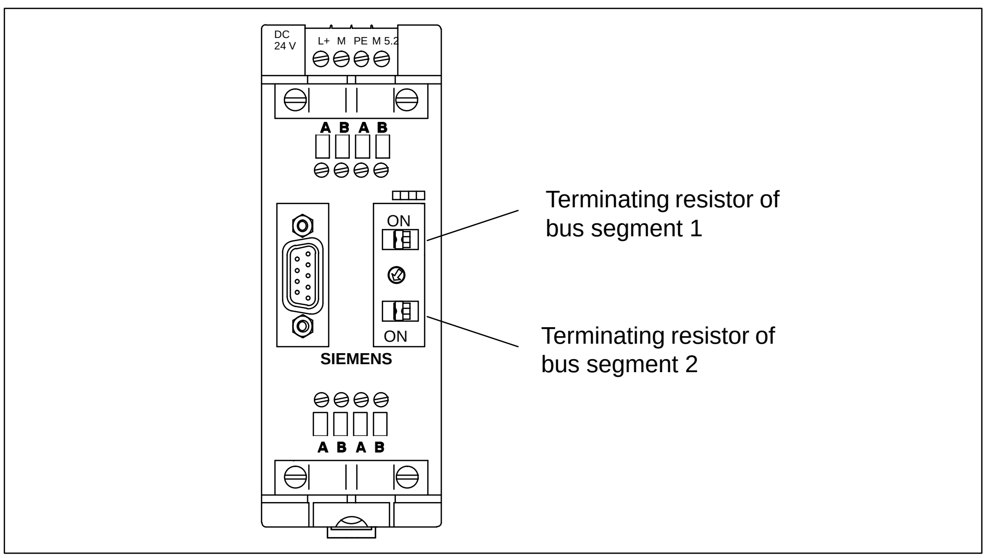
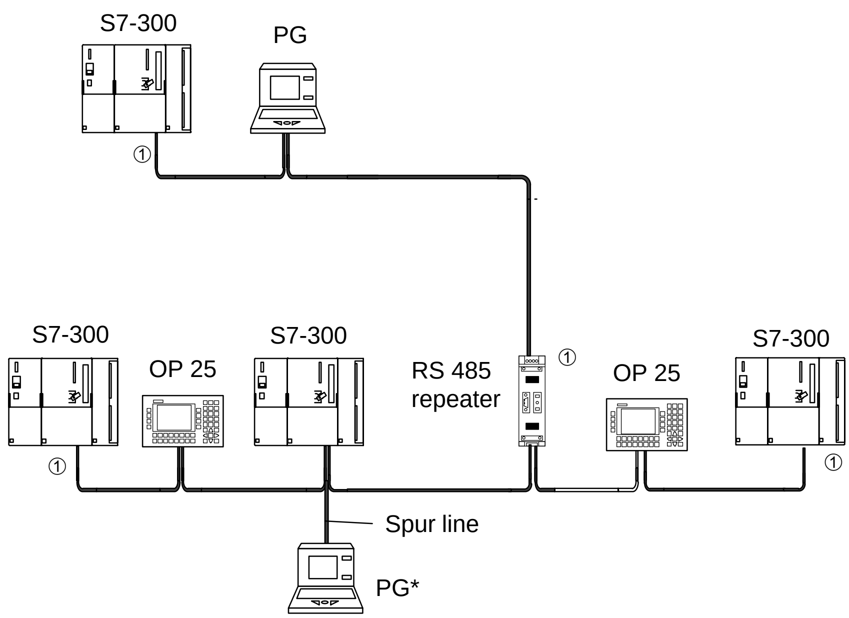


Figure 5-2 Terminating Resistor on the RS 485 Repeater

Example: Terminating Resistor in the MPI Subnet

Figure 5-3 shows where you must connect the terminating resistor in a possible MPI subnet configuration.



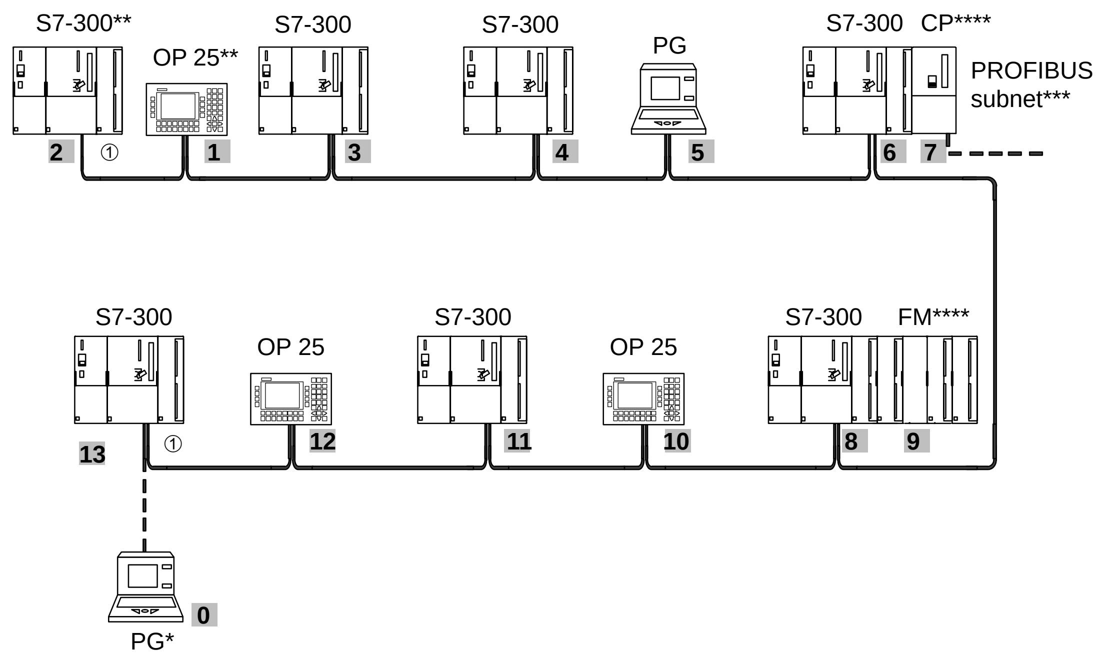
* Connected via spur line for commissioning/maintenance only

① Terminating resistor switched on

Figure 5-3 Connecting Terminating Resistors in an MPI Subnet

Example of an MPI Subnet

Figure 5-4 shows an MPI subnet that is configured in accordance with the above rules.



* Connected via spur line for commissioning/maintenance only (with default MPI address)

** Connected to the MPI subnet later (with default MPI address)

*** The CP also has a PROFIBUS address in addition to the MPI address (address 7 here)

**** In the case of the CPU 318-2-DP, the FMs/CPs do not have their own MPI addresses
In the case of the CPU 312 IFM to 316-2 DP, you can allocate the MPI addresses as you wish

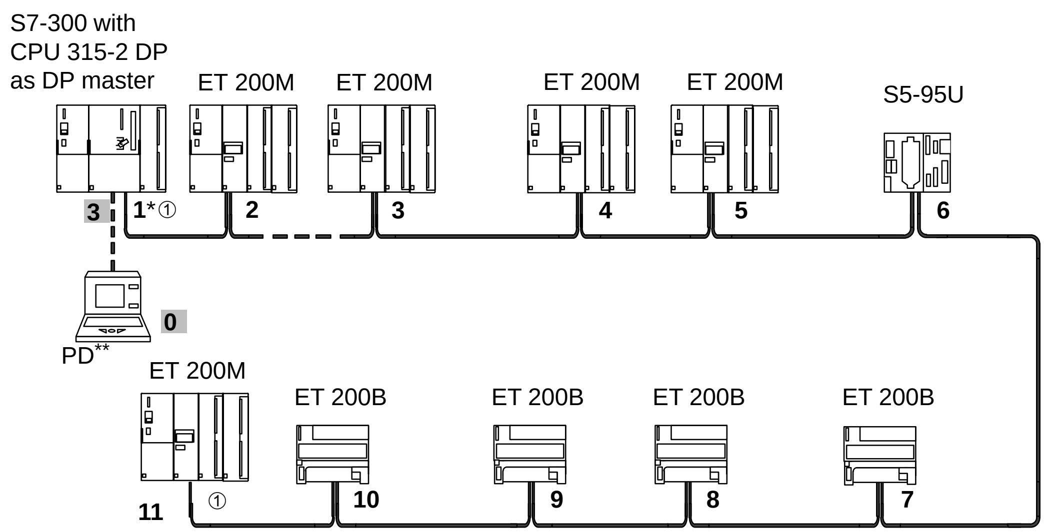
0 ... x MPI addresses of the nodes

① Terminating resistor switched on

Figure 5-4 Example of an MPI Subnet

Example of a PROFIBUS Subnet

Figure 5-5 shows a PROFIBUS subnet that is configured in accordance with the above rules.



* 1 = Default PROFIBUS address for DP master

** Connected to MPI via spur line for commissioning /maintenance only (with MPI address = 0)

0 ... x PROFIBUS addresses of the nodes

0 ... x MPI addresses of the nodes

① Terminating resistor on

Figure 5-5 Example of a PROFIBUS Subnet

Example with the CPU 315-2 DP

Figure 5-6 shows an MPI subnet with an integrated CPU 315-2 DP that is also operating as a DP master in a PROFIBUS subnet.

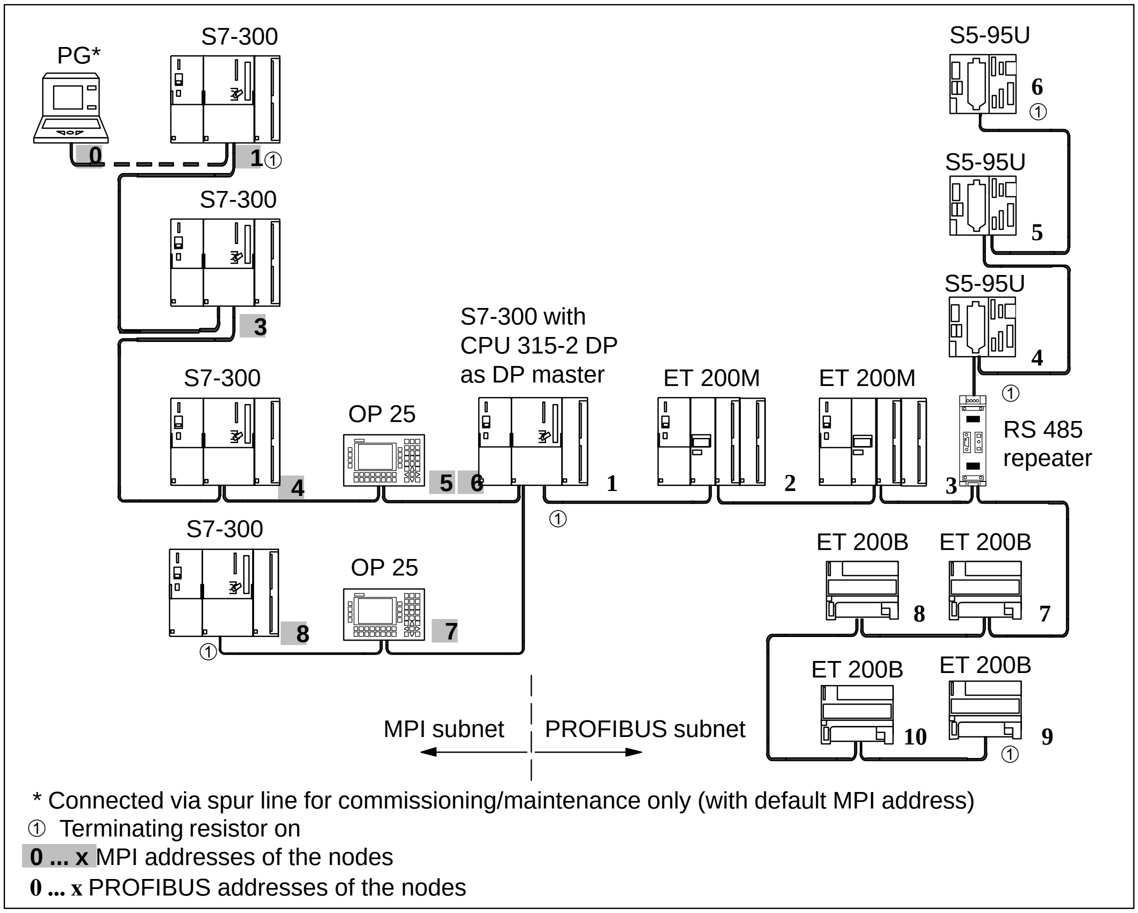


Figure 5-6 Example of a Configuration with the CPU 315-2 DP in an MPI and PROFIBUS Subnet

5.1.3 Cable Lengths

Segment in the MPI Subnet

You can implement cable lengths of up to 50 m (164 ft.) in an MPI subnet segment. The 50 m is measured from the 1st node to the last node of a segment.

Table 5-3 Permissible Cable Lengths in an MPI Subnet Segment

<table>
<tr><th rowspan="2">Transmission rate</th><th colspan="2">Maximum Cable Length of a Segment (in mm)</th></tr>
<tr><th>CPU 312 IFM to 316-2 DP (Non-Isolated MPI Interface)</th><th>318-2 (Non-Isolated MPI Interface)</th></tr>
<tr><td>19.2 kbps</td><td rowspan="2">50</td><td rowspan="2">1000</td></tr>
<tr><td>187.5 kbps</td></tr>
<tr><td>1.5 Mbps</td><td>–</td><td>200</td></tr>
<tr><td>3.0 Mbps</td><td rowspan="3">–</td><td rowspan="3">100</td></tr>
<tr><td>6.0 Mbps</td></tr>
<tr><td>12.0 Mbps</td></tr>
</table>

Segment in the PROFIBUS Subnet

The cable length in a segment of a PROFIBUS subnet depends on the transmission rate (see Table 5-4).

Table 5-4 Permissible Cable Lengths in a PROFIBUS subnet Depending on the Transmission Rate

Transmission rate	Maximum Cable Length of a Segment (in mm)
9.6 to 187.5 kbps	1000
500 kbps	400
1.5 Mbps	200
3 to 12 Mbps	100

* With a non-isolated interface

Longer Cable Lengths

If you want to implement cable lengths above those permitted in a segment, you must use RS 485 repeaters. The maximum cable length possible between two RS 485 repeaters corresponds to the cable length of a segment (see Table 5-4). Please note that these maximum cable lengths only apply if **no** other node is installed between the two RS 485 repeaters. You can connect up to 9 RS 485 repeaters in series.

When counting the total number of all nodes to be connected, you must observe, that an RS 485 repeater counts as a node of the MPI subnet, even if it is not assigned an MPI/PROFIBUS address.

Figure 5-7 shows how you can increase the maximum cable length for an MPI subnet by means of RS 485 repeaters.

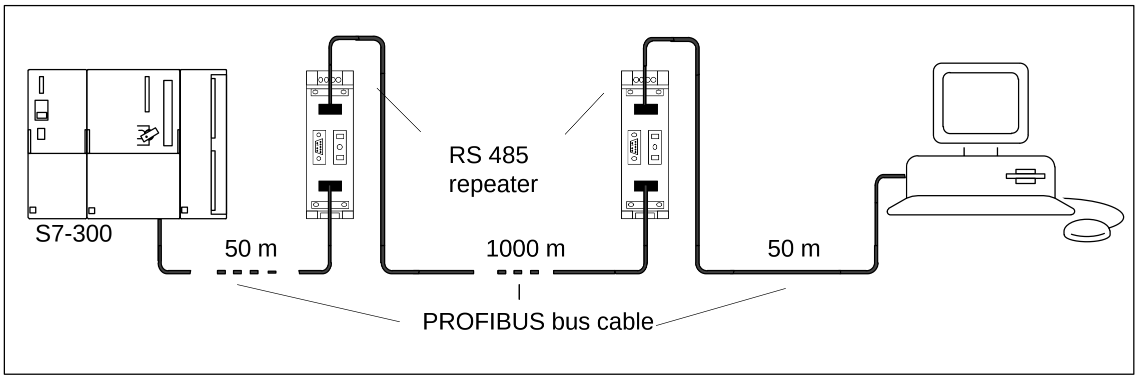


Figure 5-7 Maximum Cable Length Between Two RS 485 Repeaters

Length of the Spur Lines

If you do not attach the bus cable directly to the bus connector (for example when using a L2 bus terminal), you must take into account the maximum possible length of the spur line!

The following table lists the maximum permissible lengths of spur lines per segment:

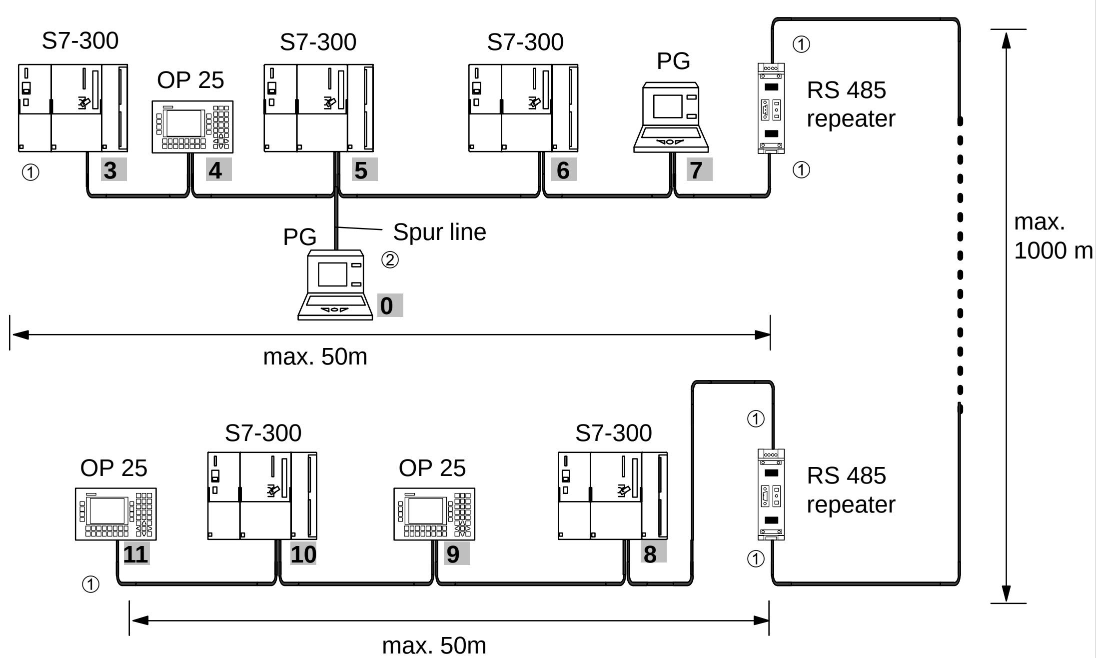
As of 3 Mbps, use the programming device connecting cable with the order no. 6ES7 901-4BD00-0XA0 to connect the programming device or PC. Other types of spur lines must not be used.

Table 5-5 Lengths of Spur Lines per Segment

Transmission Rate	Max. Length of Spur Line per Segment	Number of Nodes with Spur Line Length of ...	
		1.5 m or 1.6 m	3 m
9.6 to 93.75 kbps	96 m	32	32
187.5 kbps	75 m	32	25
500 kbps	30 m	20	10
1.5 Mbps	10 m	6	3
3 to 12 Mbps	–	–	–

Example

Figure 5-8 shows you a possible configuration of an MPI subnet. This example illustrates the maximum possible distances in an MPI subnet.



① Terminating resistor on

② Programming device connected for maintenance purposes via spur line

0 ... x MPI addresses of the nodes

Figure 5-8 Cable Lengths in an MPI Subnet

5.2 Network Components

Purpose

Table 5-6 Network Components

Purpose	Components	Description
... to configure a network	PROFIBUS bus cable	Section 5.2.1
... to connect a node to the network	Bus connector	Section 5.2.2
... to amplify the signal ... to connect segments	RS 485 repeater	Section 5.2.4 and Reference Manual *Module Specifications*
... to convert the signal for a fiber-optic network (for PROFIBUS-DP network only)	Optical Link Module	In the manual *SIMATIC NET PROFIBUS Networks*
... to connect programming devices/OPs to the network	Programming device connecting cables (spur line)	Section 5.1.3

In This Section

This section describes the properties of the network components and information for their installation and handling. You will find the technical specifications of the RS 485 repeater in the Reference Manual *Module Specifications*.

5.2.1 PROFIBUS Bus Cable

PROFIBUS Bus Cable

We can provide you with the following PROFIBUS bus cables:

PROFIBUS bus cable	6XV1 830-0AH10
PROFIBUS underground cable	6XV1 830-3AH10
PROFIBUS drum cable	6XV1 830-3BH10
PROFIBUS bus cable with PE sheath (for food and beverages industry)	6XV1 830-0BH10
PROFIBUS bus cable for festooning	6XV1 830-3CH10

Properties of the PROFIBUS Bus Cable

The PROFIBUS bus cable is a shielded twisted-pair cable with the following properties:

Table 5-7 Properties of the PROFIBUS Bus Cable

Properties	Values
Line impedance	Approx. 135 to 160 Ω (f = 3 to 20 MHz)
Loop resistance	≦ 115 Ω/km
Effective capacitance	30 nF/km
Attenuation	0.9 dB/100 m (f = 200 kHz)
Permissible cross-sectional core area	0.3 mm^2 to 0.5 mm^2
Permissible cable diameter	8 mm ± 0.5 mm

Rules for Laying

When laying the PROFIBUS bus cable, you should take care not to:

- Twist the cable
- Stretch the cable
- Compress the cable

You should also observe the following when laying the indoor bus cable (d_A = outer diameter of the cable):

Table 5-8 Specifications for Installation of Indoor Bus Cable

Properties	Specifications
Bending radius (one-off)	$\geq$ 80 mm ($10 \times d_A$)
Bending radius (multiple times)	$\geq$ 160 mm ($20 \times d_A$)
Permissible temperature range during installation	– 5 °C to + 50 °C
Storage and stationary operating temperature range	– 30 °C to + 65 °C

5.2.2 Bus Connectors

Purpose of the Bus Connector

The bus connector is used to connect the PROFIBUS cable to the MPI or PROFIBUS-DP interface. You thus make the connections to further nodes.

The following bus connectors are available:

- Up to 12 Mbps
  - Without programming device socket (6ES7 972-0BA10-0XA0)
  - With programming device socket (6ES7 972-0BB10-0XA0)
- Up to 12 Mbps, angular outgoing cable
  - Without programming device socket (6ES7 972-0BA40-0XA0)
  - With programming device socket (6ES7 972-0BB40-0XA0)

No Application

You do **not** require the bus connector for:

- DP slaves in degree of protection IP 65 (e.g. ET 200C)
- RS 485 repeaters

5.2.3 Plugging the Bus Connector into a Module

Connecting the Bus Connector

Proceed as follows to connect the bus connector:

1. Plug the bus connector into the module.
2. Screw the bus connector tight on the module.
3. If the bus connector is installed at the start or end of a segment, you must switch on the terminating resistor (switch setting “ON”) (see Figure 5-9).

Note

The bus connector 6ES7 972-0BA30-0XA0 does not have a terminating resistor. You cannot connect it at the beginning or end of a segment.

Please make sure that power is always supplied to the stations where the terminating resistor is fitted during start-up and normal operation.

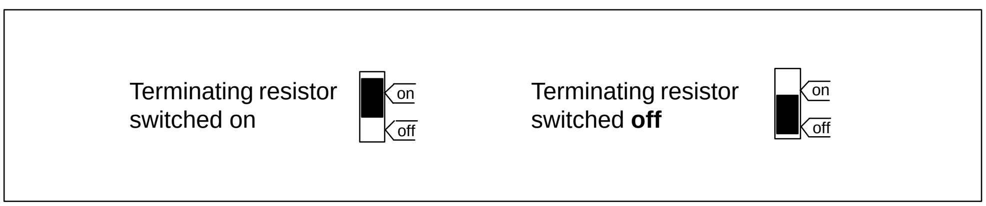


Figure 5-9 Bus Connector (6ES7 ...): Terminating Resistor Switched On and Off

Disconnecting the Bus Connector

With a **looped-through network cable**, you can unplug the bus connector from the PROFIBUS-DP interface at any time, without interrupting data communication on the network.

Warning

A data communication error may occur on the network.

A network segment must always be terminated at both ends with the terminating resistor. This is not the case, for example, if the power supply is not activated on the last slave with a bus connector. Since the bus connector draws power from the station, the terminating resistor has no effect.

Please make sure that power is always supplied to stations on which the terminating resistor is active.

5.2.4 RS 485 Repeater

The Purpose of the RS 485 Repeater

The RS 485 repeater amplifies data signals on bus lines and interconnects network segments.

You need an RS 485 repeater if:

- more than 32 nodes are connected to the network
- a grounded segment is to be connected to a non-grounded segment, or
- the maximum cable length of a segment is exceeded.

Description of the RS 485 Repeater

You will find a description and the technical specifications of the RS 485 repeater in Chapter 7 of the *Module Specifications* Reference Manual.

Installation

You can mount the RS 485 repeater either on the S7-300 rail or on a 35-mm standard rail.

To mount it on the S7-300 rail, remove the slide at the rear of the RS 485 repeater as follows:

1. Insert a screwdriver under the edge of the latching element.
2. Move the screwdriver towards the rear of the module. Keep this position.
3. Move the slide upwards.

Figure 5-10 shows how the slide of the RS 485 repeater is removed.

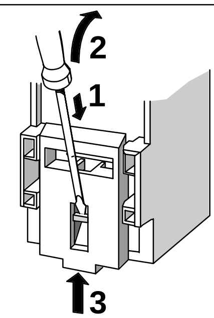


Figure 5-10 Removing the Slide on the RS 485 Repeater

After you have removed the slide, you can install the RS 485 repeater on the rail in the same way as the other S7-300 modules (see Chapter 2).

Use flexible cables with a cross-sectional core area of 0.25 mm^2 to 2.5 mm^2 (AWG 26 to 14) to connect the 24V DC power supply.

Wiring the Power Supply Module

Proceed as follows to wire the power supply of the RS 485 repeater:

1. Loosen the screws “M” and “PE”.
2. Strip the insulation off the 24V DC power supply cable.
3. Connect the cable to terminals “L+” and “M” or “PE”.

Terminal “M5.2”

Terminal “M5.2” is a terminal that you do not need to wire, as it is only used for servicing. The terminal “M5.2” supplies the reference potential. You need this reference potential to measure the voltage characteristic between terminals “A1” and “B1”.

Connecting the PROFIBUS Bus Cable

You must connect the PROFIBUS bus cable to the RS 485 repeater as follows:

1. Cut the PROFIBUS bus cable to the length you require.
2. Strip the insulation off the PROFIBUS bus cable as shown in Figure 5-11.

   The shield braiding must be turned up onto the cable. Only thus, the shielding point can later act as a strain relief and a shield support element.

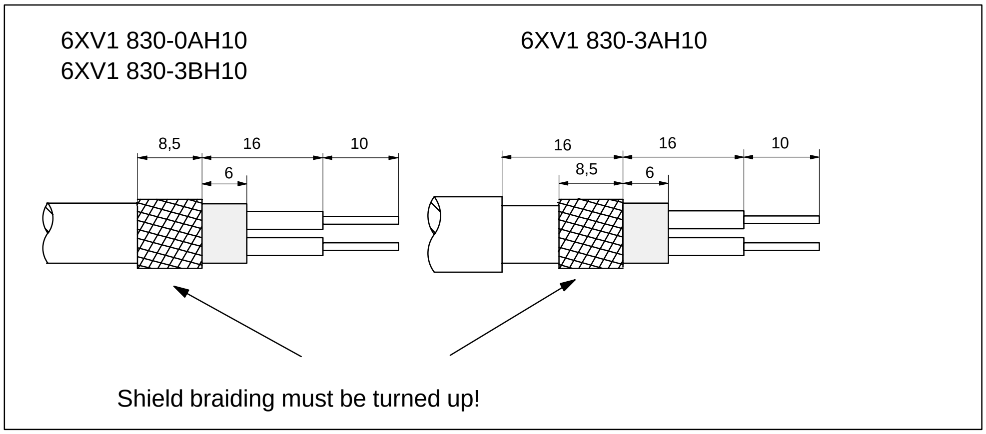


Figure 5-11 Lengths of the Stripped Insulation for Connection to the RS 485 Repeater

3. Connect the PROFIBUS bus cable to the RS 485 repeater:

   Connect similar cores (green/red for PROFIBUS bus cable) to similar terminals A or B (for example, always connect a green wire to terminal A and a red wire to terminal B).
4. Tighten the pressure saddles, so that the shielding is bare under the pressure saddle.

Commissioning 6

Software Prerequisites

You must be familiar with ***STEP 7*** **as of V 5.x** to be able to use the complete range of functions of the CPUs listed in the chapter entitled *Important Information*.

If you have installed ***STEP 7*** **< V 5.x** and you want to configure your system with these CPUs, you have the following alternatives:

- If you don't upgrade *STEP 7* < V 5.x, you can use the relevant CPUs with low order numbers from the *STEP 7* hardware catalogue.

  Note that you can only use the functions of the previous CPU and of *STEP 7* for the new CPU.

  Important: The CPUs 316-2 DP and 318-2 are not in the *STEP 7* < V 5.x hardware catalogue.
- Upgrade *STEP 7*. Get information on update options from the Internet at our Customer Support site or ask your Siemens customer advisor.
- Install the new version of *STEP 7*.

Prerequisites for Commissioning

Prerequisite	See...
The S7-300 must be installed	Chapter 2
The S7-300 must be wired	Chapter 4
In the case of a networked S7-300: • MPI/PROFIBUS addresses must be set • Terminating resistors must be switched on (at the segment borders)	Chapter 5

In This Chapter

6.1 Inserting and Changing the Memory Card (Not CPU 312 IFM/314 IFM)

Exception

You cannot insert a memory card with the CPU 312 IFM and 314 IFM.

Inserting/Changing a Memory Card

1. Set the CPU to STOP mode.

Note

If you insert the memory card in a CPU mode other than STOP, the CPU will go into STOP mode and the STOP LED will flash at 1 second intervals to request a reset (see Section 6.5).

---

2. Is a memory card already inserted? If so: remove it.
3. Insert the new memory card in the CPU module shaft. Please note that the insertion marking on the memory card points to the marking on the CPU (see Figure 6-1).
4. Reset the CPU (see Section 6.5).

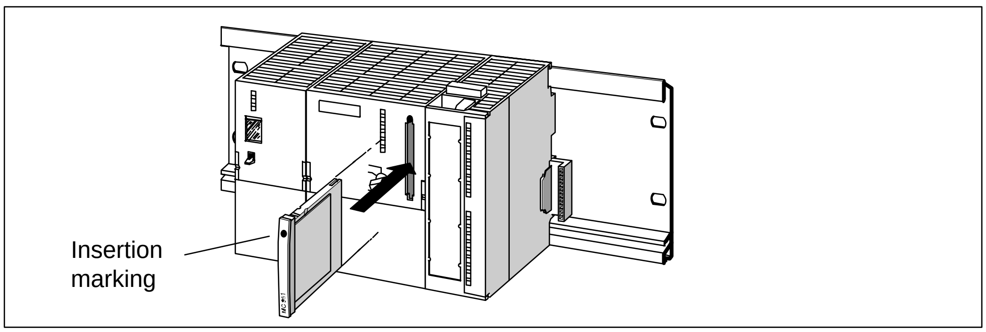


Figure 6-1 Inserting the Memory Card in the CPU

6.2 Inserting the Backup Battery/Accumulator (Not CPU 312 IFM)

Exceptions

A **CPU 312 IFM** doesn't have a backup battery or accumulator.

Since the **CPU 313** doesn't have a real-time clock, you don't need an accumulator for backup purposes (see Section 8.1.3).

Inserting the Backup Battery/Accumulator

You insert a backup battery or the accumulator in the CPU as follows:

Note

Only insert the backup battery in the CPU at power on.

If you insert the backup battery before power on, the CPU requests a reset.

---

1. Open the front door of the CPU.
2. Plug the battery or accumulator connector into the corresponding socket in the battery compartment of the CPU. The notch on the connector must point to the left.
3. Place the backup battery/accumulator into the battery compartment on the CPU.
4. Close the front door of the CPU.

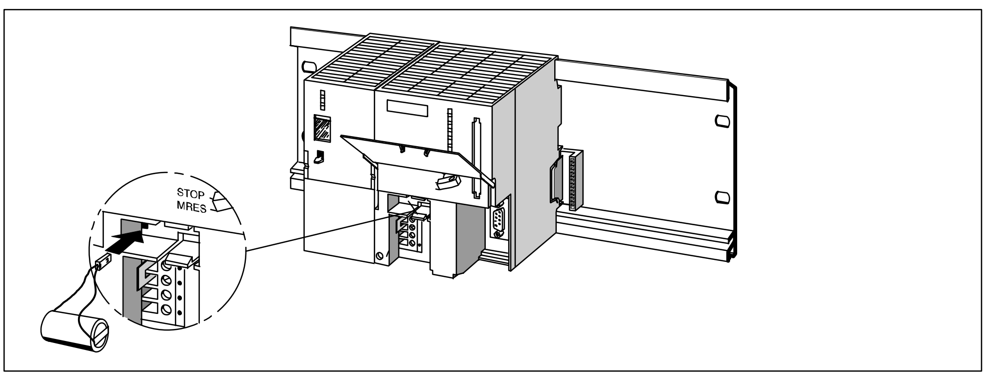


Figure 6-2 Inserting a Backup Battery in the CPUs 313/314

6.3 Connecting a Programming Device

Prerequisites

The programming device must be equipped with an integrated MPI interface or an MPI card in order to connect it to an MPI.

Cable length

For information on possible cable lengths, refer to Section 5.1.3.

6.3.1 Connecting a Programming Device to an S7-300

You can connect the programming device to the MPI of the CPU via a preprepared programming device cable.

Alternatively, you can prepare the connecting cable yourself using the PROFIBUS bus cable and bus connectors (see Section 5.2.2).

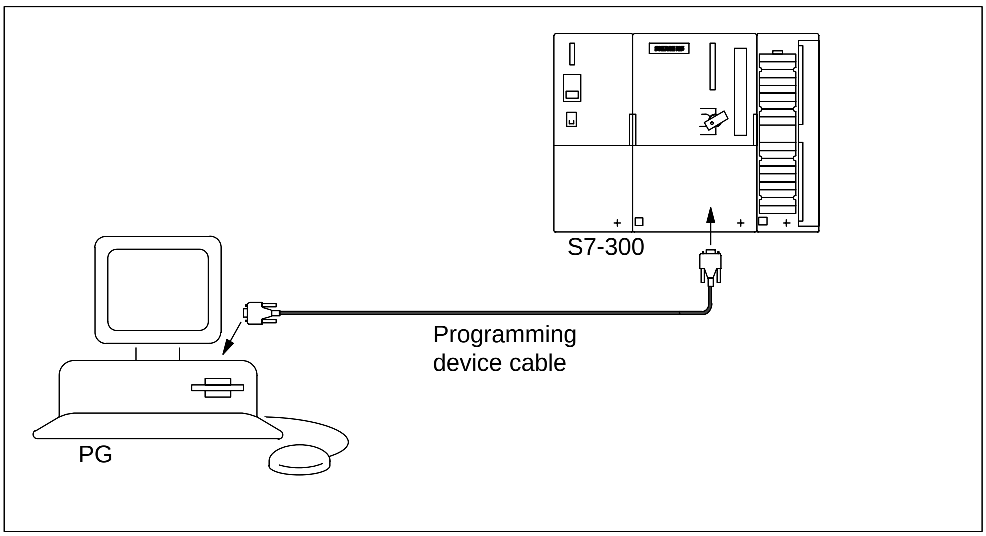


Figure 6-3 Connecting a Programming Device to an S7-300

6.3.2 Connecting the Programming Device to Several Nodes

Two Configuration Options

When connecting a programming device to several nodes, you must differentiate between two types of configuration:

- Programming device permanently installed in the MPI subnet
- Programming device connected for startup or maintenance purposes.

Depending on which of these configurations you choose, connect the programming device to the other nodes as follows (see also Section 5.1.2).

Type of Configuration	Connection
Programming device permanently installed in the MPI subnet	Integrated directly in the MPI subnet
Programming device installed for commissioning or maintenance	Programming device connected to a node via a spur line

Permanently Installed Programming Device

You connect the programming device that is permanently installed in the MPI subnet directly to the other nodes in the MPI subnet via bus connectors in accordance with the rules described in Section 5.1.2).

Figure 6-4 shows two networked S7-300s. The two S7-300s are interconnected via bus connectors.

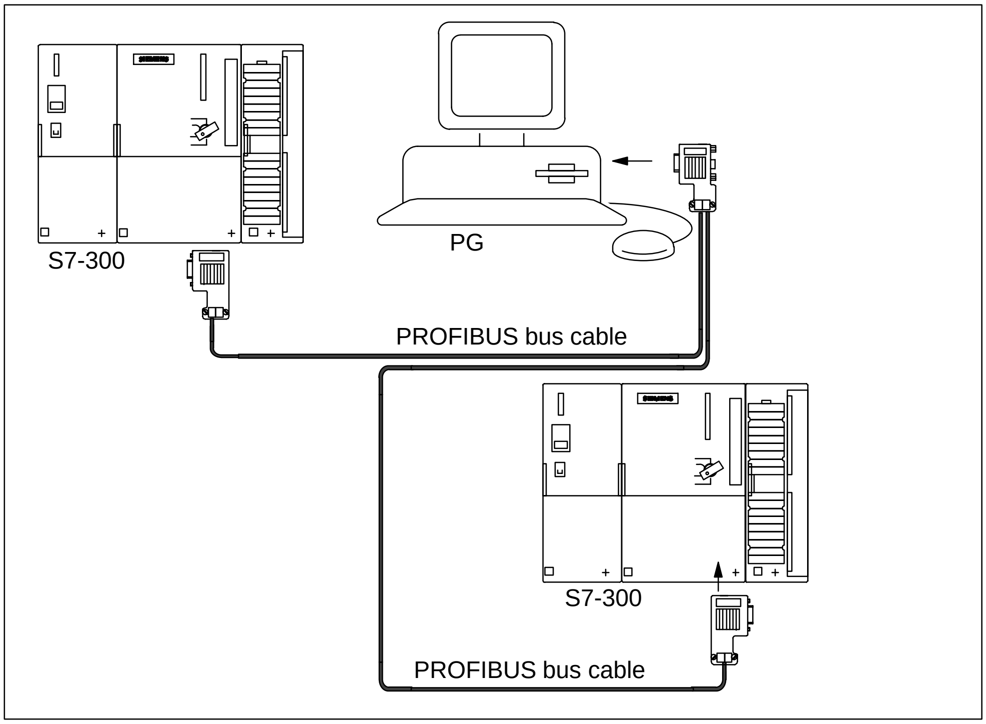


Figure 6-4 Connecting a Programming Device to Several S7-300s

Connecting the Programming Device for Service Purposes: Recommendation for MPI Addresses

If there is no stationary programming device, we recommend the following:

In order to connect a programming device for service purposes to an MPI subnet with “unknown” nodes addresses, we recommend to set the following address on the service programming device:

- MPI address: 0
- Highest MPI address: 126.

Afterwards, use *STEP 7* to determine the highest MPI address in the MPI subnet and adjust the highest MPI address in the programming device to that of the MPI subnet.

Programming Device During Commissioning or Maintenance

For commissioning or maintenance purposes, you connect the programming device via a spur line to a node of the MPI subnet. The bus connector of this node must therefore be provided with a programming device socket (see also Section 5.2.2).

Figure 6-5 shows two S7-300s to which a programming device is connected.

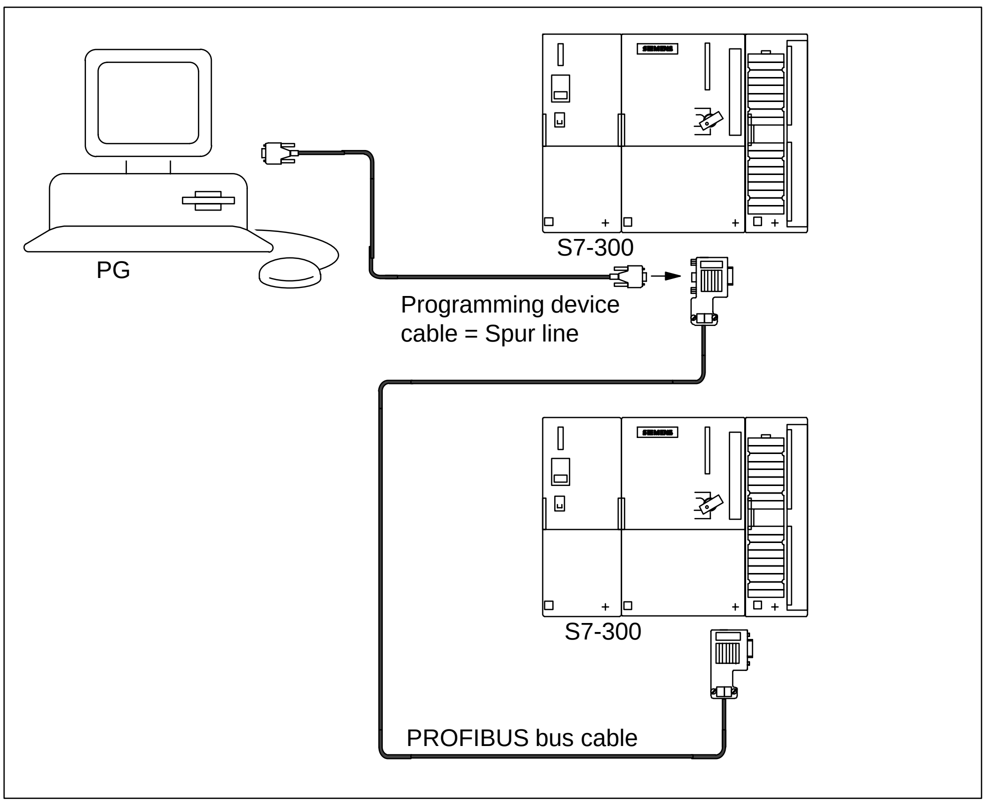


Figure 6-5 Connecting a Programming Device to a Subnet

6.3.3 Connecting a Programming Device to Ungrounded Nodes of an MPI Subnet

Connecting a Programming Device to Ungrounded Nodes

If you have an ungrounded configuration of nodes in an MPI subnet or an ungrounded S7-300 (see Section 4.1.4), you may only connect an ungrounded programming device to the MPI subnet or the S7-300.

Connecting a Grounded Programming Device to the MPI

You want to operate the nodes in an ungrounded configuration (see Section 4.1.4). If the MPI at the programming device is grounded, you must connect an RS 485 repeater between the nodes and the programming device. You must connect the ungrounded nodes to bus segment 2, if you connect the programming device to bus segment 1 (terminals A1 B1) or the PG/OP interface (see Chapter 7 in the *Module Specifications*, Reference Manual).

Figure 6-6 shows the RS 485 repeater as an interface between a grounded and an ungrounded node in the MPI subnet.

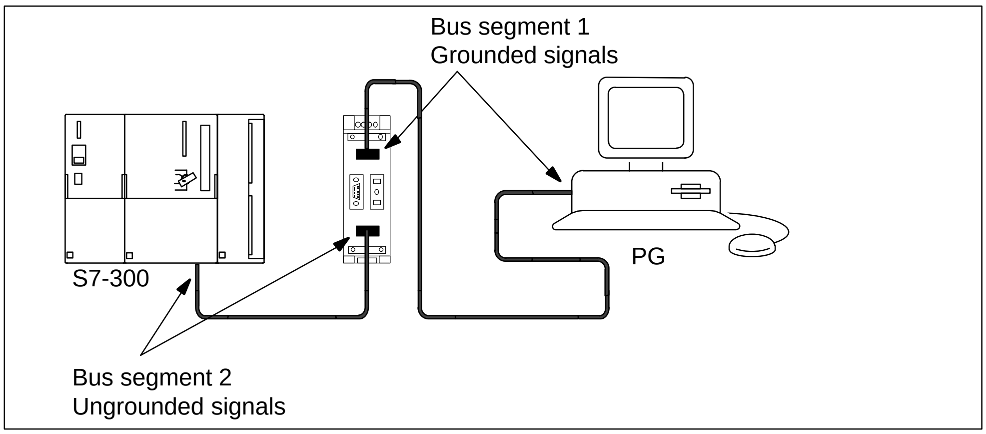


Figure 6-6 Programming Device Connected to an Ungrounded S7-300

6.4 Switching On a S7-300 for the First Time

Prerequisites

The S7-300 is installed and wired.

The mode selector should be in STOP mode.

Switching On for the First Time.

Switch the PS 307 power supply module on.

Result:

- The 24V DC LED on the power supply module comes on.
- On the CPU
  - The 5V DC LED comes on.
  - The STOP LED flashes at one second intervals while the CPU carries out an automatic reset.
  - The STOP LED comes on after the memory reset.

If there is no backup battery in the CPU, the BATF LED comes on.

Note

If you insert a memory card and a backup battery before power on, the CPU also requests a memory reset after start-up.

6.5 Resetting the CPU

When Do You Reset the CPU Memory?

You must reset the CPU memory:

- Before you transfer a new (complete) user program to the CPU
- If the CPU requests a MRES with its STOP LED flashing at 1-second intervals Possible reasons for this request are listed in Table 6-1.

Table 6-1 Possible Reasons for MRES Request by CPU

Reasons for MRES Request by CPU	Remarks
Wrong memory card has been plugged in.	**not** with **CPU 312 IFM/314 IFM**
RAM error in CPU	–
Working memory too small, that is not all blocks of the user program on a memory card could be loaded.	CPU with 5V-FEPROM memory card inserted: In these circumstances the CPU requests a one-off memory reset. After that, the CPU ignores the contents of the memory card, enters the error reasons in the diagnostics buffer and goes to STOP. You can erase the contents of the 5V-FEPROM memory card in the CPU or enter new program.
Attempt to load blocks with errors, for example if a wrong command has been programmed.	

How to Reset the Memory

There are two ways of resetting the CPU memory:

Memory Reset with the Mode Selector	Memory Reset with Programming Device
... is described in this section.	... is only possible in STOP mode of the CPU (see *STEP 7*-Online help).

Cold start in the CPU 318-2

In the CPU 318-2 you can also carry out a cold start instead of resetting the memory.

Cold start means:

- The data blocks in the working memory created by SFC 22 are deleted. The remaining data blocks have the preassigned value from the load memory.
- The process image as well as all times, counters and memory markers are reset – irrespective of whether they were parameterized as retentive.
- The OB 102 is processed.
- Before the first command in OB 1, the process image of the inputs is read.

Resetting the CPU Memory or Carrying Out a Cold Start (CPU 318-2 only) with the Mode Selector

Step	Resetting the CPU Memory (Figure 6-7)	Carrying Out a Cold Start (Figure 6-8) CPU 318-2 Only
1	Turn the key to the STOP position	
2	Turn the key to the MRES position Hold the key in this position until the STOP LED comes on for the second time and remains on (this takes 3 seconds).	
3	Within 3 seconds you must turn the switch back to the MRES position and keep holding it until the STOP LED flashes (at 2 Hz). When the CPU has completed the reset, the STOP LED stops flashing and remains lit. The CPU has reset the memory.	Within 3 seconds you must turn the switch to the RUN position. During start-up the RUN LED flashes at 2 Hz.

Memory Reset

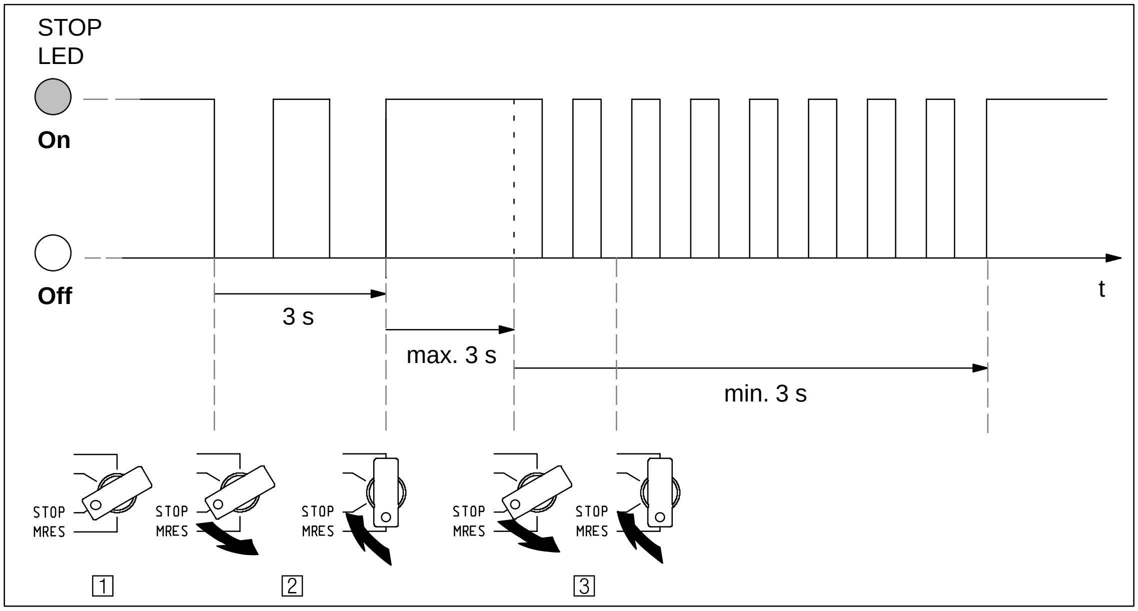


Figure 6-7 Switching Sequence for the Mode Selector for Resetting the CPU

Is the STOP LED Not Flashing During Memory Reset?

If the STOP LED doesn’t flash during memory reset or other LEDs come on (with the exception of the BATF LED), you must repeat steps 2 and 3. If the CPU does not perform the reset this time, evaluate the diagnostic buffer of the CPU.

Cold Start

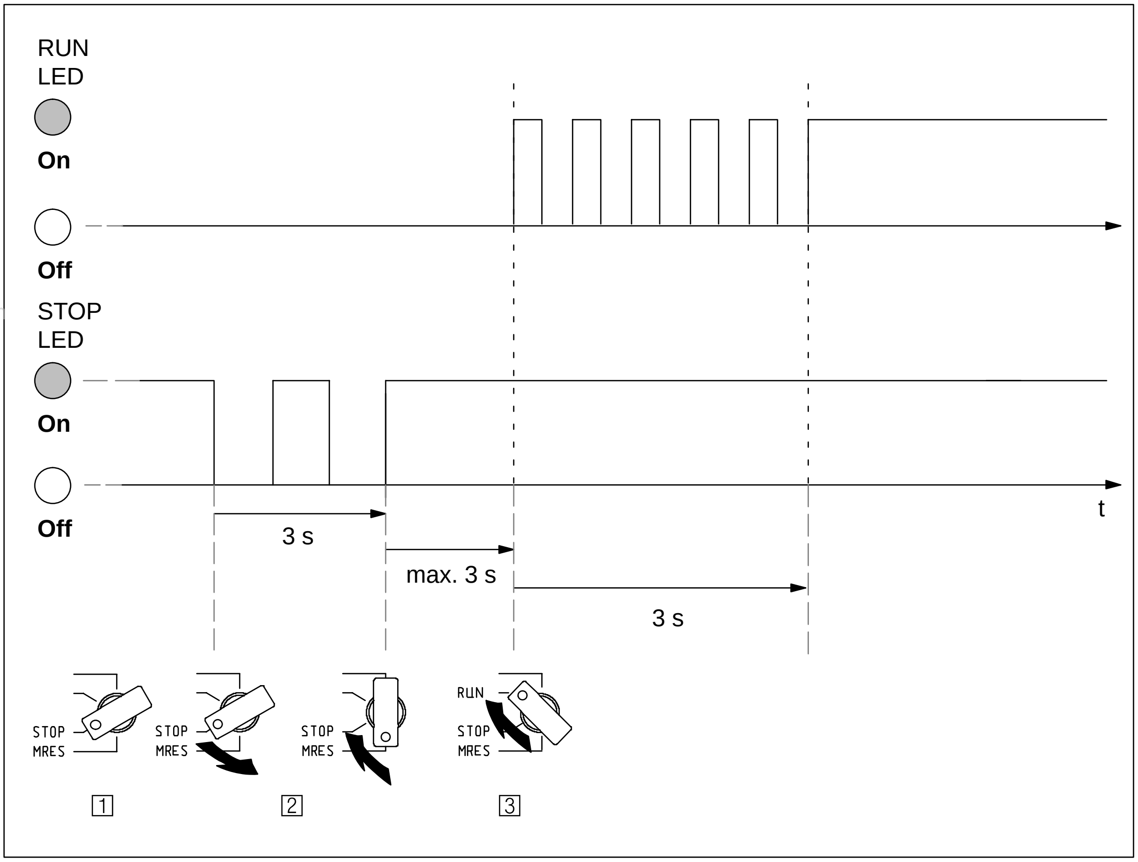


Figure 6-8 Switching Sequence for the Mode Selector for Cold Start (CPU 318-2 Only)

What Happens in the CPU During Memory Reset?

Table 6-2 Internal CPU Events on Memory Reset

<table>
<tr><th>Event</th><th>CPU 313/314/315/315-2 DP/
316-2 DP/318-2</th><th>CPU 312 IFM/314 IFM</th></tr>
<tr><td rowspan="4">CPU activities</td><td colspan="2">1. The CPU deletes the entire user program in its RAM and in the load memory (not the EPROM load memory).</td></tr>
<tr><td colspan="2">2. The CPU deletes the backup memory.</td></tr>
<tr><td colspan="2">3. The CPU tests its own hardware.</td></tr>
<tr><td>4. If you have inserted a memory card, the CPU copies the relevant contents of the memory card into the working memory.
Tip: If the CPU cannot copy the contents of the memory card and requests memory reset:
– Remove the memory card.
– Reset the CPU memory.
– Read the diagnostic buffer.</td><td>The CPU copies the relevant contents of the EPROM memory into the working memory</td></tr>
<tr><td>Memory contents after reset</td><td>The CPU memory is initialized to “0”. If there is a memory card plugged in, the user program is loaded back into the RAM.</td><td>The user program is loaded back into the RAM from the integrated retentive EPROM of the CPU.</td></tr>
<tr><td rowspan="3">What’s left?</td><td colspan="2">The contents of the diagnostics buffer.
You can read the diagnostic buffer with the programming device (see the STEP 7 online help system).</td></tr>
<tr><td colspan="2">The parameters of the MPI (MPI address and highest MPI address, transmission rate, configured MPI addresses of CPs/FMs in an S7-300).</td></tr>
<tr><td colspan="2">The contents of the operating hours counter (not for CPU 312 IFM).</td></tr>
</table>

Note: MPI Parameters

The following applies for the validity of the MPI parameters at memory reset:

Memory Reset ...	MPI Parameters ...
With memory card inserted (CPU 313/314/315/31x-2 DP)	... located on the memory card or on the EPROM of the CPU are valid.
In the case of an integral EPROM (CPU 312 IFM/314 IFM)	
Without memory card inserted (CPU 313/314/315/31x-2 DP)	... are retained and are valid.

6.6 Commissioning the PROFIBUS-DP

In This Section

This section provides you with vital information on commissioning a PROFIBUS subnet with a CPU 31x-2 DP.

Software Prerequisites

CPU 315-2 DP	As of *STEP 7* V 3.1 As of *COM PROFIBUS* V 3.0
CPU 316-2 DP:	As of *STEP 7* V 5.x As of *COM PROFIBUS* V 5.0
CPU 318-2	

6.6.1 Commissioning the CPU 31x-2 DP as a DP Master

Prerequisites for Commissioning

- The PROFIBUS subnet must be configured.
- The DP slaves must be prepared for operation (see relevant DP slave manual).

Commissioning

To commission the CPU 31x-2 DP as a DP master in a PROFIBUS subnet, proceed as follows:

1. Load the PROFIBUS subnet configuration (preset configuration) created using *STEP 7* with the programming device in the CPU 31x-2 DP.
2. Switch on all of the DP slaves.
3. Switch the CPU 31x-2 DP from STOP mode to RUN mode.

Start-Up of the CPU 31x-2 DP as a DP Master

When the CPU 31x-2 DP is powered up, it checks the preset configuration of your DP master system against the actual configuration.
Tip: You can set a check time for the test in *STEP 7*.

If the preset configuration matches the actual configuration, the CPU switches to RUN.

If the preset configuration does not match the actual configuration, the response of the CPU depends on the setting of the parameter “Startup if preset configuration not equal to actual configuration”:

Startup If Preset Configuration Not Equal to Actual Configuration = Yes (Default Setting)	Startup If Preset Configuration Not Equal to Actual Configuration = No
The CPU 31x-2 DP switches to RUN mode (BUSF LED flashes if any of the DP slaves cannot be addressed)	The CPU 31x-2 DP remains in STOP mode and the BUSF LED flashes after the time set parameter transfer to modules has elapsed. The flashing BUSF LED indicates that at least one DP slave is not addressable. In this case, you should check that all DP slaves are switched on, or you should read out the diagnostic buffer (see *STEP 7* User Manual).

Recognizing the Operational States of the DP Slave

In Chapter 9 you will find the dependencies of the operating modes of the CPU 31x-2 DP as a DP master and of a DP slave.

Tip: When starting up the CPU as a DP master, always program OBs 82 and 86. This allows you to identify and evaluate faults and interruptions in data transfer (for CPUs configured as DP slaves see also Table 9-3 on page 9-9).

6.6.2 Commissioning the CPU 31x-2 DP as a DP Slave

Prerequisites for Commissioning

- The CPU 31x-2 DP must be parameterized and configured as a DP slave (see Chapter 9).

  When configuring it as a DP slave, you must already have decided on the following:

  – Should functions such as programming and status/control be available via the DP interface?

  – Is the DP master an S7 DP master or another DP master?

- All other DP slaves are parameterized and configured.
- The DP master is parameterized and configured.

  Note that the CPU 31x-2 DP as DP slave provides address areas of an immediate memory for data interchange with the DP master. You use *STEP 7* to configure these address areas when configuring the CPU as a DP slave (see Chapter 9).

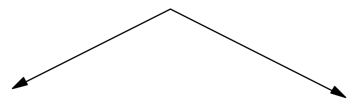
Commissioning

To commission the CPU 31x-2 DP as a DP slave in the PROFIBUS subnet, proceed as follows:

1. Switch the CPU 31x-2 DP from STOP mode to RUN.
2. Switch on all of the DP slaves.
3. Switch on the DP master.

The CPU 31x-2 DP as a DP Slave at Start-Up

When the CPU 31x-2 DP is switched to RUN, two operating mode transitions take place independently of each other:



The **CPU** switches from STOP mode to RUN.

At the **PROFIBUS-DP interface** the CPU starts data transfer with the DP master.

Recognizing the Operational Modes of the DP Master

In Chapter 9 you will find the dependencies of the operating modes of the CPU 31x-2 DP as a DP slave or as a DP master.

Tip: When commissioning the CPU as a DP slave, always program OBs 82 and 86. This allows you to identify and evaluate operating modes and interruptions in data transfer (see Table 9-8 on page 9-20).

Maintenance

7

Maintenance = Replacement

The S7-300 is a **maintenance-free** programmable controller.

Maintenance involves replacing the following parts:

- Backup battery/accumulator
- Modules
- Fuses on the digital output modules

In This Section

7.1 Changing the Backup/Accumulator (Not CPU 312 IFM)

Replacing the Backup Battery/Accumulator

You should only change the backup battery or accumulator when the power is on, in order to prevent the loss of data from the internal user memory, and to keep the clock of the CPU running.

Note

The data in the internal user memory are lost if you change the backup battery when the power is off.

Change the backup battery with the power switch in the ON position only!

To change the backup battery/accumulator proceed as follows:

Step	CPU 313/314	CPU 314 IFM/315/315-2 DP/ 316-2 DP/318-2
1.	Open the front door of the CPU.	
2.	Pull the backup battery/accumulator out of the compartment with a screwdriver.	Pull the backup battery or accumulator out of the compartment by the cable
3.	Plug the connector of the new backup battery/accumulator into the corresponding socket in the battery compartment of the CPU. The notch on the battery connector must point to the left!	
4.	Place the backup battery/accumulator into the battery compartment on the CPU.	
5.	Close the front door of the CPU	

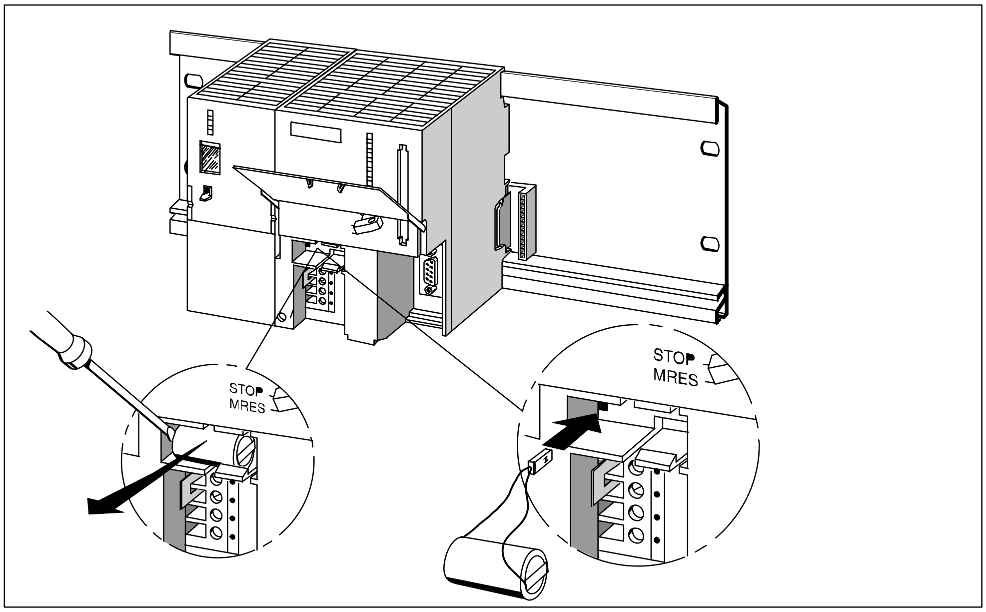


Figure 7-1 Changing the Backup Battery in the CPU 313/314

How Often Is Replacement Necessary?

Backup battery: We recommend changing the backup battery every year.

Accumulator: The accumulator never needs changing.

Disposal

Backup batteries must be disposed of in keeping with the relevant national environment protection regulations/guidelines.

Storing Backup Batteries

Store backup batteries in a dry and cool place.

Backup batteries can be stored for five years.

Warning

If backup batteries are not treated properly, they can ignite, explode and cause severe burning.

Store backup batteries in a dry and cool place.

Rules for the Handling of Backup Batteries

To reduce the risk of danger when handling backup batteries, you must observe the following rules:

Warning

Improper handling of backup batteries can cause injuries and property damage.

Backup batteries that are not handled properly can explode and cause severe burns.

Do not

- recharge
- overheat
- burn
- puncture
- crush
- short-circuit backup batteries!

Rules for Handling the Accumulator

You must not charge the accumulator when not inserted in the CPU! The accumulator can only be charged by the CPU when the power is on.

7.2 Replacing Modules

Rules for Installation and Wiring

The following table tells you what you have to do when wiring, detaching and installing the S7-300 modules.

Rules Governing	... Power Supply	... CPU	... SM/FM/CP
Blade width of screwdriver	3.5 mm (cylindrical model)		
Tightening torque			
Attaching modules to the rail	0.8 to to 1.1 Nm		0.8 to to 1.1 Nm
Terminating cables	0.5 to 0.8 Nm		–
POWER OFF when replacing the ...	Yes		No
Operating mode of S7-300 when replacing the ...	–		STOP
Load voltage OFF when replacing the ...	Yes		Yes

Initial Situation

The module you want to replace is installed and wired. You want to install a new module of the same type.

Warning

If you remove or plug in the S7-300 modules during data transmission via the MPI, the data might be corrupted by disturbing pulses.

You must not plug in or remove any S7-300 modules during data transmission via the MPI!

If you are not sure whether any communications activities are taking place, pull the connector out of the MPI port.

Removing a Module (SM/FM/CP)

Detach the module from the rail as follows:

Step	20-pin Front Connector	40-pin Front Connector
1.	Set the CPU to the STOP mode with the key-operated switch.	
2.	Switch off the load voltage to the module.	
3.	Take out the labeling strip.	
4.	Open the front door.	
5.	Unlock the front connector and pull it off the module.	
	To do this, press down on the locking button (5) and, with the other hand, grip the front connector (5a) and pull it out.	Remove the fixing screw from the middle of the front connector. Pull the front connector out while holding the grips.
6.	Undo the module fixing screw(s).	
7.	Swing the module up and off the rail.	

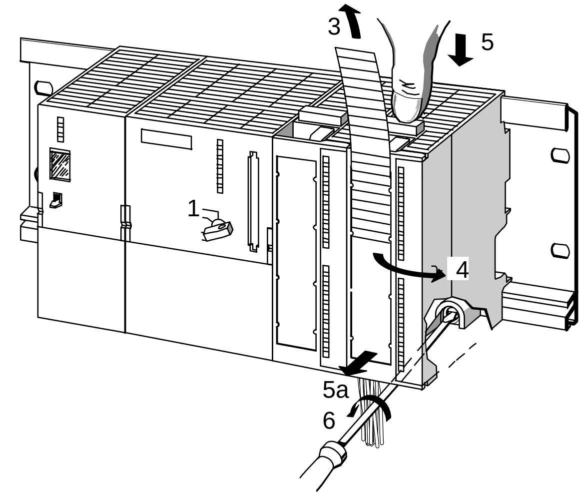


Figure 7-2 Unlocking the Front Connector and Detaching the Module from the Rail

Removing the Front Connector Coding Key from the Module

Prior to installing the new module, you must remove the front connector coding key from the new module.

Reason: This part is already in the front connector (see Figure 7-3).

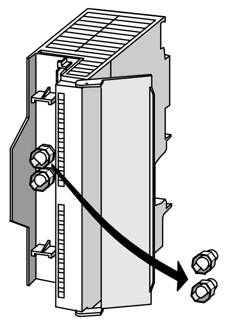


Figure 7-3 Removing the Front Connector Coding Key

Installing a New Module

Install the new module as follows:

1. Hook the new module of the same type onto the rail and swing it down into place.
2. Bolt the module tight.
3. Slip the labeling strip of the old module into its guide on the new module.

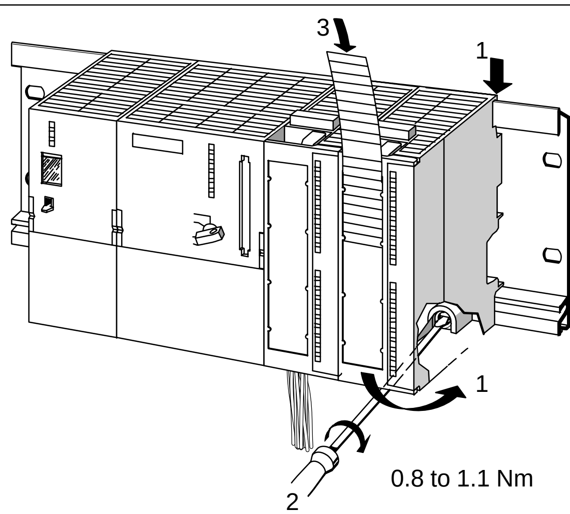


Figure 7-4 Installing a New Module

Removing the Front Connector Coding Key from the Front Connector

If you want to wire a used front connector for another module, just remove the front connector coding key from the front connector by pressing it out of the front connector with a screwdriver. This upper part of the coding key must then be plugged back into the old module.

Putting a New Module into Service

Proceed as follows to put the new module into service:

1. Open the front door.
2. Bring the front connector back into its operating position (see Section 4.3.3)

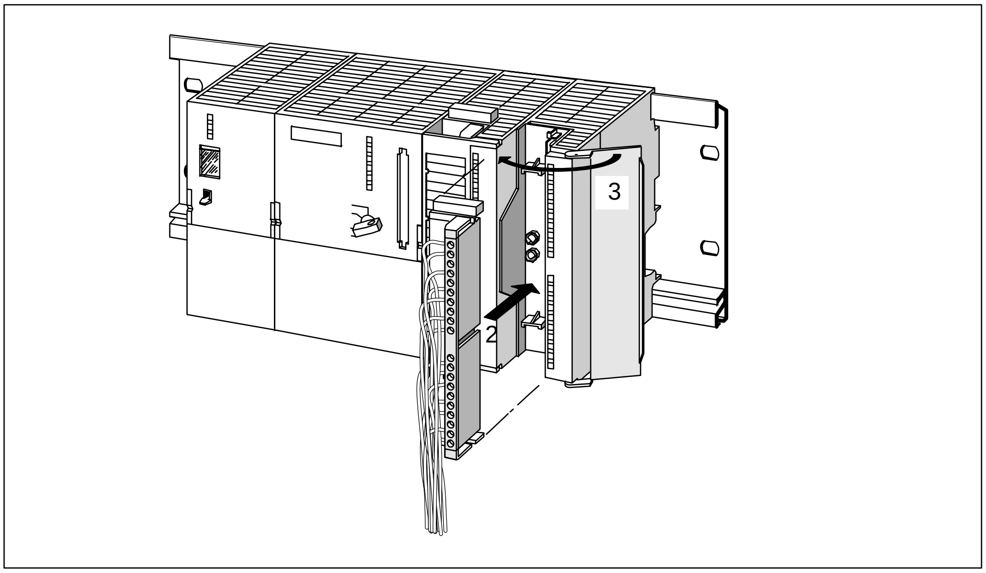


Figure 7-5 Plugging In the Front Connector

3. Close the front door.
4. Switch the load voltage back on.
5. Set the CPU again to RUN.

Performance of the S7-300 After Module Replacement

When you have replaced a module and no errors have occurred, the CPU enters the RUN mode. If the CPU stays in the STOP mode, you can have the cause of the error displayed with *STEP 7* (see *STEP 7 User Manual*).

7.3 Replacing Fuses on 120/230V AC Digital Output Modules

Fuses for Digital Outputs

Fuses are used for the individual channel groups of the digital outputs of the following digital output modules, to protect these against short circuit:

- SM 322 DO 16 × AC120V digital output module
- SM 322 DO 8 × AC120/230V digital output module

Replacement Fuses

If you have to change fuses, you can use, for example, the following replacement fuses:

- 8 A, 250 V fuse
  - Wickmann 19 194-8 A
  - Schurter SP001.013
  - Littlefuse 217.008
- Fuse holder
  - Wickmann 19 653

Position of the Fuses

The digital output modules have 1 fuse per channel group. The fuses are located at the left side of the digital output module. Figure 7-6 shows you where to find the fuses on the digital output modules.

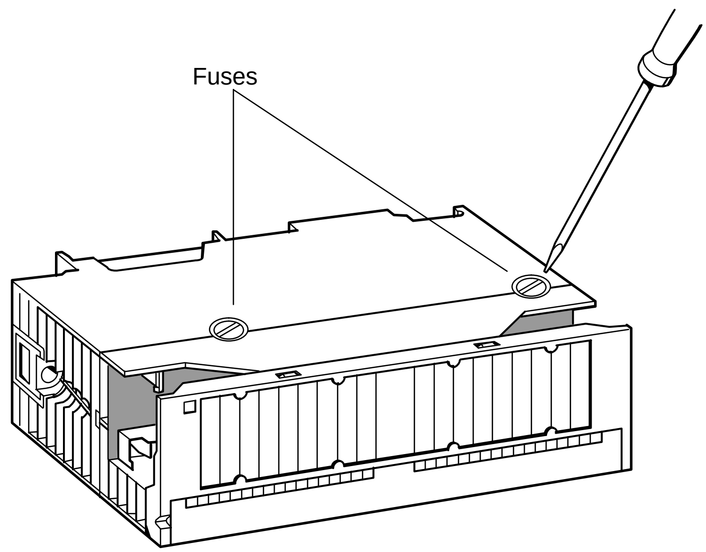


Figure 7-6 Location of the Fuses on Digital Output Modules

Changing Fuses

The fuses are located at the left side of the module. To change the fuses, proceed as follows:

1. Switch the CPU to STOP using the key switch.
2. Switch off the load voltage of the digital output module.
3. Remove the front connector from the digital output module.
4. Loosen the fixing screw of the digital output module.
5. Swing out the digital output module.
6. Remove the fuse holder from the digital output module.
7. Replace the fuse.
8. Screw the fuse holder back into the digital output module.
9. Install the digital output module (see Section 2.2.2).

CPUs 8

In This Section

8.1 Control and Display Elements

Figure 8-1 shows you the control and display elements of a CPU.
The order of the elements in some CPUs might differ from the order shown in the figure below. The individual CPUs do not always have all the elements shown here. Table 8-1 shows you the differences.

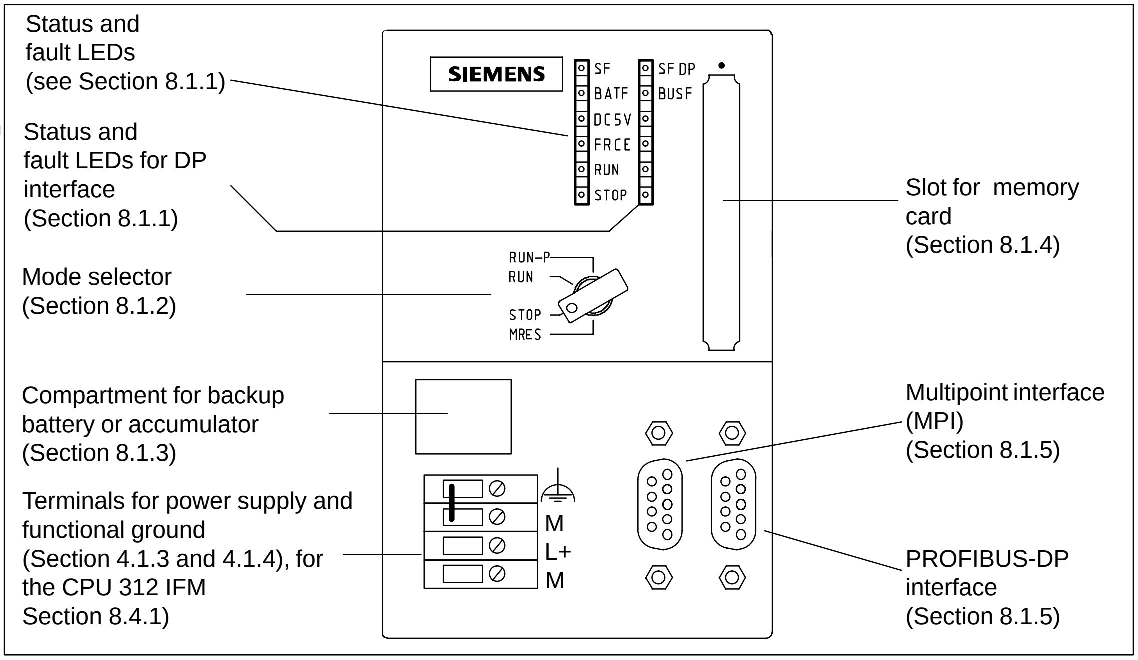


Figure 8-1 Control and Display Elements of the CPUs

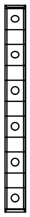
Differences Between CPUs

Table 8-1 The Differences in Control and Display Elements Between CPUs

<table>
<tr><th>Element</th><th>312 IFM</th><th>313</th><th>314</th><th>314 IFM</th><th>315</th><th>315-2 DP</th><th>316-2 DP</th><th>318-2</th></tr>
<tr><td>LEDs for DP interface</td><td colspan="5">No</td><td colspan="3">Yes</td></tr>
<tr><td>Backup battery/ accumulator</td><td>No</td><td>No accumulator</td><td colspan="6">Yes</td></tr>
<tr><td>Terminal connection for power supply</td><td>No; via front connector</td><td colspan="7">Yes</td></tr>
<tr><td>Memory card</td><td>No</td><td colspan="2">Yes</td><td>No</td><td colspan="4">Yes</td></tr>
<tr><td>PROFIBUS-DP interface</td><td colspan="5">No</td><td colspan="3">Yes</td></tr>
</table>

8.1.1 Status and Fault Displays

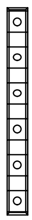
Displays for the CPU:



SF ... (red) ... hardware or software faults (see Section 8.3.2)
BATF ... (red) ... battery fault (see Section 8.3.2) (not CPU 312 IFM)
DC5V ... (green) ... 5V DC supply for CPU and S7-300 bus is ok.
FRCE ... (yellow) ... force request is active (see Section 8.3.1)
RUN ... (green) ... CPU in RUN mode; LED flashes at start-up w. 1 Hz; in HALT mode w. 0.5 Hz
STOP mode ... (yellow) ... CPU in STOP or HALT or start-up; LED flashes at memory reset request (see Section 6.5)

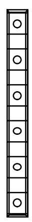
Displays for PROFIBUS: (see Chapter 9)

CPU 315-2 DP/
CPU 316-2 DP



BUSF ... (red) ... hardware or software fault at PROFIBUS interface

CPU 318-2



BUS1F ... (red) ... hardware or software fault at interface 1
BUS2F ... (red) ... hardware or software fault at interface 2

Figure 8-2 Status and Fault Displays of the CPUs

8.1.2 Mode Selector

The mode selector is the same in all CPUs.

Mode Selector Positions

The positions of the mode selector are explained in the order in which they appear on the CPU.

You will find detailed information on the modes of the CPU in the *STEP 7* online help system.

Position	Description	Description
RUN-P	RUN PROGRAM mode	The CPU scans the user program. The key cannot be taken out in this position.
RUN mode	RUN mode	The CPU scans the user program. The user program cannot be changed without password confirmation. The key can be removed in this position to prevent anyone changing the operating mode.
STOP mode	STOP mode	The CPU does not scan user programs. The key can be removed in this position to prevent anyone changing the operating mode.
MRES mode	Memory reset	Momentary-contact position of the mode selector for CPU memory reset (or a cold start as well in the case of the 318-2). Resetting the memory using the mode selector requires a special sequence of operations (see Section 6.5)

8.1.3 Backup Battery/Accumulator

Exceptions

CPU 312 IFM has no backup battery or accumulator.
The CPU 313 does not require an accumulator since the accumulator does not back up the software clock.

Backup Battery or Accumulator?

Table 8-2 shows the differences in the backup provided by an accumulator and a backup battery.

Table 8-2 Using a Backup Battery or Accumulator

Backup with...	... Backs up	Remarks	Backup Time
Accumula-tor	Real-time clock only	The accumulator is recharged when the power of the CPU is on. **Note:** The user program must be stored on the memory card or in the CPU 314 IFM in read-only memory.	120 hours (at 25°C) 60 hours (at 60°C) ... after 1 hour recharging
Backup battery	• User program (if not stored on memory card and protected against loss on power failure) • More data areas in data blocks are to be retained than possible without battery • The real-time clock	**Note:** The CPU can retain some of the data without a battery. You only need a backup battery if you want to retain more data than this.	1 year

8.1.4 Memory Card

Exceptions

You cannot insert a memory card with the CPU 312 IFM and 314 IFM. These CPUs have an integrated read-only memory.

Purpose of the Memory Card

With the memory card, you can expand the load memory of your CPU.

You can store the user program and the parameters that set the responses of the CPU and modules on the memory card. You can also save the firmware of your CPU on the memory card (not CPU 318-2).

If you store the user program on the memory card, it will remain in the CPU when the power is off even without a backup battery.

Available Memory Cards

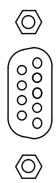
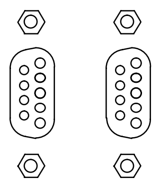
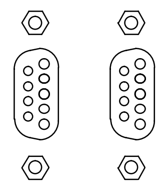
The following memory cards are available:

Table 8-3 Memory Cards

Capacity	Type	Remarks
16 KB	5 V FEPROM	The CPU supports the following functions: • Loading of the user program on the module into the CPU In this function, the memory of the CPU is reset, the user program is loaded on to the memory card, and then from the memory card to the CPU's working memory. • Copying of RAM to ROM (not with the CPU 318-2)
32 KB		
64 KB		
256 KB		
128 KB		
512 KB		
1 MB		
2 MB		
4 MB		
128 KB	5 V RAM	Only with the CPU 318-2
256 KB		
512 KB		
1 MB		
2 MB		

8.1.5 MPI and PROFIBUS-DP Interface

Table 8-4 CPU Interfaces

CPU 312 IFM CPU 313 CPU 314 IFM CPU 314	CPU 315-2 DP CPU 316-2 DP		CPU 318-2	
MPI interface	MPI interface	PROFIBUS-DP interface	MPI/DP Interface	PROFIBUS-DP interface
 MPI	 MPI DP		 MPI/DP DP	
–	–	–	Reconfiguration as a PROFIBUS-DP interface is possible	–

MPI Interface

The MPI is the interface of the CPU for the programming device/OP and for communication in an MPI subnet.
The typical (preset) transmission rate is 187.5 kbps (CPU 318-2: can be set up to 12 Mbps)
You must set 19.2 kbps to communicate with a S7-200.

PROFIBUS-DP Interface

CPUs with 2 interfaces offer you the PROFIBUS-DP interface, which allows them to be connected to a PROFIBUS-DP bus system. Transmission rates up to 12 Mbps are possible.

Connectable Devices

MPI	PROFIBUS-DP
• Programming device/PC and OP • S7 programmable controller with MPI interface (S7-300, M7-300, S7-400, M7-400, C7-6xx) • S7-200 (**Note:** only 19.2 kbps)	• PG/PC and OP • S7 programmable controllers with the PROFIBUS-DP interface (S7-200, S7-300, M7-300, S7-400, M7-400, C7-6xx) • Other DP masters and DP slaves

Only 19.2 Kbps for S7-200 in MPI Subnet

Note

At 19.2 kbps for communication with an S7-200, the following applies:
– A **maximum of 8 nodes** (CPU, PG/OP, FM/CP with own MPI address) are allowed in one subnet.
– You cannot carry out **any global data communication**.

Please consult the *S7-200 Manual* for further information!

Removing and Inserting Modules in the MPI Subnet

You must not plug in or remove any modules (SM, FM, CP) of an S7-300 configuration while data are being transmitted over the MPI.

Warning

If you remove or plug in S7-300 modules (SM, FM, CP) during data transmission via the MPI, the data might be corrupted by disturbing pulses.

You must not plug in or remove modules (SM, FM, CP) of an S7-300 configuration during data transmission via the MPI!

Loss of GD packets Following Change in the MPI Subnet During Operation

Warning

Loss of data packets in the MPI subnet:

Connecting an additional CPU to the MPI subnet during operation can lead to loss of GD packets and to an increase in cycle time.

Remedy:

1. Disconnect the node to be connected from the supply.
2. Connect the node to the MPI subnet.
3. Switch the node on.

8.1.6 Clock and Runtime Meter

Table 8-5 shows the characteristics and functions of the clock for the various CPUs.

When you parameterize the CPU in *STEP 7*, you can also set functions such as synchronization and the correction factor(see the *STEP 7* online help system).

Table 8-5 Characteristics of the Clock of the CPUs

Characteristics	312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP	318-2
Type	Software clock		Hardware clock (integrated “real-time clock”)					
Manufacturer setting	DT#1994-01-01-00:00:00							
Backup	Not possible		• Backup battery • Accumulator					
Operating hours counter	–	1						8
Number		0						0 to 7
Value range		0 to 32767 hours						0 to 32767 hours
Accuracy	... max deviation per day:							
• With power supply switched on 0 to 60° C	± 9s							
• With power supply switched off								
0° C	+2s to –5s							
25° C	± 2s							
40° C	+2s to –3s							
60° C	+2s to –7s							

With the Power Off

The following table shows the clock behavior with the power of the CPU off, depending on the backup:

Backup	Clock Behavior
With backup battery	The clock continues to operate in POWER OFF (except the software clock).
With accumulator	The clock of the CPU continues to operate when the power is off for the backup time of the accumulator (except the software clock). When the power is on, the accumulator is recharged.
	In the event of backup failure, an error message is **not** generated. When the power comes on again, the clock continues at the clock time at which the power went off.
None	At POWER ON, the clock continues to operate using the clock time at which POWER OFF took place. Since the CPU is not backed up, the clock does not continue at POWER OFF.

8.2 Communication Options of the CPU

The CPUs offer you the following communication options:

Table 8-6 CPU Communication Options

Communications	MPI	DP	Description
PG/OP-CPU	x	x	A CPU can maintain several on-line connections simultaneously to one or more programming devices or operator panels. One connection is reserved for a programming device and one for an operator panel.
Communication SFCs for non-configured S7 connections			These functions can be used to transfer data over the MPI subnet or within an S7-300. (You will find a list of the SFCs in Appendix C.1)
• Via an MPI subnet	x	–	
• Within an S7-300	x	x	
Communication SFCs for configured S7 connections	x	x	With these S7 connections, the S7-300-CPUs are servers for S7-400 CPUs. That means the S7-400 CPUs can write data to or read data from the S7-300 CPUs.
Global data communication	x	–	The CPUs of the S7-300 can exchange global data.

Detailed Information

You can find out more about communication in the *STEP 7* online help system and in the *Communication with SIMATIC* Manual.

Routing with 31x-2 CPUs

With the 31x-2 CPUs and STEP7 as of V 5.x you can reach S7 stations online beyond subnet borders with the programming device/PC and, for example, load user programs or a hardware configuration or execute testing and startup functions. To route via the DP interface, you must enable the “Programming, modifying and monitoring via the PROFIBUS” function when configuring and parameterizing the CPU.
The CPUs 315-2 DP and 316-2 DP provide you with additional connections for routing. In other words, routing does not occupy any other CPU connections. With the CPU 318-2 you must also consider the routing connections for the corresponding interface connections.
You can find a detailed description of routing in the *STEP 7* online help system.

Global Data Communication with S7-300 CPUs

Below you will find important features of global data communication in the S7-300.

Send and Receive Conditions

For the communication via GD circuits, you should observe the following conditions:

- The following must apply for a GB packet sender:
  Scan $rate_{sender} \times$ cycle $time_{sender} \geq 60$ ms (CPU 318-2: ≥ 10 ms)
- The following must apply for a GD packet receiver:
  Scan $rate_{receiver} \times$ cycle $time_{receiver} <$ scan $rate_{sender} \times$ cycle $time_{sender}$

Non-observance of these conditions can lead to the loss of a GD packet. The reasons for this are:

- The performance capability of the smallest CPU in the GD circuit
- Sending and receiving of global data is carried out asynchronously by the sender and receiver.

Loss of global data is displayed in the status field of a GD circuit if you have configured this with *STEP 7*.

Note

Please note the following in relation to global data communication: global data sent will not be acknowledged by the receiver!

The sender therefore receives no information on whether a receiver and which receiver has received the sent global data.

Send Cycles for Global Data

If you set “Send after every CPU cycle” in *STEP 7* (as of version 3.0) and the CPU has a short CPU cycle (< 60 ms), the operating system might overwrite an unsent CPU GD packet. **Tip:** The loss of global data is displayed in the status field of a GD circuit if you have configure this using *STEP 7*.

8.3 Testing Functions and Diagnostics

The CPUs provide you with:

- Testing functions for commissioning
- Diagnostics via LEDs and via *STEP 7*

8.3.1 Testing Functions

The CPUs offer you the following testing functions:

- Monitor Variables
- Modify Variables
- Forcen (note the differences between CPUs)
- Monitor block
- Set Breakpoint

You can find a detailed description of the testing functions in the *STEP 7* online help system.

Important with "Monitor Block"

The *STEP 7* function "Monitor Block" increases the cycle time of the CPU.

In *STEP 7* you can set a maximum permissible increase in cycle time (not in the case of the CPU 318-2). To do this, you must set "Process Mode" when setting the CPU parameters in *STEP 7*.

Different Features of Forcing S7-300

Please note the different features of forcing in the different CPUs:

CPU 318-2	CPU 312 IFM to 316-2 DP
The variables of a user program with fixed preset values (force values) cannot be changed or overwritten by the user program.	The variables of a user program with fixed preset values (force values) can be changed or overwritten in the user program. (See Figure 8-3 on page 8-14)
The following can be variables: Inputs/outputs Peripheral I/Os Memory markers You can force up to 256 variables.	The following can be variables: Inputs/Outputs You can force up to 10 variables.

Forcing with the CPU 312 IFM to 316-2 DP:

Caution

The forced values in the process-image input table can be overwritten by write commands (for example T IB x, = I x.y, copy with SFC, etc.) as well as by peripheral read commands (for example L PIW x) in the user program or by PG/OP write functions!

Outputs initialized with forced values only return the forced value if the user program does not execute any write accesses to the outputs using peripheral write commands (e.g. T PQB x) and if no PG/OP functions write to these outputs!

Note: The interrupt response time may increase up to 5.5 ms if forcing is active.

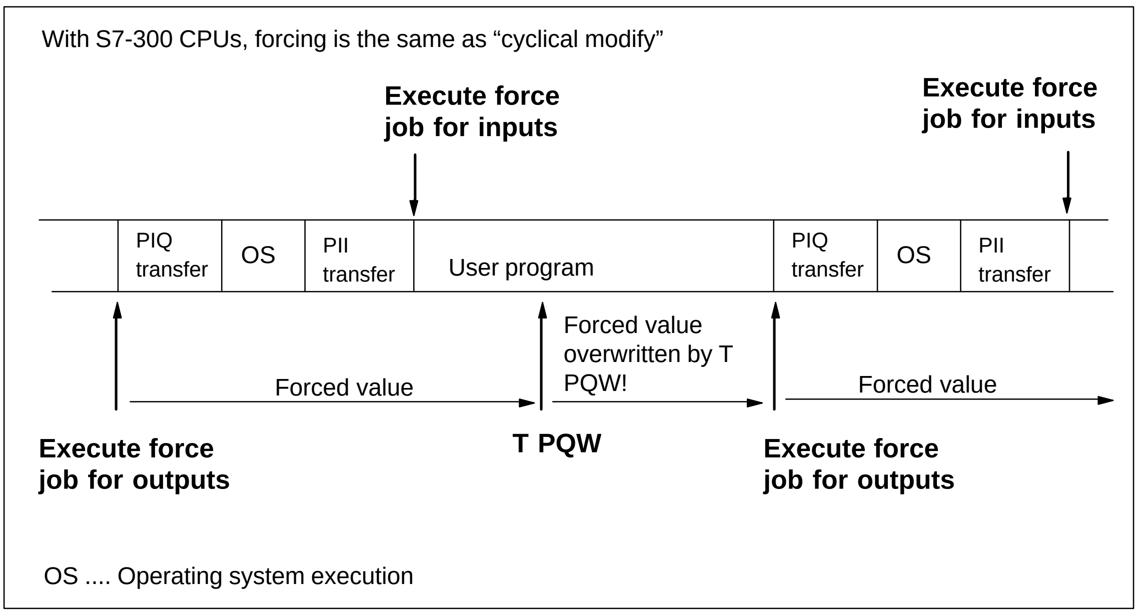


Figure 8-3 The Principle of Forcing with S7-300 CPUs (CPU 312 IFM to 316-2 DP)

8.3.2 Diagnosis with LED Displays

In Table 8-7, only the LEDs relevant to the diagnosis of the CPU and S7-300 are listed. You will find the significance of the PROFIBUS-DP interface LEDs explained in Chapter 9.

Table 8-7 Diagnostic LEDs of the CPU

LED	Description	
SF	**Comes on** in the event of	Hardware faults Programming errors Parameter assignment errors Calculation errors Timing errors Faulty memory card Battery fault or no backup at power on I/O fault/error (external I/O only) Communication error
BATF	**Comes on** when	The backup battery is missing, faulty or not charged. **Note:** It also comes on when an accumulator is connected. The reason for this is that the user program is not backed up by the accumulator.
STOP	**Comes on** when	The CPU is not processing a user program
	Flashes when	The CPU requests a memory reset

8.3.3 Diagnosis with *STEP 7*

Note

Please note that despite the extensive monitoring and error response functions provided, this is not a safety-oriented or fault-tolerant system.

If an error occurs, the CPU enters the cause of the error in the diagnostic buffer.You can read the diagnostic buffer using the programming device.

When an error occurs or there is an interrupt event, the CPU either goes into STOP mode or you can respond in the user program via error or interrupt OBs. You will find a detailed description of diagnosis with *STEP 7* in the *STEP 7* online help system.

In Appendix B you will find an overview of the following:

- Which errors or interrupt events you can respond to with which OBs
- Which OB you can program in which CPU

CPU Behavior When There Is No Error OB

If you have not programmed an error OB, the CPU reacts as follows:

CPU Goes to STOP with Missing ...	CPU Remains in RUN with Missing ...
OB 80 (Time-out) OB 85 (Program execution error) OB 86 (Node failure in PROFIBUS-DP network) OB 87 (Communication error) OB 121 (Programming error) OB 122 (I/O direct access error)	OB 81 (Power supply fault)

CPU Behavior When There Is No Interrupt OB

If you have not programmed an interrupt OB, the CPU reacts as follows:

CPU Goes to STOP with Missing ...	CPU Remains in RUN with Missing ...
OB 10/11 (Time-of-day interrupt) OB 20/21 (Delay interrupt) OB 40/41 (Process interrupt) OB 82 (Diagnostic interrupt)	OB 32/35 (Watchdog interrupt)

Tip for OB 35 (CPU 318-2: and OB 32)

For the watchdog interrupt OB 35/32, you can set times from 1 ms upwards. Note: The smaller the selected watchdog interrupt period, the more likely watchdog interrupt errors will occur. You must take into account the operating system times of the CPU in question, the runtime of the user program and the extension of the cycle by active programming device functions, for example.

8.4 CPUs – Technical Specifications

In This Section

- You will find the technical specifications of the CPU.
- You will find the technical specifications of the integrated inputs/outputs of the CPU 312 IFM and 314 IFM.
- You will **not** find the features of the CPU 31x-2 DP as a DP master/DP slave. Refer to Chapter 9.

8.4.1 CPU 312 IFM

Order No.

6ES7 312-5AC02-0AB0

Special Features

- Integrated inputs and outputs (wired up via a 20-pin front connector)
- No backup battery and therefore maintenance-free
- An S7-300 with CPU 312 IFM can be mounted only on one rack

Integrated Functions of the CPU 312 IFM

Integrated Functions	Description
Process interrupt	Interrupt inputs: Inputs parameterized in this way trigger a process interrupt at the corresponding signal edge. If you wish to use the digital inputs 124.6 to 125.1 as interrupt inputs, you must program these using *STEP 7*.
Counter	The CPU 312 IFM offers these special functions as an alternative at the digital inputs 124.6 to 125.1. For a description of the special functions “Counter” and “Frequency meter”, please refer to the *Integrated Functions* Manual.
Frequency meter	

“Interrupt Inputs” of the CPU 312 IFM

If you wish to use the digital inputs 124.6 to 125.1 as interrupt inputs, you must program these in *STEP 7* in the CPU parameters.

Note the following points:

- These digital inputs have a very low signal delay. At this interrupt input, the module recognizes pulses with a length as of approx. 10 to 50 μs. In order to prevent interference pulses from triggering interrupts, you must connect shielded cables to the activated interrupt inputs (see Section 4.3.4).
  Note: The interrupt-triggering pulse must be at least 50 μs in length.

- The input status associated with an interrupt in the process image input table or with L PIB always changes with the normal input delay of approx. 3 ms.

Start Information for OB 40

Table 8-8 describes the relevant temporary (TEMP) variables of OB 40 for the “interrupt inputs” of the CPU 312 IFM. The process interrupt OB 40 is described in the *System and Standard Functions* Reference Manual.

Table 8-8 Start Information for OB 40 for the Interrupt Inputs of the Integrated I/Os

Byte	Variable	Data Type	Description	
6/7	OB40_MDL_ADDR	WORD	B#16#7C	Address of the interrupt triggering module (the CPU here)
8 on	OB40_POINT_ADDR	DWORD	See Figure 8-4	Signaling of the interrupt triggering integrated inputs

Display of the Interrupt Inputs

You can read which interrupt input has triggered a process interrupt from the variable OB40_POINT_ADDR. Figure 8-4 shows the allocation of the interrupt inputs to the bits of the double word.

Note: If interrupts of different inputs occur at very short intervals (< 100 μs apart), more than one bit can be set at the same time. This means that several interrupts may cause OB 40 to start only once.

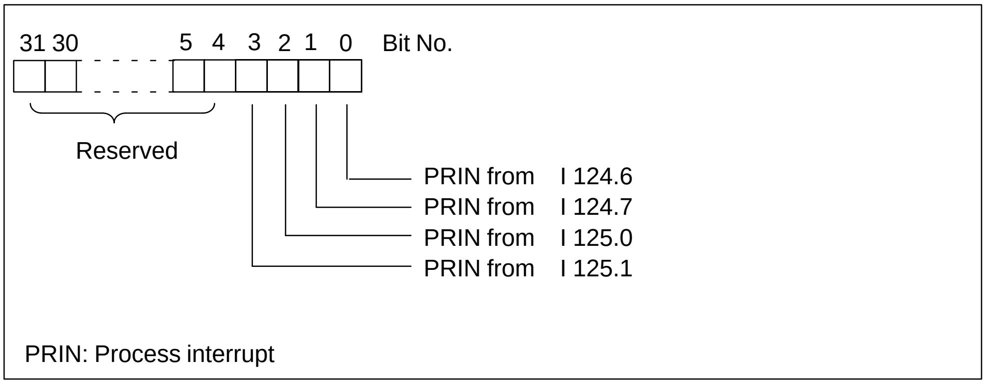


Figure 8-4 Display of the States of the Interrupt Inputs of the CPU 312 IFM

Front View

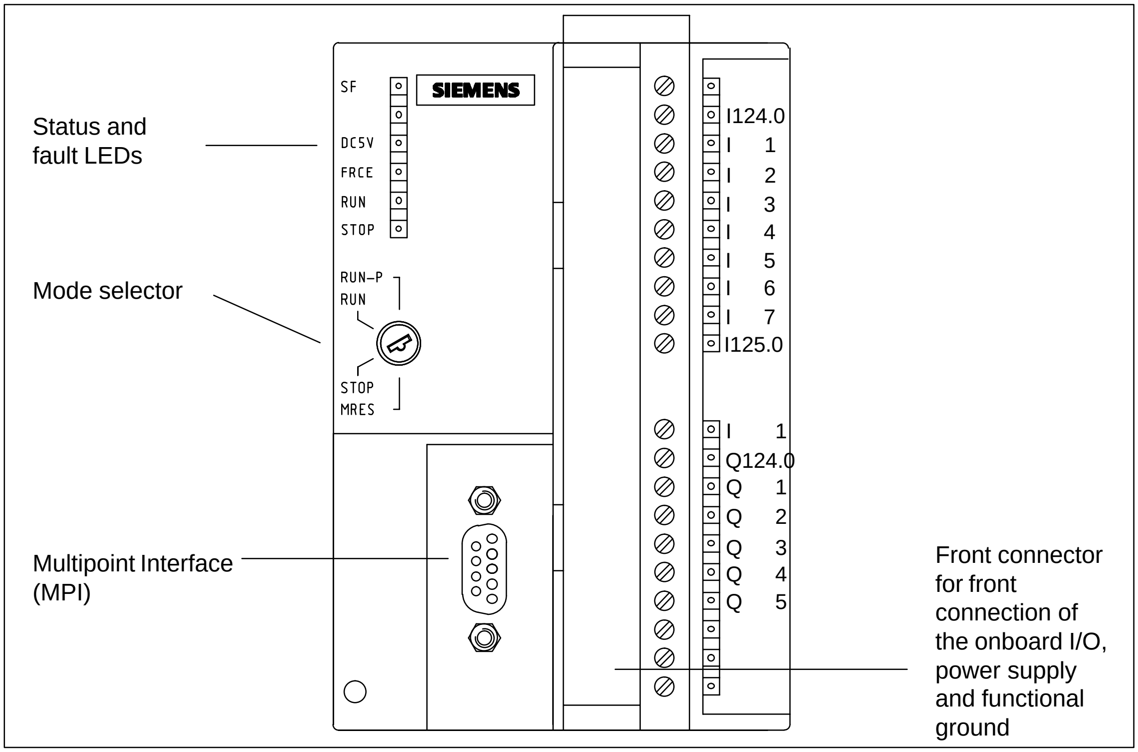


Figure 8-5 Front View of the CPU 312 IFM

Technical Specifications of the CPU 312 IFM

Memory	
Working memory (integral)	6 KB
Load memory	
• integral	20 KB RAM 20 KB EEPROM
Speed	approx. 0.7 ms per 1000 binary instructions
Bit memories	1024
• Adjustable retentivity	MB 0 to MB 71
• Preset	MB 0 to MB 15
Counter	32
• Adjustable retentivity	from C 0 to C 31
• Preset	from C 0 to C 7
Times (only updated in OB1!)	64
• Adjustable retentivity	No
Retentive data area	1 DB; max. 72 data bytes
Maximum sum of retentive data	72 bytes
Clock memories	8 (1 memory byte)
Local data	
• In all	512 bytes
• Per priority class	256 bytes
Nesting depth	8 per priority class
Digital inputs Digital outputs	128 + 10 integrated 128 + 6 integrated
Analog inputs Analog outputs	32 32
Process image	
• Integrated Inputs Outputs	124 to 127 I 124.0 to I 127.7 Q 124.0 to Q 127.7
• External Inputs Outputs	0 to 32 I 0.0 to I 31.7 Q 0.0 to Q 31.7

Blocks	
• OBs max. size	See Appendix B 8 KB
• FBs max. size	32 8 KB
• FCs max. size	32 8 KB
• DBs max. size	127 (DB 0 reserved) 8 KB
• SFCs	See Appendix
• SFBs	See Appendix
Integrated functions	
• Counter	1 counter, counter frequency 10 kHz; 2 directional comparators
• Frequency meter	up to 10 kHz max.
Functions	
Real-time clock	Software clock
Communication	
MPI	
• Guaranteed PG connections	1
• Guaranteed OP connections	1
• Free connections for PG/OP/configured S7 connections	2
• Guaranteed connections for non-configured S7 connections	2
• Global data communication	
No. of GD circuits	4
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	1
max. net data per packet	22 bytes
Length of consistent data per packet	8 bytes
• No. of nodes	max. 32 nodes
• Transmission rate	19.2; 187.5 kbps

Communication – Continued	
MPI	
• Distance without repeaters with 2 repeaters with 10 repeaters in series	 50 m (54.5 yd.) 1100 m (1199 yd.) 9100 m (9919 yd.)
• MPI interface	Non-isolated
Voltages, Currents	
Rated voltage	24V DC
Power input from 24V (without load current for outputs)	0.7 A (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External protection for supply lines	Circuit breaker; 10 A, type B or C
Power losses	9 W (typical)

Dimensions, Configuration	
Installation dimensions W × H × D (mm)	80 × 125 130
Weight	0.45 kg (15.75 oz)
Configuration	max. 8 modules on 1 rack
Norms, Test Specifications	
Norms and test specifications	see *Module Specifications* Reference Manual

Technical Specifications of the Special Inputs of the CPU 312 IFM

Module-Specific Data	
Number of inputs	4 I 124.6 to 125.1
Cable length	
• Shielded	max. 100 m (109 yd.)
Voltages, Currents, Potentials	
Number of inputs that can be triggered simultaneously	4
• (horizontal configuration)	
up to 60 °C	4
• (vertical configuration)	
up to 40 °C	4
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	
• Process interrupt	Parameterizable
Diagnostic functions	None

Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal I 125.0 and I 125.1 I 124.6 and I 124.7	 15 to 30 V 15 to 30 V
• For “0” signal	–3 to 5 V
Input current	
• For “1” signal I 125.0 and I 125.1 I 124.6 and I 124.7	 min. 2 mA min. 6.5 mA
Input delay time	
• For “0” to “1”	max. 50 µs
• For “1” to “0”	max. 50 µs
Input characteristic	
E 125.0 and E 125.1 E 124.6 and 124.7	to IEC 1131, type 1 to IEC 1131, type 1
Connection of 2-wire BEROs	no
• Permissible quiescent current I 125.0 and I 125.1 I 124.6 and I 124.7	 max. 0.5 mA max. 2 mA

Time, Frequency	
Internal conditioning time for	
• Interrupt processing	max. 1.5 ms
Input frequency	≤ 10 kHz

Technical Specifications of the Digital Inputs of the CPU 312 IFM

Note

Alternatively, you can parameterize the inputs I 124.6 and I 124.7 as special inputs, in which case the technical specifications listed for the special inputs apply to the inputs I 124.6 and I 124.7.

Module-Specific Data	
Number of inputs	8
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Number of inputs that can be triggered simultaneously	8
• (horizontal configuration)	
up to 60 °C	8
• (vertical configuration)	
up to 40 °C	8
Galvanic isolation	No

Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None
Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal	11 to 30 V
• For “0” signal	–3 to 5 V
Input current	
• For “1” signal	7 mA (typical)
Input delay time	
• For “0” to “1”	1.2 to 4.8 ms
• For “1” to “0”	1.2 to 4.8 ms
Input characteristic	to IEC 1131, Type 2
Connection of 2-wire BEROs	Possible
• Permissible quiescent current	max. 2 mA

Technical Specifications of the Digital Outputs of the CPU 312 IFM

Module-Specific Data	
Number of outputs	6
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Total current of outputs (per group)	
• (horizontal configuration)	
up to 40 °C	max. 3 A
up to 60 °C	max. 3 A
• (vertical configuration)	
up to 40 °C	max. 3 A
Galvanic isolation	No
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None

Actuator Selection Data	
Output voltage	
• For "1" signal	min. L + (– 0.8 V)
Output current	
• For "1" signal	
Rated value	0.5 A
Permissible range	5 mA to 0.6 A
• For "0" signal Residual current	max. 0.5 mA
Load impedance range	48 Ω to 4 kΩ
Lamp load	max. 5 W
Parallel connection of 2 outputs	
• For dual-channel triggering of a load	Possible
• For performance increase	Not possible
Triggering of a digital input	Possible
Switching frequency	
• For resistive load	max. 100 Hz
• For inductive load to IEC 947-5-1, DC 13	max. 0.5 Hz
• For lamp load	max. 100 Hz
Inductive breaking voltage limited internally to	30 V (typical)
Short-citcuit protection of the output	yes, electronically timed
• Response threshold	1 A (typical)

Terminal Assignment Diagram of the CPU 312 IFM

Figure 8-6 shows the terminal assignment of the CPU 312 IFM. You wire the integrated inputs/outputs of the CPU using a 20-pin front connector (see Section 4.3.3).

Caution

The CPU 312 IFM has no reverse polarity protection. If the poles are reversed, the integral outputs are defective but despite this, the CPU does not go to STOP and the status LEDs light up. In other words, the fault is not indicated.

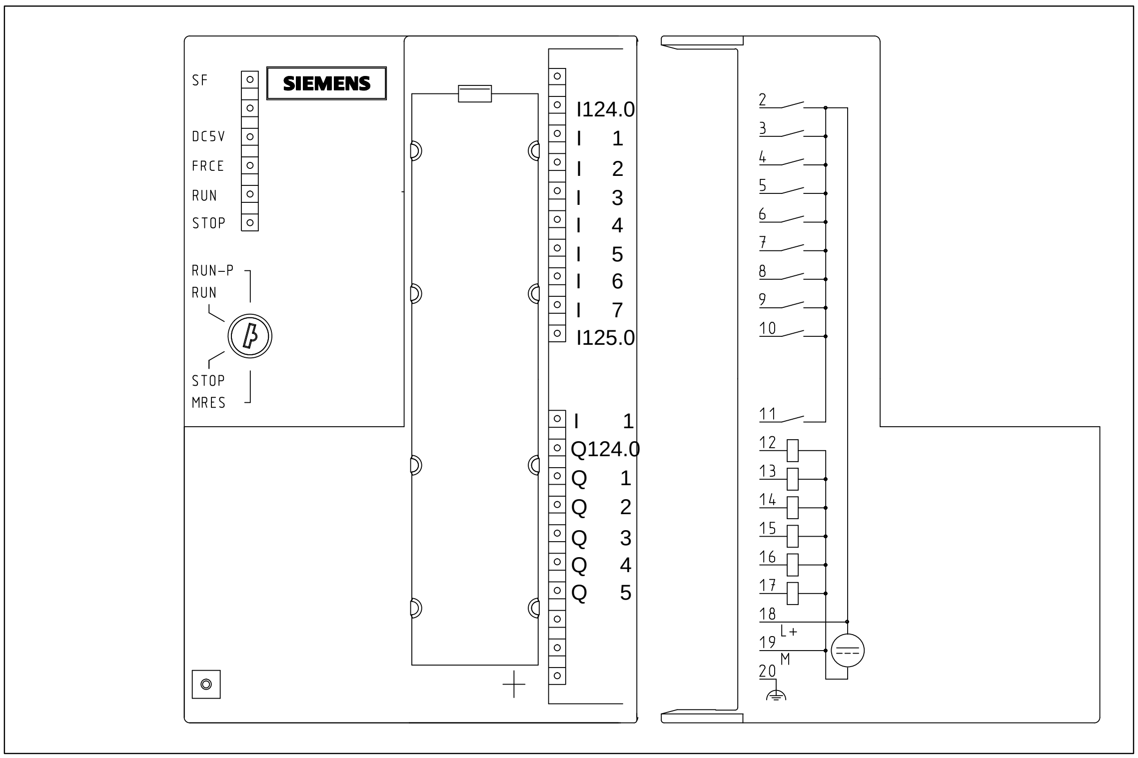


Figure 8-6 Terminal Assignment Diagram of the CPU 312 IFM

Grounded Configuration Only

You can use the CPU 312 IFM in a grounded configuration only. The functional ground is jumpered internally in the CPU 312 IFM with the M terminal (see Figure 8-7 on page 8-27).

Power Supply Connections

The power supply

- for CPU 312 IFM **and**
- for integrated I/Os

is connected to terminals 18 and 19 (see Figure 8-6).

Short-Circuit Characteristics

If a short-circuit occurs at one of the integral outputs of the CPU 312 IFM, you must proceed as follows:

1. Switch the CPU 312 IFM to STOP or switch off the power supply.
2. Remove the cause of the short-circuit.
3. Switch the CPU 312 IFM back to RUN or switch the power supply back on.

Basic Circuit Diagram of the CPU 312 IFM

Figure 8-7 shows the basic circuit diagram of the CPU 312 IFM.

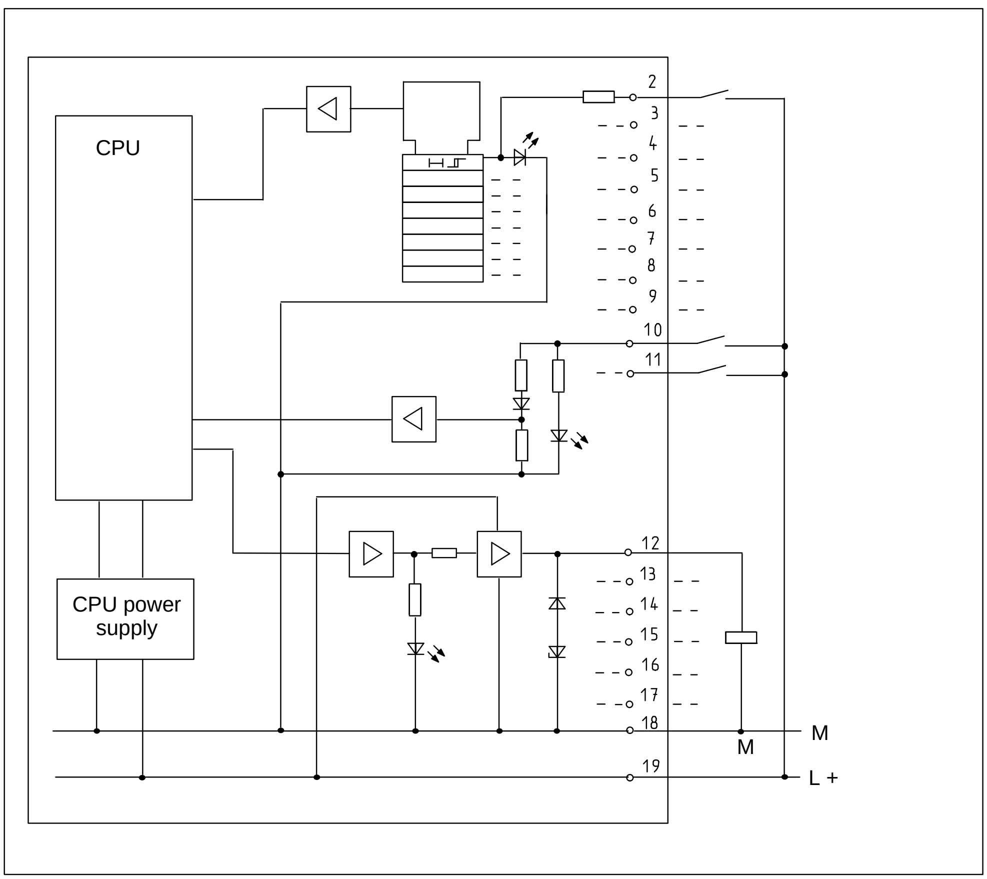


Figure 8-7 Basic Circuit Diagram of the CPU 312 IFM

8.4.2 CPU 313

Order No.

6ES7 313-1AD03-0AB0

Technical Specifications of the CPU 313

Memory	
Working memory (integral)	12 KB
Load memory	
• Integral	20 KB RAM
• Expandable	up to 4 MB FEPROM (memory card)
Speed	approx. 0.7 ms per 1000 binary instructions
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 71
• Preset	MB 0 to MB 15
Counter	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
Times (only updated in OB1!)	128
• Adjustable retentivity	from T 0 to T 31
• Preset	No retentive times
Retentive data area	1 DB; max. 72 data bytes
Maximum sum of retentive data	72 bytes
Clock memories	8 (1 memory byte)
Local data	
• In all	1536 bytes
• Per priority class	256 bytes
Nesting depth	8 per priority class; 4 additional levels within a synchro-nous error OB
Digital inputs Digital outputs	128 128
Analog inputs Analog outputs	32 32

Process image	0 to 127
Inputs Outputs	I 0.0 to I 127.7 Q 0.0 to Q 127.7
Blocks	
• OBs max. size	See Appendix B 8 KB
• FBs max. size	128 8 KB
• FCs max. size	128 8 KB
• DBs max. size	127 (DB 0 reserved) 8 KB
• SFCs	See Appendix C
• SFBs	See Appendix C
Functions	
Real-time clock	Software clock
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Backup battery	
• Backup time at 25 °C and uninterrupted backup of the CPU	min. 1 year
• Storage at 25 °C	approx. 5 years

Communications	
MPI	
• Guaranteed PG connections	1
• Guaranteed OP connections	1
• Free connections for PG/OP/configured S7 connections	2
• Guaranteed connections for non-configured S7 connections	4
• Global data communication	
No. of GD circuits	4
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	1
max. net data per packet	22 bytes
Length of consistent data per packet	8 bytes
• Number of nodes	max. 32; 127 with repeaters
• Transmission rate	19.2; 187.5 kbps
• Distance	
without repeaters	50 m (54.5 yd.)
with 2 repeaters	1100 m (1199 yd.)
with 10 repeaters in series	9100 m (9919 yd.)
• MPI interface	Non-isolated

Voltages, Currents	
Rated voltage	24V DC
Current drawn from 24 V (idle)	0.7 A (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, type B or C
Power losses	8 W (typical)
Dimensions, Configuration	
Installation dimensions W × H × D (mm)	80 × 125 130
Weight (without memory card and backup battery)	0.53 kg (15.75 oz)
Configuration	max. 8 modules on 1 rack
Norms, Test Specifications	
Norms, test specifications	see *Module Specifications* Reference Manual

8.4.3 CPU 314

Order No.

6ES7 314-1AE04-0AB0

Technical Specifications of the CPU 314

Memory	
Working memory (integral)	24 KB
Load memory	
• Integral	40 KB RAM
• Expandable	up to 4 MB FEPROM (memory card)
Speed	approx. 0.3 ms per 1000 binary instructions
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 15
Counter	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
Times (only updated in OB1!)	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
Retentive data area	8 DBs; max. 4096 data bytes (in total)
Maximum sum of retentive data	4736 bytes
Clock memories	8 (1 memory byte)
Local data	
• In all	1536 bytes
• Per priority class	256 bytes
Nesting depth	8 per priority class; 4 additional levels within a synchro-nous error OB

Digital inputs Digital outputs	512 512
Analog inputs Analog outputs	64 64
Process image	0 to 127
Inputs Outputs	I 0.0 to I 127.7 Q 0.0 to Q 127.7
Blocks	
• OBs max. size	See Appendix B 8 KB
• FBs max. size	128 8 KB
• FCs max. size	128 8 KB
• DBs max. size	127 (DB0 reserved) 8 KB
• SFCs	See Appendix
• SFBs	See Appendix
Functions	
Real-time clock	Hardware clock
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Backup battery	
• Backup time at 25 °C and uninterrupted backup of the CPU	min. 1 year
• Storage at 25 °C	approx. 5 years

Buffer time of clock with accumulator	
at 0°C	4 weeks (typical)
at 25°C	4 weeks (typical)
at 40°C	3 weeks (typical)
at 60°C	1 week (typical)
Battery charging time	1 h (typical)
Communications	
MPI	
• Guaranteed PG connections	1
• Guaranteed OP connections	1
• Free connections for PG/OP/configured S7 connections	2
• Guaranteed connections for non-configured S7 connections	8
• Global data communication	
No. of GD circuits	4
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	1
max. net data per packet	22 bytes
Length of consistent data per packet	8 bytes
• Number of nodes	max. 32; 127 with repeaters
• Transmission rate	19.2; 187.5 kbps
• Distance	
without repeaters	50 m (54.5 yd.)
with 2 repeaters	1100 m (1199 yd.)
with 10 repeaters in series	9100 m (9919 yd.)
• MPI interface	Non-isolated

Voltages, Currents	
Rated voltage	24V DC
Current drawn from 24 V (idle)	0.7 A (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, type B or C
Power losses	8 W (typical)
Dimensions, Configuration	
Installation dimensions W × H × D (mm)	80 × 125 × 130
Weight (without memory card and backup battery)	0.53 kg (15.75 oz)
Configuration	max. 32 modules on 4 racks
Norms, Test Specifications	
Norms, test specifications	see *Module Specifications* Reference Manual

8.4.4 CPU 314 IFM

Order No.

6ES7 314-5AE03-0AB0

Special Features

- Integrated inputs/outputs (wired up via 40-pin front connectors)

You can find detailed information on analog value processing and on connecting measuring sensors and loads/actuators to the analog inputs/outputs in the *Module Specifications* Reference Manual. Figures 8-13 and 8-14 on page 8-47 show wiring examples.

Integrated Functions of the CPU 314 IFM

Integrated functions	Description
Process interrupt	Interrupt inputs: Inputs parameterized in this way trigger a process interrupt at the corresponding signal edge. If you wish to use the digital inputs 126.0 to 126.3 as interrupt inputs, you must program these using *STEP 7*. **Note:** To prevent the interrupt response times of the CPU being increased, you should address the analog inputs of the CPU separately in the user program using L PIW. Double-word addressing can increase the access times by up to 200 μs!
Counter	The CPU 314 IFM offers these special functions as an alternative at digital inputs 126.0 to 126.3. For a description of these special functions, please refer to the *Integrated Functions* Manual.
Frequency meter	
Counter A/B	
Positioning	
CONT_C	These functions are not restricted to specific inputs and outputs of the CPU 314 IFM. For a description of these functions, please refer to the *System and Standard Functions* Reference Manual.
CONT_S	
PULSEGEN	

“Interrupt Inputs” of the CPU 314 IFM

If you wish to use the digital inputs 126.0 to 126.4 as interrupt inputs, you must program these in *STEP 7* in the CPU parameters.

Note the following points:

These digital inputs have a very low signal delay. At this interrupt input, the module recognizes pulses with a length as of approx. 10 to 50 μs. In order to prevent interference pulses from triggering interrupts, you must connect shielded cables to the activated interrupt inputs (see Section 4.3.4).

Note: The interrupt-triggering pulse must be at least 50 μs in length.

Start Information for OB 40

Table 8-8 describes the relevant temporary (TEMP) variables of OB 40 for the “interrupt inputs” of CPU 314 IFM. The process interrupt OB 40 is described in the *System and Standard Functions* Reference Manual.

Table 8-9 Start Information for OB 40 for the Interrupt Inputs for the Integrated I/O

Byte	Variable	Data Type	Description	
6/7	OB40_MDL_ADDR	WORD	B#16#7C	Address of the interrupt triggering module (the CPU here)
8 on	OB40_POINT_ADDR	DWORD	See Figure 8-8	Signaling of the interrupt triggering integrated inputs

Display of the Interrupt Inputs

You can read which interrupt input has triggered a process interrupt from the variable OB40_POINT_ADDR. Figure 8-8 shows the allocation of the interrupt inputs to the bits of the double word.

Note: If interrupts of different inputs occur at very short intervals (< 100 μs apart), several bits can be set at the same time. This means that more than one interrupt may cause OB 40 to start only once.

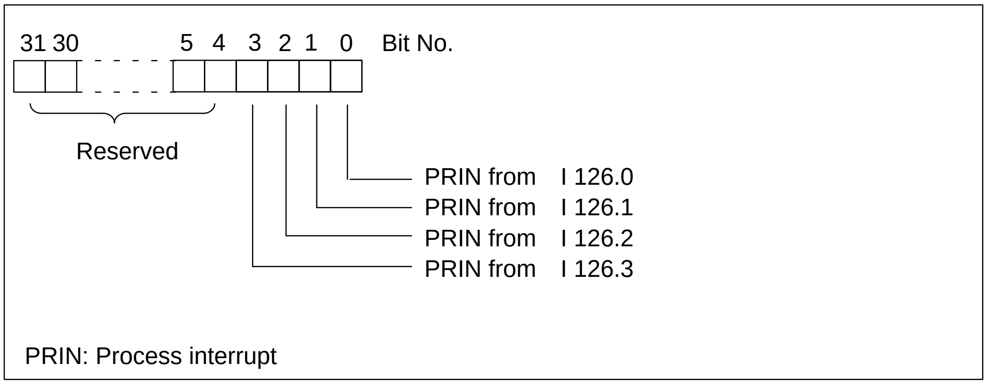
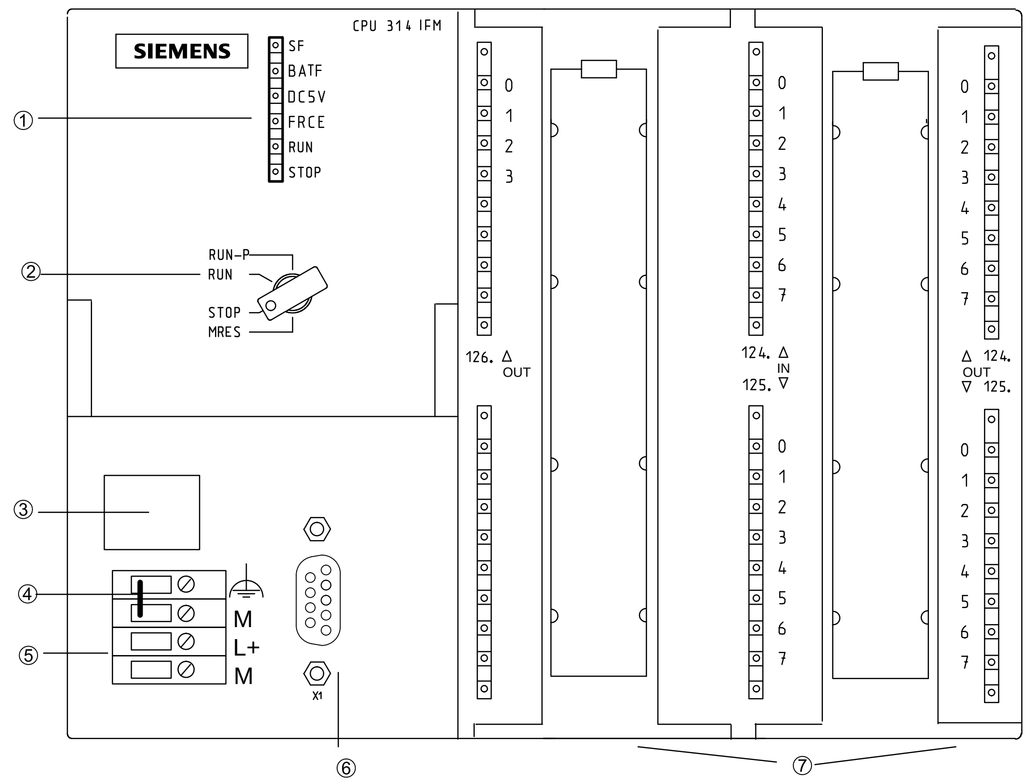


Figure 8-8 Display of the States of the Interrupt Inputs of the CPU 314 IFM

Front View of the CPU 314 IFM



① Status and fault LEDs
② Mode selector
③ Compartment for backup battery or accumulator
④ Jumper (removable)
⑤ Terminals for power supply and functional ground
⑥ Multipoint interface (MPI)
⑦ Integrated inputs/outputs

Figure 8-9 Front View of the CPU 314 IFM

Technical Specifications of the CPU 314 IFM

Memory	
Working memory (integral)	32 KB
Load memory	
• Integral	48 KB RAM 48 KB FEPROM
Speed	approx. 0.3 ms per 1000 binary instructions
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 143
• Preset	MB 0 to MB 15
Counter	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
Times (only updated in OB1!)	128
• Adjustable retentivity	from T 0 to T 71
• Preset	No retentive times
Retentive data area	2 DBs; max. 144 data bytes (in total)
Maximum sum of retentive data	144 bytes
Clock memories	8 (1 memory byte)
Local data	
• In all	1536 bytes
• Per priority class	256 bytes
Nesting depth	8 per priority class; 4 additional levels within a synchro-nous error OB
Digital inputs	496 + 20 integrated (of which 4 are spe-cial inputs)
Digital outputs	496 + 16 integrated
Analog inputs Analog outputs	64 + 4 integrated 64 + 1 integrated
Process image	
• Integrated Inputs Outputs	124 to 127 E 124.0 to E 127.7 A 124.0 to A 127.7
• External Inputs Outputs	0 to123 E 0.0 to E 123.7 A 0.0 to A 123.7

Blocks	
• OBs max. size	See Appendix B 8 KB
• FBs max. size	128 8 KB
• FCs max. size	128 8 KB
• DBs max. size	127 (DB 0 reser-ved) 8 KB
• SFCs	See Appendix C
• SFBs	See Appendix C

Integrated functions	
• Counter	1 or 2 counters, counting fre-quency 10 kHz; 2 directional compa-rators
• Frequency meter	up to 10 kHz max.
• Positioning	Channel 1

Functions	
Real-time clock	Hardware clock
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Backup battery	
• Backup time at 25 °C and uninterrupted backup of the CPU	min. 1 year
• Storage at 25 °C	approx. 5 years
Buffer time of clock with ac-cumulator	
at 0°C	typ. 4 weeks
at 25°C	typ. 4 weeks
at 40°C	typ. 3 weeks
at 60°C	typ. 1 week
Battery charging time	1 h (typical)

Communications	
MPI	
• Guaranteed PG connections	1
• Guaranteed OP connections	1
• Free connections for PG/OP/configured S7 connections	2
• Guaranteed connections for non-configured S7 connections	8
• Global data communication	
No. of GD circuits	4
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	1
max. net data per packet	22 bytes
Length of consistent data per packet	8 bytes
• Number of nodes	max. 32; 127 with repeaters
• Transmission rate	19.2; 187.5 kbps
• Distance	
without repeaters	50 m (54.5 yd.)
with 2 repeaters	1100 m (1199 yd.)
with 10 repeaters in series	9100 m (9919 yd.)
• MPI Interface	Non-isolated

Voltages, Currents	
Rated voltage	24V DC
Current drawn from 24 V (idle)	1.0 A (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, type B or C
PG supply on MPI (15 to 30V DC)	max. 200 mA
Power losses	16 W (typical)
Dimensions, Configuration	
Installation dimensions W × H × D (mm)	160 × 125 × 130
Weight (without memory card and backup battery)	0.9 kg (15.75 oz)
Configuration	max. 31 modules on 4 racks
Norms, Test Specifications	
Norms, test specifications	see *Module Specifications* Reference Manual

Characteristic Features of the Integrated Inputs and Outputs of the CPU 314 IFM

Table 8-10 Characteristic Features of the Integrated Inputs and Outputs of the CPU 314 IFM

Inputs/Outputs	Characteristics	
Analog inputs	• Voltage inputs ± ±10 V • Current inputs ±20 mA • Resolution 11 bits + sign bit • Galvanically isolated	All information required for • Analog value display and • Connecting measuring sensors and loads/actuators to the analog inputs and outputs can be found in the *Module Specifications* Reference Manual.
Analog output	• Voltage output ± ±10 V • Current output ±20 mA • Resolution 11 bits + sign bit • Galvanically isolated	
Digital inputs	**Special Inputs (I 126.0 to I 126.3)**	**“Standard” Inputs**
	• Input frequency up to 10 kHz • Non-isolated	• Galvanically isolated
	• Rated input voltage 24V DC • Suitable for switch and 2-wire proximity switches (BEROs)	
Digital outputs	• Output current 0.5 A • Rated load voltage 24V DC • Galvanically isolated • Suitable for solenoid valves and DC contactors	

Technical Specifications of the Analog Inputs of the CPU 314 IFM

Module-Specific Data	
Number of inputs	4
Cable length	
• Shielded	max. 100 m (109 yd.)
Voltages, Currents, Potentials	
Galvanic isolation	
• between channels and backplane bus	Yes
Permissible potential difference	
• between inputs and M_{ANA} (U_{CM})	1.0V DC
• between M_{ANA} and $M_{internal}$ (U_{ISO})	75V DC 60V AC
Insulation tested at	500V DC
Analog Value Generation	
Measuring principle	Momentary value encoding (successive approximation)
Conversion time/resolution (per channel)	
• Basic conversion time	100 µs
• Resolution (inc. overdrive range)	11 bits + sign bit
Interference Suppression, Error Limits	
Interference voltage suppression	
• Common-mode interference (U_{CM} < 1.0 V)	> 40 dB
Crosstalk between the inputs	> 60 dB
Operational error limits (throughout temperature range, relative to input range)	
• Voltage input	± 1.0 %
• Current input	± 1.0 %

Interference Suppression, Error Limits, Continued	
Basic error limits (operational limit at 25 °C, relative to input range)	
• Voltage input	± 0.9 %
• Current input	± 0.8 %
Temperature error (related to input range)	± 0.01 %/K
Linearity error (related to input range)	± 0.06 %
Repeatability (in the settled state at 25 °C, relative to input range)	± 0.06 %
Status, Interrupts; Diagnostics	
Interrupts	None
Diagnostic functions	None
Sensor Selection Data	
Input ranges (rated value)/input resistance	
• Voltage	± 10 V/50 kΩ
• Current	± 20 mA/105.5 Ω
Permissible input voltage for voltage input (destruction limit)	max. 30 V continuous; 38 V for max. 1 s (pulse duty factor 1:20)
Permissible input current for current input (destruction limit)	34 mA
Connection of signal encoders	
• For voltage measurement	Possible
• For current measurement	
as 2-wire measurement transducer	Not possible
as 4-wire measurement transducer	Possible

Technical Specifications of the Analog Output of the CPU 314 IFM

Module-Specific Data	
Number of outputs	1
Cable length	
• Shielded	max. 100 m (109 yd.)
Voltages, Currents, Potentials	
Galvanic isolation	
• Between channels and backplane bus	Yes
Permissible potential difference	
• Between M_{ANA} and $M_{internal}$ (U_{ISO})	75V DC 60V AC
Insulation tested at	500V DC
Analog Value Generation	
Resolution (incl. overdrive range)	11 bits + sign bit
Conversion time	40 µs
Settling time	
• For resistive load	0.6 ms
• For capacitive load	1.0 ms
• For inductive load	0.5 ms
Connection of substitute values	No
Interference Suppression, Error Limits	
Operational error limits (throughout temperature range, relative to output range)	
• Voltage output	± 1.0 %
• Current output	± 1.0 %
Basic error limit (operational limit at 25 °C, relative to output range)	
• Voltage output	± 0.8 %
• Current output	± 0.9 %
Temperature error (relative to output range)	± 0.01 %/K
Linearity error (relative to output range)	± 0.06 %
Repeat accuracy (in the settled state at 25 °C, relative to output range)	± 0.05 %

Output ripple; Range 0 to 50 kHz (relative to output range)	± 0.05 %
Status, Interrupts; Diagnostics	
Interrupts	None
Diagnostic functions	None
Actuator Selection Data	
Output ranges (rated values)	
• Voltage	± 10 V
• Current	± 20 mA
Load impedance	
• For voltage output	min. 2.0 kΩ
capacitive load	max. 0.1 µF
• For current output	max. 300 Ω
inductive load	max. 0.1 mH
Voltage output	
• Short-circuit protection	Yes
• Short-circuit current	max. 40 mA
Current output	
• Idle voltage	max. 16 V
Destruction limit for externally applied voltages/currents	
• Voltages at the output with ref. to M_{ANA}	max. ± 15 V continuous; ± 15 V for max. 1 s (pulse duty factor 1:20)
• Current	max. 30 mA
Connection of actuators	
• For voltage output	
2-wire connection	Possible
4-wire connection	Not possible
• For current output	
2-wire connection	Possible

Technical Specifications of the Special Inputs of the CPU 314 IFM

Module-Specific Data	
Number of inputs	4 I 126.0 to 126.3
Cable length	
• Shielded	max. 100 m (109 yd.)
Voltages, Currents, Potentials	
Number of inputs that can be triggered simultaneously	4
• (horizontal configuration)	
up to 60 °C	4
• (vertical configuration)	
up to 40 °C	4
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	
• Process interrupt	Parameterizable
Diagnostic functions	None

Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal	11 to 30 V or 18 to 30 V for angle step encoder for int. function “Positioning”
• For “0” signal	–3 to 5 V
Input current	
• For “1” signal	6.5 mA (typical)
Input delay time	
• For “0” to “1”	< 50 μs (17 ms typical)
• For “1” to “0”	< 50 μs (20 ms typical)
Input characteristic	to IEC 1131, Type 2
Connection of 2-wire BEROs	Possible
• Permissible quiescent current	max. 2 mA
Time, Frequency	
Internal conditioning time for	
• Interrupt processing	max. 1.2 ms
Input frequency	≤ 10 kHz

Technical Specifications of the Digital Inputs of the CPU 314 IFM

Module-Specific Data	
Number of inputs	16
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Rated load current L+	24V DC
• Polarity reversal protection	Yes
Number of inputs that can be triggered simultaneously	16
• (horizontal configuration)	
up to 60 °C	16
• (vertical configuration)	
up to 40 °C	16
Galvanic isolation	
• Between channels and backplane bus	Yes
Permissible potential difference	
• Between different circuits	75V DC 60V AC
Insulation tested at	500V DC
Current consumption	
• From L+ supply	max. 40 mA

Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None
Sensor Selection Data	
Input voltage	
• Rated value	24V DC
• For “1” signal	11 to 30 V
• For “0” signal	–3 to 5 V
Input current	
• For “1” signal	7 mA (typical)
Input delay time	
• For “0” to “1”	1.2 to 4.8 ms
• For “1” to “0”	1.2 to 4.8 ms
Input characteristic	to IEC 1131, Type 2
Connection of 2-wire BEROs	Possible
• Permissible quiescent current	max. 2 mA

Technical Specifications of the Digital Outputs of the CPU 314 IFM

Remarks

When the supply voltage is switched on a pulse occurs on the digital outputs! This can be 50 µs long within the permissible output current range. You must not, therefore, use the digital outputs to trigger high-speed counters.

Module-Specific Data	
Number of outputs	16
Cable length	
• Unshielded	max. 600 m
• Shielded	max. 1000 m
Voltages, Currents, Potentials	
Rated load current L+	24V DC
• Polarity reversal protection	No
Total current of outputs (per group)	
• (horizontal configuration)	
up to 40 °C	max. 4 A
up to 60 °C	max. 2 A
• (vertical configuration)	
up to 40 °C	max. 2 A
Galvanic isolation	
• Between channels and backplane bus	Yes
• Between the channels	Yes
in groups of	8
Permissible potential difference	
• Between different circuits	75V DC 60V AC
Insulation tested at	500V DC
Current consumption	
• From L+ supply (no-load)	max. 100 mA
Status, Interrupts; Diagnostics	
Status display	1 green LED per channel
Interrupts	None
Diagnostic functions	None

Actuator Selection Data	
Output voltage	
• For “1” signal	min. L + (– 0.8 V)
Output current	
• For “1” signal	
Rated value	0.5 A
Permissible range	5 mA to 0.6 A
• For “0” signal (residual current)	max. 0.5 mA
Load impedance range	48 Ω to 4 kΩ
Lamp load	max. 5 W
Parallel connection of 2 outputs	
• For dual-channel triggering of a load	Possible, only outputs of the same group
• For performance increase	Not possible
Triggering of a digital input	Possible
Switching frequency	
• For resistive load	max. 100 Hz
• For inductive load to IEC 947-5-1, DC 13	max. 0.5 Hz
• For lamp load	max. 100 Hz
Inductive breaking voltage limited internally to	L+ (– 48 V) typical
Short-citcuit protection of the output	yes, electronically timed
• Response threshold	1 A (typical)

Terminal Assignment Diagram of the CPU 314 IFM

Figure 8-10 shows the terminal assignment of the CPU 314 IFM.

For wiring up the integrated I/Os you require two 40-pin front connectors (order number: 6ES7 392-1AM00-0AA0).

Always wire up digital inputs 126.0 to 126.3 with shielded cable due to their low input delay time.

Caution

Wiring errors at the analog outputs can cause the integrated analog I/O of the CPU to be destroyed! (for example, if the interrupt inputs are wired by mistake to the analog output).
The analog output of the CPU is only indestructible up to 15 V (output with respect to M_{ANA}).

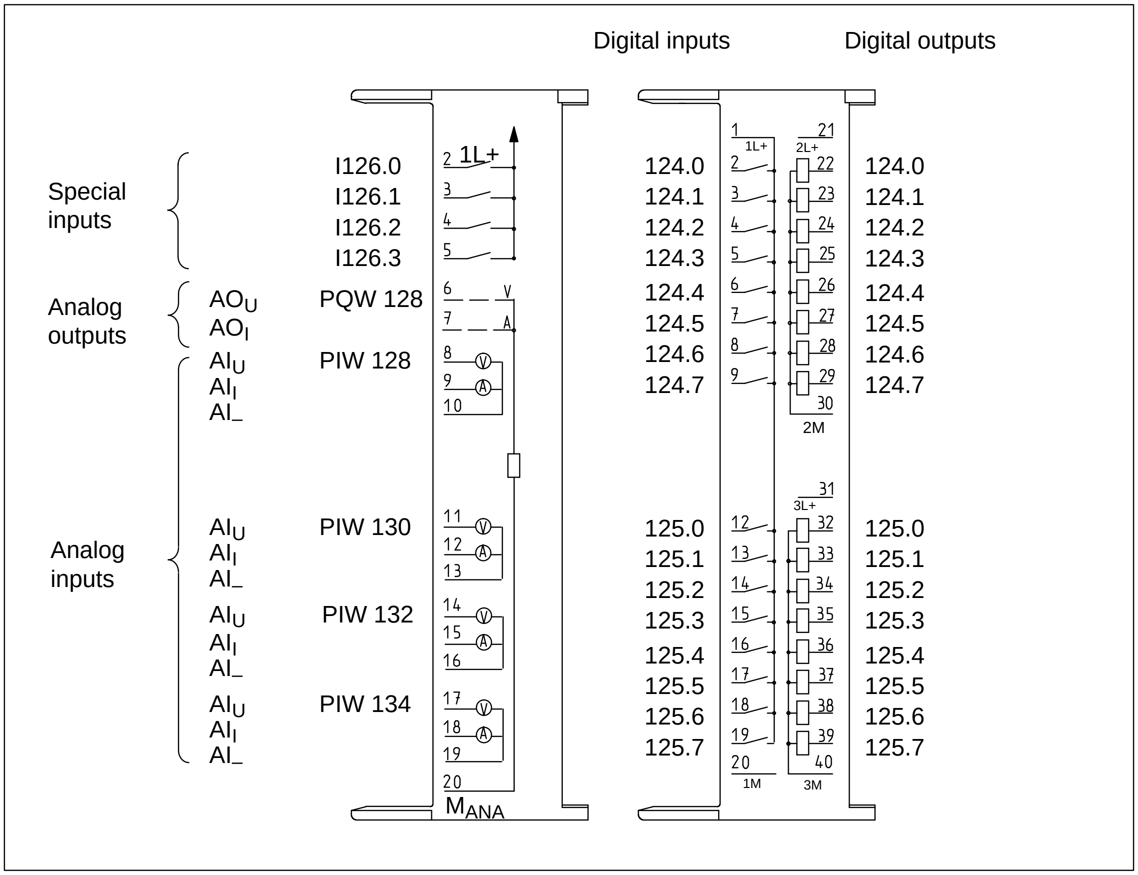


Figure 8-10   Terminal Assignment Diagram of the CPU 314 IFM

Basic Circuit Diagrams of the CPU 314 IFM

Figures 8-11 and 8-12 show the basic circuit diagrams for the integrated inputs/outputs of the CPU 314 IFM.

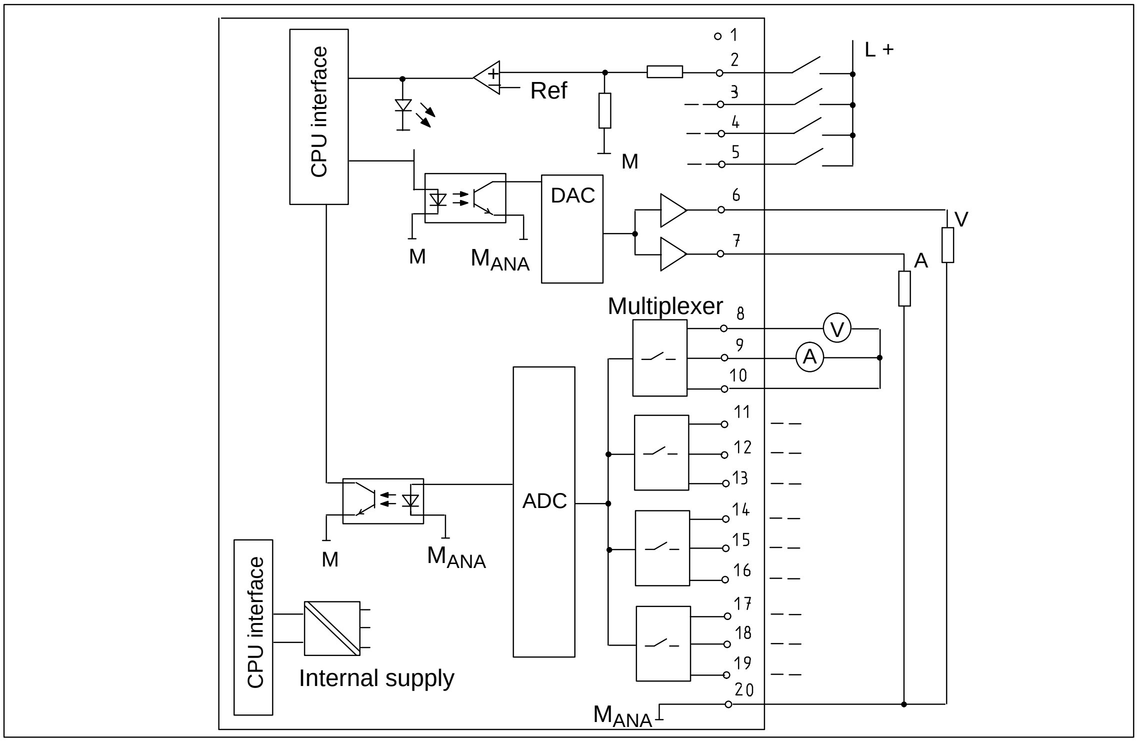


Figure 8-11 Basic Circuit Diagram of the CPU 314 IFM (Special Inputs and Analog Inputs/Outputs)

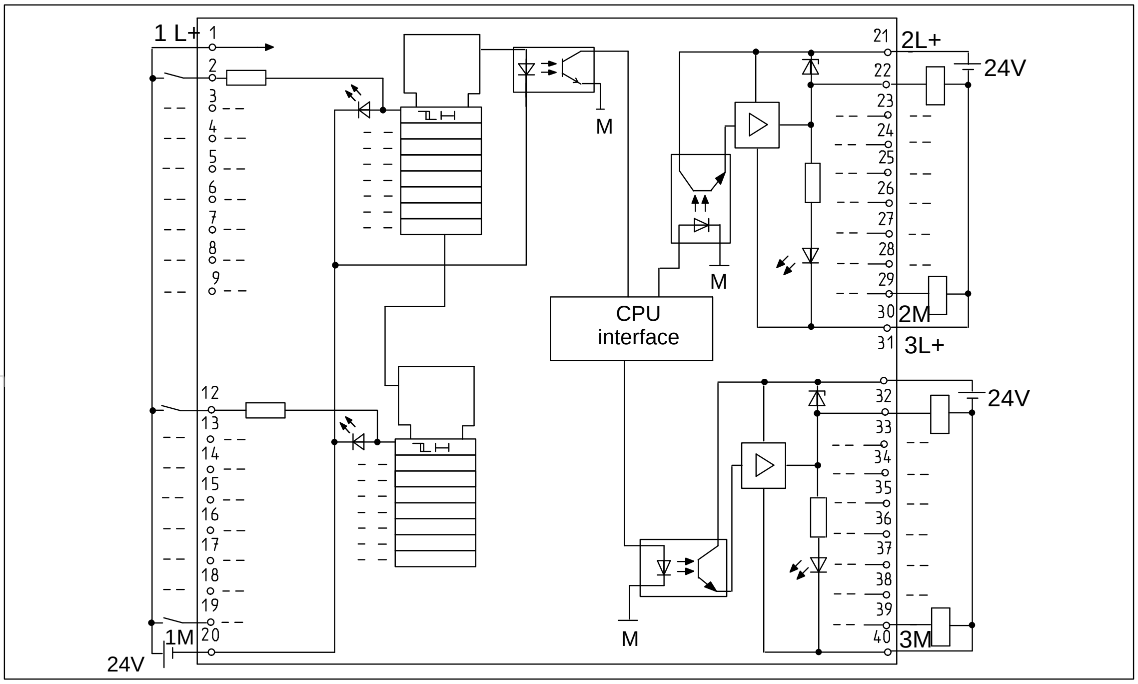


Figure 8-12 Basic Circuit Diagram of the CPU 314 IFM (Digital Inputs/Outputs)

Wiring the Analog Inputs

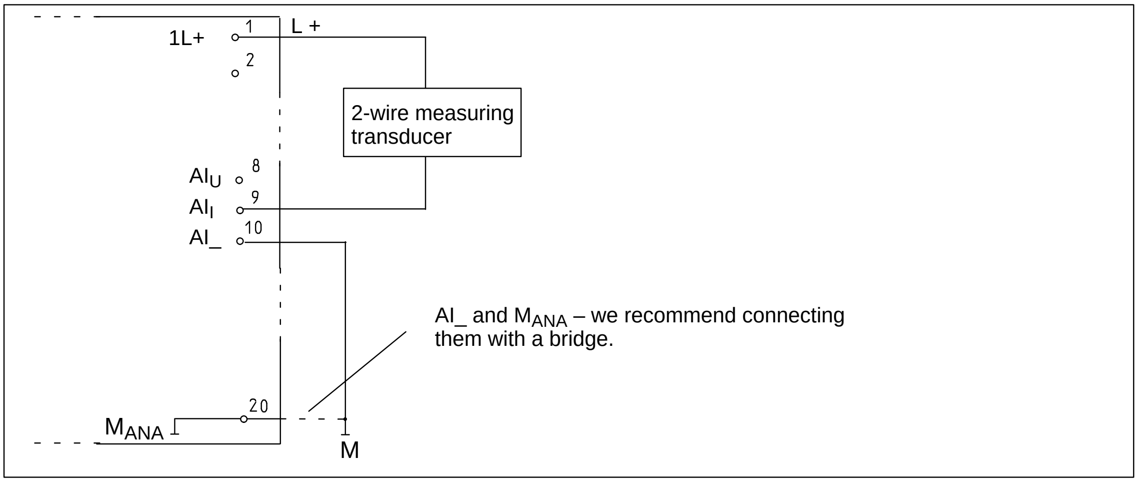


Figure 8-13 Wiring the Analog Inputs of the CPU 314 IFM with a 2-Wire Measuring Transducer

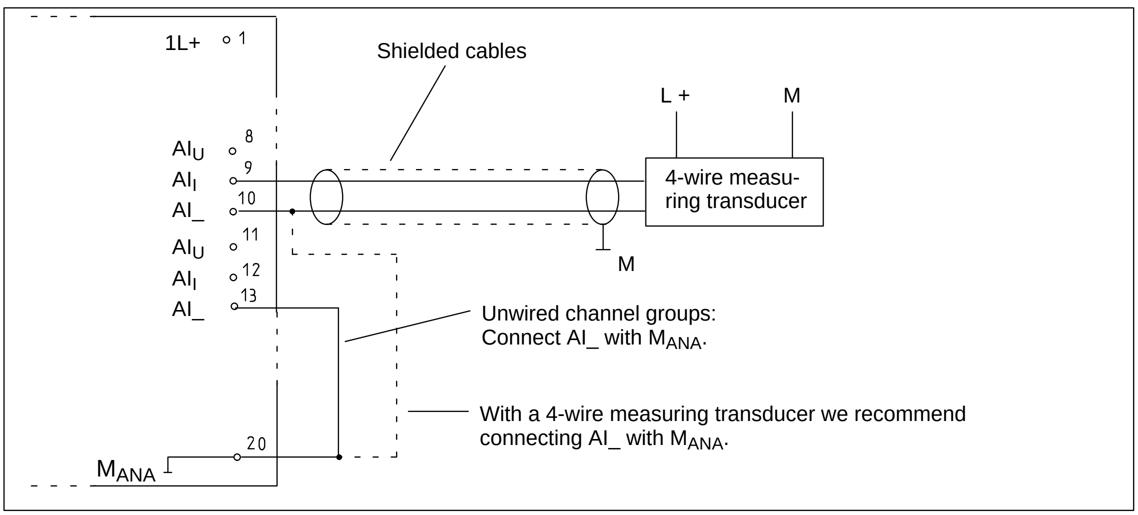


Figure 8-14 Wiring the Analog Inputs of the CPU 314 IFM with a 4-Wire Measuring Transducer

8.4.5 CPU 315

Order No.

6ES7 315-1AF03-0AB0

Technical Specifications of the CPU 315

Memory	
Working memory (integral)	48 KB
Load memory	
• Integral	80 KB RAM
• Expandable	up to 4 MB FEPROM (memory card)
Speed	approx. 0.3 ms per 1000 binary instructions
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 15
Counter	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
Times (only updated in OB1!)	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
Retentive data area	8 DBs; max. 4096 data bytes (in total)
Maximum sum of retentive data	4736 bytes
Clock memories	8 (1 memory byte)
Local data	
• In all	1536 bytes
• Per priority class	256 bytes
Nesting depth	8 per priority class; 4 additional levels within a synchro-nous error OB
Digital inputs Digital outputs	1024 1024
Analog inputs Analog outputs	128 128
Process image	0 to 127
Inputs Outputs	I 0.0 to I 127.7 Q 0.0 to Q 127.7
Blocks	
• OBs max. size	See Appendix B 16 KB
• FBs max. size	192 16 KB
• FCs max. size	192 16 KB
• DBs max. size	254 (DB0 reserved) 16 KB
• SFCs	See Appendix C
• SFBs	See Appendix C
Functions	
Real-time clock	Hardware clock
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Backup battery	
• Backup time at 25 °C and uninterrupted backup of the CPU	min. 1 year
• Storage at 25 °C	approx. 5 years
Buffer time of clock with ac-cumulator	
at 0°C at 25°C at 40°C at 60°C	4 weeks (typical) 4 weeks (typical) 3 weeks (typical) 1 week (typical)

Battery charging time	1 h (typical)
Communications	
MPI	
• Guaranteed PG connections	1
• Guaranteed OP connections	1
• Free connections for PG/OP/configured S7 connections	2
• Guaranteed connections for non-configured S7 connections	8
• Global data communication	
No. of GD circuits	4
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	1
max. net data per packet	22 bytes
Length of consistent data per packet	8 bytes
• Number of nodes	max. 32; 127 with repeaters
• Transmission rate	19.2; 187.5 kbps
• Distance	
without repeaters	50 m (54.5 yd.)
with 2 repeaters	1100 m (1199 yd.)
with 10 repeaters in series	9100 m (9919 yd.)
• MPI interface	Non-isolated
Voltages, Currents	
Rated voltage	24V DC (– 10 %/+ 15 %)
Current drawn from 24 V (idle)	0.7 A (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, type B or C
Power losses	8 W (typical)

Dimensions, Configuration	
Installation dimensions W × H × D (mm)	80 × 125 × 130
Weight (without memory card and backup battery)	0.53 kg (15.75 oz)
Configuration	max. 32 modules on 4 racks
Norms, Test Specifications	
Norms, test specifications	see *Module Specifications* Reference Manual

8.4.6 CPU 315-2 DP

Order No.

6ES7 315-2AF03-0AB0

DP master or DP slave

You can use the CPU 315-2 DP with its 2nd interface (PROFIBUS-DP interface) either as a DP master or as a DP slave in a PROFIBUS-DP network.

See Chapter 9 for a detailed description of the PROFIBUS-DP features of the CPU 315-2 DP.

Technical Specifications of the CPU 315-2 DP

Memory	
Working memory (integral)	64 KB
Load memory	
• Integral	96 KB RAM
• Expandable	up to 4 MB FEPROM (memory card)
Speed	approx. 0.3 ms per 1000 binary instr.
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 15
Counter	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
Times (only updated in OB1!)	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
Retentive data area	8 DBs; max. 4096 data bytes (in total)
Maximum sum of ret. data	4736 bytes
Clock memories	8 (1 memory byte)
Local data	
• In all	1536 bytes
• Per priority class	256 bytes

Nesting depth	8 per priority class; 4 additional levels within a synchro-nous error OB
Digital inputs Digital outputs (central and in a distributed configuration)	1024 1024
Analog inputs Analog outputs (central and in a distributed configuration)	128 128
Process image	0 to 127
Inputs Outputs	I 0.0 to I 127.7 Q 0.0 to Q 127.7
DP Address Area	1 KB (see Section 9)
Blocks	
• OBs max. size	See Appendix B 16 KB
• FBs max. size	192 16 KB
• FCs max. size	192 16 KB
• DBs max. size	254 (DB reserved) 16 KB 0
• SFCs	See Appendix C
• SFBs	See Appendix C

Functions	
Real-time clock	Hardware clock
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Backup battery	
• Backup time at 25 °C and uninterrupted backup of the CPU	min. 1 year
• Storage at 25 °C	approx. 5 years
Buffer time of clock with accumulator	
at 0°C	typ. 4 weeks
at 25°C	typ. 4 weeks
at 40°C	typ. 3 weeks
at 60°C	typ. 1 week
Battery charging time	1 h (typical)
Communications	
MPI	
• Guaranteed PG connections	1
• Guaranteed OP connections	1
• Free connections for PG/OP/configured S7 connections	2
• Guaranteed connections for non-configured S7 connections	8
• Global data communication	
No. of GD circuits	4
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	1
max. net data per packet	22 bytes
Length of consistent data per packet	8 bytes
• Number of nodes	max. 32; 127 with repeaters

• Transmission rate	19.2; 187.5 kbps
• Distance without repeaters with 2 repeaters with 10 repeaters in series	 50 m (54.5 yd.) 1100 m (1199 yd.) 9100 m (9919 yd.)
• MPI interface	Non-isolated
PROFIBUS-DP	
• Possible no. of DP slaves	64
• Address area per DP slave largest consistent block	244 bytes inputs/ outputs 32 bytes
• Transmission rate	up to 12 Mbps
• Transmission rate detection as a DP slave	no
• SYNC/FREEZE (as DP master)	yes
• Routing connections	yes max. 4
• Direct communication	Yes
• Equidistance	Yes
• Intermediate memory (as a DP slave)	244 bytes inputs and 244 bytes outputs, up to 32 address areas can be configured, max. 32 bytes per address area
• Distance	Depending on the transmission rate (see Section 5.1.3)
• PROFIBUS-DP interface	Galvanically isolated
Voltages, Currents	
Rated voltage	24V DC (– 10 %/+ 15 %)
Current drawn from 24 V (idle)	0.9 W (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, type B or C
Power losses	10 W (typical)

Dimensions, Configuration	
Installation dimensions W × H × D (mm)	80 × 125 × 130
Weight (without memory card and backup battery)	0.53 kg (15.75 oz)
Configuration	max. 32 modules on 4 racks

Norms, Test Specifications	
Norms, test specifications	see *Module Specifications* Reference Manual

8.4.7 CPU 316-2 DP

Order No.

6ES7 316-2AG00-0AB0

DP master or DP slave

You can use the CPU 316-2 DP with its 2nd interface (PROFIBUS-DP interface) either as a DP master or as a DP slave in a PROFIBUS-DP network.

See Chapter 9 for a detailed description of the PROFIBUS-DP features of the CPU 316-2 DP.

Technical Specifications of the CPU 316-2 DP

Memory	
Working memory (integral)	128 KB
Load memory	
• Integral	192 KB RAM
• Expandable	up to 4 MB FEPROM (memory card)
Speed	approx. 0.3 ms per 1000 binary instructions
Bit memories	2048
• Adjustable retentivity	MB 0 to MB 255
• Preset	MB 0 to MB 15
Counter	64
• Adjustable retentivity	from C 0 to C 63
• Preset	from C 0 to C 7
Times (only updated in OB1!)	128
• Adjustable retentivity	from T 0 to T 127
• Preset	No retentive times
Retentive data area	8 DBs; max. 4096 data bytes (in total)
Maximum sum of retentive data	4736 bytes
Clock memories	8 (1 memory byte)
Local data	
• In all	1536 bytes
• Per priority class	256 bytes

Nesting depth	8 per priority class; 4 additional levels within a synchronous error OB
Digital inputs Digital outputs (central and in a distributed configuration)	2048 2048
Analog inputs Analog outputs (central and in a distributed configuration)	128 128
Process image	0 to 127
Inputs	I 0.0 to I 127.7
Outputs	Q 0.0 to Q 127.7
DP Address Area	2 KB (see Section 9)
Blocks	
• OBs max. size	See Appendix B 16 KB
• FBs max. size	256 16 KB
• FCs max. size	512 16 KB
• DBs max. size	511 (DB reserved) 16 KB 0
• SFCs	See Appendix C
• SFBs	See Appendix C

Functions	
Real-time clock	Hardware clock
Operating hours counter	1
• Number	0
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Backup battery	
• Backup time at 25 °C and uninterrupted backup of the CPU	min. 1 year
• Storage at 25 °C	approx. 5 years
Buffer time of clock with accumulator	
at 0°C	typ. 4 weeks
at 25°C	typ. 4 weeks
at 40°C	typ. 3 weeks
at 60°C	typ. 1 week
Battery charging time	1 h (typical)
Communications	
MPI	
• Guaranteed PG connections	1
• Guaranteed OP connections	1
• Free connections for PG/OP/configured S7 connections	2
• Guaranteed connections for non-configured S7 connections	8
• Global data communication	
No. of GD circuits	4
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	1
max. net data per packet	22 bytes
Length of consistent data per packet	8 bytes
• Number of nodes	max. 32; 127 with repeaters
• Transmission rate	19.2; 187.5 kbps
• Distance without repeaters with 2 repeaters with 10 repeaters in series	 50 m (54.5 yd.) 1100 m (1199 yd.) 9100 m (9919 yd.)
• MPI interface	Non-isolated
PROFIBUS-DP	
• Possible no. of DP slaves	125
• Address area per DP slave largest consistent block	244 bytes inputs/ outputs 32 bytes
• Transmission rate	up to 12 Mbps
• Transmission rate detection as a DP slave	no
• SYNC/FREEZE (as DP master)	yes
• Routing connections	yes max. 4
• Direct communication	Yes
• Equidistance	Yes
• Intermediate memory (as a DP slave)	244 bytes inputs and 244 bytes outputs, up to 32 address areas can be configured, max. 32 bytes per address area
• Distance	Depending on the transmission rate (see Section 5.1.3)
• PROFIBUS-DP interface	Galvanically isolated
Voltages, Currents	
Rated voltage	24V DC (– 10 %/+ 15 %)
Current drawn from 24 V (idle)	0.9 W (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, type B or C
Power losses	10 W (typical)

Dimensions, Configuration	
Installation dimensions W × H × D (mm)	80 × 125 × 130
Weight (without memory card and backup battery)	0.53 kg (15.75 oz)

Configuration	max. 32 modules on 4 racks
Norms, Test Specifications	
Norms, test specifications	see *Module Specifications* reference Manual

8.4.8 CPU 318-2

Order No.

6ES7 318-2AF00-0AB0

Special Features

- 4 accumulators
- The MPI interface can be reconfigured: MPI or PROFIBUS DP (DP master).
- Data areas can be set (process image, local data)

For more information on the differences between the CPU 318-2 and the other CPUs, see Section 11.1.

DP master or DP slave

You can use the CPU 318-2 DP either as a DP master or as a DP slave in a PROFIBUS-DP network.

See Chapter 9 for a detailed description of the PROFIBUS-DP features of the CPU 318-2.

Definable Data Areas and Occupied Working Memory

You can change the size of the process image for the inputs/outputs and the local data areas when parameterizing the CPU 318-2.
If you increase the preset values for the process image and local data, this occupies additional working memory that is then no longer available for user programs.
The following proportions must be taken into consideration:

- Process image input table: 1 byte PII occupied 12 bytes in the working memory
  Process image output table: 1 byte PIQ occupied 12 bytes in the working memory

  For example:
  256 bytes in the PII occupy 3072 bytes and
  2047 bytes in the PII occupy 24564 bytes in the working memory.
- Local data 1 local data byte occupies 1 byte in the working memory
  There are 256 preset bytes per priority class. With 14 priority classes there are therefore 3584 bytes occupied in the working memory. With a maximum size of 8192 bytes you can still allocate 4608 bytes, which are then no longer available for the user program in the working memory.

Communication

You can reconfigure the first interface of the CPU from an MPI interface to a DP interface (DP master).
You can run the CPU as a DP master or a DP slave via the second DP interface.

In routing, the maximum number of possible connections is reduced for each of the two interfaces by 1 connection for each active PG/OP connection that the CPU 318-2 uses as a gateway.

Technical Specifications of the CPU 318-2

Memory	
Working memory (integral)	512 KB
• For user program	256 KB
• For data	256 KB
Load memory	
• Integral	64 KB RAM
• Expandable	up to 4 MB FEPROM (memory card) or up to 2 MB RAM (memory card)
Speed	approx. 0.1 ms per 1000 binary instructions
Bit memories	8192
• Adjustable retentivity	MB 0 to MB 1023
• Preset	MB 0 to MB 15
Counter	512
• Adjustable retentivity	from C 0 to C 511
• Preset	from C 0 to C 7
Times	512
• Adjustable retentivity	from T 0 to T 511
• Preset	No retentive times
Retentive data area	8 DBs; max. 8192 data bytes (in total)
Maximum sum of retentive data	11 KB
Clock memories	8 (1 memory byte)
Local data	
• Preset expandable to	4096 bytes 8192 bytes
• Per priority class	256 bytes

Nesting depth	16 per priority class; 3 additional levels within a synchro-nous error OB
Address area (central and in a distributed configuration)	8 KB
Process image (default)	0 to 255
Inputs Outputs	I 0.0 to I 255.7 Q 0.0 to Q 255.7
Process image (expanda-ble)	to 2047
Inputs Outputs	I 0.0 to I 2047.7 Q 0.0 to Q 2047.7
Blocks	
• OBs max. size	See Appendix B 64 KB
• FBs max. size	1024 64 KB
• FCs max. size	1024 64 KB
• DBs max. size	2047 (DB 0 reser-ved) 64 KB
• SFCs	See Appendix C
• SFBs	See Appendix C

Functions	
Real-time clock	Hardware clock
Operating hours counter	8
• Number	0 to 7
• Value range	0 to 32767 hours
• Selectivity	1 hour
• Retentive	Yes
Backup battery	
• Backup time at 25 °C and uninterrupted backup of the CPU (incl. 1 MB RAM memory card)	min. 1 year
• Storage at 25 °C	approx. 5 years
Buffer time of clock with accumulator	
at 0°C	typ. 4 weeks
at 25°C	typ. 4 weeks
at 40°C	typ. 3 weeks
at 60°C	typ. 1 week
Battery charging time	1 h (typical)

Communications	
Total number of connections using both interfaces (PG/OP/configured/not configured S7 connections with terminal point on the CPU)	max. 32;
1st MPI/DP Interface	
MPI Functionality	
• Connections for PG/OP/configured/not configured S7 connections/routing	max. 32
Of these, the following are reserved:	1 PG and 1 OP connection
• Global data communication	
No. of GD circuits	8
No. of send packets per GD circuit	1
No. of receive packets per GD circuit	2
max. net data per packet	54 bytes
Length of consistent data per packet	32 bytes
• Number of nodes	max. 32; 127 with repeaters
• Transmission rate	9.6; 19.2; 93.75; 187.5; 500 kbps; 1.5; 3; 6; 12 Mbps
• Distance	see Tables 5-3 and 5-4 on page 5-12

DP Functionality	
• Connections for PG/OP/configured/non-configured S7 connections/routing	max. 32
Of these, the following are reserved:	1 PG and 1 OP connection
• Connectable DP slaves	32
• Address area per DP slave largest consistent block	244 bytes inputs/ outputs 32 bytes
• Transmission rate	up to 12 Mbps
• SYNC/FREEZE	Yes
• Routing	Yes
• Direct communication	Yes
• Equidistance	Yes
• Intermediate memory (as a DP slave)	244 bytes inputs and 244 bytes outputs, up to 32 address areas can be configured, max. 32 bytes per address area
2nd DP Interface	
• Connections for PG/OP/configured S7 connections/routing	max. 16
• Connectable DP slaves	125
• Address area per DP slave	244 bytes inputs/ outputs
• Transmission rate	up to 12 Mbps
• Transmission rate detection as a DP slave	no
• SYNC/FREEZE (as DP master)	yes
• Routing	Yes
• Direct communication	Yes
• Equidistance	Yes

• Intermediate memory (as a DP slave)	244 bytes inputs and 244 bytes outputs, up to 32 address areas can be configured, max. 32 bytes per address area
• Distance	see Table 5-4 on page 5-12
Voltages, Currents	
Rated voltage	24V DC (– 10 %/+ 15 %)
Current drawn from 24 V (idle)	1.2 A (typical)
Inrush current	8 A
I^2t	0.4 A^2s
External fusing for supply lines (recommendation)	Circuit breaker; 2 A, type B or C
Power losses	12 W (typical)
Dimensions, Configuration	
Installation dimensions W × H × D (mm)	160 × 125 × 130
Weight (without memory card and backup battery)	0.93 kg (15.75 oz)
Configuration	max. 32 modules on 4 racks
Norms, Test Specifications	
Norms, test specifications	see *Module Specifications* Reference Manual

CPU 31x-2 as DP Master/DP Slave and Direct Communication

9

Introduction

In this chapter you will find the features and technical specifications of the CPUs 315-2 DP, 316-2 DP and 318-2. You will need these in order to use the CPU as a DP master or a DP slave and configure it for direct communication.

Declaration: Since the DP master/DP slave behavior is the same for all CPUs, the CPUs are described below as CPU 31x-2.

In This Chapter

Additional Literature

Descriptions and notes pertaining to configuration in general, configuration of a PROFIBUS subnet and diagnostics in the PROFIBUS subnet can be found in the *STEP 7* online help system.

9.1 DP Address Areas of the CPUs 31x-2

Address Areas of the CPU 31x-2

Address Area	315-2 DP	316-2 DP	318-2
DP address area for both inputs and outputs	1024 bytes	2048 bytes	8192 bytes
Number of those in the process image for both inputs and outputs	Bytes 0 to 127	Bytes 0 to 127	Bytes 0 to 255 (default) Can be set up to byte 2047

DP diagnostic addresses occupy 1 byte for the DP master and for each DP slave in the address area for the inputs. Under these addresses, for example, the DP standard diagnosis for the respective nodes can be called (LADDR parameter of SFC 13). The DP diagnostic addresses are specified during configuration. If you do not specify any DP diagnostic addresses, *STEP 7* allocates the addresses from the highest byte address downwards as DP diagnostic addresses.

9.2 CPU 31x-2 as DP Master

Introduction

This section covers the features and technical specifications of the CPU when it is used as a DP master.

The features and technical specifications of the CPU 31x-2 as the "standard" CPU are listed in Section 8.

Prerequisites

Should the MPI/DP interface be a DP interface? If so, you must then configure the interface as a DP interface.

Before the CPU can be put into operation, it must be configured as a DP master. This means carrying out the following steps in *STEP 7*:

- Configure the CPU as a DP master.
- Assign a PROFIBUS address.
- Assign a master diagnostic address.
- Integrate DP slaves into the DP master system.

  Is a DP slave a CPU 31x-2?

  If so, you will find that DP slave in the PROFIBUS-DP catalog as "pre-configured station". This DP slave CPU must be assigned a slave diagnostic address in the DP master. You must then interconnect the DP master with the DP slave CPU and stipulate the address areas for data interchange with the DP slave CPU.

Programming, Modifying and Monitoring via the PROFIBUS

As an alternative to the MPI interface, you can program the CPU or execute the PG's Monitor and Modify functions via the PROFIBUS-DP interface.

Note

The use of Monitor and Modify via the PROFIBUS-DP interface lengthens the DP cycle.

Equidistance

As of STEP7 V 5.x you can parameterize bus cycles of the same length (equidistant) for PROFIBUS subnets. You can find a detailed description of equidistance in the STEP7 online help system.

Power-Up of the DP Master System

CPU 31x-2 DP is DP Master	CPU 318-2 is DP Master
You can also set power-up time monitoring of the DP slaves with the "Transfer of parameters to modules" parameter.	Using the parameters "Transfer of parameters to modules" and "Ready message from modules" you can set power-up time monitoring for the DP slaves.
This means that the DP slaves must be powered up and parameterized by the CPU (as DP master) in the set time.	

PROFIBUS Address of the DP Master

You cannot set the 126 as the PROFIBUS address for the CPU 31x-2.

9.3 Diagnostics of the CPU 31x-2 as DP Master

Diagnosis with LEDs

Table 9-1 explains the meaning of the BUSF LED.
The BUSF LED assigned to the interface configured as the PROFIBUS-DP interface will always come on or flash.

Table 9-1 Meaning of the BUSF LED of the CPU 31x-2 as DP Master

BUSF	Description	Remedy
LED off	Configuring data OK; all configured slaves are addressable.	–
LED on	• Bus fault (hardware fault). • DP interface fault. • Different transmission rates in multiple DP master mode.	• Check the bus cable for short or interruption. • Evaluate the diagnostic data. Reconfigure or correct the configuring data.
LED flashes	• Station failure. • At least one of the configured slaves cannot be addressed.	• Ensure that the bus cable is connected to the CPU 31x-2 and that the bus is not interrupted. • Wait until the CPU 31x-2 has powered up. If the LED does not stop flashing, check the DP slaves or evaluate the diagnostic data for the DP slaves.

Reading Out the Diagnostic Data with STEP 7

Table 9-2   Reading Out the Diagnostic Data with *STEP 7*

DP Master	Block or Register in *STEP 7*	Application	See...
CPU 31x-2	DP slave diagnosis register	Display slave diagnosis as plain text on the *STEP 7* user interface	See the section on hardware diagnostics in the *STEP 7* online help system and in the *STEP 7* User Manual
	SFC 13 “DPNRM_DG”	Read out slave diagnosis (store in the data area of the user program)	Configuration for the CPU 31x-2, see Section 9.5.4; SFC, see *System and Standard Functions* Reference Manual Configuration for other slaves, see their description
	SFC 59 “RD_REC”	Read out data records of the S7 diagnosis (store in the data area of the user program)	*System and Standard Functions* Reference Manual
	SFC 51 “RDSYSST”	Read out system state sublists. Call SFC 51 in the diagnostic interrupt with the system state list ID W#16#00B4, and read out the system state list of the slave CPU.	

Evaluating a Diagnosis in the User Program

The following figures show you how to evaluate the diagnosis in the user program. Note the order number for the CPU 315-2 DP:

CPU 315-2 DP **<** 6ES7 315-2AF**03**-0AB0	CPU 315-2 DP as of 6ES7 315-2AF**03**-0AB0 CPU 316-2 DP as of 6ES7 316-2AG00-0AB0 CPU 318-2 as of 6ES7 318-2AJ00-0AB0
See Figure 9-1 on page 9-6	See Figure 9-2 on page 9-7

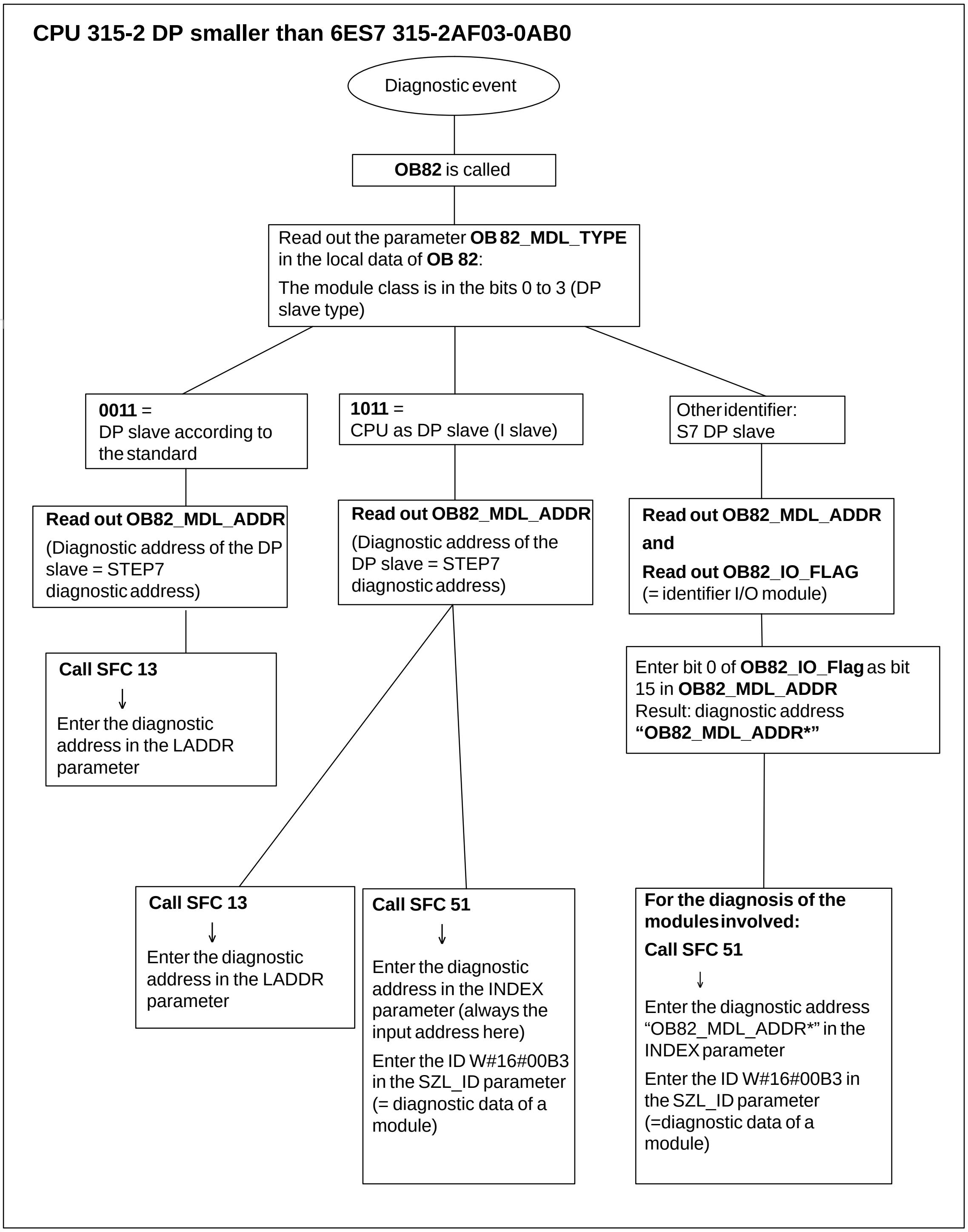


Figure 9-1 Diagnostics with CPU 315-2 DP **<** 315-2AF**03**

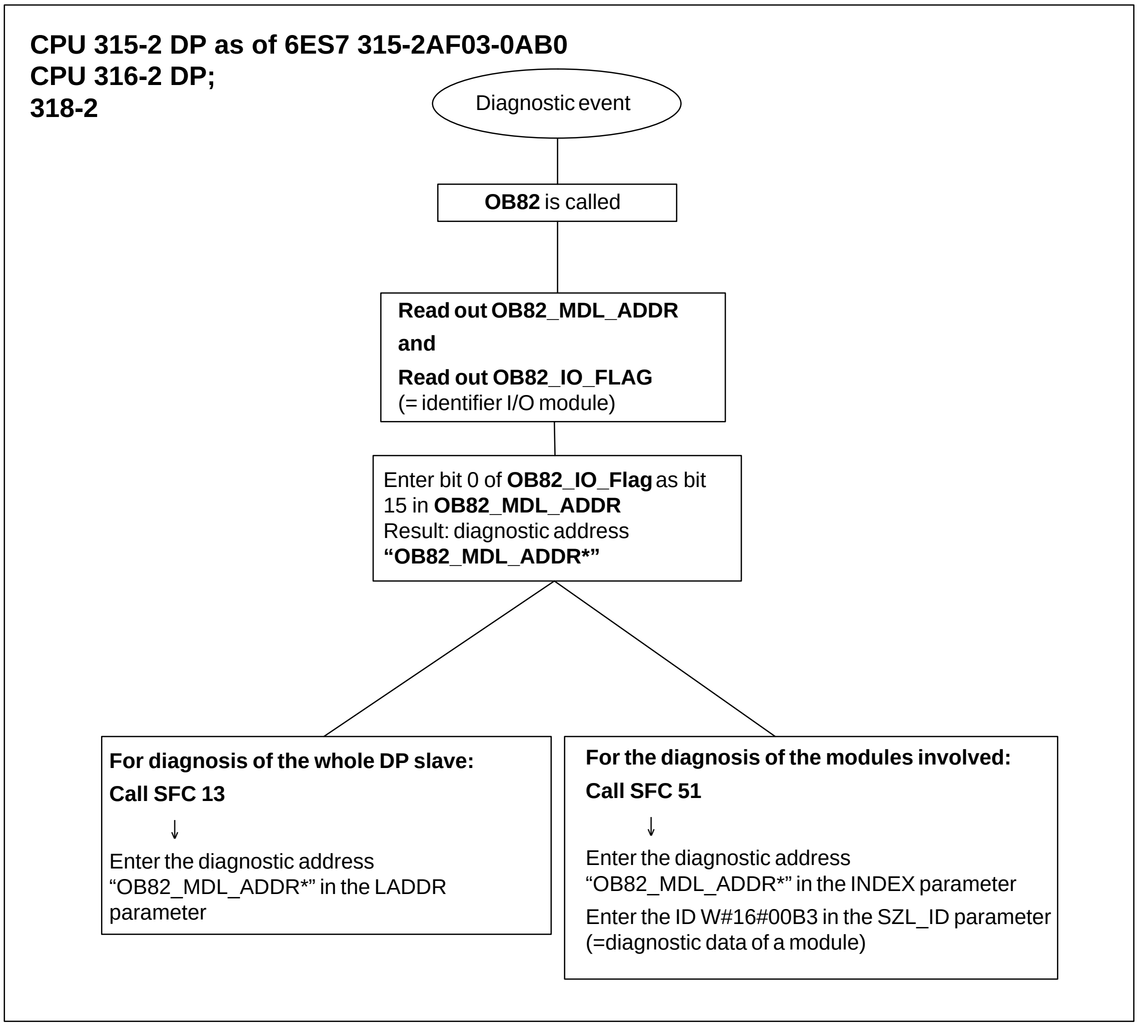


Figure 9-2 Diagnostics with CPU 31x-2 (315-2 DP as of 315-2AF**03**)

Diagnostic Addresses

With the CPU 31x-2 you assign diagnostic addresses for the PROFIBUS-DP bus system. Make sure during configuration that DP diagnostic addresses are assigned to both the DP master and the DP slave.

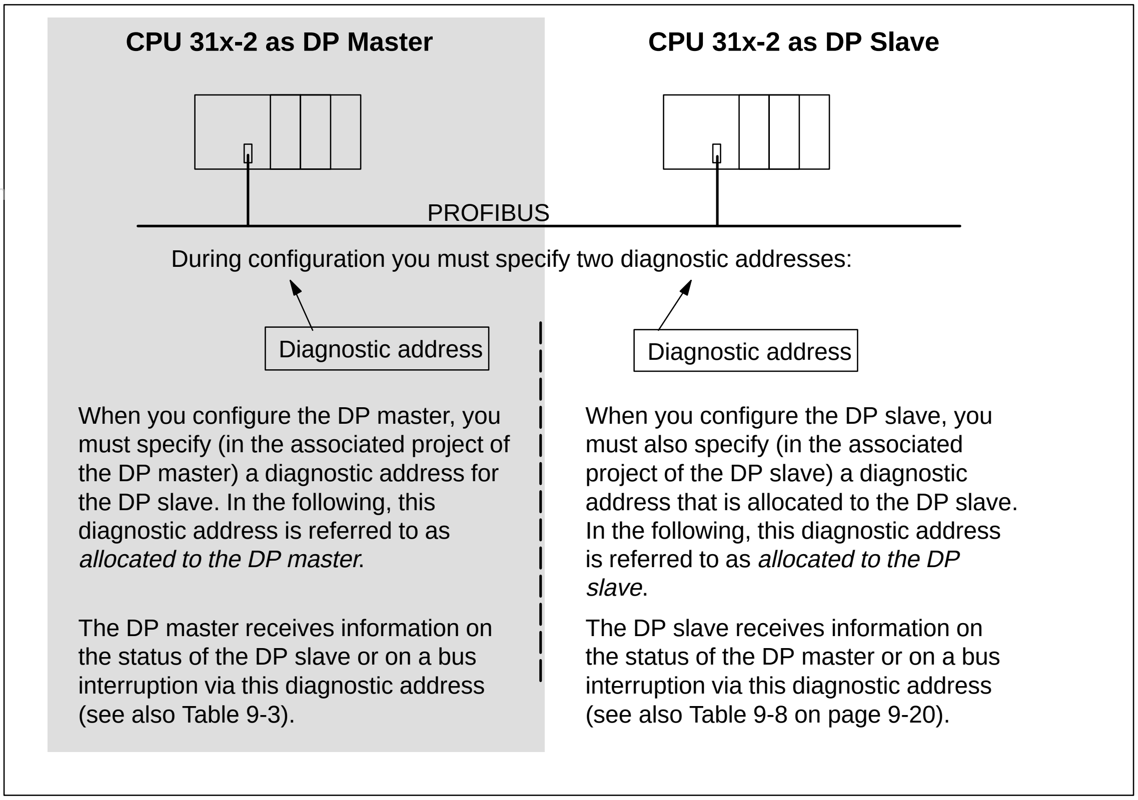


Figure 9-3 Diagnostic Addresses for DP Master and DP Slave

Event Detection

Table 9-3 shows how the CPU 31x-2 as DP master recognizes status changes in a CPU as DP slave or interruptions in data transfer.

Table 9-3 Event Detection of the CPU 31x-2 as DP Master

Event	What Happens in the DP Master
Bus interruption (short-circuit, plug pulled)	• OB 86 is called and a *station failure* reported (incoming event; Diagnostic address of the DP slave, assigned to the DP master) • With I/O access: OB 122 is called up (I/O access error)
DP slave: RUN → STOP	• OB 82 is called and *Module fault* reported (incoming event; Diagnostic address of the DP slave assigned to the DP master; Variable OB82_MDL_STOP=1)
DP slave: STOP → RUN	• OB 82 is called and *Module ok* reported. (outgoing event; diagnostic address of the DP slave assigned to the DP master; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

Table 9-4 shows you how you can, for example, evaluate RUN-STOP transitions of the DP slave in the DP master (see Table 9-3).

Table 9-4 Evaluating RUN-STOP Transitions of the DP Slaves in the DP Master

In the DP Master		In the DP Slave (CPU 31x-2 DP)
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**		Diagnostic addresses: (example) Slave diagnostic address=**422** Master diagnostic address=Irrelevant
The CPU calls OB 82 with the following information: • OB 82_MDL_ADDR:=**1022** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=Module fault Tip: This information is also in the CPU's diagnostic buffer In the user program, you should also include the SFC 13 "DPNRM_DG" to read out the DP slave diagnostic data.	←	CPU: RUN → STOP CPU generates a DP slave diagnostic frame (see Section 9.5.4).

9.4 CPU 31x-2 as DP Slave

Introduction

This section lists the characteristics and technical specifications for the CPU when it is operated as a DP slave.

The characteristics and technical specifications of the CPU as the “standard” CPU can be found in Section 8.

Prerequisites

Should the MPI/DP interface be a DP interface? If so, you must configure the interface as a DP interface.

Prior to start-up, the CPU must be configured as a DP slave. This means carrying out the following steps in *STEP 7*:

- “Switch on” the CPU as DP slave.
- Assign a PROFIBUS address.
- Assign a slave diagnostic address.
- Stipulate the address areas for data interchange with the DP master.

Device Master Files

You need a device master file to configure the CPU 31x-2 as a DP slave in a DP master system.
The device master file is included in *COM PROFIBUS* as of version 4.0.

If you are working with an older version or another configuration tool, you can get the device master file from the following sources:

- On the Internet at http://www.ad.siemens.de/csi_e/gsd

or

- Via modem from the **SSC** (Interface Center) Fuerth by calling +49/911/737972.

Programming, Modifying and Monitoring via the PROFIBUS

As an alternative to the MPI interface, you can program the CPU or execute the PG's Monitor and Modify functions via the PROFIBUS-DP interface. To do so, you must enable these functions when configuring the CPU as a DP slave in *STEP 7*.

Note

The use of Monitor and Modify via the PROFIBUS-DP interface lengthens the DP cycle.

Data Transfer Via an Intermediate Memory

The CPU 31x-2 provides an intermediate memory as DP slave for the PROFIBUS DP bus system. The data transfer between the CPU as DP slave and the DP master always takes place via this intermediate memory. You can configure up to 32 address areas for this.

This means that the DP master writes its data in these address areas in the intermediate memory and that the CPU reads this data in the user program and vice versa.

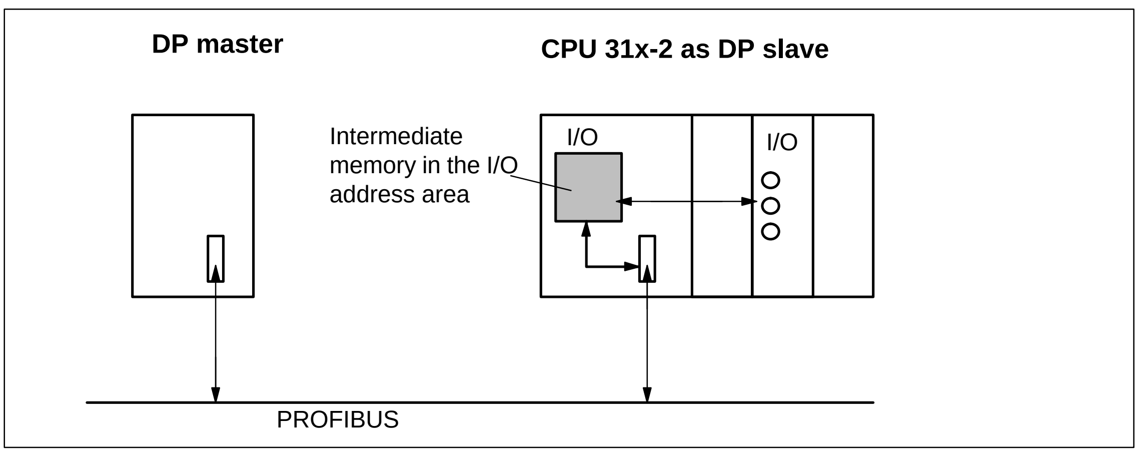


Figure 9-4 Intermediate Memory in the CPU 31x-2 as DP Slave

Address Areas of the Intermediate Memory

In *STEP 7* you configure input and output address areas:

- You can configure up to 32 input and output address areas.
- Each of these address areas can have up to 32 bytes.
- You can configure a maximum of 244 bytes for inputs and 244 bytes for outputs.

The following table shows the principle of address areas. You can also find this figure in the *STEP 7* configuration.

Table 9-5 Configuration Example for the Address Areas of the Intermediate Memory

	Type	Master Address	Type	Slave Address	Length	Unit	Consistency
1	E	222	A	310	2	Byte	Unit
2	A	0	E	13	10	Word	Total length
:							
32							
	Address areas in the DP master CPU		Address areas in the DP slave CPU		These address area parameters must be identical for DP master and DP slave		

Rules

The following rules must be followed when using the intermediate memory:

- Allocating the address areas:
  - Input data of the DP slave are **always** output data of the DP master
  - Output data of the DP slave are **always** input data of the DP master
- The addresses can be freely allocated. In the user program, access the data with Load/Transfer statements or with SFCs 14 and 15. You may also specify addresses from the process input or process output image (also see Section 3.2).

Note

You assign addresses for the intermediate memory from the DP address area of the CPU 31x-2.

You cannot assign addresses already allocated to the intermediate memory to the I/O modules in the CPU 31x-2!

- The lowest address in any given address area is that address area's start address.
- The length, unit and consistency of the address areas for DP master and DP slave must be identical.

S5 DP Master

If you are using an IM 308 C as a DP master and the CPU 31x-2 as a DP slave, the exchange of consistent data requires the following:

In the IM 308 C, you must program FB 192 to enable the exchange of consistent data between DP master and DP slave. With FB 192, the data of the CPU 31x-2 data is output or read out contiguously only in a single block.

S5-95 as a DP master

If you are using an AG S5-95 as a DP master, you must also set its bus parameters for the CPU 31x-2 as a DP slave.

Sample Program

Below you will see a small sample program for the exchange of data between DP master and DP slave. The addresses used in the example are those from Table 9-5.

In the DP Slave CPU	In the DP Master CPU
L 2 — Data preprocessing in DP slave T MB 6 L IB 0 T MB 7	
L MW 6 — Forward data to DP master T PQW 310	
	L PIB 222 — Postprocess receive data in DP master T MB 50 L PIB 223 L B#16#3 + I T MB 51
	L 10 — Data Processing in DP master + 3 T MB 60
	CALL SFC 15 — Send data to DP slave LADDR:= W#16#0 RECORD:= P#M60.0 Byte20 RET_VAL:=MW 22
CALL SFC 14 — Receive data from DP master LADDR:=W#16#D RET_VAL:=MW 20 RECORD:=P#M30.0 Byte20	
L MB 30 — Postprocess receive data L MB 7 + I T MW 100	

Data Transfer in STOP Mode

The DP slave CPU goes into STOP mode: The data in the intermediate memory of the CPU is overwritten with “0”. In other words, the DP master reads “0”.

The DP master goes into STOP mode: The current data in the intermediate memory of the CPU is preserved and can still be read by the CPU.

PROFIBUS address

You cannot set the 126 as the PROFIBUS address for the CPU 31x-2.

9.5 Diagnostics of the CPU 31x-2 as DP Slave

In This Section

9.5.1 Diagnosis with LEDs

Diagnosis with LEDs – CPU 31x-2

Table 9-6 explains the meaning of the BUSF LEDs.
The BUSF LED assigned to the interface configured as the PROFIBUS-DP interface will always come on or flash.

Table 9-6 Meaning of the BUSF LEDs in the CPU 31x-2 as DP Slave

BUSF	Description	Remedy
LED off	Configuring OK.	–
LED flashes	The CPU 31x-2 is incorrectly parameterized. There is no data interchange between the DP master and the CPU 31x-2. Reasons: • Timeout. • Bus communication via PROFIBUS interrupted. • Incorrect PROFIBUS address.	• Check the CPU 31x-2. • Check to make sure that the bus connector is properly inserted. • Check for interruptions in the bus cable to the DP master. • Check configuring data and parameters.
LED on	• Short-circuit on bus.	• Check the bus configuration.

9.5.2 Diagnosis with *STEP 5* or *STEP 7*

Slave Diagnosis

The slave diagnosis complies with EN 50170, Volume 2, PROFIBUS. Depending on the DP master, the diagnosis can be read for all DP slaves that comply with the standard using *STEP 5* or *STEP 7*.

The following sections describe how the slave diagnosis is read and structured.

S7 Diagnosis

An S7 diagnosis can be requested for all the modules in the SIMATIC S7/M7 range of modules in the user program. The structure of the S7 diagnostic data is the same for both central and distributed modules.

The diagnostic data of a module is in data records 0 and 1 of the system data area of the module. Data record 0 contains 4 bytes of diagnostic data describing the current state of a module. The data record 1 also contains module-specific diagnostic data.

You can find out how to configure the diagnostic data in the *System and Standard Functions* Reference Manual.

9.5.3 Reading Out the Diagnostic Data

Table 9-7 Reading Out the Diagnostic Data with *STEP 5* and *STEP 7* in the Master System

Programmable Controller with DP Master	Block or Register in *STEP 7*	Application	See...
SIMATIC S7/M7	DP slave diagnosis register	Displaying slave diagnosis as plain text to the *STEP 7* surface	See the section on hardware diagnostics in the *STEP 7* online help system and in the *STEP 7* User Manual
	SFC 13 “DP NRM_DG”	Reading out slave diagnosis (store in the data area of the user program)	See Section 9.5.4; SFC: see *System and Standard Functions* Reference Manual
	SFC 51 “RDSYSST”	Reading out system state sublist. In the diagnostic interrupt alarm with the system state list ID W#16#00B4, calling SFC 51 and reading out the system state list of the slave CPU.	*System and Standard Functions* Reference Manual
	SFC 59 “RD_REC”	Reading out data records of the S7 diagnosis (store in the data area of the user program)	
	FB 99/FC 99	Evaluating slave diagnosis	On the Internet at http://www.ad.siemens.de/simatic-cs ID 387 257
SIMATIC S5 with IM 308-C as DP master	FB 192 “IM308C”	Reading out slave diagnosis (store in the data area of the user program)	Configuration – see Section 9.5.4 FBs – see *ET 200 Distributed I/O Device* Manual
SIMATIC S5 with S5-95U programmable controller as DP master	FB 230 “S_DIAG”		

Example of Reading Out the Slave Diagnosis with FB 192 “IM 308C”

Here you will find an example of how to use FB 192 to read out the slave diagnosis for a DP slave in the *STEP 5* user program.

Assumptions

The following assumptions are made for this *STEP 5* user program:

- As a DP master, the IM 308-C occupies the page frames 0... 15 (number 0 of the IM 308-C).
- The DP slave has the PROFIBUS address 3.
- The slave diagnosis should be stored in data block 20. You can also use any data block for this.
- The slave diagnosis consists of 26 bytes.

STEP 5 User Program

STL			Description
	:A	DB 30	
	:SPA	FB 192	
Name	:IM308C		
DPAD	:	KH F800	Default address area of the IM 308-C
IMST	:	KY 0, 3	IM no. = 0, PROFIBUS address of the DP slave = 3
FCT	:	KC SD	Function: Read slave diagnosis
GCGR	:	KM 0	Not evaluated
TYP	:	KY 0, 20	S5 data area: DB 20
STAD	:	KF +1	Diagnostic data as of data word 1
LENG	:	KF 26	Length of dignostic data = 26 bytes
ERR	:	DW 0	Error code storage in DW 0 of the DB 30

Example of Reading Out the S7 Diagnosis with SFC 59 “RD_REC”

Here you will find an example of how to use the SFC 59 to read out the data records of the S7 diagnosis for a DP slave in the *STEP 7* user program. Reading out the slave diagnosis with SFC 13 is similar.

Assumptions

The following assumptions are made for this *STEP 7* user program:

- The diagnosis for the input module with the address $FFFF_H$ is to be read out.
- Data record 1 is to be read out.
- Data record 1 is to be stored in DB 10.

STEP 7 User Program

STL	Description
CALL SFC 59	
REQ :=TRUE	Request to Read
IOID :=B#16#54	Identifier of the Address Area, here the I/O input
LADDR :=W#16#FFFF	Logical address of the module
RECNUM :=B#16#1	Data record 1 is to be read out
RET_VAL :=	Errors result in the output of an error code
BUSY :=TRUE	Reading process is not finished
RECORD :=DB 10	Destination area for the read data record 1 is data block 10

Diagnostic Addresses

With the CPU 31x-2, you assign diagnostic addresses for the PROFIBUS-DP bus system. During configuration, make sure that DP diagnostic addresses are assigned to both the DP master and the DP slave.

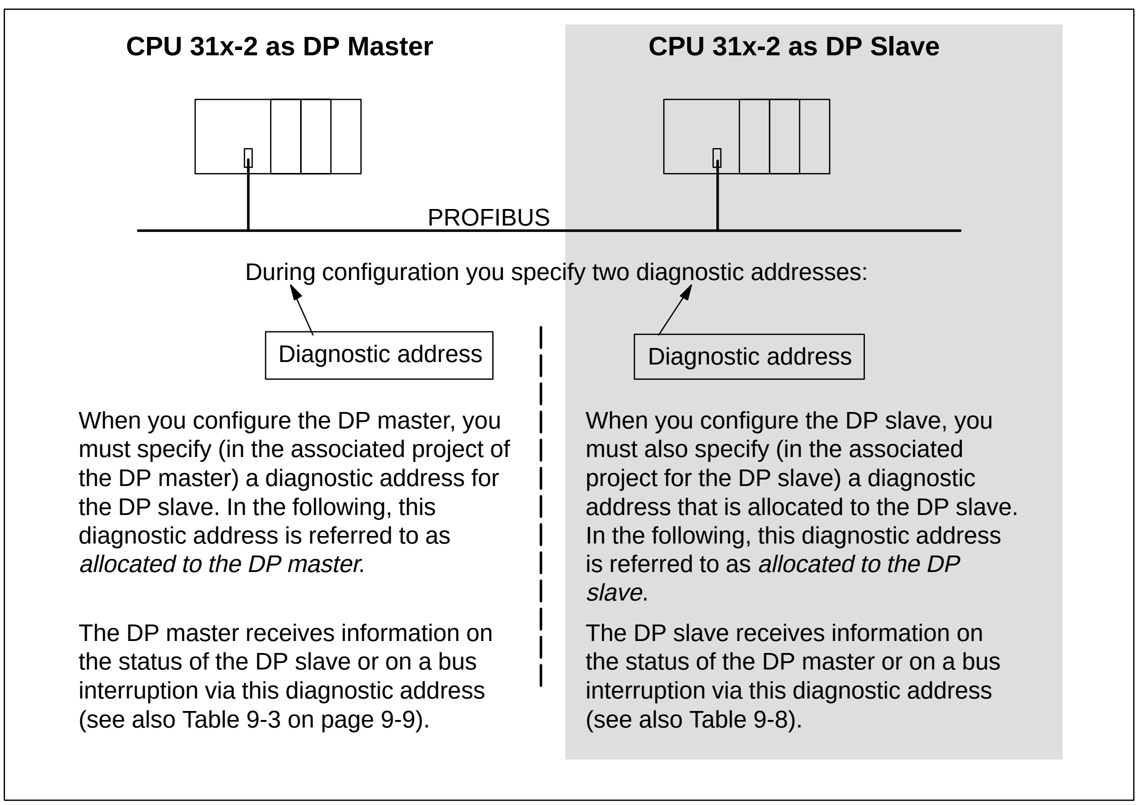


Figure 9-5 Diagnostic Addresses for DP Master and DP Slave

Event Detection

Table 9-8 shows how the CPU 31x-2 as DP slave recognizes status changes or interruptions in the transfer of data.

Table 9-8 Event Detection of the CPU 31x-2 as DP Slave

Event	What Happens in the DP Slave
Bus interruption (short-circuit, plug pulled)	• OB 86 is called and *Station failure* reported (incoming event; diagnostic address of the DP slave assigned to the DP slave) • In the case of I/O access: OB 122 is called (I/O access error)
DP master: RUN → STOP	• OB 82 is called and *Module fault* reported (incoming event; diagnostic address of the DP slave assigned to the DP slave) Variable OB82_MDL_STOP=1)
DP master: STOP → RUN	• OB 82 is called and *Module ok* reported. (outgoing event; diagnostic address of the DP slave assigned to the DP slave) Variable OB82_MDL_STOP=0)

Evaluation in the User Program

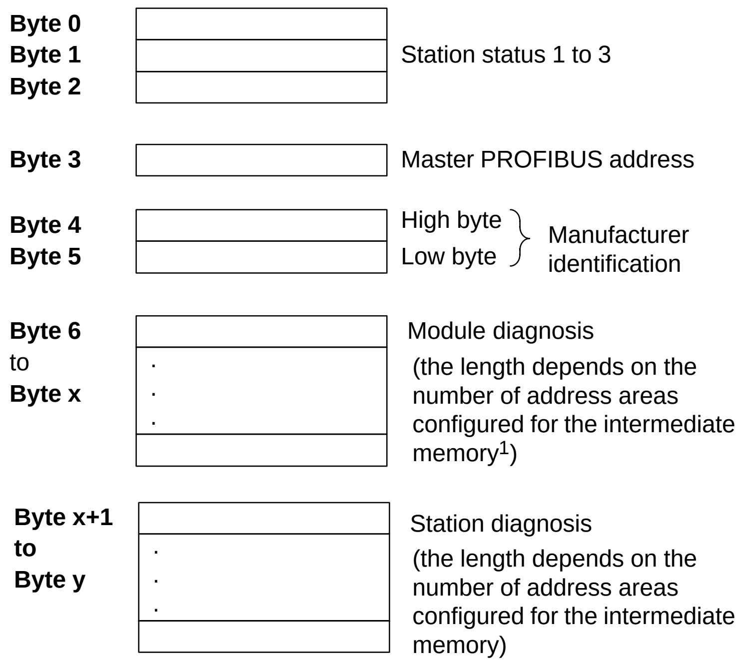
Table 9-9 shows you how you can, for example, evaluate RUN-STOP transitions of the DP master in the DP slave (see Table 9-8).

Table 9-9 Evaluating RUN-STOP Transitions in the DP Master/DP Slave

In the DP Master	In the DP Slave
Diagnostic addresses: (sample) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**	Diagnostic addresses: (example) Slave diagnostic address=**422** Master diagnostic address=not relevant
CPU: RUN → STOP →	The CPU calls OB 82 with the following information: • OB 82_MDL_ADDR:=**422** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=module fault Tip: This information is also in the CPU's diagnostic buffer

9.5.4 Structure of the Slave Diagnostic Data

Structure of the Slave Diagnostic Data



[1] Exception: If the DP master is incorrectly configured, the DP slave interprets 35 configured address areas (46_H).

Figure 9-6 Structure of the Slave Diagnostic Data

9.5.5 Station Status 1 to 3

Definition

Station status 1 to 3 provides an overview of the status of a DP slave.

Station Status 1

Table 9-10 Structure of Station Status 1 (Byte 0)

Bit	Description	Remedy
0	1: DP slave **cannot** be addressed by DP master.	• Is the correct DP address set on the DP slave? • Is the bus connector inserted? • Does the DP slave have power? • Is the RS 485 repeater correctly set? • Execute a Reset on the DP slave.
1	1: DP slave is not ready for data interchange.	• Wait; the DP slave is still doing its run-up.
2	1: The configuration data which the DP master sent to the DP slave do not correspond with the DP slave's actual configuration.	• Was the software set for the right station type or the right DP slave configuration?
3	1: Diagnostic interrupt, generated by a RUN/STOP transition on the CPU 0: Diagnostic interrupt, generated by a STOP/RUN transition on the CPU	• You can read out the diagnostic data.
4	1: Function is not supported, for instance changing the DP address at the software level.	• Check the configuring data.
5	0: This bit is always "0".	–
6	1: DP slave type does not correspond to the software configuration.	• Was the software set for the right station type? (parameter assignment error)
7	1: DP slave was parameterized by a different DP master to the one that currently has access to it.	• Bit is always "1" when, for instance, you are currently accessing the DP slave via the PG or a different DP master. The DP address of the master that parameterized the slave is located in the "Master PROFIBUS address" diagnostic byte.

Station Status 2

Table 9-11 Structure of Station Status 2 (Byte 1)

Bit	Description
0	1: DP slave must be parameterized again and reconfigured.
1	1: A diagnostic message has arrived. The DP slave cannot continue operation until the error has been rectified (static diagnostic message).
2	1: This bit is always “1” when there is a DP slave with this DP address.
3	1: The watchdog monitor has been activated for this DP slave.
4	0: This bit is always “0”.
5	0: This bit is always “0”.
6	0: This bit is always “0”.
7	1: DP slave is deactivated, that is to say, it has been removed from the scan cycle.

Station Status 3

Table 9-12 Structure of Station Status 3 (Byte 2)

Bit	Description
0 to 6	0: These bits are always “0”.
7	1: • More diagnostic messages have arrived than the DP slave can buffer. • The DP master cannot enter all the diagnostic messages sent by the DP slave in its diagnostic buffer.

9.5.6 Master PROFIBUS Address

Definition

The DP address of the DP master is stored in the master PROFIBUS address diagnostic byte:

- The master that parameterized the DP slave
- The master that has read and write access to the DP slave

Master PROFIBUS address

Table 9-13 Structure of the Master PROFIBUS Address (Byte 3)

Bit	Description
0 to 7	DP address of the DP master that parameterized the DP slave and has read/write access to that DP slave.
	FF_H: DP slave was not parameterized by a DP master.

9.5.7 Manufacturer ID

Definition

The manufacturer identification contains a code specifying the DP slave's type.

Manufacturer Identification

Table 9-14 Structure of the Manufacturer Identification (Bytes 4 and 5)

Byte 4	Byte 5	Manufacturer Identification for
80_H	2FH	CPU 315-2 DP
80_H	$6F_H$	CPU 316-2 DP
80_H	$7F_H$	CPU 318-2

9.5.8 Module Diagnosis

Definition

The module diagnosis specifies which of the configured address areas of the intermediate memory an input has been made for.

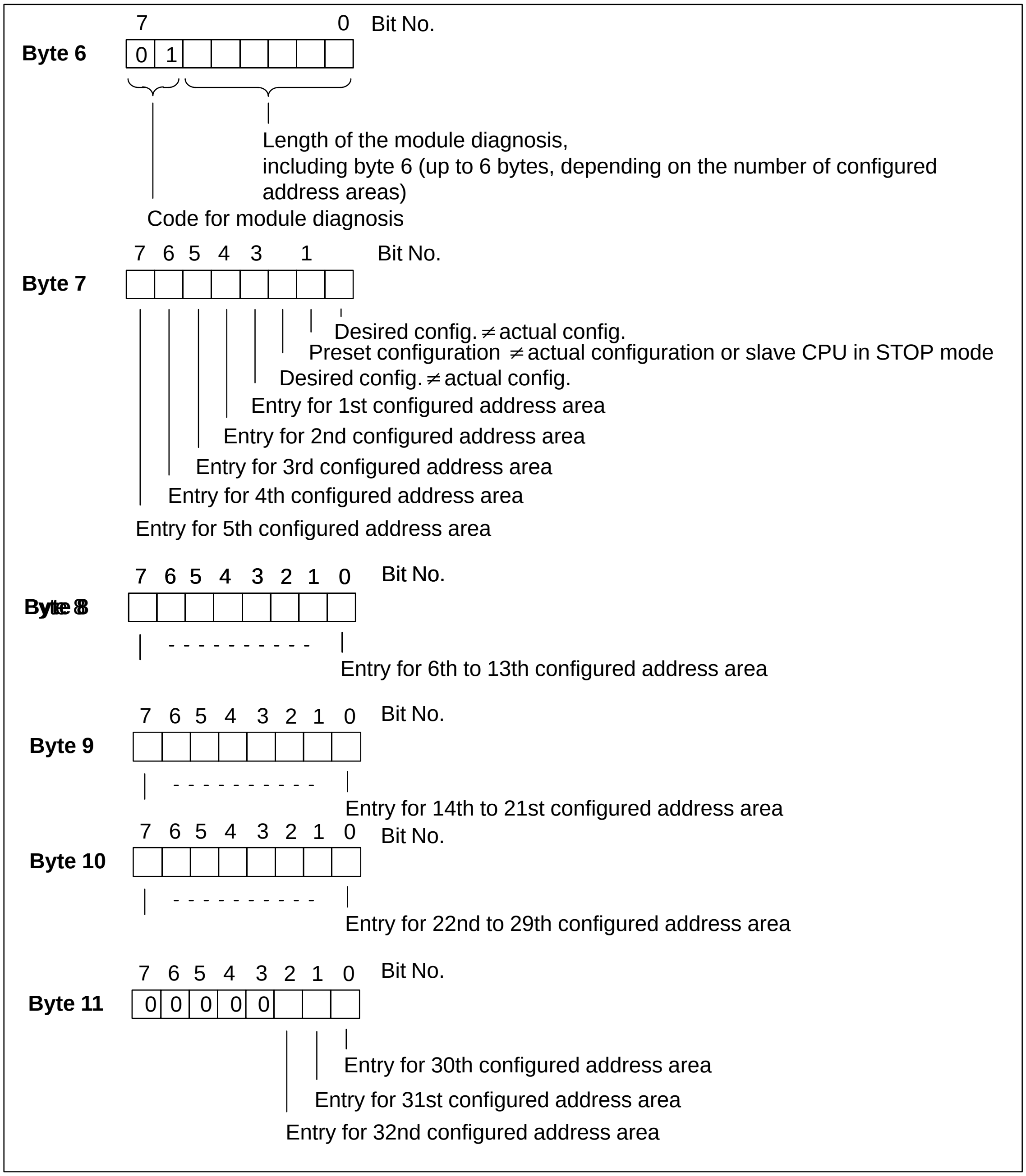


Figure 9-7 Structure of the Module Diagnosis of the CPU 31x-2

9.5.9 Station Diagnosis

Definition

The station diagnosis gives detailed information on a DP slave. The station diagnosis begins as of byte x and can have a maximum of 20 bytes.

Station Diagnosis

The following figure describes the structure and content of the bytes for a configured address area of the intermediate memory.

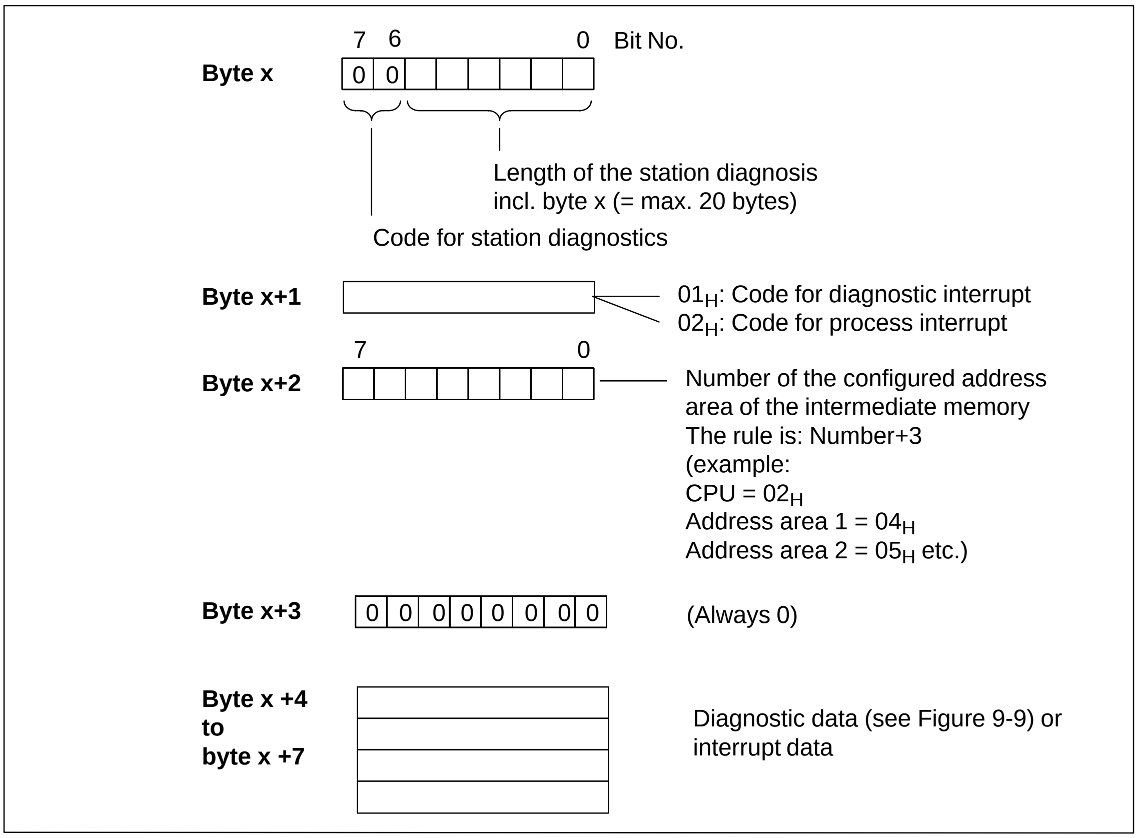


Figure 9-8 Structure of the Station Diagnosis

As of byte x +4

The purpose of the bytes beginning with byte x+4 depends on byte x+1 (see Figure 9-8).

Byte x+1 Contains the Code for...	
Diagnostic Interrupt (01_H)	**Process Interrupt (02_H)**
The diagnostic data contain the 16 bytes of status information from the CPU. Figure 9-9 shows the contents of the first four bytes of diagnostic data. The next 12 bytes are always 0.	For a process interrupt, you can program four bytes of interrupt information. These four bytes are forwarded to the DP master in *STEP 7* with the SFC 7 command “DP_PRAL” (see Section 9.5.10).

Bytes x+4 to x+7 for Diagnostic Interrupts

Figure 9-9 shows the configuration and contents of bytes x +4 to x +7 for diagnostic interrupt. The contents of these bytes correspond to the contents of data record 0 of the diagnostic data in *STEP 7* (in this case, not all bits are assigned).

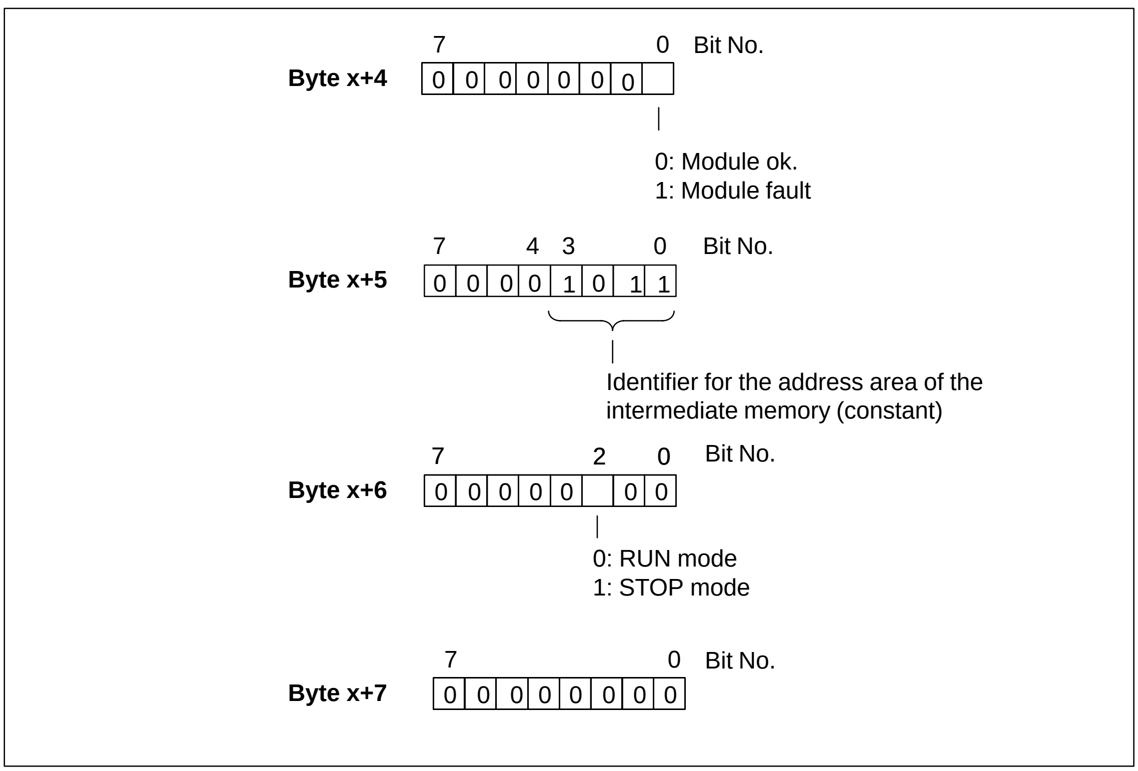


Figure 9-9 Bytes +4 to +7 for Diagnostic and Process Interrupts

9.5.10 Interrupts

Interrupts with the S7/M7 DP Master

In the CPU 31x-2 as DP slave you can trigger a process interrupt in the DP master from the user program. OB 40 is called in the DP master's user program by calling SFC 7 "DP_PRAL". SFC 7 allows you to forward interrupt information in a doubleword to the DP master; this information can then be evaluated in OB 40 in variable OB40_POINT_ADDR. You can program the interrupt information as desired. A detailed description of SFC 7 "DP_PRAL" can be found in the reference manual entitled *System Software S7-300/400 - System and Standard Functions*.

Interrupts with Another DP Master

If you are running the CPU 31x-2 with another DP master, these interrupts are reflected in the station diagnosis of the CPU 31x-2. You must postprocess the relevant diagnostic events in the DP master's user program.

Note

Note the following in order to be able to evaluate diagnostic interrupts and process interrupts via the device-related diagnostics when using a different DP master:

- The DP master should be able to store the diagnostic messages, that is, the DP master should have a ring buffer in which to place these messages. If the DP master can not store diagnostic messages, only the last diagnostic message would be available for evaluation.
- You must scan the relevant bits in the device-related diagnostic data in your user program at regular intervals. You must also take the PROFIBUS-DP's bus cycle time into consideration so that you can scan the bits at least once in sync with the bus cycle time, for example.
- When using an IM 308-C as DP master, you can not utilize process interrupts in device-related diagnostics, as only incoming interrupts can be signaled, not outgoing interrupts.

9.6 Parameter Assignment Frame and Configuration Frame

With *STEP 7*

When you configure and parameterize the address areas of the intermediate memory of the CPU 31x-2 with *STEP 7*, *STEP 7* and the online help system support you.

With *COM PROFIBUS*

When you configure and parameterize the address areas of the intermediate memory of the CPU 31x-2 with *COM PROFIBUS* V 4.0, *COM PROFIBUS* and the online help system support you.

Configuration/Parameterization

When you enter the address areas of the intermediate memory of the CPU 31x-2 using a configuration frame and a parameter assignment frame, e.g. CP 342-5 in an S7-300 or CP 5431 as DP master or another DP master, you will find the structure of the configuration frame and the parameter assignment frame in the following sections.

In This Section

The following section contains all the information you need to configure and parameterize the address areas of the intermediate memory with a software tool.

9.6.1 Structure of the Parameter Assignment Frame

Definition: Parameter Assignment Frame

All the values of a DP slave that can be parameterized are stored in the parameter assignment frame. The length of the parameter assignment frame may not exceed 178 bytes.

Structure of the Parameter Assignment Frame

The length of the parameter assignment frame for the CPU 31x-2 is 10 bytes:

- Standardized portion (bytes 0 to 6)
- Parameters of the CPU 31x-2 (bytes 7 to 9).

Standard Part

The first seven bytes of the parameter assignment frame are standardized to EN 50170; for the CPU 315-2, for example, they can have the following contents:

Byte 0	88_H	Station status
Byte 1	01_H	WD factor 1
Byte 2	06_H	WD factor 2
Byte 3	$0B_H$	T_{RDY}
Byte 4	80_H	Manufacturer identification high byte
Byte 5	$2F_H$	Manufacturer identification low byte
Byte 6	00_H	Group identification

Figure 9-10 Standardized Portion of the Parameter Assignment Frame (Example)

Configuration of the Parameters for the CPU 31x-2

The length of the parameters for the CPU 31x-2 is 3 bytes: The default assignment for these 3 bytes is: $C0_H$ 60_H 00_H.

The parameters have the following meanings:

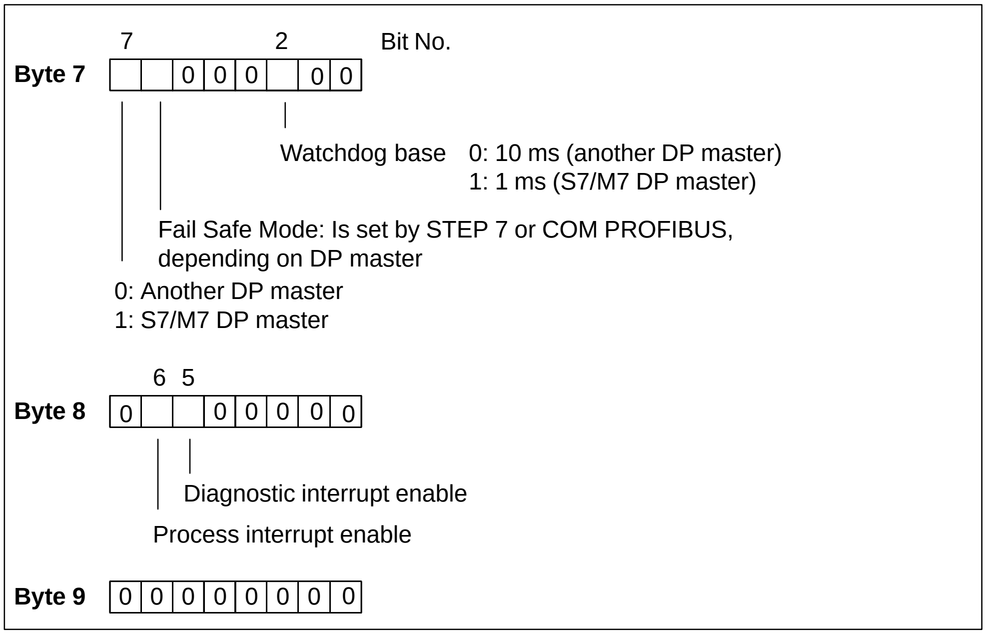


Figure 9-11 Parameters for the CPU 31x-2

9.6.2 Structure of the Configuration Frame (S7 Format)

Structure of the Configuration Frame

The length of the configuration frame depends on the number of address areas configured for the CPU's intermediate memory. The first 15 bytes in the configuration frame are reserved. The format of the configuration frame is as follows:

Table 9-15 Structure of the Configuration Frame

Configured Address Area	Byte				
	n	n + 1	n + 2	n + 3	n + 4
These bytes are reserved:	04	00	00	AD	C4
	04	00	00	8B	41
	04	00	00	8F	C0
1st configured address area (n = 15)	See Table 9-16				
2nd configured address area (n = 20)					
...					
32nd configured address area (n = 170)					

Identifiers for the Address Areas

The identifiers for configuring depend on the type of the address area. Table 9-16 lists all the identifiers for the address areas.

Table 9-16 Identifiers for the Address Areas of the Intermediate Memory

Address Area	Identifiers (hexadecimal)				
	Special identifier format	Length byte	Manufacturer-specific data Comment length = 3		
	Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
Input	See Figure 9-12	See Figure 9-13	00_H	83_H	40_H
Output			00_H	93_H	40_H

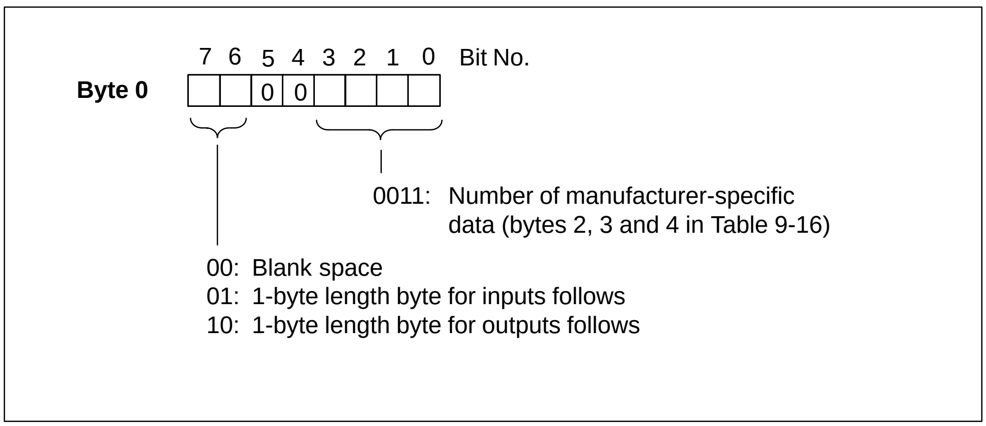


Figure 9-12 Description of Byte 0 of the CPU's Address Area Identifiers

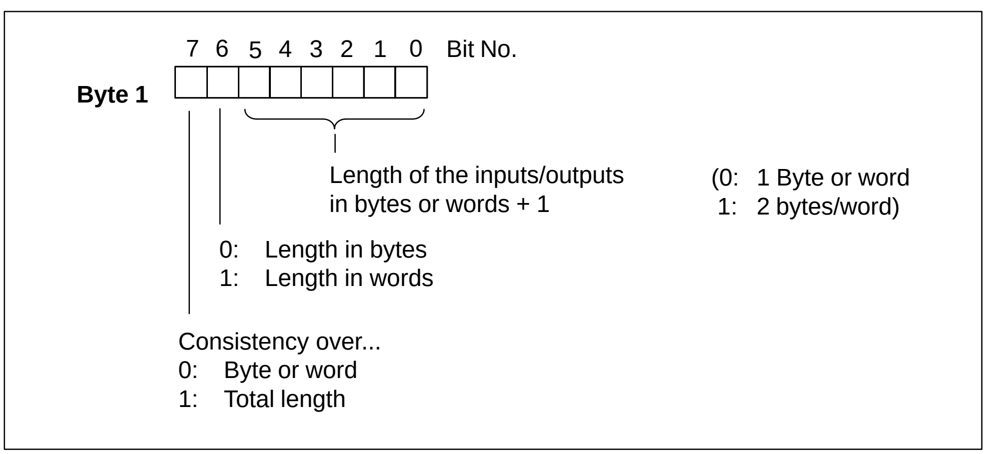


Figure 9-13 Description of Byte 1 of the CPU's Address Area Identifiers

Example of a Configuration Frame

Below is a sample configuration frame for the CPU 315-2 DP.

Format:

- A power supply module
- The CPU 315-2 DP
- An address area in the DP master (= output address area in the DP slave), two bytes in length and with consistency over the entire area

The configuration frame thus comprises 20 bytes and looks like this:

04 00 00 AD C4	04 00 00 8B 41	04 00 00 8F C0	43 81 00 83 40
Permanent value	Permanent value	Permanent value	1st configured input address area of the CPU's intermediate memory

9.6.3 Structure of the Configuration Frame for Non-S7 DP Masters

Type/Device Master File

If your DP master does not support the configuration frame in S7 format (see Section 9.6.2), you can obtain a type/device master file in non-S7 format by calling the **SSC** (Interface Center) Fuerth.

The device master file can be obtained via modem from the **SSC** (Interface Center) Fuerth by calling +49/911/737972.

Structure of the Configuration Frame

The length of the configuration frame depends on the number of address areas configured for the CPU’s intermediate memory. The first three bytes of the configuration frame are always “0”. The format of the configuration frame is as follows:

In this format, you can only configure a length of no more than 16 bytes or 16 words. For a length of 32 bytes, you would thus have to configure a length of 16 words.

Table 9-17 Structure of the Configuration Frame for Non-S7 DP Masters

Configured Address Areas	Byte
1.	0 0 0 0 0 0 0 0
2.	0 0 0 0 0 0 0 0
3.	0 0 0 0 0 0 0 0
4. : : 32nd	7 6 5 4 3 2 1 0 Bit No. in bytes or words Bits 3–0: Length of the inputs/outputs in bytes or words Bits 5–4: 01: Inputs; 10: Outputs Bit 6: 0: Length in bytes; 1: Length in words Bit 7: Consistency over... 0: Byte or word; 1: Total length

9.7 Direct Communication

As of *STEP 7* V 5.x you can configure direct communication for PROFIBUS nodes. The CPU 31x-2 can take part in direct communication as the sender or receiver.

Direct communication is a special communication relationship between PROFIBUS-DP nodes.

Principle

Direct communication is characterized by the fact that the PROFIBUS-DP nodes listen in to find out which data a DP slave is sending back to its DP master. Using this function the eavesdropper (receiver) can directly access changes in the input data of remote DP slaves.

During configuration in *STEP 7*, in addition to defining the relevant I/O input addresses, you can also define which of the receiver's address areas the required data from the sender will be read to.

A CPU 31x-2 can be one of the following:

Sender	as DP slave
Receiver	as DP slave or DP master or as CPU not included in a master system (see Figure 9-14).

Example

Figure 9-14 gives you an example of the direct communication relationships you can configure. In the figure all the DP masters and DP slaves are CPU 31x-2s. Note that other DP slaves (ET 200M, ET 200X, ET 200S) can only be senders.

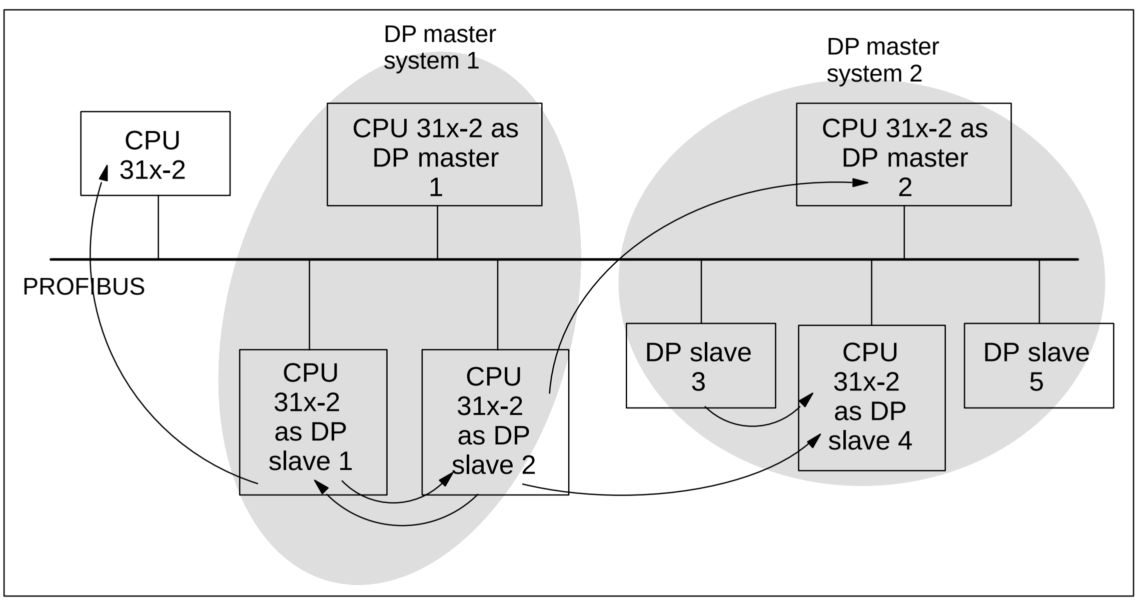


Figure 9-14 Direct Communication with CPU 31x-2

9.8 Diagnostics in Direct Communication

Diagnostic Addresses

In direct communication you allocate a diagnostic address in the receiver:

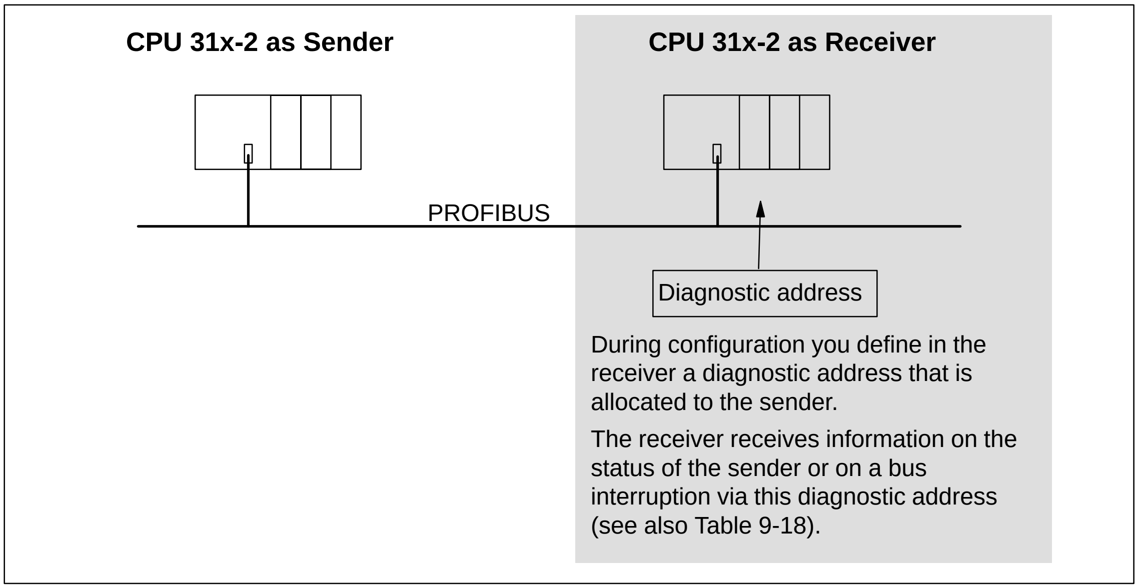


Figure 9-15 Diagnostic Address for the Receiver During Direct Communication

Event Detection

Table 9-18 shows how the CPU 31x-2 as receiver detects interruptions in the transfer of data.

Table 9-18 Event Detection of the CPU 31x-2 as Receiver During Direct Communication

Event	What Happens in the Receiver
Bus interruption (short-circuit, plug pulled)	• OB 86 is called and *Station failure* reported (incoming event; diagnostic address of the receiver, assigned to the sender) • In the case of I/O access: OB 122 is called (I/O access error)

Evaluation in the User Program

Table 9-19 shows you how you can, for example, evaluate the station failure of the sender in the receiver (see also Table 9-18).

Table 9-19 Evaluation of the Station Failure of the Sender During Direct Communication

In the Sender	In the Receiver
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**	Diagnostic address: (example) Diagnostic address=**444**
Station failure →	The CPU calls OB 86 with the following information: • OB 86_MDL_ADDR:=**444** • OB86_EV_CLASS:=B#16#38 (incoming event) • OB86_FLT_ID:=B#16#C4 (failure of a DP station) Tip: This information is also in the CPU's diagnostic buffer

Cycle and Response Times of the S7-300 10

Introduction

In this section, we explain what the cycle time and the response time of the S7-300 consist of.

You can use the programming device to read out the cycle time of your user program on the CPU (see the *STEP 7 online help system*).

The example below shows you how to calculate the cycle time.

The response time is more important for the process. In this chapter we will show you in detail how to calculate the response time.

In This Chapter

Further Information

You will find further information on the processing times in ...

- ... the *S7-300 instruction list*. There you will find all the *STEP 7* instructions which can be processed on the various CPUs, together with their execution time.
- ....see Appendix C. Here you will find a list of all the SFCs/SFBs integrated in the CPUs, as well as the *STEP 7* IEC functions and their execution times.

10.1 Cycle Time

Cycle Time – A Definition

The cycle time is the time that elapses during one program cycle.

Component Parts of the Cycle Time

The cycle time comprises:

Factors	Remarks
Operating system execution time	See Section 10.2
Process image transfer time (PII and PIQ)	
User program execution time	Can be calculated on the basis of the execution times of the individual instructions (see the *S7-300 Instruction List*) and a CPU-specific factor (see Table 10-3)
S7 timer (not in the case of the CPU 318-2)	See Section 10.2
PROFIBUS DP	
Integrated functions	
Communication via the MPI	You parameterize the maximum permissible cycle load produced by communication in percent in *STEP 7*
Loading through interrupts	See Sections 10.4 and 10.5

Figure 10-1 shows the component parts of the cycle time

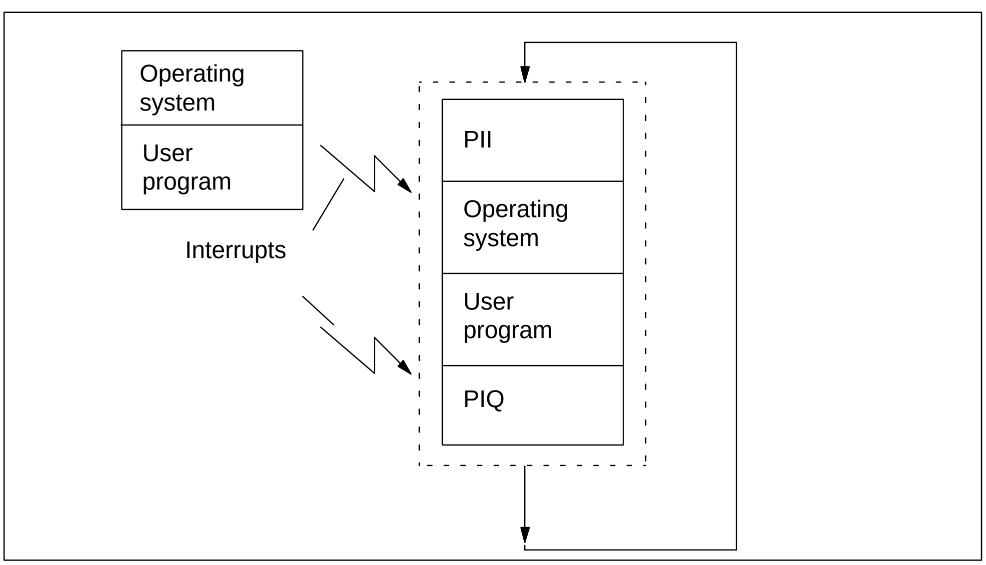


Figure 10-1 Component Parts of the Cycle Time

Extending the Cycle Time

Note that the cycle time of a user program is extended by the following:

- Time-controlled interrupt handling
- Process interrupt handling (see also Section 10.4)
- Diagnostics and error handling (see also Section 10.4)
- Communication via MPI

10.2 Response Time

Response Time – A Definition

The response time is the time between detection of an input signal and modification of an associated output signal.

Factors

The response time depends on the cycle time and the following factors:

Factors	Remarks
Delay of the inputs and outputs	The delay times are given in the technical specifications • In the *Module Specifications* Reference Manual for the signal modules • In Section 8.4.1 for the integrated inputs/outputs of the CPU 312 IFM. • In Section 8.4.4 for the integrated inputs/outputs of the CPU 314 IFM.
Additional bus runtimes on the PROFIBUS subnet	CPU 31x-2 DP only

Range of Fluctuation

The actual response time lies between a shortest and a longest response time. You must always reckon on the longest response time when configuring your system.

The shortest and longest response times are considered below to let you get an idea of the width of fluctuation of the response time.

Shortest Response Time

Figure 10-2 shows you the conditions under which the shortest response time is reached.

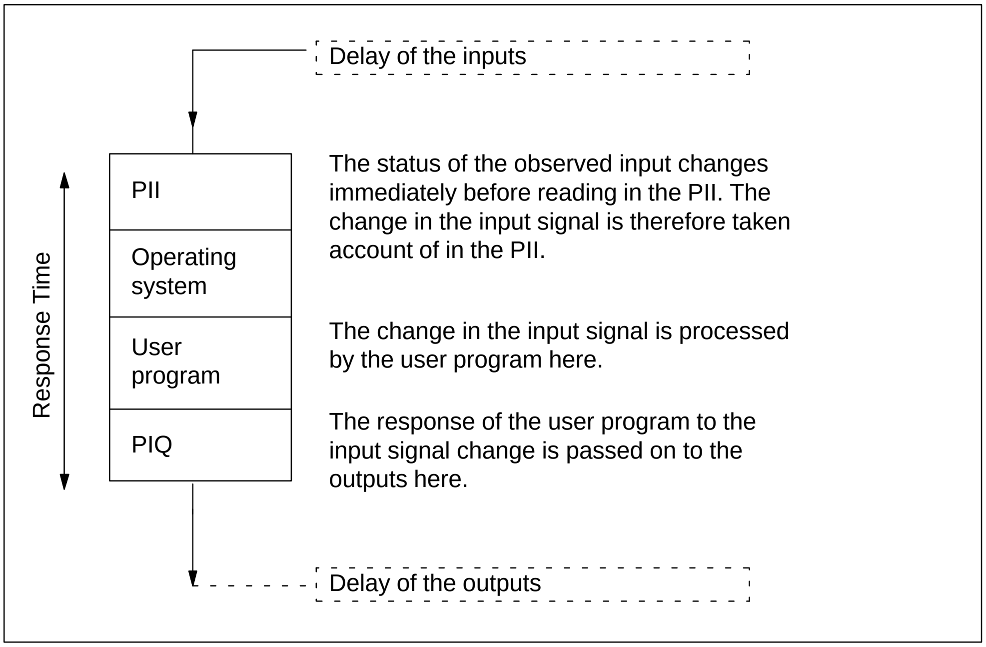


Figure 10-2 Shortest Response Time

Calculation

The (shortest) response time consists of the following:

- 1 × process image transfer time for the inputs +
- 1 × operating system execution time +
- 1 × program execution time +
- 1 × process image transfer time for outputs +
- Execution time of S7 timer
- Delay of the inputs and outputs

This corresponds to the sum of the cycle time and the delay of the inputs and outputs.

Longest Response Time

Figure 10-3 shows the conditions that result in the longest response time.

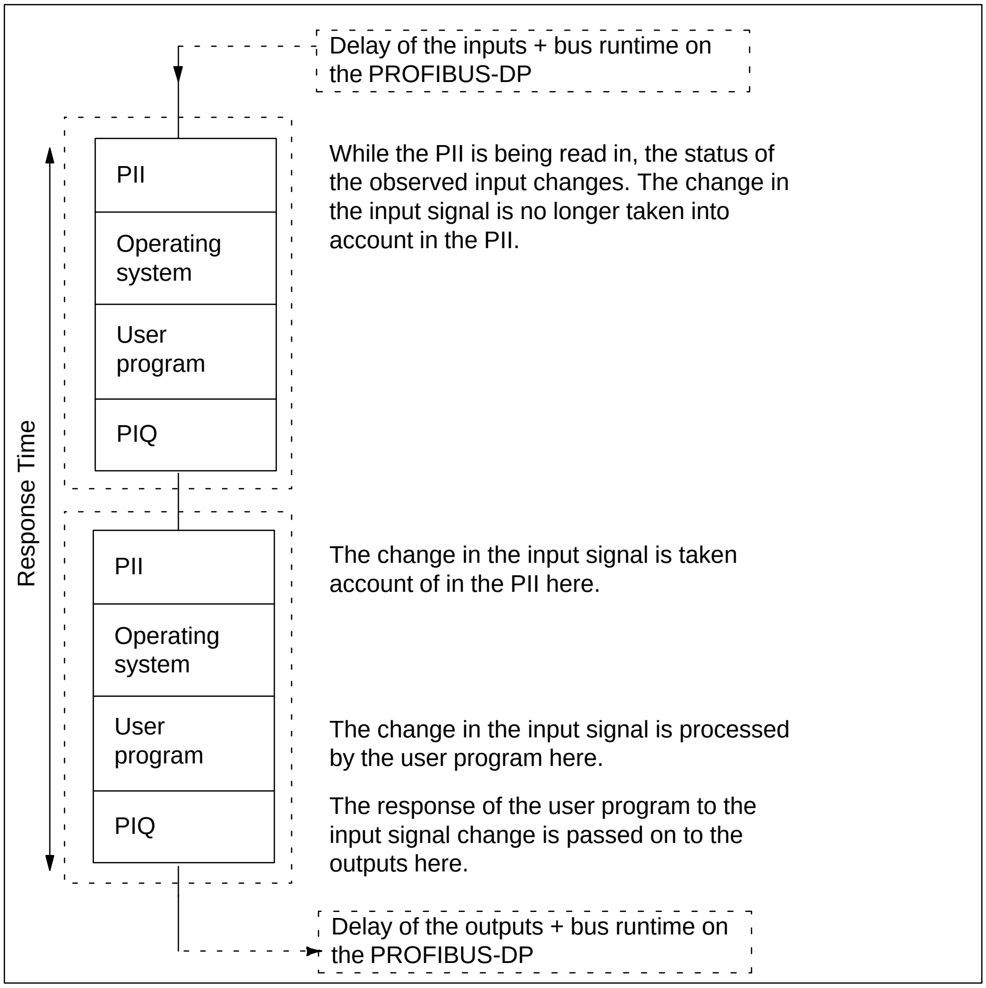


Figure 10-3 Longest Response Time

Calculation

The (longest) response time consists of the following:

- 2 × process image transfer time for the inputs +
- 2 × process image transfer time for the outputs +
- 2 × operating system execution time +
- 2 × program execution time +
- 2 × Bus runtime on the PROFIBUS-DP bus system (with CPU 31x-2 DP)
- Execution time of the S7 timer +
- Delay of the inputs and outputs

This corresponds to the sum of the double cycle time and the delay of the inputs and outputs plus the double bus runtime.

Operating System Processing Time

Table 10-1 contains all the times needed to calculate the operating system processing times of the CPUs.

The times listed do not take account of

- Test functions, e.g. monitor, modify
- Functions: Load block, delete block, compress block
- Communication

Table 10-1 Operating System Processing Times of the CPUs

Sequence	CPU 312 IFM	CPU 313	CPU 314	CPU 314 IFM	CPU 315	CPU 315-2 DP	CPU 316-2 DP	CPU 318-2
Cycle control	600 to 1200 μs	540 to 1040 μs	540 to 1040 μs	770 to 1340 μs	390 to 820 μs	500 to 1030 μs	500 to 1030 μs	200 to 340 ms

Process Image Update

Table 10-2 lists the CPU times for the process image update (process image transfer time). The times specified are "ideal values" which are prolonged by interrupts or by communication of the CPU.
(Process image = PI)

The CPU time for the process image update is calculated as follows:

K + number of bytes in the PI in rack "0" × A
+ number of bytes in the PI in racks "1 to 3" B
+ number of bytes in the PI via DP D
= Process image transfer time

Table 10-2 Process Image Update of CPUs

	Components	CPU 312 IFM	CPU 313	CPU 314	CPU 314 IFM	CPU 315	CPU 315-2 DP	CPU 316-2 DP	CPU 318-2
K	Base load	162 µs	142 µs	142 µs	147 µs	109 µs	10 µs	10 µs	20 µs
A	For each byte in rack “0”	14.5 µs	13.3 µs	13.3 µs	13.6 µs	10.6 µs	20 µs (per word)	20 µs (per word)	6 µs
B	For each byte in racks “1 to 3”	16.5 µs	15.3 µs	15.3 µs	15.6 µs	12.6 µs	22 µs (per word)	22 µs (per word)	12.4 µs
D	For each byte in DP area for integrated DP interface	–	–	–	–	–	12 µs (per word)	12 µs (per word)	1 µs

User Program Processing Time:

The user program processing time is made up of the sum of the execution times for the instructions and the SFB/SFCs called up. These execution times can be found in the Instruction List. Additionally, you must multiply the user program processing time by a CPU-specific factor. This factor is listed in Table 10-3 for the individual CPUs.

Table 10-3 CPU-specific Factors for the User Program Processing Time

Sequence	CPU 312 IFM	CPU 313	CPU 314	CPU 314 IFM	CPU 315	CPU 315-2 DP	CPU 316-2 DP	CPU 318-2
Factor	1,23	1,19	1,15	1,15	1,15	1,19	1,19	1,025

S7 timers

In the case of the CPU 318-2, the updating of the S7 timers does not extend the cycle time.

The S7 timers are updated every 10 ms.
You can find out in Section 10.3 how to include the S7 timers in calculations of the cycle and response times.

Table 10-4 Updating the S7 Timers

Sequence	312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP
Updating the S7 timers (every 10 ms)	Number of simulta-neously active S7 timers × 10 µs	Number of simultaneously active S7 timers × 8 µs					

PROFIBUS-DP interface

In the case of the CPU 315-2 DP/316-2 DP, the cycle time is typically extended by 5% when the PROFIBUS-DP interface is used.

In the case of the CPU 318-2, there is no increase in cycle time when the PROFIBUS-DP interface is used.

Integrated functions

In the case of the CPU 312-IFM and the CPU 314-IFM, the cycle time is increased by a maximum of 10 % when integrated functions are used. In addition, you must, where applicable, take into account the update of the instance DB at the scan cycle checkpoint.

Table 10-5 shows the update times of the instance DB at the scan cycle checkpoint, together with the corresponding SFB runtimes.

Table 10-5 Update Time and SFB Runtimes

CPU 312 IFM/314 IFM	Update Time of the Instance DB at the Scan Cycle Checkpoint	SFB Runtime
IF Frequency measurement (SFB 30)	100 µs	220 µs
IF Counting (SFB 29)	150 µs	300 µs
IF Counting (Parallel counter) (SFB 38)	100 µs	230 µs
IF Positioning (SFB 39)	100 µs	150 µs

Delay of the Inputs and Outputs

You must take account of the following delay times, depending on the module:

- For digital inputs: The input delay time
- For digital outputs: Negligible delay times
- For relay outputs: Typical delay times of between 10 ms and 20 ms. The delay of the relay outputs depends, among other things, on the temperature and voltage.
- For analog inputs: Cycle time of the analog input
- For analog outputs: Response time of the analog output

Bus Runtimes in the PROFIBUS Subnet

When you have configured your PROFIBUS subnet using *STEP 7*, *STEP 7* will calculate the typical bus runtime to be expected. You can then display the bus runtime of your configuration on the programming device (see *STEP 7 User Manual*).

An overview of the bus runtime is provided in Figure 10-4. In this example, we assume that each DP slave has an average of 4 bytes of data.

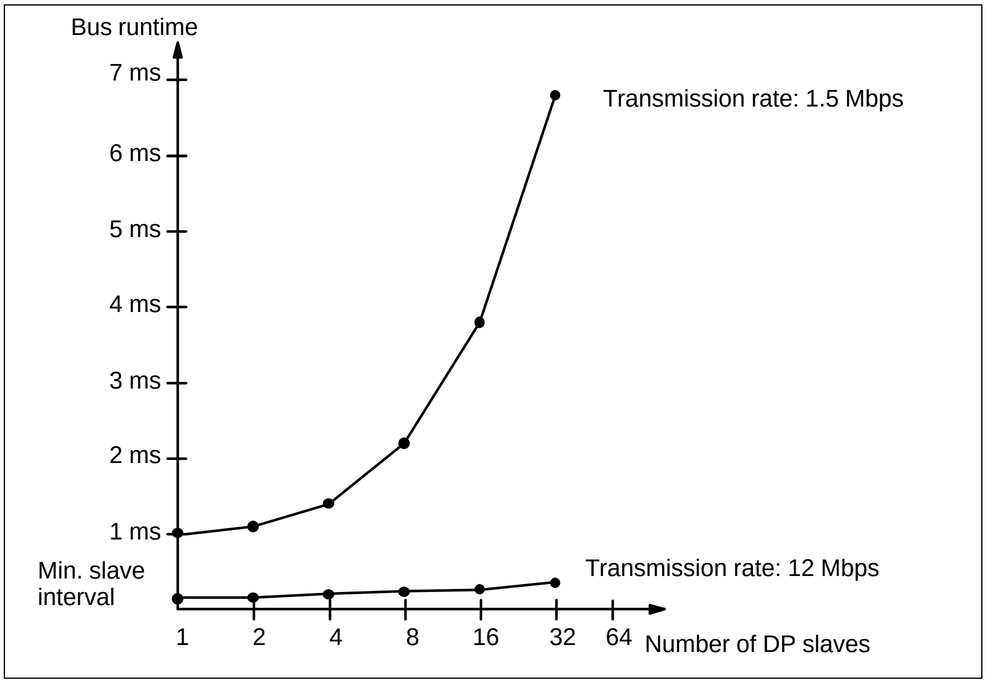


Figure 10-4 Overview of the Bus Runtime on PROFIBUS-DP at 1.5 Mbps and 12 Mbps

If you run a PROFIBUS subnet with several masters, you must allow for the bus runtime of each master (i.e. total bus runtime = bus runtime × number of masters).

Extending the Cycle by Nesting Interrupts

Table 10-6 shows typical extensions of the cycle time through nesting of an interrupt. The program runtime at the interrupt level must be added to these. If several interrupts are nested, the corresponding times need to be added.

Table 10-6 Extending the Cycle by Nesting Interrupts

Interrupts	312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP	318-2
Process interrupt	approx. 840 µs	approx. 700 µs	approx. 700 µs	approx. 730 µs	approx. 480 µs	approx. 590 µs	approx. 590 µs	approx. to 340ms
Diagnostic interrupt	–	approx. 880 µs	approx. 880 µs	approx. 1000 µs	approx. 700 µs	approx. 860 µs	approx. 860 µs	approx. 450 µs
Time-of-day interrupt	–	–	approx. 680 µs	approx. 700 µs	approx. 460 µs	approx. 560 µs	approx. 560 µs	approx. 350 µs
Delay interrupt	–	–	approx. 550 µs	approx. 560 µs	approx. 370 µs	approx. 450 µs	approx. 450 µs	approx. 260 µs
Watchdog interrupt	–	–	approx. 360 µs	approx. 380 µs	approx. 280 µs	approx. 220 µσ	approx. 220 µσ	approx. 260 µs
Programming/ access error/ program execution error	–	approx. 740 µs	approx. 740 µs	approx. 760 µs	approx. 560 µs	approx. 490 µs	approx. 490 µs	approx. 130/ 155/ 285 µs

10.3 Calculation Examples for Cycle Time and Response Time

Component Parts of the Cycle Time

Remember: The cycle time consists of the following:

- Process image transfer time +
- Operating system processing time +
- User program processing time +
- Processing time of S7 timers

Sample Configuration 1

You have configured an S7-300 with the following modules on one rack:

- 1 CPU 314
- 2 SM 321 DI 32 × DC 24 V digital input modules (4 bytes each in the PI)
- 2 SM 322 DO 32 × DC 24 V/0.5A digital output modules (4 bytes each in the PI)

According to the Instruction List, the user program has a runtime of 1.5 ms. There is no communication.

Calculation

In this example, the cycle time is calculated from the following times:

- Process image transfer time

  Process image of the inputs: 147 μs + 8 bytes × 13.6 μs = ca. **0.26 ms**

  Process image of the outputs: 147 μs + 8 bytes × 13.6 μs = ca. **0.26 ms**

- Operating system runtime

  Cyclic control: approx. **1 ms**

- User program processing time:

  approx. 1.5 ms × CPU-specific factor 1.15 = approx. **1.8 ms**

- Processing time of S7 timers

  Assumption: 30 S7 timers are in operation.

  For 30 S7 timers, the single update takes

  30 × 8 ms = 240 μs.

  Adding the process image transfer time, the operating system processing time and the user program processing time gives us the time interval:

  0.26 ms + 0.26 ms + 1 ms + 1.8 ms = 3.32 ms.

  Since the S7 timers are called every 10 ms, a maximum of one call can be made in this time interval, i.e. the cycle time can be increased through the S7 timers by a maximum of 240 μs.

The cycle time is calculated from the sum of the listed times:

Cycle time= 0.26 ms + 0.26 ms + 1 ms + 1.8 ms + 0.024 ms **= 3.34 ms**

Parts of the Response Time

Remember: The response time is the sum of the following:

- 2 × process image transfer time of the inputs +
- 2 × process image transfer time of the outputs +
- 2 × operating system processing time +
- 2 × program processing time +
- Processing time of the S7 timers +
- Delay times of the inputs and outputs

Tip: Simple calculation: Calculated cycle time × 2 + delay times.

For sample configuration 1 the following therefore applies: 3.34 ms × 2 + delay timesI/O modules.

Sample Configuration 2

You have configured an S7-300 with the following modules on two racks:

- 1 CPU 314
- 4 SM 321 DI 32×DC 24 V digital input modules (4 bytes each in the PI)
- 3 SM 322 DO 16×DC 24 V/0.5A digital output modules (2 bytes each in the process image)
- 2 SM 331 AI 8×12Bit analog input modules (not in the process image)
- 2 SM 332 AOI 4×12Bit analog output modules (not in the process image)

User program

According to the Instruction List, the user program has a runtime of 2 ms. By taking into account the CPU-specific factor of 1.15, the resulting runtime is approx. 2.3 ms. The user program employs up to 56 S7 timers simultaneously. No activities are required at the scan cycle checkpoint.

Calculation

In this example, the response time is calculated from the following times:

- Process image transfer time

  Process image of the inputs: 147 μs + 16 bytes×13.6 μs = ca. **0.36 ms**

  Process image of the outputs: 147 μs + 6 bytes×13.6 μs = ca. **0.23 ms**
- Operating system processing time

  Cyclic control: approx. **1 ms**
- User program processing time: **2.3 ms**

- **1st intermediate calculation** The time base for calculating the processing time of the S7 timers is the sum of all previously listed times:

2×0.36 ms	(process image transfer time of inputs)
+ 2×0.23 ms	(process image transfer time of outputs) +
2×1 ms	(operating system processing time) +
2×2.3 ms	(user program processing time) $\approx$ **7.8 ms**.

- Processing time of S7 timers

  A one-off update of 56 S7 timers takes 56×8 μs = 448 μs $\approx$ 0.45 ms.

  Since the S7 timers are called every 10 ms, a maximum of one call can be made in the cycle time, i.e. the cycle time can be increased through the S7 timers by a maximum of 0.45 ms.

- **2nd intermediate calculation:** The response time **excluding** the delay times of the inputs and outputs is calculated from the sum of:

8.0 ms	(result of the first subtotal)
+ 0.45 ms	(processing time of the S7 timers)
=8.45 ms.	

- Delay times of the inputs and outputs
  - The SM 321 DI $32 \times$ DC 24 V digital input module has an input delay of **4.8 ms** per channel.
  - The output delay of the SM 322; DO $16 \times$ DC 24 V/0.5A digital output group can be ignored.
  - The SM 331; AI $8 \times$ 12Bit analog input module was parameterized for interference frequency suppression of 50 Hz. This yields a conversion time of 22 ms per channel. Since 8 channels are active, the cycle time for the analog input module is **176 ms**.
  - The SM 332; AO $4 \times$ 12Bit analog output module was parameterized for the measurement range 0 ...10V. The conversion time is **0.8 ms** per channel. Since 4 channels are active, a cycle time of 3.2 ms is obtained. A settling time of 0.1 ms for a resistive load must be added to this figure. This yields a response time of **3.3 ms** for an analog output.
- Response times with delay times for inputs and outputs:
- **Case 1:** An output channel of the digital output module is set when a digital input signal is read in. This results in a response time of:

  Response time = 4.8 ms + 8.45 ms **= 13.25 ms**.
- **Case 2** An analog value is read in and an analog value is output. This results in a response time of:

  Response time = 176 ms + 8.45 ms + 3.3 ms **= 187.75 ms**.

10.4 Interrupt Response Time

Interrupt Response Time – A Definition

The interrupt response time is the time that elapses between the first occurrence of an interrupt signal and the calling of the first instruction in the interrupt OB.

The following rule generally applies: High-priority interrupts are executed first. This means the interrupt response time is increased by the program processing time of the higher-priority interrupt OBs and the interrupt OBs of equal priority that have not yet been executed.

Calculation

The interrupt response time is calculated as follows:

Shortest interrupt response time =
Minimum interrupt response time of the CPU +
Minimum interrupt response time of the signal modules +
Bus runtime on the PROFIBUS-DP

Longest interrupt response time =
Maximum interrupt response time of the CPU +
Maximum interrupt response time of the signal modules +
2 × bus runtime on the PROFIBUS-DP bus system

Process Interrupt Response Time of the CPUs

Table 10-7 lists the process interrupt response times of the CPUs (without communication).

Table 10-7 Process Interrupt Response Times of the CPUs

CPU	Min.	Max.
312 IFM	0.6 ms	1.5 ms
313	0.5 ms	1.1 ms
314	0.5 ms	1.1 ms
314 IFM	0.5 ms	1.1 ms
315	0.3 ms	1.1 ms
315-2 DP	0.4 ms	1.1 ms
316-2 DP	0.4 ms	1.1 ms
318-2	0.23 ms	0.41 ms

Diagnostic Interrupt Response Times of the CPUs

Table 10-8 lists the diagnostic interrupt response times of the CPUs (without communication).

Table 10-8 Diagnostic Interrupt Response Times of the CPUs

CPU	Min.	Max.
312 IFM	–	–
313	0.6 ms	1.3 ms
314	0.6 ms	1.3 ms
314 IFM	0.7 ms	1.3 ms
315	0.5 ms	1.3 ms
315-2 DP	0.6 ms	1.3 ms
316-2 DP	0.6 ms	1.3 ms
318-2	0.32 ms	0.52 ms

Signal Modules

The process interrupt response time of the signal modules is composed of the following components:

- Digital input modules

  Process interrupt response time = internal interrupt preparation time + input delay

  You will find the times in the data sheet for the individual analog input module.

- Analog input modules

  Process interrupt response time = internal interrupt preparation time + conversion time

  The internal interrupt preparation time for the analog input modules is negligible. The conversion times can be found in the data sheet for the individual digital input modules.

The diagnostic interrupt response time of the signal modules is the time that elapses between the detection of a diagnostic event by the signal module and the triggering of the diagnostics interrupt by the signal module. This time is negligible.

Process Interrupt Handling

Process interrupt handling begins when the process interrupt OB 40 is called. Higher-priority interrupts cause the process interrupt handling routine to be interrupted. Direct accesses to the I/O are made at the execution time of the instruction. When the process interrupt handling routine has finished, either cyclic program execution continues or further same-priority or lower-priority interrupt OBs are called up and executed.

10.5 Calculation Example for the Interrupt Response Time

Parts of the Interrupt Response Time

Remember: The process interrupt response time consists of the following:

- The process interrupt response time of the CPU and
- The process interrupt response time of the signal module.

Example: You have configured an S7-300 with a CPU 314 and four digital modules. One digital input module is the SM 321; DI 16 × DC 24V; with process and diagnostic interrupt. You have only enabled the process interrupt when setting the parameters for the CPU and the SM. You decided not to use time-controlled processing, diagnostics or error handling. You configured an input delay of 0.5 ms for the digital input module. No activities are necessary at the scan cycle checkpoint. There is no communication via the MPI.

Calculation

The process interrupt response time in this example is calculated from the following times:

- Process interrupt response time of the CPU 314: approx. 1.1 ms
- Process interrupt response time of the SM 321; DI 16 × DC 24V:
  - Internal interrupt preparation time: 0.25 ms
  - Input delay 0.5 ms

The process interrupt response time is calculated from the sum of the listed times:

Process interrupt response time = 1.1 ms + 0.25 ms + 0.5 ms = approx. **1.85 ms**.

This process interrupt response time elapses from the time a signal is applied to the digital input until the first instruction in OB 40.

10.6 Reproducibility of Delay and Watchdog Interrupts

Reproducibility – A Definition

Delay Interrupt:

The interval between the call-up of the first instruction in the OB and the programmed time of the interrupt.

Watchdog Interrupt:

The fluctuation of the time interval between two successive call-ups, measured in each case between the first instruction in the OB.

Reproducibility

Table 10-9 lists reproducibility of the delay and watchdog interrupts of the CPUs (without communication).

Table 10-9 Reproducibility of the Delay and Watchdog Interrupts of the CPUs

CPU	Reproducibility	
	Delay Interrupt	Watchdog Interrupt
314	approx. –1/+0.4 ms	approx. ± 0.2 ms
314 IFM	approx. –1/+0.4 ms	approx. ± 0.2 ms
315	approx. –1/+0.4 ms	approx. ± 0.2 ms
315-2 DP	approx. –1/+0.4 ms	approx. ± 0.2 ms
316-2 DP	approx. –1/+0.4 ms	approx. ± 0.2 ms
318-2	approx. –0.8/+0.34 ms	approx. ± 0.05 ms

CPU Functions Dependent on the CPU and *STEP 7* Version 11

In This Chapter

In this chapter we describe the functional differences between the various CPU versions.

These differences are determined by the following factors:

- By the performance features of the CPUs, especially the CPU 318-2 in comparison with other CPUs.
- By functionality of the CPUs described in this manual in comparison to previous versions.

11.1 The Differences Between the CPU 318-2 and the CPU 312 IFM to 316-2 DP

4 accumulators

CPU 318-2	CPUs 312 IFM to 316-2 DP
4 accumulators	2 accumulators

The following table shows you what to watch for if you want to use an STL user program of a CPU 312 IFM to a CPU 316-2 DP for the CPU 318-2.

Instructions	User Program from the CPU 312 IFM to 316-2 DP for the CPU 318
Integer math instructions (+D, –D, *D, /D, MOD)	The CPU 318 transfers the contents of accumulators 3 and 4 to accumulators 2 and 3 after these operations. If accumulator 2 is evaluated in the (accepted) user program, you now receive incorrect values with the CPU 318-2 because the value has been overwritten by the contents of accumulator 3.

Configuration

The CPU 318-2 only accepts a project from a CPU 312 IFM to 316-2 DP if it has been created for these CPUs with *STEP 7* V 5.x.

You cannot use programs that contain configuration data for FMs (FM 353/354, for example) or CPs (SDB 1xxx) for the CPU 318-2.
You must revise or recreate the relevant project.

Starting a Timer in the User Program

If you start a timer in the user program (with SI T, for example), there must be a number in BCD format in the accumulator of the CPU 318-2.

Global Data Status

CPU 318-2	CPUs 312IFM to 316-2DP
You can specify the global data status from the memory marker/data area.	You can specify the global data status from the I/O area and the memory marker/data area.

MPI Addressing

CPU 318-2	CPUs 312 IFM to 316-2 DP
The CPU addresses the MPI nodes within its configuration (FM/CP) via the **module start address**. If FM/CP are in the central configuration of an S7-300 with their own MPI address, the CPU forms its own communication bus (via the backplane bus) with the FM/CP, separate from the other subnets. The MPI address of the FM/CP is no longer relevant for the nodes of other subnets. Communication to the FM/CP takes place via the CPU MPI address.	The CPUs address the MPI nodes within their configuration via the **MPI address**. If FM/CP are in the central configuration of an S7-300 with their own MPI address, the FM/CP and CPU MPI nodes are in the same CPU subnet.

You have an S7-300 configuration with FM/CP addressed via the MPI and want to replace the CPU 312 IFM ... 316 with a CPU 318-2. Figure 11-1 on page 11-3 shows an example.

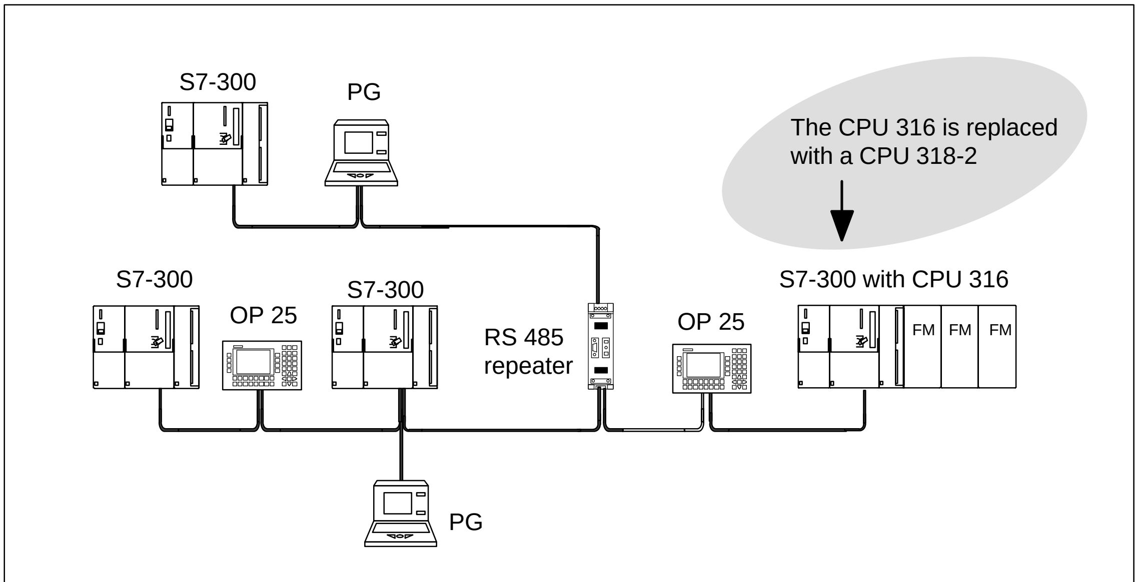


Figure 11-1 Sample Configuration

After the CPUs have been swapped, you must proceed as follows (based on the above example):

- Replace the CPU 316 with the CPU 318-2 in the STEP 7 project.
- Reconfigure the operator panel/programming device. This means reallocating the programmable controller and reassigning the destination address (= MPI address of the CPU 318-2 and the slot of the relevant FM)
- Reconfigure the configuration data for the FM/CP to be loaded onto the CPU.

This is necessary to ensure that the FM/CP in this configuration remain accessible to the operator panel/programming device.

11.2 The Differences Between the CPUs 312 IFM to 316 and Their Previous Versions

Memory Cards and Backing Up Firmware on Memory Card

As of the following CPUs:

CPU	Order No.	As of Version	
		Firmware	Hardware
CPU 313	6ES7 313-1AD**03-**0AB0	1.0.0	01
CPU 314	6ES7 314-1AE**04-**0AB0	1.0.0	01
CPU 315	6ES7 315-1AF**03-**0AB0	1.0.0	01
CPU 315-2	6ES7 315-2AF**03-**0AB0	1.0.0	01
CPU 316-2	6ES7 316-1AG**00-**0AB0	1.0.0	01

You can:

- Insert the 16 bit-wide memory cards:

  256 KB FEPROM 6ES7 951-1KH00-0AA0

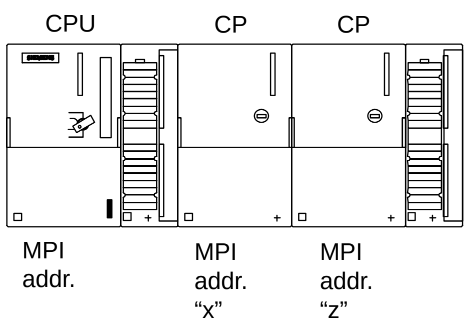
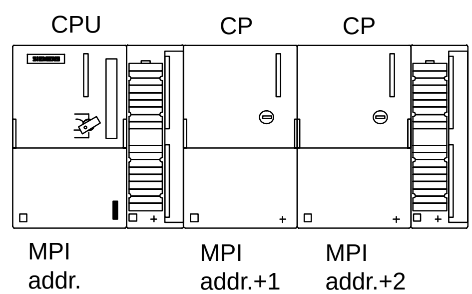
  1 MB FEPROM 6ES7 951-1KK00-0AA0

  2 MB FEPROM 6ES7 951-1KL00-0AA0

  4 MB FEPROM 6ES7 951-1KM00-0AA0
- Back up the CPU firmware on memory card

MPI Addressing

<table>
<tr><th>You Have a CPU as of Order Number and Version:</th><th>You Have a CPU as of Order Number and Version:</th></tr>
<tr><td colspan="2">6ES7 312-5AC01-0AB0, version 01</td></tr>
<tr><td colspan="2">6ES7 313-1AD02-0AB0, version 01</td></tr>
<tr><td colspan="2">6ES7 314-1AE03-0AB0, version 01</td></tr>
<tr><td colspan="2">6ES7 314-5AE02-0AB0, version 01</td></tr>
<tr><td colspan="2">6ES7 315-1AF02-0AB0, version 01</td></tr>
<tr><td colspan="2">6ES7 315-2AF02-0AB0, version 01</td></tr>
<tr><td>6ES7 316-1AG00-0AB0, version 01</td><td>–</td></tr>
<tr><td>and STEP 7 as of V4.02</td><td>and STEP 7 < V4.02</td></tr>
<tr><td>The CPU accepts the MPI addresses configured by you in STEP 7 for the relevant CP/FM in an S7-300

or
automatically determines the MPI address of the CP/FM in an S7-300 on the pattern
MPI addr. CPU; MPI addr.+1 MPI addr.+2 etc.
</td><td>The CPU automatically establishes the MPI address of the CP/FM in an S7-300 on the pattern MPI addr. CPU;MPI addr.+1 MPI addr.+2 etc.
</td></tr>
</table>

MPI with 19.2 kbps

With STEP 7 as of V4.02 you can set a transmission rate for the MPI of 19.2 kbps.

The CPUs support 19.2 kbps as of the following order numbers:

6ES7 312-5AC01-0AB0, version 01
6ES7 313-1AD02-0AB0, version 01
6ES7 314-1AE03-0AB0, version 01
6ES7 314-5AE02-0AB0, version 01
6ES7 315-1AF02-0AB0, version 01
6ES7 315-2AF02-0AB0, version 01

CPU 315-2 DP

CPU 315-2 DP	**v 6ES7 315-2AF03-0AB0 and *STEP 7* < V 5.x**	**As of 6ES7 315-2AF03-0AB0 and *STEP 7* as of V 5.x**
Direct communication	No	Yes
Equidistance	No	Yes
Activation/deactivation of DP slaves	No	Yes
Routing	No	Yes
Reading out of slave diagnosis	See Figure 9-1 on page 9-6	See Figure 9-2 on page 9-7

Tips and Tricks 12

Behavior of the Hardware Clock When the Power Is Off

The following table shows the behavior of the clock when the power of the CPU is off, depending on the backup:

Backup	Clock Behavior
With backup battery	The clock continues to operate in power off mode.
With accumulator	The clock continues to operate in power off mode for the backup time of the accumulator. In POWER ON mode, the accumulator is recharged.
	In the event of backup failure, **no** error message is generated. At POWER ON, the clock continues to operate using the clock time at which power off took place.
None	At POWER ON, the clock continues to operate using the clock time at which power off took place. Since the CPU is not backed up, the clock does not continue at power off.

Tip on the “Monitoring Time for ...” Parameter in STEP 7

If you are not sure of the required times in the S7-300, parameterize the highest values for the parameters of “Monitoring Time for

- Transfer of parameters to modules”
- Ready message from modules”

CPU 31x-2 DP is DP Master	CPU 318-2 is DP Master
You can also set power-up time monitoring for the DP slaves with the “Transfer of parameters to modules” parameter.	You can set power-up time monitoring for the DP slaves with **both** of the above parameters.
This means that the DP slaves must be powered up and parameterized by the CPU (as DP master) in the set time.	

FM in a Distributed Configuration in an ET 200M (CPU 31x-2 is DP Master)

If you use the FM 353/354/355 in an ET 200M with the IM 153-2 and remove and insert the FM in the ET 200M, then you must subsequently turn the power supply of the ET 200M off and on.
The reason for this is that the CPU does not write the new parameters into the FM until power of the ET 200M is switched on.

The Retentive Feature of Data Blocks

You must note the following for the retentivity of data areas in data blocks:

<table>
<tr><th rowspan="2">With Backup Battery</th><th colspan="2">Without Backup Battery</th></tr>
<tr><th>CPU program on Memory Card or in the integral EPROM of the 312 IFM/314 IFM</th><th>Memory card not plugged in</th></tr>
<tr><td rowspan="2">All DBs are retentive, whatever parameterization has been performed. The DBs generated using SFC 22 “CREAT_DB” are also retentive.</td><td>All DBs (retentive, non-retentive) are transferred from the memory card or from the integral EPROM into RAM on restart.</td><td>The DBs parameterized as retentive retain their contents</td></tr>
<tr><td colspan="2">• The DBs or data areas generated using SFC 22 “CREAT_DB” are not retentive.
• After a power failure, the retentive data areas are retained. Note:These data areas are stored in the CPU, not on the memory card. The non-retentive data areas contain whatever has been programmed on EPROM.</td></tr>
</table>

Watchdog Interrupt: Periodicity > 5 ms

For the watchdog interrupt, you should set periodicity > 5 ms. In the case of lower values, the danger of frequent occurrence of watchdog interrupt errors increases depending on, for example, the

- Program execution time of an OB 35 program
- Frequency and program execution time of higher priority classes
- Programming device functions.

Process Interrupt of I/O Modules

In the case of process interrupt-critical applications, insert the process interrupt-triggering modules as near as possible to the CPU.
The reason for this is that an interrupt is read most quickly by rack 0, slot 4 and then in ascending order of the slots.

Standards, Certificates and Approvals A

Introduction

This Appendix provides the following information on the S7-300 modules and components:

- The most important standards and criteria met by S7-300 and
- Approvals that have been granted for the S7-300.

IEC 1131

The S7-300 programmable controller meets the requirements and criteria to standard IEC 1131, Part 2.

CE Symbol

Our products meet the requirements and protection guidelines of the following EC Directives and comply with the harmonized European standards (EN) issued in the Official Journal of the European Communities with regard to programmable controllers:

- 89/336/EEC "Electromagnetic Compatibility" (EMC Directive)
- 73/23/EEC "Electrical Equipment Designed for Use between Certain Voltage Limits" (Low-Voltage Directive)

The declarations of conformity are held at the address below, where they can be obtained if and when required by the respective authorities:

Siemens Aktiengesellschaft
Automation Group
A&D AS E 4
P.O. Box 1963
D-92209 Amberg
Federal Republic of Germany

EMC Guidelines

SIMATIC products have been designed for use in the industrial area.

They can also be used in residential environments (residential, commercial and light industry) with individual approval. You must acquire the individual approval from the respective national authority or testing body. In Germany individual approval is granted by the Bundesamt für Post und Telekommunikation and its associated offices.

Area of Application	Requirements:	
	Emitted interference	**Immunity**
Industry	EN 50081-2 : 1993	EN 50082-2 : 1995
Domestic	Individual approval	EN 50082-1 : 1992

UL Recognition

UL Recognition Mark
Underwriters Laboratories (UL) to
UL standard 508, Report 116536

CSA Certification

CSA Certification Mark
Canadian Standard Association (CSA) to
Standard C22.2 No. 142, File No. LR 48323

FM Approval

FM Approval to Factory Mutual Approval Standard Class Number 3611, Class I, Division 2, Group A, B, C, D.

Warning

Personal injury or property damage can result.

In hazardous areas, personal injury or property damage can result if you withdraw any connectors while an S7-300 is in operation.

Always isolate the S7-300 in hazardous areas before withdrawing connectors.

PNO

CPU	Certificate No. As ...	
	DP Master	DP Slave
315-2 DP	Z00349	Z00258
316-2 DP		
318-2		

B

OBs

In This Appendix

In this appendix you will find an overview of which organization blocks can be executed in which CPU.

The operating system of the CPU is designed for event-controlled user program processing. The following table shows which organization blocks (OBs) the operating system invokes in response to which events.

You can find a detailed description of the OBs in the *STEP 7* online help system.

OBs for ...			Possible Start Events		Excep-tions
Cycle	OB 1	Cycle	1101_H 1103_H	OB1 starting event Running OB1 start event (conclusion of the free cycle)	–
	OB 90	Background OB	 1191_H 1192_H 1193_H 1195_H	OB 90 initiated by... Restart Deletion of a block Transfer of a block in RUN mode OB 90 start event	Only 318-2
Start-up	OB 100	Start-up at STOP-RUN transition	1381_H 1382_H	Manual restart requests Automatic restart requests	–
	OB 102	Cold start	1385_H 1386_H	Manual cold-start request Automatic cold-start request	Only 318-2

OBs for ...			Possible Start Events		Excep- tions
Inter- rupts	OB 10	Time-of-day interrupt	1111_H	Time-of-day interrupt event	Not 312 IFM
	OB 11		1112_H		Only: 318-2
	OB 20	Delay Interrupt	1121_H	Delay interrupt event	Not 312 IFM
	OB 21		1122_H		Only: 318-2
	OB 32	Watchdog interrupt	1133_H	Watchdog interrupt event	Only: 318-2
	OB 35		1136_H		Not 312 IFM
	OB 40	Process interrupt	1141_H	Process interrupt	–
	OB 41		1141_H		Only: 318-2
	OB 82	Diagnostic interrupt	3842_H 3942_H	Module o. k. Module fault	Not 312 IFM
Error re- sponses	OB 80	Timing error	3501_H 3502_H 3505_H 3507_H	Cycle time violation OB or FB request error Time-of-day interrupt elapsed due to time jump Multiple OB request error caused start info buffer overflow	Not 312 IFM
	OB 81	Power supply error	3822_H 3922_H	BAF: Backup voltage returns to CPU BAF: No backup voltage in CPU	Not 312 IFM
	OB 85	Program execution error	$35A1_H$ $35A3_H$ $39B1_H$ $39B2_H$	No OB or FB Error during access of a block by the operating system I/O access error during process image updating of the inputs I/O access error during transfer of the process image to the output modules	Not 312 IFM
	OB 86	Station failure in PROFIBUS-DP subnet	???	–	Only CPU 31x-2 DP
	OB 87	Communication error	$35E1_H$ $35E2_H$ $35E6_H$	Incorrect frame identifier in GD GD packet status cannot be entered in DB GD whole status cannot be entered in DB	Not 312 IFM

OBs for ...			Possible Start Events		Exceptions
Error responses	OB 121	Programming error	2521_H	BCD conversion error	Not 312 IFM
			2522_H	Range length error during reading	
			2523_H	Range length error during writing	
			2524_H	Range error during reading	
			2525_H	Range error during writing	
			2526_H	Timer number error	
			2527_H	Counter number error	
			2528_H	Alignment error during reading	
			2529_H	Alignment error during writing	
			2530_H	Write error during access to DB	
			2531_H	Write error during access to DI	
			2532_H	Block number error opening a DB	
			2533_H	Block number error opening a DI	
			2534_H	Block number error at FC call	
			2535_H	Block number error at FB call	
			$253A_H$	DB not loaded	
			$253C_H$	FC not loaded	
			$253E_H$	FB not loaded	
	OB 122	I/O direct access error	2944_H	I/O access error at nth read access (n > 1)	Not 312 IFM
			2945_H	I/O access error at nth write access (n > 1)	

OB 121 and 122 (Special Features in the CPUs 313 to 316-2 DP)

Please note the following special feature of the S7-300 (except in the CPU 312 IFM/318-2) with OBs 121 and 122:

Note

Please note the following special features with OBs 121 and 122:

The CPU enters in the OBs' local data value "0" in the following temporary variables of the variable declaration table:

- **Byte no. 3:** OB121_BLK_TYPE or OB122_BLK_TYPE (type of the block in which the error has occurred)
- **Byte nos. 8 and 9:** OB121_BLK_NUM or OB122_BLK_NUM (number of the block in which the error has occurred)
- **Byte nos. 10 and 11:** OB121_PRG_ADDR or OB122_PRG_ADDR (address of the block in which the error has occurred)

Execution Times of the SFCs/SFBs and IEC Functions

C

Introduction

The CPUs provide you with various system functions, for example, for program handling and diagnostics. You invoke these system functions in your user program with the number of the SFC or SFB.

IEC functions, which you can call from your user program, are integrated in *STEP 7*.

You can find a detailed description of all SFCs, SFBs and IEC functions in the *STEP 7 online help system*.

Contents

This Appendix shows the execution times for the SFCs/SFBs and for each IEC function. The execution times depend on the CPU used.

C.1 SFCs and SFBs

SFC No.	Name	Description	Execution Time in ms							
			312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP	318-2
0	SET_CLK	Sets the clock time	290	240			240			137
1	READ_CLK	Reads the clock time	205	190			185			28
2	SET_RTM	Sets the operating hours counter	–	65			60			21
3	CTRL_RTM	Starts/stops the operating hours counter	–	55			55			21
4	READ_RTM	Reads the operating hours counter	–	90			80			24
5	GADR_LGC	Reads the free address of the channel *x* of the signal module on module slot *y*.	–	–			–	170	–	38
6	RD_SINFO	Reads the start information of the current OB.	180	150			120			34
7	DP_PRAL	Triggers a process interrupt from the user program of the CPU as DP slave through to DP master.	–	–			–	100	–	29
11	SYC_FR	Synchronizes outputs on the PROFIBUS-DP bus	–	–			–			124 +2.1*
12	D_ACT_DP	Activates or deactivates DP slaves	–	–			–			–
13	DPNRM_DG	Reads the DP-compliant slave diagnosis	–	–			–	180	–	97
14	DPRD_DAT	Reads consistent data from DP standard slaves with a DP standard identifier > 4 bytes	–	–			–	180	–	47
15	DPWR_DAT	Writes consistent data from DP standard slaves with a DP standard identifier > 4 bytes	–	–			–	180	–	47
17	ALARM_SQ	Generates a message and sends it to display devices. The message can be acknowledged by the display device.	–	–	310		250			74

* μs per request

SFC No.	Name	Description	Execution Time in µs							
			312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP	318-2
18	ALARM_S	Generates a message and sends it to a display device. The message is always acknowledged.	–	–	310		250			74
19	ALARM_SC	Determines the acknowledgment state, the last ALARM_SQ received message and the state of the message-initiating signal at the last call-up of the SFC 17 “ALARM_SQ” or the SFC 18 “ALARM_S”.	–	–	130		110			56
20	BLKMOV	Copies variables of random type	105 +2*	90+2*			75+2*			43 + 0.17*
21	FILL	Sets array default variables	105 +3.2 *	90+3.2*			75+2*			45 + 0.12*
22	CREAT_DB	Generates a data block of specified length in a specified area	126 +3.5 **	110+3.5**			100+3.5**			27
23	DEL_DB	Deletes a data block	–	–			–			22
24	TEST_DB	Tests a data block	–	134	98	110	108	126	134	30
25	COMPRESS	Compresses a user program	–	–			–			22
26	UPDAT_PI	Updates process image of the inputs	–	–			–			32 + 4.2***
27	UPDAT_PO	Updates process image of the outputs	–	–			–			30 + 3.5***
28	SET_TINT	Sets the times of a time-of-day interrupt	–	190			190			51
29	CAN_TINT	Cancels the times of a time-of-day interrupt	–	50			50			22
30	ACT_TINT	Activates a time-of-day interrupt	–	50			50			19
31	QRY_TINT	Queries the status of a time-of-day interrupt	–	85			75			30
32	SRT_DINT	Starts a delay interrupt	–	85			80			45
33	CAN_DINT	Cancels a delay interrupt	–	50			50			29

* µs per byte
** µs per DB in stated area
*** µs per module

SFC No.	Name	Description	Execution Time in ms							
			312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP	318-2
34	QRY_DINT	Queries started delay interrupts	–	80			80			32
36	MSK_FLT	Masks sync faults	185	150			110			21
37	DMSK_FLT	Enables sync faults	205	160			130			23
38	READ_ERR	Reads and erases programming and access errors that have occurred or have been disabled	205	160			115			23
39	DIS_IRT	Disables the handling of new interrupts	300	215			200			42
40	EN_IRT	Enables the handling of new interrupt events	490	305			280			42
41	DIS_AIRT	Delays the handling of interrupts	55	35			35			18
42	EN_AIRT	Enables the handling of interrupts	55	35			35			18
43	RE_TRIGR	Re-triggers the scan time monitor	40	30			30			98
44	REPL_VAL	Copies a substitute value into accumulator 1 of the level causing the error	–	45			45			20
46	STP	Forces the CPU into the STOP mode	–	–			–			–
47	WAIT	Implements waiting times	200	200			200			5
48	SNC_RTCB	Sychronizes slave clocks	–	–			–			17
49	LGC_GADR	Converts a free address to the slot and rack for a module	140	140			140			38
50	RD_LGADR	Reads all the declared free addresses for a module	190	190			190			77
51	RDSYSST	Reads out the information from the system state list SFC 51 is not interruptible through interrupts.	350 +10 ***	280+10***			270+10***			150
52	WR_ USMSG	Writes specific diagnostic information in the diagnostic buffer	140	110			110			82
54	RD_DPARM	Reads predefined dynamic parameters from a module	1300	1300			1300			116
55	WR_PARM	Writes dynamic parameters to a module	1000	1600			1600			118

SFC No.	Name	Description	Execution Time in ms							
			312 IFM	**313**	**314**	**314 IFM**	**315**	**315-2 DP**	**316-2 DP**	**318-2**
56	WR_DPARM	Writes predefined dynamic parameters to a module	1600	1750			1750			101
57	PARM_MOD	Assigns a module's parameters	1920	2200			2200			87
58	WR_REC	Writes a module-specific data record	1400 +32 *	1400+32			1400+32			720+ 15*
59	RD_REC	Reads a module-specific data record	500	500			500			810+ 15*
60	GD_SND	Programmed transmission of a GD packet	–	–			–			200+ 9.4*
61	GD_RCV	Programmed acceptance of a GD packet	–	–			–			56
64	TIME_TICK	Reads out the system time You can read out the system time with an accuracy in the ms range.	56	45			45			18
65	X_SEND	Sends data to a communication partner external to your own S7 station.	510	420			310			300
66	X_RCV	Receives data from a communication partner external to your own S7 station.	190	160			120			220
67	X_GET	Reads data from a communication partner external to your own S7 station. The communication partner has no associated SFC.	310	250			190			130+ 8.3*
68	X_PUT	Writes data to a communication partner outside your own S7 station. The communication partner has no associated SFC.	310	250			190			130+ 8.3*
69	X_ABORT	Aborts an existing connection to a communication partner external to your own S7 station.	150	120			100			138

* µs per byte
*** µs per byte of a data record

SFC No.	Name	Description	Execution Time in ms							
			312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP	318-2
72	I_GET	Reads data from a communication partner within your own S7 station.	300		250			190		140+ 9.8*
73	I_PUT	Writes data to a communication partner within your own S7 station.	300		250			190		150+ 10.6*
74	I_ABORT	Aborts an existing connection to a communication partner within your own S7 station.	150		120			100		138
79	SET	Sets a bit field in the I/O area	–		–			–		56
80	RSET	Deletes a bit field in the I/O area	–		–			–		56
81	UBLKMOV	Consistent data transmission with PUT/GET	–		–			–		42 + 0.17*

* µs per byte

Functions for the integrated inputs/outputs (only 312 IFM and 314 IFM)

The CPUs 312 IFM and 314 IFM provide the following system functions for the special channels of the onboard I/O:

The SFBs 29, 30, 38 and 39 are described in the *Integrated Functions* Manual.

The SFBs 41, 42 and 43 are described in the *STEP 7 System and Standard Functions* Reference Manual.

SFB-No.	Name	Description	Execution Time in ms	
			312 IFM	314 IFM
29	HS_COUNT	Counts pulses at the special inputs of the integrated inputs/outputs	approx. 300	approx. 300
30	FREQ_MES	Measures frequency via a special input of the integrated inputs/outputs	approx. 220	approx. 220
38	HSC_A_B	Counts pulses with 2 counters A and B at the special inputs of the integrated inputs/outputs	–	approx. 230
39	POS	Controlled positioning of axes in cooperation with the user program	–	approx. 150
41	CONT_C	Continuous control	–	approx. 3300
42	CONT_S	Step control	–	approx. 2800
43	PULSEGEN	Pulse generation	–	approx. 1500

Implementation of a Sequence Processor

SFB No.	Name	Description	Execution Time in ms							
			312 IFM	313	314	314 IFM	315	315-2 DP	316-2 DP	318-2
32	DRUM	Implements a sequence processor with a maximum of 16 sequences.	480	360			300			33

C.2 IEC Timers and IEC Counters

<table>
<tr><th rowspan="2">SFB No.</th><th rowspan="2">Name</th><th rowspan="2">Description</th><th colspan="8">Execution Time in ms</th></tr>
<tr><th>312 IFM</th><th>313</th><th>314</th><th>314 IFM</th><th>315</th><th>315-2 DP</th><th>316-2 DP</th><th>318-2</th></tr>
<tr><td colspan="11">IEC Timers</td></tr>
<tr><td>3</td><td>TP</td><td>Generates a pulse of duration PT.</td><td>140</td><td colspan="3">100</td><td colspan="3">90</td><td>23</td></tr>
<tr><td>4</td><td>TON</td><td>Delays a leading edge of duration PT.</td><td>140</td><td colspan="3">100</td><td colspan="3">90</td><td>23</td></tr>
<tr><td>5</td><td>TOF</td><td>Delays of falling edge of duration PT.</td><td>145</td><td colspan="3">100</td><td colspan="3">90</td><td>18</td></tr>
<tr><td colspan="11">IEC Counters</td></tr>
<tr><td>0</td><td>CTU</td><td>Counts up. The counter is increased by 1 for each leading edge.</td><td>120</td><td colspan="3">80</td><td colspan="3">70</td><td>16</td></tr>
<tr><td>1</td><td>CTD</td><td>Counts down. The counter is decreased by 1 for each leading edge.</td><td>120</td><td colspan="3">80</td><td colspan="3">70</td><td>16</td></tr>
<tr><td>2</td><td>CTUD</td><td>Counts up and count down.</td><td>150</td><td colspan="3">95</td><td colspan="3">80</td><td>19</td></tr>
</table>

C.3 IEC Functions

You can use the following functions in STEP 7:

FC No.	Name	Description	Execution Time in ms
DATE_AND_TIME			
3	D_TOD_DT	Concatenates the data formats DATE and TIME_OF_DAY (TOD) and convert to data format DATE_AND_TIME.	approx. 680
6	DT_DATE	Extracts the DATE data format from the DATE_AND_TIME data format.	approx. 230
7	DT_DAY	Extracts the day of the week from the data format DATE_AND_TIME.	approx. 230
8	DT_TOD	Extracts the TIME_OF_DAY data format from the DATE_AND_TIME data format.	approx. 200

FC No.	Name	Description	Execution Time in ms
Time Formats			
33	S5TI_TIM	Converts S5 TIME data format to TIME data format	approx. 80
40	TIM_S5TI	Converts TIME data format to S5 TIME data format	approx. 160
Duration			
1	AD_DT_TM	Adds a duration in the TIME format to a time in the DT format. The result is a new time in the DT format.	750
35	SB_DT_TM	Subtracts a duration in the TIME format from a time in the DT format. The result is a new time in the DT format.	750
34	SB_DT_DT	Subtracts two times in the DT format. The result is a duration in the TIME format.	700
Compare DATE_AND_TIME			
9	EQ_DT	Compares the contents of two variables in the DATE_AND_TIME format for equal to.	190
12	GE_DT	Compares the contents of two variables in the DATE_AND_TIME format for greater than or equal to.	190
14	GT_DT	Compares the contents of two variables in the DATE_AND_TIME format for greater than.	190
18	LE_DT	Compares the contents of two variables in the DATE_AND_TIME format for less than or equal to.	190
23	LT_DT	Compares the contents of two variables in the DATE_AND_TIME format for less than.	190
28	NE_DT	Compares the contents of two variables in the DATE_AND_TIME format for not equal to.	190
Compare STRING			
10	EQ_STRNG	Compares the contents of two variables in the STRING format for equal to.	150+ (n × 32)
13	GE_STRNG	Compares the contents of two variables in the STRING format for greater than or equal to.	150+ (n × 32)
15	GT_STRNG	Compares the contents of two variables in the STRING format for greater than.	140+ (n × 38)
19	LE_STRNG	Compares the contents of two variables in the STRING format for less than or equal to.	150+ (n × 32)

L, P = block parameters (if 1 + P = 0, then the execution time L + P = 254 μs)
n = number of characters
k = number of characters in parameter IN1

FC No.	Name	Description	Execution Time in ms
24	LT_STRNG	Compares the contents of two variables in the STRING format for less than.	140+ (n × 38)
29	NE_STRNG	Compares the contents of two variables in the STRING format for not equal to.	150+ (n × 32)
STRING Variable Processing			
21	LEN	Reads the length of a STRING variable.	90
20	LEFT	Reads the first L characters of a STRING variable.	150+ (L × 26)
32	RIGHT	Reads the last L characters of a STRING variable.	150+ (L × 26)
26	MID	Reads the middle L characters of a STRING variable (starting at the defined character).	150+ (L × 26)
2	CONCAT	Concatenates two STRING variables in one STRING variable.	180+ (n × 28)
17	INSERT	Inserts a STRING variable into another STRING variable at a defined point.	250+ (n × 26)
4	DELETE	Deletes L characters of a STRING variable.	300+ ((L + P) × 27)
31	REPLACE	Replaces L characters of a STRING variable with a second STRING variable.	300+ ((L + P) × 27)
11	FIND	Finds the position of the second STRING variable in the first STRING variable.	k × 50
Format Conversions with STRING			
16	I_STRNG	Converts a variable from INTEGER format to STRING format.	1110
5	DI_STRNG	Converts a variable from INTEGER (32-bit) format to STRING format.	1500
30	R_STRNG	Converts a variable from REAL format to STRING format.	1720
38	STRNG_I	Converts a variable from STRING format to INTEGER format.	500
37	STRNG_DI	Converts a variable from STRING format to INTEGER (32-bit) format.	840
39	STRNG_R	Converts a variable from STRING format to REAL format.	200
Number Processing			
22	LIMIT	Limits a number to a defined limit value.	450
25	MAX	Selects the largest of three numeric variables.	430

L, P = block parameters (if 1 + P = 0, then the execution time L + P = 254 μs)
n = number of characters
k = number of characters in parameter IN1

FC No.	Name	Description	Execution Time in ms
27	MIN	Selects the smallest of three numeric variables.	430
36	SEL	Selects one of two variables.	320

L, P = block parameters (if 1 + P = 0, then the execution time L + P = 254 µs)
n = number of characters
k = number of characters in parameter IN1

System Status List in the CPUs

D

Introduction

The CPU is able to provide you, the S7-300 user, with certain information. The CPU stores this information in the “System status list”.

In this appendix you will find the sublists of the system state list made available by the CPUs.

Reading the System State List

You can use SFC 51 “RDSYSST” to read the entries in the system status list from the user program (see the *STEP 7 online help system*).

Listing the Sublists

Table C-1 below shows the individual sublists of the system status list with the entries relevant for the individual CPUs.

Table D-1 Sublists of the System Status List of the CPUs

SZL_ID	Sublist	Index (= ID of the individual records of the sublist)	Record Contents (Sublist Excerpt)	Remarks
	CPU identification		CPU type and version number	–
0111_H	One record of the sublist	0001_H		
	CPU features			–
0012_H	All records of the sublist			
0112_H	Only those records of a group of features	0000_H	STEP 7 processing	
		0100_H	Time system in the CPU	
		0300_H	STEP 7 operation set	
$0F12_H$	Header information only			
0013_H	**User memory areas**	–	Work memory	–

Table D-1 Sublists of the System Status List of the CPUs, continued

SZL_ID	Sublist	Index (= ID of the individual records of the sublist)	Record Contents (Sublist Excerpt)	Remarks
0014_H	**Operating system areas**	–	Process image of the inputs (number in bytes) Process image of the outputs (number in bytes) Number of memory markers Number of timers Number of counters Size of the I/O address area Entire local data area of the CPU (in bytes)	–
 0015_H	**Block types** All records of the sublist	 –	 OBs (number and size) DBs (number and size) SDBs (number and size) FCs (number and size) FBs (number and size)	–
 0019_H $0F19_H$	**State of module LEDs** Status of each LED Header information only		–	–
0132_H	**Communications status information** on the communications type specified	0001_H 0005_H 0008_H	Number and type of connections Diagnostics status data Time system, correction factor, operating hours counter, date/time of day	–
 0222_H	**Interrupt status**; Record for the specified interrupt	 OB number	–	–
0232_H	**CPU Protection Level**	0004_H	CPU protection level and position of the key switch	–
0692_H	**Status information of module rack** for all racks of an S7-300	–	OK status of individual racks	–

Table D-1 Sublists of the System Status List of the CPUs, continued

SZL_ID	Sublist	Index (= ID of the individual records of the sublist)	Record Contents (Sublist Excerpt)	Remarks
$0D91_H$	**Module status information**		Features/parameters of the module plugged in	–
	of all modules in the specified rack (all CPUs)	0000_H	Rack 0	
		0001_H	Rack 1	
		0002_H	Rack 2	
		0003_H	Rack 3	
	Diagnostic buffer	–	Event information	–
$00A0_H$	All entered event information		The information in each case depends on the event	
$01A0_H$	The x latest information entries			
	Module diagnostics			
$00B1_H$	Data record 0 of the module diagnostics information	Module starting address	Module-dependent diagnostics information	
$00B2_H$	Complete module-dependent record of the module diagnostics information	Module rack and slot number		
$00B3_H$	Complete module-dependent record of the module diagnostics information	Module starting address		

PROFIBUS-DP Sublists

Below you will find a list of the sublists that the CPU 315-2 DP can evaluate in its role as DP master or DP slave in addition to those listed in Table D-2.

Table D-2 Sublists of the System Status List of the CPU 315-2 DP as DP Master

SZL_ID	Sublist	Index (= ID of the individual records of the sublist)	Record Contents (Sublist Excerpt)	Remarks
	Module status information in the CPU			
$0A91_H$	Status information of all DP subsystems and DP masters			not 318-2
$0C91_H$	Module status information of a module	Module starting address	Features/parameters of the module plugged in	
	Module status information			–
$0D91_H$	In the station named (for CPU 315-2 DP)	$xxyy_H$	All modules of station *yy* in the DP subnet *xx* As DP slave: Status data for transfer memory areas	
	Status information of module rack or stations in DP network			–
0092_H	Target status of racks in central configuration or of stations in a subnet	0000_H	Information on the state of the mounting rack in the central configuration	
0292_H	Actual status of racks in central configuration or of stations in a subnet	Subnet ID	Information of status of stations in subnet	
0692_H	OK status of expansion racks in central configuration or of stations in a subnet			
$00B4_H$	**Module diagnostics** All standard diagnostic data of a station (only with DP master)	Module start address (Diagnostic address)	Module-dependent diagnostic information	–

Dimensioned Drawings

E

Introduction

In this appendix you will find dimensioned drawings of the CPUs for the S7-300. You need the specifications in these drawings in order to dimension the S7-300 configuration. The dimensioned drawings of the other S7-300 modules and components are contained in the *Module Specifications* Reference Manual.

CPU 312 IFM

Figure E-1 shows the dimensioned drawing of the CPU 312 IFM.

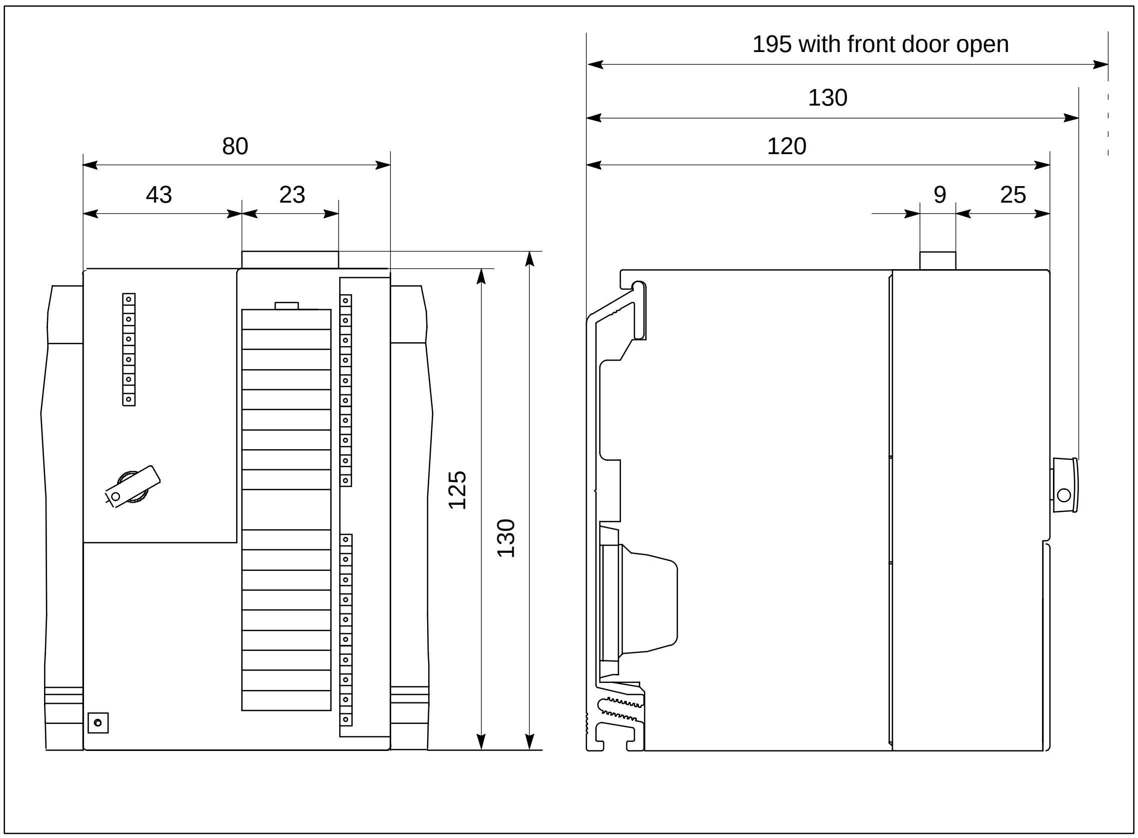


Figure E-1 Dimensioned Drawing of the CPU 312 IFM

CPU 313/314/315/315-2 DP/316-2 DP

Figure E-2 shows the dimensioned drawing of the CPU 313/314/315/315-2 DP/316-2 DP. The dimensions are the same for all the CPUs listed. Their appearance can differ (see Chapter 8). For example, the CPU 315-2 DP has two LED strips.

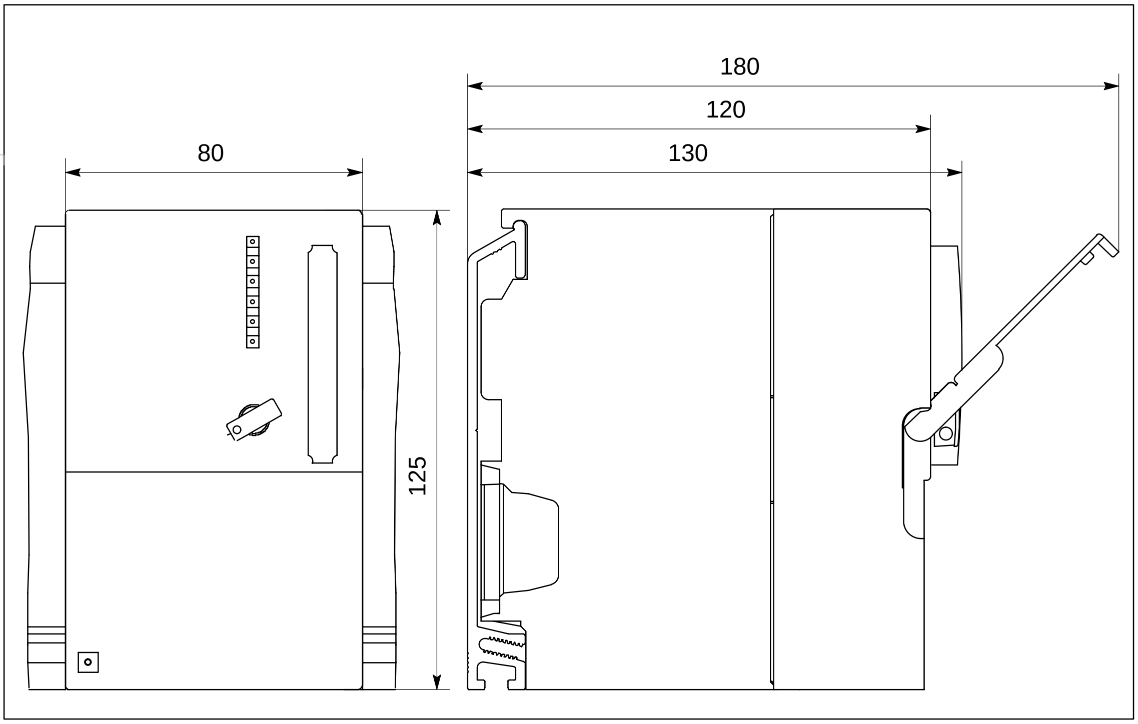


Figure E-2 Dimensioned Drawing of the CPU 313/314/315/315-2 DP/316-2 DP

CPU 318-2

Figure E-3 shows the dimensioned drawing of the CPU 318-2, front view. The side view is illustrated in Figure E-2

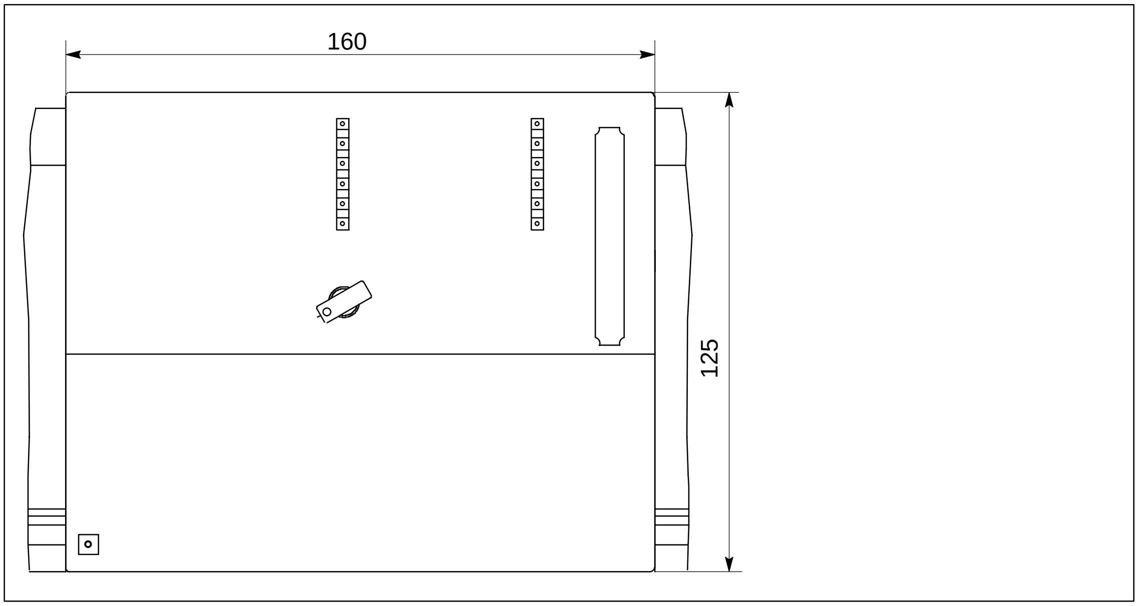


Figure E-3 Dimensioned Drawing of the CPU 318-2

CPU 314 IFM, Front View

Figure E-4 shows the dimensioned drawing of the CPU 314 IFM, front view. The side view is shown in Figure E-5.

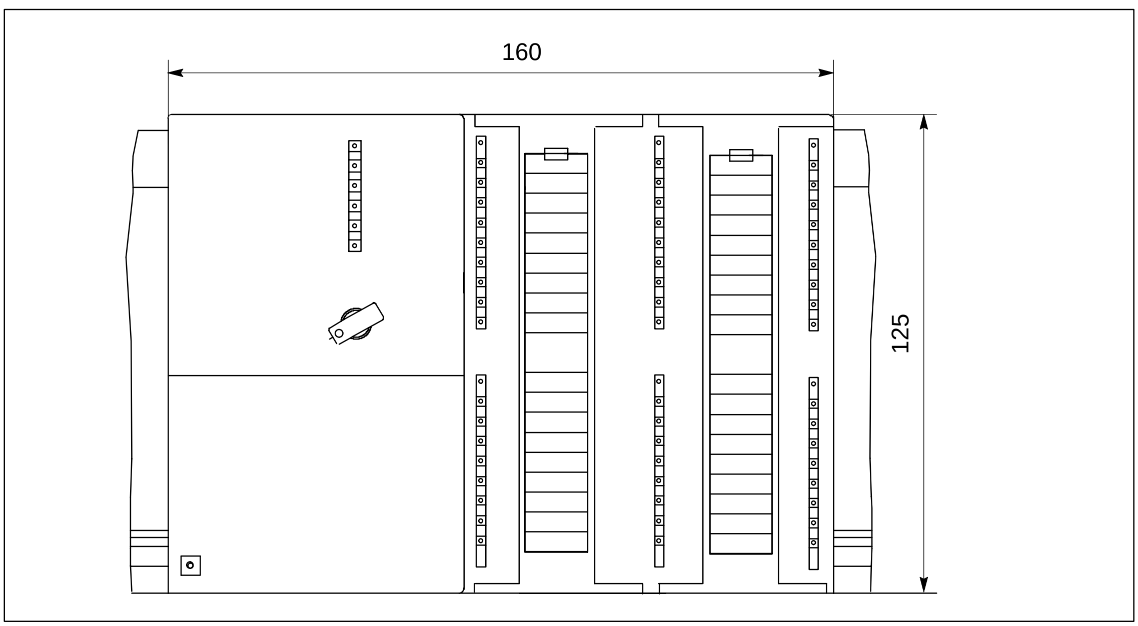


Figure E-4 Dimensioned Drawing of the CPU 314 IFM, Front View

CPU 314 IFM, Side View

Figure E-5 shows the dimensioned drawing of the CPU 314 IFM, side view.

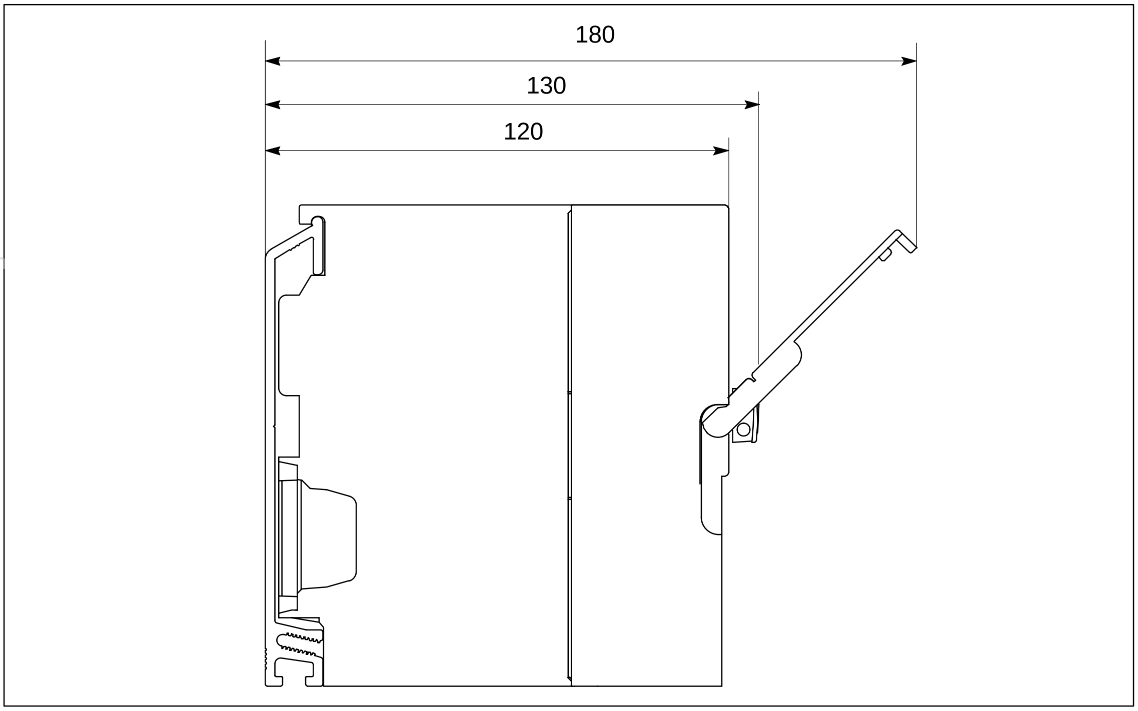


Figure E-5 Dimensioned Drawing of the CPU 314 IFM, Side View

Guidelines for Handling Electrostatic Sensitive Devices (ESD)

F

Introduction

In this appendix, we explain

- what is meant by “electrostatic sensitive devices”
- the precautions you must observe when handling and working with electrostatic sensitive devices.

Contents

This chapter contains the following sections on electrostatic sensitive devices:

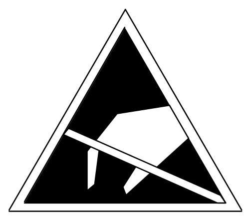
F.1 What is ESD?

Definition

All electronic modules are equipped with large-scale integrated ICs or components. Due to their design, these electronic elements are very sensitive to overvoltages and thus to any electrostatic discharge.

These **e**lectrostatic **s**ensitive **d**evices **have the internationally recognized shortformESD**.

Electrostatic sensitive devices are labeled with the following symbol:



Caution

Electrostatic sensitive devices are subject to voltages that are far below the voltage values that can still be perceived by human beings. These voltages are present if you touch a component or the electrical connections of a module without previously being electrostatically discharged. In most cases, the damage caused by an overvoltage is not immediately noticeable and results in total damage only after a prolonged period of operation.

F.2 Electrostatic Charging of Persons

Charging

Every person with a non-conductive connection to the electrical potential of its surroundings can be charged electrostatically.

Figure F-1 shows you the maximum values for electrostatic voltages to which a person can be exposed by coming into contact with the materials indicated in the figure. These values are in conformity with the specifications of IEC 801-2.

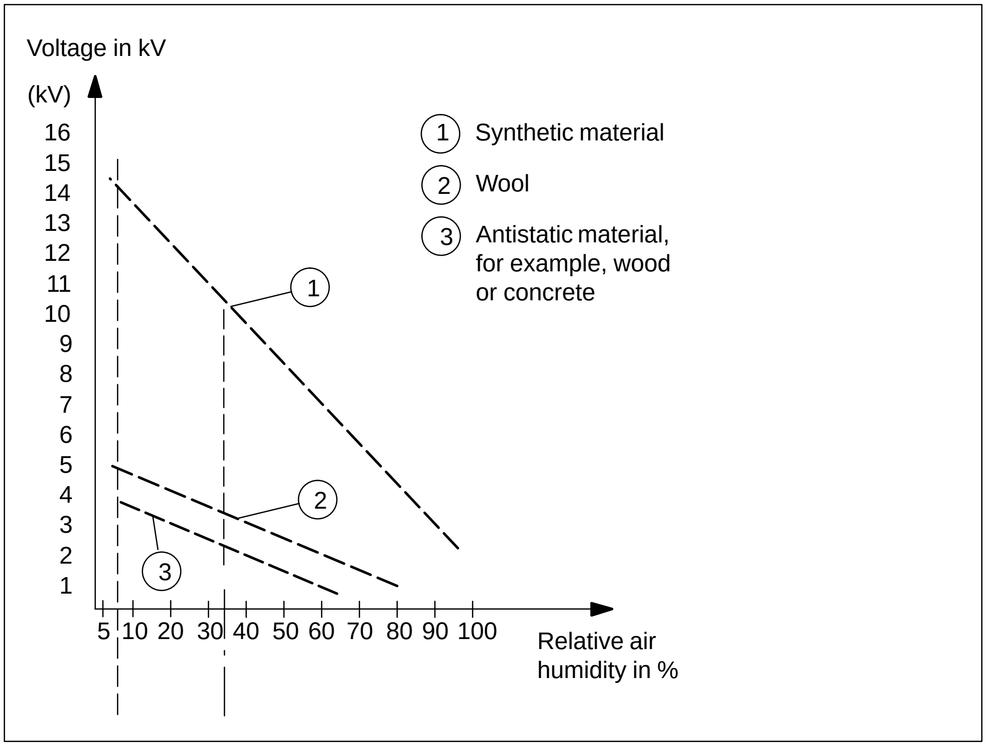


Figure F-1 Electrostatic Voltages which can Build up on a Person

F.3 General Protective Measures against Electrostatic Discharge Damage

Ensuring Sufficient Grounding

Make sure that the personnel, working surfaces and packaging are sufficiently grounded when handling electrostatic sensitive devices. You thus avoid electrostatic charging.

Avoiding Direct Contact

You should touch electrostatic sensitive devices only if it is unavoidable (for example, during maintenance work). Hold modules without touching the pins of components or printed conductors. In this way, the discharged energy cannot affect the sensitive devices.

If you have to carry out measurements on a module, you must discharge your body before you start the measurement by touching grounded metallic parts. Use grounded measuring devices only.

Replacement Parts and Accessories for the CPUs of the S7-300

G

Replacement Parts

Table G-1 lists all the parts you can order separately or later for the CPUs of the S7-300 programmable controllers.

Table G-1 Accessories and Replacement Parts

S7-300 Parts	Order No.	Acces-sories	Re-place-ment Parts
Bus connector	6ES7 390-0AA00-0AA0	–	X
Power connector between power supply unit and CPU	6ES7 390-7BA00-0AA0	–	X
2 × Key for CPU (for mode selector)	6ES7 911-0AA00-0AA0	–	X
Backup battery	6ES7 971-1AA00-0AA0	X	–
Accumulator for real-time clock	6ES7 971-5BB00-0AA0	X	–
Memory card		X	
5 V - FEPROM			
• 16 KB	6ES7 951-0KD00-0AA0		
• 32 KB	6ES7 951-0KE00-0AA0		
• 64 KB	6ES7 951-0KF00-0AA0		
• 128 KB	6ES7 951-0KG00-0AA0		
• 256 KB	6ES7 951-1KH00-0AA0		
• 512 KB	6ES7 951-0KJ00-0AA0		
• 1 MB	6ES7 951-1KK00-0AA0		
• 2 MB	6ES7 951-1KL00-0AA0		
• 4 MB	6ES7 951-1KM00-0AA0		
5 V RAM			
• 128 KB	6ES7 951-0KG00-0AA0		
• 256 KB	6ES7 951-1AH00-0AA0		
• 512 KB	6ES7 951-1AJ00-0AA0		
• 1 MB	6ES7 951-1AK00-0AA0		
• 2 MB	6ES7 951-1AL00-0AA0		
Labeling strip (Qty 10)	6ES7 392-2XX00-0AA0	–	X
Slot numbering label	6ES7 912-0AA00-0AA0	–	X

Table G-1 Accessories and Replacement Parts, continued

S7-300 Parts	Order No.	Acces-sories	Re-place-ment Parts
20-pin front connector		X	–
• Screw terminals	6ES7 392-1AJ00-0AA0		
• Spring-loaded terminals	6ES7 392-1BJ00-0AA0		
40-pin front connector		X	–
• Screw terminals	6ES7 392-1AM00-0AA0		
• Spring-loaded terminals	6ES7 392-1BM01-0AA0		
Shield contact element	6ES7 390-5AA00-0AA0	X	–
Shield terminals for		X	–
• 2 cables with a shield diameter of 2 to 6 mm (0.08 to 0.23 in.) each	6ES7 390-5AB00-0AA0		
• 1 cable with a shield diameter of 3 to 8 mm (0.12 to 0.31 in.)	6ES7 390-5BA00-0AA0		
• 1 cable with a shield diameter of 4 to 13 mm (0.16 to 0.51 in.)	6ES7 390-5CA00-0AA0		
Instruction List	6ES7 398-8AA03-8AN0	X	–

SIMATIC S7 Reference Literature

H

Introduction

This Appendix contains references

- to manuals that you require for configuring and programming the S7-300,
- to manuals describing the components of a PROFIBUS-DP network,
- to technical books providing information beyond the S7-300,

Manuals on Configuration and Commissioning

Comprehensive user documentation is available to assist you in configuring and programming the S7-300. You can select and use this documentation as required. Table H-1 gives you an overview of the documentation for *STEP 7*.

Table H-1 Manuals for Configuring and Programming the S7-300

Title	Contents
System Software for S7-300/400 Program Design *Programming Manual*	The programming manual offers basic information on the design of the operating system and a user program of an S7-300. For novice users of an S7-300/400 it provides an overview of the programming principles on which the design of user programs is based.
Standard Software for S7 und M7 STEP 7 *User Manual*	The STEP 7 User Manual describes the principle and functions of the STEP 7 software for programmable logic controllers. The manual provides both novice and experienced users of STEP 5 with an overview of the procedures used to configure, program and start up an S7-300/400. STEP 7 includes an online help system for detailed answers to questions regarding the use of the software.
Statement List (STL) for S7-300/400 Programming *Manual*	The manuals for the STL, LAD and SCL packages each comprise the user manual and the language description. For programming an S7-300/400 you need only one of the languages, but, if required, you can switch between the language to be used in a project. If it is the first time that you use one of the languages, the manuals will help you in getting familiar with the programming principles. When working with the software, you can use the on-line help, which provides you with detailed information on editors and compilers.
Ladder Logic (LAD) for S7-300 and S7-400 Programming *Manual*	
Structured Control Language (SCL)[1] *for S7-300 and S7-400 Programming* *Manual*	

Table H-1 Manuals for Configuring and Programming the S7-300, continued

Title	Contents
GRAPH[1] for S7-300 and S7-400 Sequential Function Charts *Manual*	With the GRAPH, HiGraph, CFC languages, you can implement sequential function charts, state diagrams or graphic interconnections of blocks. Each of the manuals comprises a user manual and a language description. If it is the first time that you use one of these languages, the manual will help you in getting familiar with the programming principles. When working with the software, you can also use the on-line help (not for HiGraph), which provides you with detailed information on editors and compilers.
HiGraph1 for S7-300 and S7-400 Programming State Diagrams *Manual*	
Continuous Function Charts (CFC)[1] for S7 and M7 Programming Continuous Function Charts *Manual*	
System Software for S7-300 and S7-400 System and Standard Functions *Reference Manual*	The S7-CPU's offer systems and standard functions which are integrated in the operating system. You can use these functions when writing programs in one of the languages, that is STL, LAD and SCL. The manual provides an overview of the functions available with S7 and, for reference purposes, detailed interface descriptions which you require in your user program.

1 Optional system software packages for S7-300/400

Communication Manual

The *Communication with SIMATIC* manual gives you an introduction to and overview of the communication possible in SIMATIC.

Manuals for PROFIBUS-DP

For the configuration and startup of a PROFIBUS-DP network, you will need the descriptions of the other nodes and network components integrated in the network. To help you with this, you can order the manuals listed in Table H-2.

Table H-2 Manuals for PROFIBUS-DP

Manual
ET 200 Distributed I/O System
SIMATIC NET - PROFIBUS Networks
ET 200M Distributed I/O Station
SINEC L2-DP Interface of the S5-95U Programmable Controller
ET 200B Distributed I/O Station
ET 200C Distributed I/O Station
ET 200U Distributed I/O Station
ET 200 Handheld Unit
Technical Overviews
S7/M7 Programmable Controllers *Distributed I/O with PROFIBUS-DP and AS-I*

Technical Literature

Table H-3 lists a selection of technical literature which you can obtain directly from Siemens or from book retailers.

Table H-3 List of Books You Can Order

Title	Siemens Order Number	Book Retailers' Order Number
Speicherprogrammierbare Steuerungen, Grundbegriffe Siemens-AG, Berlin and Munich, 1989	A19100-L531-F913	ISBN 3-8009-8031-2
SPS Speicherprogrammierbare Steuerungen vom Relaisersatz bis zum CIM-Verbund Eberhardt E. Grötsch Oldenbourg Verlag; Munich, Vienna 1989	A19100-L531-G231	ISBN 3-486-21114-5
Speicherprogrammierbare Steuerungen SPS; Band 1: Verknüpfungs- und Ablaufsteuerungen; von der Steuerungsaufgabe zum Steuerungsprogramm Günter Wellenreuther, Dieter Zastrow Braunschweig (3rd edition) 1988	–	ISBN 3-528-24464-X
Steuern und Regeln mit SPS Andratschke, Wolfgang Franzis-Verlag	–	ISBN 3-7723-5623-0
Dezentralisieren mit PROFIBUS DP *Aufbau, Projektierung und Einsatz des PROFIBUS DP mit SIMATIC S7* Josef Weigmann, Gerhard Kilian Publicis MCD Verlag, 1998	A19100-L531-B714	ISBN 3-89578-074-X

Safety of Electronic Control Equipment

I

Introduction

The information provided here is of a predominantly fundamental nature and applies regardless of the type of electronic control system and its manufacturer.

Reliability

Maximum reliability of the SIMATIC systems and components is achieved by implementing the following extensive and cost-effective measures during the development and manufacture:

This includes the following:

- Use of high-quality components;
- Worst-case design of all circuits;
- Systematic and computer-controlled testing of all components supplied by subcontractors;
- Burn-in of all LSI circuits (e.g. processors, memories, etc.);
- Measures to prevent static charge building up when handling MOS ICs;
- Visual checks at different stages of manufacture;
- Continuous heat-run test at elevated ambient temperature over a period of several days;
- Careful computer-controlled final testing;
- Statistical evaluation of all faulty systems and components to enable the immediate initiation of suitable corrective measures;
- Monitoring of the most important control components using on-line tests (watchdog for the CPU, etc.).

These measures are basic measures. They prevent or rectify a large proportion of possible faults.

Risks

In all cases where the occurrence of failures can result in material damage or injury to persons, special measures must be taken to enhance the safety of the installation – and therefore also of the situation. For this type of application, relevant, plant-specific regulations exist that must be observed on installing the control systems (e.g. VDE 0116 for burner control systems).

For electronic control equipment with a safety function, the measures that have to be taken to prevent or rectify faults are based on the risks involved in the installation. Above a certain potential danger, the basic measures listed above are no longer sufficient. In such cases, additional measures (e.g. redundant configurations, tests, etc.) must be implemented for the control equipment and certified (DIN VDE 0801). The S5-95F fail-safe programmable controller has been prototype tested by the German Technical Inspectorate, BIA and GEM III and several certificates have been granted. It is, therefore, just as able as the S5-115F fail-safe PLC that has already been tested to control and monitor safety-related areas of the installation.

Subdivision into Safety-Related and Non-Safety-Related Areas

In almost every installation there are sections that perform safety-related tasks (e.g. Emergency Stop pushbuttons, protective guards, two-hand-operated switches). To avoid the need to examine the entire controller from the aspect of safety, the controller is usually divided into a **safety-related** and **non-safety-related area**. In the non-safety-related area, no special demands are placed on the safety of the control equipment because any failure in the electronics will have no effect on the safety of the installation. In the safety-related area, however, the only control systems and switchgear that are permitted to be used are those that comply with the relevant regulations.

The following divisions are common in practical situations:

1. For control equipment with few safety-related functions (e.g. machine controls)

   The conventional PLC is responsible for machine control and the safety-related functions are implemented with the fail-safe S5-95F mini PLC.

2. For control equipment with a medium degree of safety-related functionality (e.g. chemical installations, cable cars)

   The non-safety-related area is also implemented here with a conventional PLC and the safety-related area is implemented with a tested fail-safe PLC (S5-115F or several S5-95Fs).

   The entire installation is implemented with a fail-safe control system.

3. For control equipment with mainly safety-related functions (e.g. burner control systems)

   The entire control system is implemented with fail-safe technology.

Important Information

Even when electronic control equipment has been configured for maximum design safety, for example using multi-channel setups, it is still of the utmost importance that the instructions given in the operating manual are followed exactly. Incorrect handling can render measures intended to prevent dangerous faults ineffective, or generate additional sources of danger.

Siemens Worldwide

J

In This Appendix

In this appendix you will find a list of the following:

- Siemens offices in the Federal Republic of Germany
- All European and non-European offices and representatives of Siemens AG.

SIMATIC Partners in the Federal Republic of Germany

N Branch

N 52066 Aachen
AUT P 13, Mr Georgens
Kurbrunnenstr. 22
☎ (02 41) 4 51-2 52
Fax (02 41) 4 51-3 98

N 86159 Augsburg
AUT S11, Mr Hirth
Werner-von-Siemens Str. 6
☎ (08 21) 25 95-4 50
Fax (08 21) 25 95-4 08

N 95448 Bayreuth
AUT P/S 11, Ms Hösl
Weiherstr. 25
☎ (09 21) 2 81-3 41
Fax (09 21) 2 81-4 44

N 10587 Berlin
AUT P 1, Mr Liebner
Salzufer 6-8
☎ (0 30) 39 93-23 97
Fax (0 30) 39 93-23 02

N 33605 Bielefeld
AUT P 12, Ms Schlüpmann
Schweriner Str. 1
☎ (05 21) 2 91-5 21
Fax (05 21) 2 91-5 90

N 38126 Braunschweig
AUT P 11, Mr Pelka
Ackerstr. 20
☎ (05 31) 27 12-3 05
Fax (05 31) 27 12-4 16

N 28195 Bremen
AUT P 12, Ms Ulbrich
Contrescarpe 72
☎ (04 21) 3 64-24 27
Fax (04 21) 3 64-28 42

N 09114 Chemnitz
AUT P 11, Ms Aurich
Bornaer Str. 205
☎ (03 71) 4 75-35 10
Fax (03 71) 4 75-35 25

ZN 01189 Dresden
AUT 1, Mr Lehmann
Karlsruher Str. 111
☎ (03 51) 40 22-2 77
Fax (03 51) 40 22-2 74

ZN 40219 Düsseldorf
AUT P 15, Mr Becker
Lahnweg 10
☎ (02 11) 3 99-16 64
Fax (02 11) 3 99-18 48

ZN 99097 Erfurt
AUT P 22, Mr Skudelny
Haarbergstr. 47
☎ (03 61) 4 25-23 51
Fax (03 61) 4 25-23 50

ZN 45128 Essen
AUT P 14, Mr Klein
Kruppstr. 16
☎ (02 01) 8 16-24 28
Fax (02 01) 8 16-23 31

ZN 60329 Frankfurt
AUT P 25, Mr W. Müller
Rödelheimer Landstr. 1-3
☎ (0 69) 7 97-34 18
Fax (0 69) 7 97-34 42

ZN 79104 Freiburg
AUT P, Mr Thoma
Habsburgerstr. 132
☎ (07 61) 27 12-2 38
Fax (07 61) 27 12-4 46

ZN 20099 Hamburg
AUT 1, Mr Rohde
Lindenplatz 2
☎ (0 40) 28 89-30 03
Fax (0 40) 28 89-32 09

ZN 30519 Laatzen (Hannover)
AUT P 10, Ms Hoffmann
Hildesheimer Str. 7
☎ (05 11) 8 77-23 19
Fax (05 11) 8 77-27 39

ZN 74076 Heilbronn
AUT P/S, Mr Gaul
Neckarsulmer Str. 59
☎ (0 71 31) 1 83-2 03
Fax (0 71 31) 1 83-3 20

ZN 76185 Karlsruhe
AUT 14 P, Mr Boltz
Bannwaldallee 48
☎ (07 21) 9 92-24 13
Fax (07 21) 9 92-25 85

ZN 34117 Kassel
AUT P 13, Mr Uhlig
Bürgermeister-Brunner-Str.15
☎ (05 61) 78 86-3 32
Fax (05 61) 78 86-4 48

ZN 87439 Kempten
AUT P, Mr Fink
Lindauer Str. 112
☎ (08 31) 58 18-2 25
Fax (08 31) 58 18-2 40

ZN 24109 Kiel
AUT 1, Ms Drews
Wittland 2-4
☎ (04 31) 58 60-3 26
Fax (04 31) 58 60-2 48

ZN 56068 Koblenz
AUT P 11, Mr Ricke
Frankenstr. 21
☎ (02 61) 1 32-2 44
Fax (02 61) 1 32-2 55

ZN 50823 Köln
AUT P 14, Mr Prescher
Franz-Geuer-Str. 10
☎ (02 21) 5 76-27 62
Fax (02 21) 5 76-27 95

ZN 78416 Konstanz
AUT P, Ms Wiest
Fritz-Arnold-Str. 16
☎ (075 31) 988-2 02
Fax (075 31) 988-1 40

ZN 04105 Leipzig
AUT P 2, Ms Kiesewetter
Springerstr. 15
☎ (03 41) 2 10-30 07
Fax (03 41) 2 10-30 63

ZN 39106 Magdeburg
AUT VG 33, Mr Ganschinietz
Sieverstorstr. 32-33
☎ (03 91) 5 88-17 21
Fax (03 91) 5 88-17 22

ZN 68165 Mannheim
AUT 16 P, Mr Sulzbacher
Dynamostr. 4
☎ (06 21) 4 56-28 43
Fax (06 21) 4 56-25 45

ZN 81679 München
AUT P 14, Mr Schäfer
Richard-Strauss-Str. 76
☎ (0 89) 92 21-30 64
Fax (0 89) 92 21-43 99

ZN 48153 Münster
AUT S 13, Mr Schlieckmann
Siemensstr. 55
☎ (02 51) 76 05-4 25
Fax (02 51) 76 05-3 36

ZN 90439 Nürnberg
AUT P 11, Mr Glas
Von-der-Tann-Str. 30
☎ (09 11) 6 54-35 87
Fax (09 11) 6 54-73 84

ZN 49090 Osnabrück
AUT S 13, Mr Pöhler
Eversburger Str. 32
☎ (05 41) 12 13-2 73
Fax (05 41) 12 13-3 50

ZN 93053 Regensburg
AUT P/S 12, Mr Rewitzer
Hornstr. 10
☎ (09 41) 40 07-1 97
Fax (09 41) 40 07-2 36

ZN 18069 Rostock
AUT, Ms Langhammer
Industriestr. 15
☎ (03 81) 78-21 71
Fax (03 81) 78-21 75

ZN 66111 Saarbrücken
AUT, Mr Müller
Martin-Luther-Str. 25
☎ (06 81) 3 86-22 89
Fax (06 81) 3 86-21 11

ZN 57072 Siegen
AUT P 11, Mr Patz
Sandstr. 42-48
☎ (02 71) 23 02-2 40
Fax (02 71) 23 02-2 38

ZN 70499 Stuttgart
AUT P 11, Mr Müller
Weissacherstr. 11
☎ (07 11) 1 37-26 44
Fax (07 11) 1 37-29 46

ZN 54292 Trier
AUT VG 14 P, Mr Baldauf
Löbstr. 15
☎ (06 51) 20 09-23
Fax (06 51) 20 09-24

ZN 89079 Ulm
AUT ZR, Mr Birk
Nikolaus-Otto-Str. 4
☎ (07 31) 94 50-3 28
Fax (07 31) 94 50-3 34

ZN 97084 Würzburg
AUT PIS 13, Mr Vogt
Andreas-Grieser-Str. 30
☎ (09 31) 61 01-4 59
Fax (09 31) 61 01-5 42

ZN 42103 Wuppertal
siehe ZN 45128 Essen
AUT P 14, Mr Klein
Kruppstr. 16
☎ (02 01) 8 16-24 28
Fax (02 01) 8 16-23 31

SIMATIC Partners in Europe (excluding the Federal Republic of Germany)

Belgium

1060 Bruessel
Siemens S.A., VP4, Mr Gmuer
Chaussee de Chaleroi 116
☎ 00 32 (2) 5 36 25 33
Fax 00 32 (2) 5 36 23 87

Bulgaria

1113 Sofia
Siemens AG, Ms Kirova
Blvd. Dragan Zankov Nr. 36
☎ 0 03 59 (2) 70 85 21
Fax 0 03 59 (2) 68 50 51

Denmark

2750 Ballerup
Siemens A/S, IP, Mr Hansen
Borupvang 3
☎ 00 45 (44) 77 42 90
Fax 00 45 (44)77 40 16

Finland

02601 Espoo
Siemens Osakeyhtioe,
OEM/AUT 1, Mr Saarelainen
Majurinkatu, P.O.B. 60
☎ 0 03 58 (0) 51 05 36 70
Fax 0 03 58 (0) 51 05 36 56

France

69641 Caluire-et-Cuire/Lyon
Siemens S.A., AUT 1, Leitstelle
9-11, Chemin des Petites Brosses,
BP 39
☎ 00 33/ 78 98 60 08
Fax 00 33/ 78 98 60 18

59812 Lesquin, Cedex/Lille
Siemens S.A., AUT 1, Leitstelle
78, Rue de Gustave Delroy
BP 239
☎ 00 33/ 20 95 71 91
Fax 00 33/ 20 95 71 86

33694 Merignac/Bordeaux
Siemens S.A., AUT 1,
Leitstelle, Parc Cadera Sud
36, Avenue Ariane, BP 351
☎ 00 33/ 56 13 32 66
Fax 00 33/ 56 55 99 59

44300 Nantes
Siemens S.A., AUT 1,
Leitstelle, Zac du Perray
9, Rue du Petit Chatelier
☎ 00 33/ 40 18 68 30
Fax 00 33/ 40 93 04 83

93527 Saint Denis, Cedex 2/Paris
Siemens S.A., AUT 1, Mr Granger
39/47, Bd Ornano
☎ 00 33 (1) 49 22 33 18
Fax 00 33 (1) 49 22 32 05

67016 Strasbourg, Cedex
Siemens S.A., AUT 1, Leitstelle
2, Rue du Rhin-Napoleon
BP 48
☎ 00 33/ 88 45 98 22
Fax 00 33/ 88 60 08 40

31106 Toulouse
Siemens S.A., AUT 1, Mr Huguet
ZAC de Basso Cambo
Avenue du Mirail, BP 1304
☎ 00 33/ 62 11 20 15
Fax 00 33/ 61 43 02 20

Greece

15110 Amaroussio/Athen
Siemens A.E., HB 3 AUT,
Mr Antoniou; Paradissou &
Artemidos, P.O.B. 6 10 11
☎ 00 30 (1) 68 64-5 15
Fax 00 30 (1) 68 64-5 56

54110 Thessaloniki
Siemens A.E., VB 3 AUT,
Mr Passalidis
Georgikis Scholis 89, P.O.B. 10290
☎ 00 30 (31) 47 92 12
Fax 00 30 (31) 47 92 65

Great Britain

Manchester M20 2UR
Siemens PLC, Control Systems,
Mr Hardern
Sir William Siemens House,
Princess Road
☎ 00 44 (61) 4 46 52 33
Fax 00 44 (61) 4 46 52 32

Ireland

Dublin 11
Siemens Ltd., Power & Automation Division, Mr Mulligan
8-11 Slaney Road
Dublin Industrial Estate
☎ 0 03 53 (1) 8 30 28 55
Fax 0 03 53 (1) 8 30 31 51

Iceland

121 Reykjavik
Smith & Norland H/F,
Mr Kjartansson,
Noatuni 4, P.O.B. 519
☎ 0 03 54 (1) 62 83 00
Fax 0 03 54 (1) 62 83 40

Italy

40127 Bologna
Siemens S.p.A., AUT R10A,
Mr Tosatti
Via Casciarolo, 8
☎ 00 39 (51) 6 38 45 09
Fax 00 39 (51) 24 32 13

25128 Brescia
Siemens S.p.A., AUT R10A,
Mr Gaspari, Via della Volta, 92
☎ 00 39 (30) 3 53 05 26
Fax 00 39 (30) 34 66 20

20124 Milano
Siemens S.p.A., AUT R10A,
Mr Berti, Via Lazzaroni, 3
☎ 00 39 (2) 66 76 28 36
Fax 00 39 (2) 66 76 28 20

35129 Padova
Siemens S.p.A., AUT R10A,
Mr Millevoi, Viale dell'Industria, 19
☎ 00 39 (49) 8 29 13 11
Fax 00 39 (49) 8 07 00 09

00142 Roma
Siemens S.p.A., AUT R10A,
Mr Vessio, Via Laurentina, 455
☎ 00 39 (6) 5 00 95-1
Fax 00 39 (6) 5 00 95 20

10127 Torino
Siemens S.p.A., AUT R10A,
Mr Montoli, Via Pio VII, 127
☎ 00 39 (11) 6 17 3-1
Fax 00 39 (11) 61 61 35

Croatia

41000 Zagreb
Siemens d.o.o., Mr Culjak
Trg Drazena Petrovica 3 ("Cibona")
☎ 0 03 85 (41) 33 88 95
Fax 0 03 85 (41) 32 66 95

Luxembourg

1017 Luxemburg-Hamm
Siemens S.A., AUT, Mr Nockels
20, Rue des Peupliers
B.P. 1701
☎ 0 03 52/ 4 38 43-4 21
Fax 0 03 52/ 4 38 43-4 15

Netherlands

2595 AL Den Haag
Siemens Nederland N.V., IPS/APS,
Mr Penris, Prinses Beatrixlaan 26
☎ 00 31 (70) 3 33 32 74
Fax 00 31 (70) 3 33 34 96

Norway

5033 Fyllingsdalen
Siemens A/S Bergen,
Mr Troan, Bratsbergveien 5
Postboks 36 60
☎ 00 47 (55) 17 67 41
Fax 00 47 (55) 16 44 70

0518 Oslo 5
Siemens A/S, AUT Produkter,
Mr Eggen, Ostre Aker vei 90
Postboks 10, Veitvet
☎ 00 47 (22) 63 34 09
Fax 00 47 (22) 63 33 90

7004 Trondheim
Siemens A/S Trondheim,
Mr Thorsen, Spelaugen 22
☎ 00 47 (73) 95 96 69
Fax 00 47 (73) 95 95 04

Austria

6901 Bregenz
Siemens AG, AUT, Mr Madlener
Josef-Huter-Straße 6,
Postfach 347
☎ 00 43 (55 74) 41 92 72
Fax 00 43 (55 74) 41 92 88

8054 Graz
Siemens AG, AUT, Mr Jammernegg
Strassganger Straße 315
Postfach 39
☎ 00 43 (3 16) 2 80 42 80
Fax 00 43 (3 16) 2 80 42 85

6040 Innsbruck/Neu-Rum
Siemens AG, AUT, Mr Mayr
Siemensstraße 24, Postf. 9 04
☎ 00 43 (5 12) 23 12 60
Fax 00 43 (5 12) 23 15 30

9020 Klagenfurt
Siemens AG, AUT, Mr Weber
Werner von Siemens Park 1
☎ 00 43 (4 63) 3 88 32 43
Fax 00 43 (4 63) 3 88 34 49

4020 Linz
Siemens AG, AUT, Mr Schmidt
Wolfgang-Pauli-Straße 2
Postfach 563
☎ 00 43 (7 32) 3 33 02 95
Fax 00 43 (7 32) 3 33 04 93

5020 Salzburg
Siemens AG, AUT, Mr Mariacher Jun.
Innsbrucker Bundesstraße 35
Postfach 3
☎ 00 43 (6 62) 4 48 83 35
Fax 00 43 (6 62) 4 48 83 09

1211 Wien
Siemens AG, AUT 1, Mr Strasser,
Siemensstraße 88-92,
Postfach 83
☎ 00 43 (1) 25 01 37 88
Fax 00 43 (1) 25 01 39 40

Poland

40-931 Katowice
Siemens Sp. z.o.o., Niederlassung
Katowice, Mr Krzak
Ul. Kosciuszki 30
☎ 00 48 (3) 157 32 66
Fax 00 48 (3) 157 30 75

60-815 Poznan
Siemens Sp. z.o.o., Niederlassung
Poznan, Mr Weiss
Ul. Gajowa 6
☎ 00 48 (61) 47 08 86
Fax 00 48 (61) 47 08 89

03-821 Warszawa
Siemens Sp. z.o.o., Mr Cieslak
Ul. zupnicza 11,
☎ 00 48 (2) 6 70 91 47
Fax 00 48 (2) 6 70 91 49

53-332 Wroclaw
Siemens Sp. z.o.o., Niederlassung
Wroclaw, Mr Wojniak
Ul. Powstanców Slaskich 95
☎ 00 48 (71) 60 59 97
Fax 00 48 (71) 60 55 88

Portugal

2700 Amadora
Siemens S.A., Dep. Energia e
Industria, Mr Eng. C. Pelicano
Estrada Nacional 117 ao
km 2,6 Alfragide, Apartado 60300
☎ 0 03 51 (1) 4 17 85 03
Fax 0 03 51 (1) 4 17 80 71

4450 Matosinhos-Porto
Siemens S.A., Dep. Energia e
Industria, Mr Eng. A. Amaral,
Estrada Nacional 107,
No. 3570 Freixieiro, Apartado 5145
☎ 0 03 51 (2) 9 99 21 11
Fax 0 03 51 (2) 9 99 20 01

Rumania

76640 Bucuresti
Siemens, Birou de consultatii
tehnice, Mr Fritsch
Str. Zarii No. 12, sector 5
☎ 00 40 (1) 2 23 47 95
Fax 00 40 (1) 2 23 45 69

Russia

113043 Moskau
Siemens AG, Mr Engelhard/
Mr Michailow, Ul. Dubininskaja 98
☎ 0 07 (0 95) 2 36 75 00
Fax 0 07 (0 95) 2 36 62 00

Sweden

40020 Göteborg
Siemens AB, ASP, Mr Ohlsson
Ostergardsgatan 2-4
Box 1 41 53
☎ 00 46 (31) 7 76 86 53
Fax 00 46 (31) 7 76 86 76

55111 Jönköping
Siemens AB, ASP, Mr Jonsson
Klubbhusgatan 15, Box 10 07
☎ 00 46 (36) 15 29 00
Fax 00 46 (36) 16 51 91

20123 Malmö
Siemens AB, ASP, Mr Jämtgren
Grimsbygatan 24, Box 326
☎ 00 46 (40) 17 46 14
Fax 00 46 (40) 17 46 17

85122 Sundsvall
Siemens AB, ASP, Mr Sjöberg
Lagergatan 14, Box 766
☎ 00 46 (60) 18 56 00
Fax 00 46 (60) 61 93 44

19487 Upplands Väsby/Stockholm
Siemens AB, ASP-A1, Mr Persson
Johanneslandsvägen12-14
☎ 00 46 (8) 7 28 14 64
Fax 00 46 (8) 7 28 18 00

Switzerland

1020 Renens/Lausanne
Siemens-Albis SA, Systemes
d'automation, VHRL, Ms Thevenaz
5, Av. des Baumettes
Case postale 1 53
☎ 00 41 (21) 6 31 83 09
Fax 00 41 (21) 6 31 84 48

8047 Zürich
Siemens-Albis AG, VHR 3,
Mr Engel, Freilagerstraße 28-40
☎ 00 41 (1) 4 95 58 82
Fax 00 41 (1) 4 95 31 85

Slovakian Republic

81261 Bratislava
Siemens AG, Mr Sykorcin,
Tovarenska 11
☎ 00 42 (7) 31 21 74
Fax 00 42 (7) 31 63 32

Slovenia

61000 Ljubljana
Siemens Slovenija, Mr Lavric
Dunajska C47
☎ 0 03 86 (61) 1 32 60 68
Fax 0 03 86 (61) 1 32 42 81

Spain

48011 Bilbao
Siemens S.A., AUT 1, Mr Tapia
Maximo Aguirre, 18
☎ 00 34 (4) 4 27 64 33
Fax 00 34 (4) 4 27 82 39

08940 Cornella de Llobregat/
Barcelona
Siemens S.A., AUT 1, Mr Ortiz
Joan Fernandez Vallhonrat, 1
☎ 00 34 (3) 4 74 22 12
Fax 00 34 (3) 4 74 42 34

33206 Gijon
Siemens S.A., AUT 1, Mr Huchet
Corrida, 1
☎ 00 34 (85) 35 08 00
Fax 00 34 (85) 34 93 10

15005 La Coruna
Siemens S.A., AUT 1, Mr Pereira
Linares Rivas, 12-14
☎ 00 34 (81) 12 07 51
Fax 00 34 (81) 12 03 60

30008 Murcia
Siemens S.A., AUT 1, Mr Martinez
Marques de los Velez, 13
☎ 00 34 (68) 23 36 62
Fax 00 34 (68) 23 52 36

41092 Sevilla
Siemens S.A., AUT 1,
Mr de la Fuente
ISLA DE LA CARTUJA
Paseo de la Acacias, s/n
(Edificio Siemens)
☎ 00 34 (5) 4 46 30 00
Fax 00 34 (5) 4 46 30 46

28760 Tres Cantos (Madrid)
Siemens S.A., AUT 1,
Mr Olaguibel, Ronda de Europa, 5
☎ 00 34 (1) 8 03 12 00
Fax 00 34 (1) 8 03 22 71

46021 Valencia
Siemens S.A., AUT 1, Mr Albors
Avda. Aragon, 30 (Ed. Europa)
☎ 00 34 (6) 3 69 94 00
Fax 00 34 (6) 3 62 61 19

36204 Vigo
Siemens S.A., AUT 1, Mr Garrido
Pizarro, 29
☎ 00 34 (86) 41 60 33
Fax 00 34 (86) 41 84 64

50012 Zaragoza
Siemens S.A., AUT 1, Mr Aliaga
Avda. Alcalde Gomez Laguna, 9
☎ 00 34 (76) 35 61 50
Fax 00 34 (76) 56 68 86

Czech Republic

60200 Brno
Siemens AG, Kancelar Brno,
Mr Tucek, Vinarská 6
☎ 00 42 (5) 43 21 17 49
Fax 00 42 (5) 43 21 19 86

14000 Praha 4
Siemens AG, Zastoupeni v CR,
Mr Skop, Na strzi 40
☎ 00 42 (2) 61 21 50 33 6
Fax 00 42 (2) 61 21 51 46

80040 Findliki-Istanbul
SIMKO A.S., AUT ASI 1, Ms Yargic
Meclisi Mebusan Cad. 125
☎ 00 90 (1) 25 10 90 01 706
Fax 00 90 (1) 25 10 90 07 09

Turkey

06680 Ankara-Kavaklidere
SIMKO-ANKARA, Mr Ensert,
Atatürk Bulvari No. 169/6
☎ 00 90 (312) 4 18 22 05

80040 Findikli-Istanbul
SIMKO TIC. ve SAN. A. S.,
AUT 1, Ms Yargic
Meclisi Mebusan Cad. No 125
☎ 00 90 (212) 2 51 17 06
Fax 00 90 (212) 2 52 39 16

Ukraine

252054 Kiew 54
Siemens-Vertretung, AUT,
Mr Liebschner,
Ul. Worowskowo 27
☎ 0 07 (044) 2 16 02 22
Fax 0 07 (044) 2 16 94 92

Hungary

1036 Budapest
Siemens GmbH, AUT 1, Mr Turi
Lajos utca 103
☎ 00 36 (1) 2 69 74 55
Fax 00 36 (1) 2 69 74 54

SIMATIC Partners Outside of Europe

Afrika

Ägypten

Zamalik/EGY-Cairo
ELETECH, AUT, Mr W. Y. Graiss
6 Zarkaria Rizk Street,
P.O.B. 90
☎ +20 (2) 3 42 03 71
Fax +20 (2) 3 42 03 76

Algeria

16035 Hydra/Alger
Siemens, Bureau d'Alger, Division
Energie, Mr Bennour,
44, rue Abri Areski , B.P. 112
☎ +213 (2) 60 40 88
Fax +213 (2) 60 65 98

Ivory Coast

Abidjan 15/R. C. I.
Siemens AG, SEMEN, Mr. Hellal,
16 B.P. 1062
☎ +2 25 (37) 46 57
Fax +2 25 (27) 10 21

Libya

Tripoli/Libya S.P.L.A.J.
Siemens AG, Branch Libya,
Mr Wahab, Zat-EL-Imad-
Building Tower No. 5, Floor No. 9
P.O.B. 91 531
☎ +218 (21) 4 15 34
Fax +218 (21) 4 79 40

Morocco

Casablanca 05
SETEL S.A., AUT, Mr El Bachiri,
Immeuble Siemens,
km 1, Route de Rabat,
Ain Sebaa
☎ +212 (2) 35 10 25
Fax +212 (2) 34 01 51

Namibia

Windhoek 9000
Siemens (Pty) Ltd., Mr Jürgen Hoff
9 Albert Wessels Street
Industries North, P.O.B. 23125
☎ +2 64 (61) 6 13 58/59
Fax +2 64 (61) 6 13 77

South Africa

RSA-2001 Braamfontein
Siemens Ltd., AUT, Mr E. Hillermann
Siemens House SH 401
Corner Wolmarans & Biccard
Streets, P.O. Box 4583
2000 Johannesburg
☎ +27 (11) 4 07 41 11
☎ +27 (11) 4 07 48 15
Fax +27 (11) 4 07 46 82

Tunisia

TN-2062 Romana-Le Bardo
FAZE Sarl Electrotechnique,
Mr Fantar, Immeuble Cham
☎ +2 16 (1) 51 90 91
Fax +2 16 (1) 50 19 32

TN-2035 Charguia II Tunis
SITELEC S.A. Mr Mouelhi
16, Rue de l'Usine
Zone industrielle (Aéroport),
BP 115, 1050 Tunis Cedex
☎ +2 16 (1) 70 00 99
Fax +2 16 (1) 71 70 10

Zimbabwe

Electro Technologies Corp. (Pvt.) Ltd./
Siemens Zimbabwe,
Mr Ron Claassens, Savoy House
cnr. Inez Terrace/J. Moyo Ave
P.O. Box 46 80
☎ +263 (4) 79 18 66
Fax +263 (4) 75 44 06

America

Argentina

8000 Bahia Blanca,
Prov. de Buenos Aires
Siemens S.A., Mr S.Duran,
Rudriguez 159
☎ +54 (91) 55-61 41
Fax +54 (91) 55-61 71

(1650) San Martin,
Prov. de Buenos Aires
Siemens S.A., PEI-AUT,
Mr Rudriguez Juis/Mr Roland Herron,
Gral, Roca 1865, Ruta 8, km 18 C.C.
☎ +54 (1) 7 38 71 92/7 15
☎ +54 (1) 7 38 71 85
Fax 254 (1) 7 38 71 71

5000 Cordoba, Prov. de Cordoba
Siemens S.A., Mr S. Garcia,
Campillo 70
☎ +54 (51) 73-9940/994
Fax +54 (51) 72-97 14

5539 Las Heras, Prov. de Mendoza
Siemens S.A., Mr S. Suarez,
Acceso Norte 379
☎ +54 (61) 30-00 22/0 37
Fax +54 (61) 30-00 22/0 37

2000 Rosario, Prov. de Santa Fe
Siemens S.A., Mr R. Stiza,
Ricchieri 750
☎ +54 (1) 41 37-03 21/0
Fax +54 (1) 41 37-07 87

Bolivia

La Paz
Sociedad Comercial e Industrial
Hansa Ltda., E & A, Mr Beckmann
Calle Mercado esq. Yanacocha
C. P. 10 800
☎ +591 (2) 35 44 45
Fax +591 (2) 37 03 97

Brazil

05110-900 Sao Paulo, SP, Pinituba
MAXITEC S.A., AUT-PA, Mr F. Rocco,
Avenida Mutinga, 3650
☎ +55 (11) 8 36 29 99
Fax +55 (11) 8 36 29 50

Chile

Santiago de Chile
INGELSAC,Div. Energia, Mr Browne
Avda. Holanda 64, Cas. 242-V
☎ +56 (2) 2 31 00 00
Fax +56 (2) 2 32 66 88

Costa Rica

San Jose 1000
Siemens S.A. San Jose, Division
Energia y Automatizacion, VAT,
Mr Ferraro,
La Uruca, Apartado 100 22
☎ +5 06 87 50 50
Fax +5 06 21 50 50

Ecuador

Quito
Siemens S.A., Dept. DEA,
Mr J. Guerra
Calle Manuel Zambrano y
Panamericana Norte km 2 1/2
Casilla de Correos 17-01-3580
☎ +5 93 (2) 47 40 60
Fax +5 93 (2) 40 77 38

El Salvador

San Salvador
Siemens S.A., E/A, Mr M. Dubon
43, Calle Siemens
Parque Industrial Sta. Elena
Apartado 1525
☎ +5 03 78 33 33
Fax +5 03 78 33 34

Guatemala

Ciudad de Guatemala
Siemens S.A., EA/AUT, Mr Godoy
2a Calle 6-76
Zona 10, Apartado 1959
☎ +5 02 (2) 32 44 44
Fax +5 02 (2) 34 36 70

Canada

Mississauga, ON L5N 7AG
Siemens Electric Ltd., Dept. SL 20,
Mr Fred Leon, 2185 Derry Road
West
☎ +1 (905) 7 92 81 95 82
Fax +1 (905) 58 19 58 12

Point Claire, QUE H9R-4R6
Siemens Electric Ltd., Mr D. Goulet
7300 Trans Canada Highway
☎ +1 (514) 4 26 60 99
Fax +1 (514) 4 26 61 44

Burnaby, B. C. V5J 5J1
Siemens Electic Ltd., Mr A. Mazurek
Marine Way Business Park
8875 Northbrook Court
☎ +1 (604) 4 35 08 80
Fax +1 (604) 4 35 10 23

Columbia

Baranquilla
Siemens S.A., EA, Mr C. Perez,
Carrera 58 No. 709-40
☎ +57 (958) 56 11 48
Fax +57 (958) 56 11 48

Bogota 6
Siemens S.A., Division Energia,
Mr M. Jaramillo
Carrera 65, No. 11-83
Apartado 80150
☎ +57 (1) 2 94 22 66
Fax +57 (1) 2 94 24 98

Cali
Siemens S.A., Barranquilla,
Mr Guido Hernandez
Carrera 40, No. 13-05
☎ +57 (92) 66-4 44 00
Fax +57 (92)66-5 30 56

Cali
Siemens S.A. Cali Mr C. A. Naranjo
Carrera 48 A, 15 Sur 92
☎ +57 (94) 2 66-30 66
Fax +57 (94) 2 68-25 57

Mexico

02300 Mexico, D.F.
Siemens S.A. de C.V., EI-AUT,
Mr Gregorio Sanchez
DelegacionAzcapotzalco
Poniente 116, No. 590
Colonia Industrial Vallejo
Apartado Postal
15-064, 02600 mexico
☎ +52 (5) 3 28 20 00
Fax +52 (5) 3 28 21 92
Fax +52 (5) 3 28 21 93

Peru

Lima 13
ESIM S.A., Dept. AUT,
Mr Paz-Soldan
Avda, N. Arriola 385 4to Piso
☎ +51 (14) 71 46 61
Fax +51 (14) 71 09 93

USA

Alpharetta, GA 30202
SIA Inc., Regional Sales Manager
Southeast, Mr Mich Gunyon,
Technology Drive
☎ +1 (4 04) 7 40 36 60
Fax +1 (4 04) 7 40 36 96

Andover, MA 01810
SIA Inc., North East Region,
Mr Mark Fondl, One Tech Drive,
Suite 310
☎ +1 (5 08) 6 85 60 77
Fax +1 (5 08) 6 86 88 72

Houston, TX 77040
SIA Inc., SouthWest Region,
Mr Wade Bradford
13100 Northwest Freeway, Suite 210
☎ +1 (713) 6 90 03 33
Fax +1 (713) 4 60 44 50

Mason, OH 45040-9011
SIA Inc., Central Region,
Mr Luther Crouthamel,
4770 Duke Drive suite 381
☎ +1 (5 13) 3 98 96 91
Fax +1 (5 13) 3 98 98 39

Mukilteo, WA 98275
SIA Inc., MidwWest Region,
Mr Earl Haas, 8412 54th Avenue West
☎ +1 (7 14) 9 79 66 00
Fax +1 (7 14) 5 57 90 61

Plymouth, MN 55442
SIA Inc., MidWest Region,
Mr Greg Jaster,
13235 45th Avenue No.
☎ +1 (7 08) 6 40 15 95
Fax +1 (7 08) 6 40 80 26

Venezuela

1071 Caracas
Siemens S.A., AUT-ASI,
Mr Jesus Cavada
Avda. Don Diego Cisneros
Urbanizacion Los Ruices,
Ap. 3616, Caracas 1010 A
☎ +58 (2) 2 39 07 33
Fax +58 (2) 2 03 82 00

Asia

China

510064 Guangzhou
Siemens Ltd. China, Guangzhou
Office, Mr Peter Chen,
Room 1134-1157 GARDEN Hotel
Garden Tower,
368 Huanshi Dong Lu
☎ +86 (20) 3 85 46 88
Fax +86 (20) 3 34 74 54

100015 Beijing
Siemens Ltd. China, Beijing Office,
Mr Wolfgang Söllner
7, Wangjing Zhonghuan Nan Lu
Chaoyang District
P.O. Box 8543
☎ +86 (10) 4 36 18 88
Fax +86 (10) 4 36 32 13

200090 Shanghai
Siemens Ltd. China, Shanghai
Office, Mr William Cui,
450, Lin Quing Lu
☎ +86 (21) 5 39 54 10
Fax +86 (21) 5 39 54 21

110001 Shenyang
Siemens Ltd. China, Shenyang
Office, Mr Ren Qi, Sakei Torch
Building 23rd Fl. 262A Shifu Da Lu
Shen He District
☎ +86 (24) 2 79 02 87
Fax +86 (24) 2 79 02 86

Hongkong

Hong Kong
Siemens Ltd. Hang Kong A. R. O.,
Automation System ,
Division , Mr Keiren Lake,
7th Floor, Regency Centre,
39 Wong Chuk Hang Road
☎ +85 (2) 28 70 76 11
Fax +85 (2) 25 18 04 11

India

Bangalore 560 001
Siemens Ltd., BAN/AUT-MAP,
Mr B. Sunderram
Jyoti Mahal, 3rd Floor
49, St. Marks Road, P.O.B. 5212
☎ +91 (80) 2 21 21 01
Fax +91 (80) 2 21 24 18

Bombay 400 018
Siemens Ltd., AUT/M-AP,
Mr S. Mistry
Head Office B Building
130, Ganpat Jahav Marg. Worli
☎ +91 (22) 4 93 13 50/60
Fax +91 (22) 4 95 08 22

Calcutta 700 071
Siemens Ltd., CAL/AUT-MAP,
Mr D. K. Ganguli
6, Little Russel Street, P.O.B. 715
☎ +91 (33) 2 47 83 74/-80
Fax +91 (33) 2 47 47 83

SIMATIC Partners Outside of Europe

New Delhi 110 002
Siemens Ltd., DEL/AUT-MAP,
Mr R. Narayanan
4A, Ring Road, I.P. Estate,
P.O.B. 7036
☎ +91 (11) 3 31 81 44
Fax +91 (11) 3 31 41 78

Indonesia

Jakarta 12870
Dian Graha Elektrika, Jakarta, Power
Eng. & Autom. Div., Mr M. Zafrullah
Jl. Gatot Subroto Kov. 74-75,
Mustika centre Building Floor 2a.,
P.O. Box 4267
☎ +62 (21) 8 30 65 74
Fax +62 (21) 8 30 74 02

Iran

15914 Teheran
Siemens S.S.K., Mr Din-Payuh
Khiabane Ayatollah Taleghani 32
Siemenshouse, P.O.B. 15875-4773, 15
Teheran
☎ +98 (21) 61 41
Fax +98 (21) 6 40 23 89

Japan

Tokyo 141-00
Siemens K.K., ATT, Mr Nakamichi
Siemens Fujikara Building, 8F
11-20, Nishi-Gotanda 2-chome
Shinagawa-ku
☎ +81 (3) 34 90 44 37
Fax +81 (3) 34 95 97 92

Pakistan

Karachi - 74400
Siemens Pakistan Eng. Co. Ltd.,
Power Division, Mr Ilyas
ILACO House
Abdullah Haroon Road
P.O. Box 7158
☎ +92 (21) 51 60 61
Fax +92 (21) 5 68 46 79

Philippines

Metro Manila
Siemens Inc., Mr B. Bonifacio
2nd & 4th Fl., Sterling Centre Bldg.
Esteban cor. de la Rosa
Legaspi Village
☎ +63 (2) 8 18 48 18
Fax +63 (2) 8 18 48 22

Saudi Arabia

Jeddah - 21412
Arabia Electric Ltd. Service Center,
Mr Kobeissi, P.O.B. 4621
☎ +9 66 (2) 6 65 84 20
Fax +9 66 (2) 6 65 84 90

Singapore

Singapore 1334
Siemens (Pte) Ltd. Singapore, AUT,
Mr Ulf Bexell,
2 Kallang Sector
☎ +65 8 41 35 28
Fax +65 8 41 35 29

South Korea

Seoul
Siemens Ltd., E+A, Mr Kang W. S.
Asia Tower Building, 9th Floor
726 Yeoksam-dong, Kang-nam-ku,
C.P.O. Box 3001
☎ +82 (2) 5 27 77 62
Fax +82 (2) 5 27 77 19

Taiwan

Taipei 106
Siemens Ltd., AUT 1, Mr Gulden
6th Fl., Cathy Life Insurance Bldg.
296, Jen Ai Road, Sec. 4
☎ +8 86 (2) 3 25 48 88
Fax +8 86 (2) 7 05 49 75

Thailand

Bangkok 10110
Berli Jucker Co. Ltd., Mr Narong
Berli Jucker House
99, Soi Rubia, Sukhumvit 42 Road
P.O. Box 173 BMC, Bangkok 1000
☎ +66 (2) 3 67 11 11
Fax +66 (2) 3 67 10 00

Vietnam

Hanoi
Siemens AG, Representation Office
Mr Nguyen Huang Giang
18, Phan Boi Chau Street
☎ +84 (4) 25 60 61
Fax +84 (4) 26 62 27

Australia

Adelaide
Siemens Ltd. Adelaide Office, CS/I.A.,
Mr J. Weiss, 315 Glen Osmond Road
Glenunga, S.A. 5064
☎ +61 (8) 3 79 66 66
Fax +61 (8) 3 79 08 99

Melbourne
Siemens Ltd., CS/I.A., Mr N. Gilholm,
544 Church Street
Richmond, Victoria 3121
☎ +61 (3) 4 20 75 20
Fax +61 (3) 4 20 75 00

Perth
Siemens Ltd., CS/I.A., Mr A. Lostrom
153, Burswood Road
Victoria Park, W.A. 6100
☎ +61 (9) 3 62 01 42
Fax +61 (9) 3 62 01 47

Sydney, N.S.W. 2064
Siemens Ltd. Sidney, Industrial
Automation, Mr Stephen Coop,
383 Pacific Highway, Artamon
☎ +61 (2) 4 36 78 04
Fax +61 (2) 4 36 86 24

New Zealand

Greenlane, Auckland 5
Siemens Ltd. Auckland Office,
CS/I.A., Mr A. Richmond
300 Great South Road
P.O.B 17-122
☎ +64 (9) 5 20 30 33
Fax +64 (9) 5 20 15 56

List of Abbreviations

K

Abbrevia-tions	Description
CP	Communication processor
CPU	Central processing unit
DB	Data block
FB	Function block
FC	Function
FM	Function module
FO	Fiber–optic cable
GD	Global data communication
IM	Interface module
IP	Intelligent I/O
LAD	Ladder logic (programming language representation in STEP 7)
M	Chassis ground
MPI	Multipoint Interface
OB	Organization block
OP	Operator panel
PG	Programming device
PII	Process–image input table
PIQ	Process–image output table
PS	Power supply
SFB	System function block
SFC	System function
SM	Signal module
STL	Statement List (programming language representation in STEP 7)

Glossary

Accumulator

The accumulators are registers in the → CPU and are used as intermediate memory for loading, transfer, comparison, calculation and conversion operations.

Address

An address is the identifier for a specific operand or operand area (e.g. input I 12.1, memory word MW 25, data block DB 3).

Analog module

Analog modules convert process values (e.g. temperature) into digital values, so that they can be processed by the central processing unit, or convert digital values into analog manipulated variables.

Automation system

An automation system is a → programmable controller in the context of SIMATIC S7.

Backplane bus

The backplane bus is a serial data bus over which the modules communicate and over which the necessary power is supplied to the modules. The connection between the modules is established by bus connectors.

Backup battery

The backup battery ensures that the→ user program in the → CPU is stored in the event of a power failure and that defined data areas and bit memories, timers and counters are retentive.

Backup memory

The backup memory provides a backup of memory areas for the → CPU without a backup battery. A configurable number of timers, counters, memories and data bytes (retentive timers, counters, memories and data bytes) is backed up.

Bit memory

Bit memories are part of the→ system memory of the CPU for storing interim results. They can be accessed in units of a bit, byte, word or doubleword.

Bus

A bus is a communication medium connecting several nodes. Data transmission can be serial or parallel across electrical conductors or fiber-optic cables.

Bus segment

A bus segment is a self-contained section of a serial bus system. Bus segments are interconnected using repeaters.

Chassis ground

Chassis ground is the totality of all the interconnected inactive parts of a piece of equipment on which a hazardous touch voltage cannot build up even in the event of a fault.

Clock memories

Memories that can be used for clocking purposes in the user program (1 memory byte).

Note

Note in the case of S7-300 CPUs that the clock memory byte is not exceeded in the user program.

Code block

A code block in SIMATIC S7 is a block which contains a section of the *STEP 7* user program (in contrast to a → data block which only contains data).

Communication processor

Communication processors are modules for point-to-point and bus links.

Compress

The programming device online function “Compress” is used to align all valid blocks contiguously in the RAM of the CPU at the start of the user memory. This eliminates all gaps which arose when blocks were deleted or modified.

Configuration

Assignment of modules to racks/slots and (e.g. for signal modules) addresses.

Consistent data

Data whose contents are related and which should not be separated are known as consistent data.

For example, the values of analog modules must always be handled consistently, that is the value of an analog module must not be corrupted by reading it out at two different times.

Counter

Counters are part of the → system memory of the CPU. The content of the “counter cells” can by modified by *STEP 7* instructions (e.g. count up/down).

CP

→ Communication processor

CPU

Central processing unit of the S7 programmable controller with open and closed-loop control systems, memory, operating system and interface for programming device.

Cycle time

The scan time is the time taken by the → CPU to scan the → user program once.

Data block

Data blocks (DB) are data areas in the user program which contain user data. Global data blocks can be accessed by all code blocks while instance data blocks are assigned to a specific FB call.

Data, static

Static data is data which can only be used within a function block. The data is saved in an instance data block belonging to the function block. The data stored in the instance data block is retained until the next function block call.

Data, temporary

Temporary data is local data of a block which is stored in the L stack during execution of a block and which is no longer available after execution.

Delay interrupt

→ Interrupt, time-delay

Device master file

All slave-specific characteristics are stored in a device master file (GSD file). The format of the device master file is defined in the EN 50170,
Volume 2, PROFIBUS standard.

Diagnostic buffer

The diagnostic buffer is a buffered memory area in the CPU in which diagnostic events are stored in the order of their occurrence.

Diagnostic interrupt

Diagnostics-capable modules use diagnostic interrupts to report system errors which they have detected to the → CPU.

Diagnostics

→ System diagnostics

DP master

A → master which behaves in accordance with EN 50170, Part 3 is known as a DP master.

DP slave

A → slave which is operated in the PROFIBUS bus system using the PROFIBUS-DP protocol and which behaves in accordance with EN 50170, Part 3 is known as a DP slave.

Equipotential bonding

Electrical connection (equipotential bonding conductor) which gives the bodies of electrical equipment and external conducting bodies the same or approximately the same potential, in order to prevent disturbing or dangerous voltages from being generated between these bodies.

Error display

The error display is one of the possible responses of the operating system to a → runtime error. The other possible responses are: → error response in the user program, STOP status of the CPU.

Error handling via OB

If the operating system detects a specific error (e.g. an access error with *STEP 7*), it calls the organization block (error OB) which is provided for this event and which specifies the subsequent behavior of the CPU.

Error response

Response to a → runtime error. The operating system can respond in the following ways: conversion of the programmable controller to the STOP mode, call of an organization block in which the user can program a response or display of the error.

External power supply

Power supply for the signal and function modules and the process peripherals connected to them.

FB

→ Function block

FC

→ Function

Flash EPROM

FEPROMs are the same as electrically erasable EEPROMS in that they can retain data in the event of a power failure, but they can be erased much more quickly (FEPROM = Flash Erasable Programmable Read Only Memory). They are used on → memory cards.

Force

The “Force” function overwrites a variable (e.g. memory marker, output) with a value defined by the S7 user. At the same time the variable is assigned write protection so that this value cannot be modified from any point (including from the STEP 7 user program). The value is retained after the programming device is disconnected. The write protection is not canceled until the “Unforce” function is called and the variable is written again with the value defined by the user program. During commissioning, for example, the “Force” function allows certain outputs to be set to the “ON” state for any length of time even if the logic operations of the user program are not fulfilled (e.g. because inputs are not wired).

Function

A function (FC) in accordance with IEC 1131-3 is a → code block without → static data. A function allows parameters to be passed in the user program. Functions are therefore suitable for programming complex functions, e.g. calculations, which are repeated frequently.

Function block

A function block (FB) in accordance with IEC 1131-3 is a → code block with → static data. An FB allows parameters to be passed in the user program. Function blocks are therefore suitable for programming complex functions, e.g. closed-loop controls, mode selections, which are repeated frequently.

Functional grounding

Grounding which has the sole purpose of safeguarding the intended function of the electrical equipment. Functional grounding short-circuits interference voltage which would otherwise have an impermissible impact on the equipment.

GD circle

A GD circle encompasses a number of CPUs which exchange data by means of global data communication and which are used as follows:

- One CPU sends a GD packet to the other CPUs.
- One CPU sends and receives a GD packet from another CPU.

A GD circle is identified by a GD circle number.

GD element

A GD element is generated by assigning the → global data to be shared and is identified by the global data identifier in the global data table.

GD packet

A GD packet can consist of one or more → GD objects which are transmitted together in a frame.

Global data

Global data is data which can be addressed from any → code block (FC, FB, OB). In detail, this refers to memories M, inputs I, outputs Q, timers, counters and data blocks DB. Absolute or symbolic access can be made to global data.

Global data communication

Global data communication is a procedure used to transfer → global data between CPUs (without CFBs).

Ground

The conducting earth whose electrical potential can be set equal to zero at any point.

In the vicinity of grounding electrodes, the earth can have a potential different to zero. The term “reference ground” is frequently used to describe these circumstances.

Ground (to)

To ground means to connect an electrically conducting component to the grounding electrode (one or more conducting components which have a very good contact with the earth) across a grounding system.

Instance data block

A data block, which is generated automatically, is assigned to each function block call in the *STEP 7* user program. The values of the input, output and in/out parameters are stored in the instance data block, together with the local block data.

Interface, multipoint

→ MPI

Interrupt

The → operating system of the CPU recognizes 10 different priority classes which control the execution of the user program. These runtime levels include interrupts, e.g. process interrupts. When an interrupt is triggered, the operating system automatically calls an assigned organization block in which the user can program the desired response (for example in an FB).

Interrupt, delay

The time-delay interrupt belongs to one of the priority levels for program execution in the SIMATIC S7 system. The interrupt is generated after expiry of a time delay started in the user program. A corresponding organization block is then executed.

Interrupt, diagnostic

→ Diagnostic interrupt

Interrupt, process

→ Process interrupt

Interrupt, time-of-day

The time-of-day interrupt belongs to one of the runtime levels for program execution on the SIMATIC S7 system. The interrupt is generated on a certain date (or daily) at a certain time (e.g. 9:50 or every hour, every minute). A corresponding organization block is then executed.

Interrupt, watchdog

A watchdog interrupt is generated periodically by the CPU in configurable time intervals. A corresponding → organization block is then executed.

Isolated

On isolated I/O modules, the reference potentials of the control and load circuits are galvanically isolated, for example by optocoupler, relay contact or transformer. Input/output circuits can be connected to a common potential.

Load memory

The load memory is part of the central processing unit. It contains objects generated by the programming device. It is implemented either as a plug-in memory card or a permanently integrated memory.

Local data

→ Data, temporary

Master

When they are in possession of the → token, masters can send data to other nodes and request data from other nodes (= active node).

Memory card

Memory cards are memory media in smart card format for CPUs and CPs. They are implemented as → RAM or → FEPROM.

Module parameters

Module parameters are values which can be used to control the response of the module. A distinction is made between static and dynamic module parameters.

MPI

The multipoint interface (MPI) is the programming device interface of SIMATIC S7. It enables the simultaneous operation of several stations (programming devices, text displays, operator panels) on one or more central processing units. Each station is identified by a unique address (MPI address).

MPI address

→ MPI

Nesting depth

One block can be called from another by means of a block call. Nesting depth is the number of → code blocks called at the same time.

Non-isolated

On non-isolated input/output modules, there is an electrical connection between the reference potentials of the control and load circuits.

OB

→Organization block

OB priority

The → operating system of the CPU distinguishes between various priority classes, such as cyclic program scanning, process interrupt-driven program scanning, etc. Each priority class is assigned → organization blocks (OB) in which the S7 user can program a response. The OBs have different standard priorities which determine the order in which they are executed or interrupted in the event that they are activated simultaneously.

Organization block

Organization blocks (OBs) represent the interface between the operating system of the CPU and the user program. The processing sequence of the user program is defined in the organization blocks.

Operating mode

The SIMATIC S7 programmable controllers have the following operating modes: STOP, →START-UP, RUN.

Operating system of the CPU

The operating system of the CPU organizes all functions and processes of the CPU which are not associated with a special control task.

Parameter

1. Variable of a *STEP 7* code block
2. Variable for setting the behavior of a module (one or more per module). Each module is delivered with a suitable default setting, which can be changed by configuring the parameters in *STEP 7*.

Parameters can be → static parameters or → dynamic parameters

Parameters, dynamic

Unlike static parameters, dynamic parameters of modules can be changed during operation by calling an SFC in the user program, for example limit values of an analog signal input module.

Parameters, static

Unlike dynamic parameters, static parameters of modules cannot be changed by the user program, but only by changing the configuration in *STEP 7*, for example the input delay on a digital signal input module.

PG

→ Programming device

Priority class

The operating system of an S7-CPU provides up to 26 priority classes (or "runtime levels") to which various organization blocks are assigned. The priority classes determine which OBs interrupt other OBs. If a priority class includes several OBs, they do not interrupt each other, but are executed sequentially.

PROFIBUS-DP

Digital, analog and intelligent modules of the programmable controller as well as a wide range of field devices to EN 50170, part 3, such as drivers or valve terminals, are installed in a distributed configuration in the direct vicinity of the process - across distances of up to 23 km (14.375 miles).

The modules and field devices are connected to the programmable controller via the PROFIBUS-DP fieldbus and addressed in the same way as centralized I/Os.

PLC

→ Programmable controller

Programmable controller

Programmable controllers (PLCs) are electronic controllers whose function is saved as a program in the control unit. The configuration and wiring of the unit are therefore independent of the function of the control system. The programmable controller has the structure of a computer; it consists of a → CPU (central processing unit) with memory, input/output groups and an internal bus system. The I/Os and the programming language are oriented to control engineering needs.

Process image

The process image is part of the → system memory of the CPU. The signal states of the input modules are written into the process-image input table at the start of the cyclic program. At the end of the cyclic program, the signal states in the process-image output table are transferred to the output modules.

Process interrupt

A process interrupt is triggered by interrupt-triggering modules on the occurrence of a specific event in the process. The process interrupt is reported to the CPU. The assigned → organization block is then processed in accordance with the priority of this interrupt.

Programming device

Programming devices are essentially personal computers which are compact, portable and suitable for industrial applications. They are equipped with special hardware and software for SIMATIC programmable controllers.

RAM

A RAM (random access memory) is a semiconductor read/write memory.

The following can be made retentive:

- Bit memories
- S7 timers (**not** for CPU 312 IFM)
- S7 counters
- Data areas (only with memory card or integral EPROM)

Reference ground

→ Ground

Reference potential

Potential with reference to which the voltages of participating circuits are observed and/or measured.

Restart

When a central processing unit is started up (e.g. by switching the mode selector from STOP to RUN or by switching the power on), organization block OB 100 (complete restart) is executed before cyclic program execution commences (OB 1). On a complete restart, the process-image input table is read in and the *STEP 7* user program is executed starting with the first command in OB 1.

Retentivity

A memory area is retentive if its contents are retained even after a power failure and a change from STOP to RUN. The non-retentive area of memory markers, timers and counters is reset following a power failure and a transition from the STOP mode to the RUN mode.

Runtime error

Error which occurs during execution of the user program on the programmable controller (and not in the process).

Segment

→ Bus segment

Set breakpoint

SFB

→ System function block

SFC

→ System function

Scan rate

The scan rate determines the frequency with which → GD packets are transmitted and received on the basis of the CPU cycle.

Signal module

Signal modules (SM) represent the interface between the process and the programmable controller. Input and output modules can be digital (input/output module, digital) or analog (input/output module, analog).

Slave

A slave can only exchange data with a → master when so requested by the master.

Start-up

RESTART mode is activated on a transition from STOP mode to RUN mode. Can be triggered by the → mode selector or after power on or an operator action on the programming device. In the case of the S7-300 a → restart is carried out.

STEP 7

Programming language for developing user programs for SIMATIC S7 PLCs.

Substitute value

Substitute values are configurable values which output modules transmit to the process when the CPU switches to STOP mode.

System diagnostics

System diagnostics is the term used to describe the detection, evaluation and signaling of errors which occur within the programmable controller. Examples of such errors are program errors or module failures. System errors can be displayed with LED indicators or in *STEP 7*.

System function

A system function (SFC) is a
→ function integrated in the operating system of the CPU that can be called, as required, in the STEP 7 user program.

System function block

A system function block (SFB) is a → function block which is integrated in the operating system of the CPU and which can be called in the STEP 7 user program as required.

System memory

The system memory is integrated on the central processing unit and implemented as a RAM memory. The system memory includes the operand areas (for example timers, counters, bit memories, etc.) as well as the data areas (for example communication buffers) required internally by the → operating system.

System state list

The system status list contains data describing the current status of an S7-300. You can use it to gain an overview of the following at any time:

- The S7-300 configuration
- The current parameterization of the CPU and the parameterizable signal modules
- The current statuses and sequences in the CPU and the parameterizable signal modules.

Terminating resistor

A terminating resistor is a resistor used to terminate a data communication line in order to prevent reflection.

Time-of-day interrupt

→ Interrupt, time-of-day

Timer

→ Times

Times (timer cells)

Times are part of the → system memory of the CPU. The contents of the “timer cells” are updated automatically by the operating system asynchronously to the user program. *STEP 7* instructions are used to define the exact function of the timer cells (for example on-delay) and initiate their execution (e.g. start).

Token

Access right on bus

Transmission rate

Rate of data transfer (bps)

Ungrounded

Having no galvanic connection to ground

User memory

The user memory contains the → code and → data blocks of the user program. The user memory can be integrated in the CPU or can be provided on plug-in memory cards or memory modules. The user program is always executed in the → working memory of the CPU, however.

User program

The SIMATIC system distinguishes between the → operating system of the CPU and user programs. The latter are created with the programming software → *STEP 7* in the available programming languages (ladder logic and statement list) and saved in code blocks. Data are stored in data blocks.

Varistor

Voltage-independent resistor

Version

The product version differentiates between products which have the same order number. The product version is increased with each upwardly compatible function extension, production-related modification (use of new components) or bug-fix.

Watchdog interrupt

→ Interrupt, watchdog

Working memory

The working memory is a random-access memory in the → CPU which the processor accesses during program execution.

In the event of an input access error, a substitute value can be written to the accumulator instead of the input value which could not be read (SFC 44).

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Please give each of the following questions your own personal mark within the range from 1 (very good) to 5 (poor).

1. Do the contents meet your requirements? ☐
2. Is the information you need easy to find? ☐
3. Is the text easy to understand? ☐
4. Does the level of technical detail meet your requirements? ☐
5. Please rate the quality of the graphics/tables: ☐

Additional comments:

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