FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13710-2E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90580C Series

MB90583C/583CA/F583C/F583CA/587C/587CA/V580B

■ DESCRIPTION

The MB90580C series is a line of general-purpose, Fujitsu 16-bit microcontrollers designed for process control applications which require high-speed real-time processing, such as consumer products.

While inheriting the AT architecture of the F²MC*1 family, the instruction set for the F²MC-16LX CPU core of the MB90580C series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90580C has an on-chip 32-bit accumulator which enables processing of long-word data.

The peripheral resources integrated in the MB90580C series include: an 8/10-bit A/D converter, an 8-bit D/A converter, UARTs (SCI) 0 to 4, an 8/16-bit PPG timer, 16-bit I/O timers (16-bit free-run timer, input capture units (ICUs) 0 to 3, output compare units (OCUs) 0 and 1), and an IEBus™ controller *2.

Notes: *1: F²MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.
*2: IEBus™ is a trademark of NEC Corporation.

■ FEATURES

- Minimum execution time: 62.5 ns/4 MHz oscillation (Uses PLL clock multiplication) maximum multiplier = 4
- Maximum memory space
  16 Mbyte
  Linear/bank access

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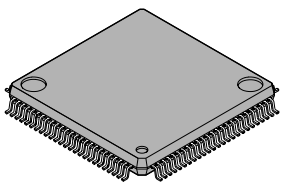
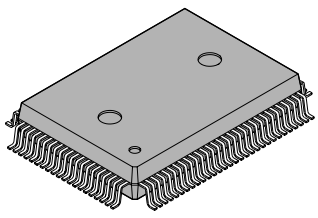
■ PACKAGES

100-pin plastic LQFP



(FPT-100P-M05)

100-pin plastic QFP



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- Instruction set optimized for controller applications
  Supported data types: bit, byte, word, and long-word types
  Standard addressing modes: 23 types
  32-bit accumulator enhancing high-precision operations
  Signed multiplication/division and extended RETI instructions
- Enhanced high level language (C) and multitasking support instructions
  Use of a system stack pointer
  Symmetrical instruction set and barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4 byte instruction queue
- Enhanced interrupt function
  Up to eight priority levels programmable
  External interrupt inputs: 8 lines
- Automatic data transmission function independent of CPU operation
  Up to 16 channels for the extended intelligent I/O service
  DTP request inputs: 8 lines
- Internal ROM
  FLASH: 128 Kbyte
  MASKROM: 128 Kbyte (MB90583C/CA) , 64 Kbyte (MB90587C/CA)
- Internal RAM
  FLASH: 6 Kbyte
  MASKROM: 6 Kbyte (MB90583C/CA) , 4 Kbyte (MB90587C/CA)
- General-purpose ports
  Up to 77 channels (Input pull-up resistor settable for: 22 channels. Output open drain settable for: 8 channels)
- IEBus™ controller*
  Three different data transfer rates selectable
  Mode 0: 3.9 Kbps (16 bytes/frame)
  Mode 1: 17.0 Kbps (32 bytes/frame)
  Mode 2: 26.0 Kbps (128 bytes/frame)
  *: IEBus™ is a trademark of NEC Corporation.
- A/D Converter (RC) : 8 ch
  8/10-bit resolution
  Conversion time: 34.7 µs (Min.) , 12 MHz operation
- D/A Converter: 2 ch
  8-bit resolutions
  Setup time: 12.5 µs
- UART : 5 ch
- 8/16 bit PPG : 1 ch
  8 bits × 2 channels: 16 bits × 1 channel: Mode switching function provided
- 16 bit reload timer: 3 ch
- 16-bit PWC timer: 1 channel
  Noise filter provided. Available to pulse width counter
- 16 bit I/O timer
  Input capture : 4 ch
  Output compare : 2 ch
  Free run timer: 1 ch
- Internal clock generator
- Time-base counter/watchdog timer: 18-bit

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- Clock monitor function integrated
- Low-power consumption mode
  Sleep mode
  Stop mode
  Hardware standby mode
  CPU intermittent operation mode
- Package: LQFP-100 / QFP-100
- CMOS technology

■ PRODUCT LINEUP

Item \ Part number	MB90587C/CA	MB90583C/CA	MB90F583C/CA	MB90V580B
Classification	Mass-produced products (MASK ROM)		Mass-produced products (Flash ROM)	Development/ evaluation product
ROM size	64 Kbytes	128 Kbytes	128 Kbytes	None
RAM size	4 Kbytes	6 Kbytes	6 Kbytes	6 Kbytes
Clock*1	Two clocks / one clock system	Two clocks / one clock system	Two clocks / one clock system	Two clocks system
Emulator-specific power supply *2	—	—	—	None
CPU functions	The number of instructions: 340 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock of 16 MHz) Interrupt processing time: 1.5 ms (at machine clock of 16 MHz, minimum value)			
Ports	General-purpose I/O ports (CMOS output) : 45 General-purpose I/O port (Can be set as open-drain) : 8 General-purpose I/O ports (Input pull-up resistors available) : 22 Total: : 77			
IEBus™ controller	None	Communication mode: Half-duplex, asynchronous communication Multi-master system Access control: CDMA/CD Three modes selectable for different transmission speeds Transmit buffer: 8-byte FIFO buffer Receive buffer: 8-byte FIFO buffer		
Timebase timer	18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (At oscillation of 4 MHz)			
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)			
Clock timer	15-bit counter Interrupt interval: 1 s, 0.5 s, 0.25 s, 31.25 ms (At oscillation of 32.768 kHz)			
8/16-bit PPG timer	Number of channels: 1 (8-bit × 2 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: 62.5 ns to 1 ms (at oscillation of 4 MHz, machine clock of 16 MHz)			
16-bit reload timer	Number of channels: 3 Event count provided Interval: 125 ns to 131 ms (at oscillation of 4 MHz, machine clock of 16 MHz)			
PWC timer	Number of channels: 1 Timer function (select the counter timer from three internal clocks.) Pulse width measuring function (select the counter timer from three internal clocks.)			

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Item \ Part number		MB90587C/CA	MB90583C/CA	MB90F583C/CA	MB90V580B
16-bit I/O timer	16-bit free run timer	Number of channels: 1 Overflow interrupts			
	Output compare (OCU)	Number of channels: 2 Pin input factor: A match signal of compare register			
	Input capture (ICU)	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)			
DTP/external interrupt circuit		Number of inputs: 8 Started by a rising edge, a falling edge, an “H” level input, or an “L” level input. External interrupt circuit or extended intelligent I/O service (EI^{2}OS) can be used.			
Delayed interrupt generation module		An interrupt generation module for switching tasks used in real time operating systems.			
UART0, 1, 2, 3, 4		Clock synchronized transmission (62.5 Kbps to 1 Mbps) Clock asynchronized transmission (1202 bps to 9615 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.			
A/D converter		Resolution: 8/10-bit changeable Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Scan conversion mode (converts two or more successive channels and can program up to 8 channels.) Continuous conversion mode (converts selected channel repeatedly) Stop conversion mode (converts selected channel and stop operation repeatedly)			
D/A converter		8-bit resolution Number of channels: 2 channels Based on the R-2R system			
Low-power consumption (standby) mode		Sleep/stop/CPU intermittent operation/clock timer/hardware standby			
Process		CMOS			
Power supply voltage for operation		4.5 V to 5.5 V*3			

*1: Connect the oscillator to both terminals XA0 and XA1 for MB90F587C / 583C / F583C.

*2: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3: Varies with conditions such as the operating frequency (See section “■ ELECTRICAL CHARACTERISTICS”).
Assurance for the MB90V580B is given only for operation with a tool at a power supply voltage of 4.5 V to 5.5 V, an operating temperature of 0 to +25 °C, and an operating frequency of 1 MHz to 16 MHz.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90583C/CA	MB90587C/CA	MB90F583C/CA
FPT-100P-M05	○	○	○
FTP-100P-M06	○	○	○

○ : Available ×: Not available

Note: For more information about each package, see section “■ PACKAGE DIMENSIONS”.

■ DIFFERENCES AMONG PRODUCTS

Memory Size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

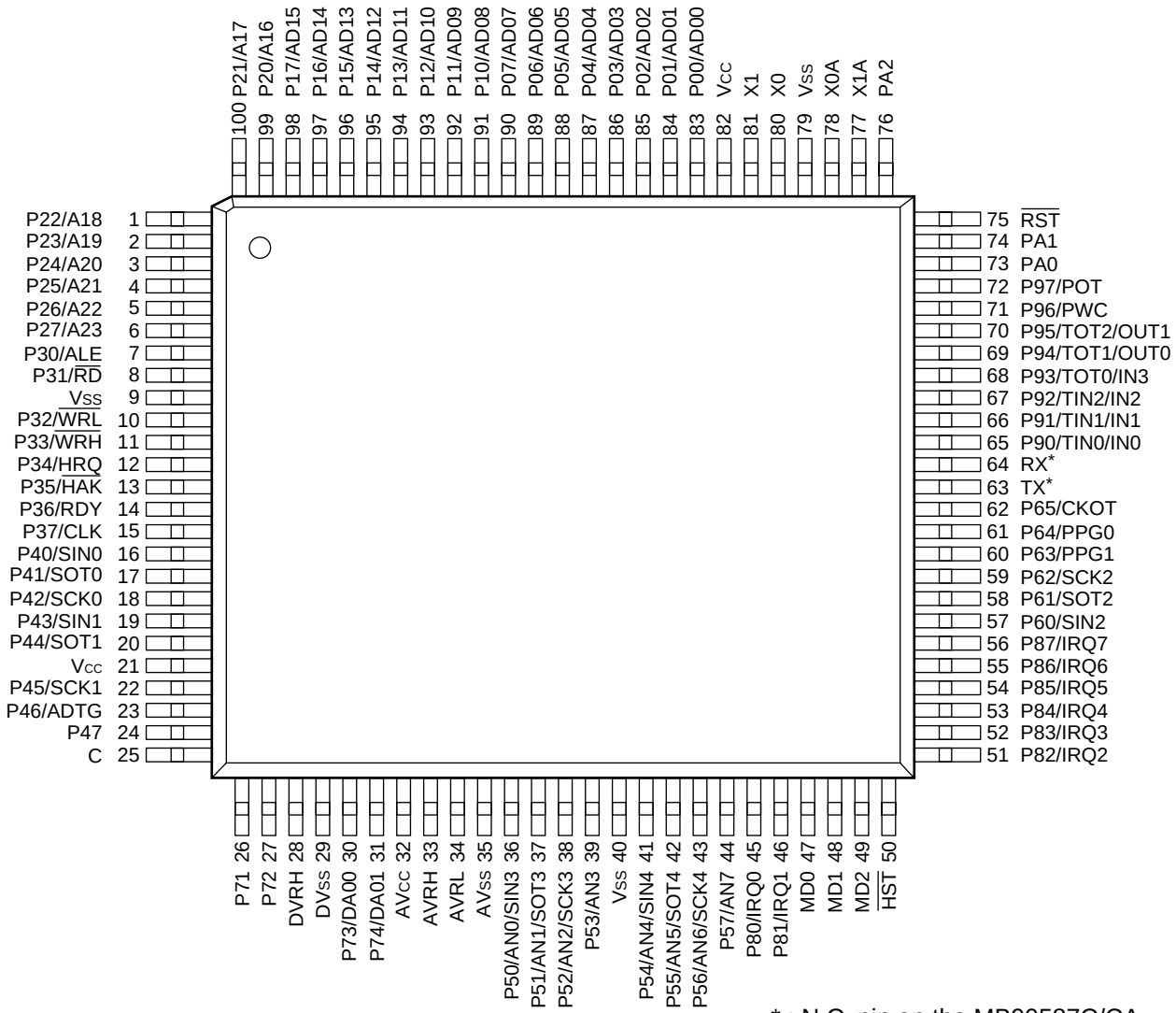
- The MB90V580B does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V580B, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF3FFF_H$ to mapped to bank FE and FF only. (This setting can be changed by configuring the development tool.)
- In the MB90583C/583CA/587C/587CA/F583C/F583CA, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FF0000_H$ to $FF3FFF_H$ to bank FF only.

IEBus™ Controller

- MB90587C/CA does not have an IEBus™ Controller.

■ PIN ASSIGNMENT

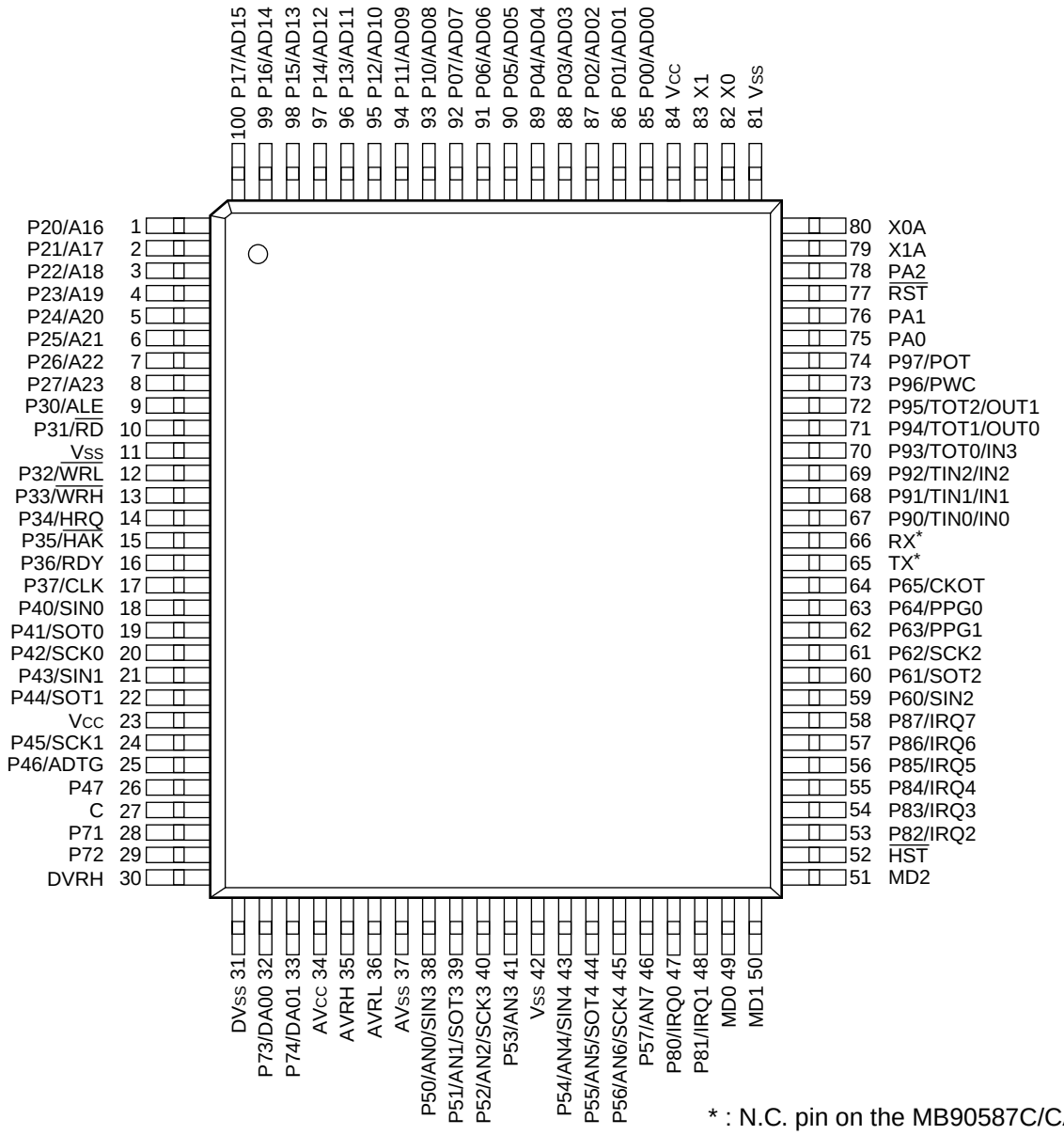
(TOP VIEW)



* : N.C. pin on the MB90587C/CA

(FPT-100P-M05)

(TOP VIEW)



* : N.C. pin on the MB90587C/CA

(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	LQFP*2			
82	80	X0	A	Oscillator pin
83	81	X1	A	Oscillator pin
52	50	$\overline{HST}$	C	Hardware standby input pin
77	75	$\overline{RST}$	B	Reset input pin
85 to 92	83 to 90	P00 to P07	D (CMOS/H)	General-purpose I/O ports. A pull-up resistor can be assigned (RD07 to RD00=“1”) by the pull-up resistor setting register (RDR0). [These pins are disabled with the output setting (DDR0 register: D07 to D00=“1”).]
		AD00 to AD07		In external bus mode, the pins function as the lower data I/O or lower address outputs (AD00 to AD07).
93 to 100	91 to 98	P10 to P17	D (CMOS/H)	General-purpose I/O ports. A pull-up resistor can be assigned (RD17 to RD10=“1”) by the pull-up resistor setting register (RDR1). [These pins are disabled with the output setting (DDR1 register: D17 to D10 =“1”).]
		AD08 to AD15		In 16-bit external bus mode, the pins function as the upper data I/O or middle address outputs (AD08 to AD15).
1 to 8	99,100, 1 to 6	P20 to P27	F (CMOS/H)	General-purpose I/O ports In external bus mode, pins for which the corresponding bit in the HACR register is “1” function as the A16 to A23 pins.
		A16 to A23		In external bus mode, pins for which the corresponding bit in the HACR register is “1” function as the upper address output pins (A16 to A23).
9	7	P30	F (CMOS/H)	General-purpose I/O port Functions as the ALE pin in external bus mode.
		ALE		Functions as the address latch enable signal pin (ALE) in external bus mode.
10	8	P31	F (CMOS/H)	General-purpose I/O port Functions as the $\overline{RD}$ pin in external bus mode.
		$\overline{RD}$		Functions as the read strobe output pin ($\overline{RD}$) in external bus mode.
12	10	P32	F (CMOS/H)	General-purpose I/O port Functions as the $\overline{WRL}$ pin in external bus mode if the WRE bit is “1”.
		$\overline{WRL}$		Functions as the lower data write strobe output pin ($\overline{WRL}$) in external bus mode.
13	11	P33	F (CMOS/H)	General-purpose I/O port Functions as the $\overline{WRH}$ pin in 16-bit external bus mode if the WRE bit in the EPCR register is “1”
		$\overline{WRH}$		Functions as the upper data write strobe output pin ($\overline{WRH}$) in external bus mode.

*1: FPT-100P-M06

*2: FPT-100P-M05

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Pin no.		Pin name	Circuit type	Function
QFP*1	LQFP*2			
14	12	P34	F (CMOS/H)	General-purpose I/O port Functions as the HRQ pin in external bus mode if the HDE bit in the EPCR register is “1”.
		HRQ		Functions as the hold request input pin (HRQ) in external bus mode.
15	13	P35	F (CMOS/H)	General-purpose I/O port Functions as the $\overline{\text{HAK}}$ pin in external bus mode if the HDE bit in the EPCR register is “1”.
		$\overline{\text{HAK}}$		Functions as the hold acknowledge output pin ($\overline{\text{HAK}}$) in external bus mode.
16	14	P36	F (CMOS/H)	General-purpose I/O port Functions as the RDY pin in external bus mode if the RYE bit in the EPCR register is “1”.
		RDY		Functions as the external ready input pin (RDY) in external bus mode.
17	15	P37	F (CMOS/H)	General-purpose I/O port Functions as the CLK pin in external bus mode if the CKE bit in the EPCR register is “1”.
		CLK		Functions as the machine cycle clock output pin (CLK) in external bus mode.
18	16	P40	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD40 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D40=“0”).]
		SIN0		UART0 serial data input (SIN0) pin. When UART0 is operating for input, this input is used as required and thus the output from any other function to the pin must be off unless used intentionally.
19	17	P41	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD41 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D41=“0”).]
		SOT0		UART0 serial data output pin (SOT0). This pin is enabled with the UART0 serial data output enabled.
20	18	P42	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD42 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D42=“0”).]
		SCK0		UART0 serial clock I/O pin (SCK0). This pin is enabled with the UART0 clock output enabled.

*1: FPT-100P-M06

*2: FPT-100P-M05

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Pin no.		Pin name	Circuit type	Function
QFP*1	LQFP*2			
21	19	P43	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD43 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D43=“0”).]
		SIN1		UART1 serial data input (SIN1) pin. When UART1 is operating for input, this input is used as required and thus the output from any other function to the pin must be off unless used intentionally.
22	20	P44	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD44 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D44=“0”).]
		SOT1		UART1 serial data output pin (SOT1). This pin is enabled with the UART1 serial data output enabled.
24	22	P45	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD45 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D45=“0”).]
		SCK1		UART1 serial clock I/O pin (SCK1). This pin is enabled with the UART1 clock output enabled.
25	23	P46	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD46 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D46=“0”).]
		ADTG		External trigger input pin (ADTG) for the A/D converter.
26	24	P47	E (CMOS/H)	General-purpose I/O port. This pin serves as an open-drain output port with OD47 in the open-drain control setting register (ODR4) set to “1”. [The pin is disabled with the input setting (DDR4 register: D47=“0”).]
38	36	P50	G (CMOS/H)	General-purpose I/O port.
		AN0		Analog input pin (AN0) for use during A/D converter operation.
		SIN3		UART3 serial data input pin (SIN3). When UART3 is operating for input, this input is used as required and thus the output from any other function to the pin must be off unless used intentionally.
39	37	P51	G (CMOS/H)	General-purpose I/O port.
		AN1		Analog input pin (AN1) for use during A/D converter operation.
		SOT3		UART3 serial data output pin (SOT3). This pin is enabled with the UART3 serial data output enabled.

*1: FPT-100P-M06

*2: FPT-100P-M05

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Pin no.		Pin name	Circuit type	Function
QFP*1	LQFP*2			
40	38	P52	G (CMOS/H)	General-purpose I/O port.
		AN2		Analog input pin (AN2) for use during A/D converter operation.
		SCK3		UART3 serial clock I/O pin (SCK3). This pin is enabled with the UART3 clock output enabled.
41	39	P53	G (CMOS/H)	General-purpose I/O port.
		AN3		Analog input pin (AN3) for use during A/D converter operation.
43	41	P54	G (CMOS/H)	General-purpose I/O port.
		AN4		Analog input pin (AN4) for use during A/D converter operation.
		SIN4		UART4 serial data input pin (SIN4). When UART4 is operating for input, this input is used as required and thus the output from any other function to the pin must be off unless used intentionally.
44	42	P55	G (CMOS/H)	General-purpose I/O port.
		AN5		Analog input pin (AN5) for use during A/D converter operation.
		SOT4		UART4 serial data output pin (SOT4). This pin is enabled with the UART4 serial data output enabled.
45	43	P56	G (CMOS/H)	General-purpose I/O port.
		AN6		Analog input pin (AN6) for use during A/D converter operation.
		SCK4		UART4 serial clock output pin (SCK4). This pin is enabled with the UART4 clock output enabled.
46	44	P57	G (CMOS/H)	General-purpose I/O port.
		AN7		Analog input pin (AN7) for use during A/D converter operation.
27	25	C	—	0.1 μF capacitor coupling pin for regulating the power supply.
28	26	P71	F (CMOS/H)	General-purpose I/O port.
29	27	P72	F (CMOS/H)	General-purpose I/O port.
32	30	P73	H (CMOS/H)	General-purpose I/O port. This pin serves as a D/A output pin (DA00) when the DAE0 bit in the D/A control register (DACR) is “1”.
		DA00		D/A converter output 0 (DA00) pin.
33	31	P74	H (CMOS/H)	General-purpose I/O port. This pin serves as a D/A output pin (DA01) when the DAE1 bit in the D/A control register (DACR) is “1”.
		DA01		D/A converter output 1 pin (DA01).
47	45	P80	F (CMOS/H)	General-purpose I/O port.
		IRQ0		Functions as external interrupt request input 0 pin (IRQ0).

*1: FPT-100P-M06

*2: FPT-100P-M05

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Pin no.		Pin name	Circuit type	Function
QFP*1	LQFP*2			
48	46	P81	F (CMOS/H)	General-purpose I/O port.
		IRQ1		Functions as external interrupt request input 1 pin (IRQ1).
53	51	P82	F (CMOS/H)	General-purpose I/O port.
		IRQ2		Functions as external interrupt request input 2 pin (IRQ2).
54	52	P83	F (CMOS/H)	General-purpose I/O port.
		IRQ3		Functions as external interrupt request input 3 pin (IRQ3).
55	53	P84	F (CMOS/H)	General-purpose I/O port.
		IRQ4		Functions as external interrupt request input 4 pin (IRQ4).
56	54	P85	F (CMOS/H)	General-purpose I/O port.
		IRQ5		Functions as external interrupt request input 5 pin (IRQ5).
57	55	P86	F (CMOS/H)	General-purpose I/O port.
		IRQ6		Functions as external interrupt request input 6 pin (IRQ6).
58	56	P87	F (CMOS/H)	General-purpose I/O port.
		IRQ7		Functions as external interrupt request input 7 pin (IRQ7).
59	57	P60	D (CMOS/H)	General-purpose I/O port. A pull-up resistor can be assigned (RD60="1") by the pull-up resistor setting register (RDR6). [This pin is disabled with the output setting (DDR6 register: D60="1").]
		SIN2		UART2 serial data input pin (SIN2). When UART2 is operating for input, this input is used as required and thus the output from any other function to the pin must be off unless used intentionally.
60	58	P61	D (CMOS/H)	General-purpose I/O port. A pull-up resistor can be assigned (RD61="1") by the pull-up resistor setting register (RDR6). [This pin is disabled with the output setting (DDR6 register: D61="1").]
		SOT2		UART2 serial data output pin (SOT2). This pin is enabled with the UART2 serial data output enabled.
61	59	P62	D (CMOS/H)	General-purpose I/O port. A pull-up resistor can be assigned (RD62="1") by the pull-up resistor setting register (RDR6). [This pin is disabled with the output setting (DDR6 register: D62="1").]
		SCK2		UART2 serial clock I/O pin (SCK2). This pin is enabled with the UART2 clock output enabled.

*1: FPT-100P-M06

*2: FPT-100P-M05

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Pin no.		Pin name	Circuit type	Function
QFP*1	LQFP*2			
62	60	P63	D (CMOS/H)	General-purpose I/O port. A pull-up resistor can be assigned (RD63="1") by the pull-up resistor setting register (RDR6). [This pin is disabled with the output setting (DDR6 register: D63="1").]
		PPG1		The pin serves as the PPG1 output when PPGs are enabled.
63	61	P64	D (CMOS/H)	General-purpose I/O port. A pull-up resistor can be assigned (RD64="1") by the pull-up resistor setting register (RDR6). [This pin is disabled with the output setting (DDR6 register: D64="1").]
		PPG0		The pin serves as the PPG0 output when PPGs are enabled.
64	62	P65	D (CMOS/H)	General-purpose I/O port. A pull-up resistor can be assigned (RD65="1") by the pull-up resistor setting register (RDR6). [This pin is disabled with the output setting (DDR6 register: D65="1").]
		CKOT		This pin serves as the CKOT output during CKOT operation.
65	63	TX*3	I	This pin serves as the IEBus™ output.
66	64	RX*3	J (CMOS)	This pin serves as the IEBus™ input.
67 to 69	65 to 67	P90 to P92	F (CMOS/H)	General-purpose I/O port.
		TIN0 to TIN2		Event input pins for reload timers 0, 1, and 2. During reload timer input, these inputs are used continuously and thus the output from any other function to the pins must be avoided unless used intentionally.
		IN0 to IN2		Trigger inputs for input capture channels 0 to 2
70	68	P93	F (CMOS/H)	General-purpose I/O port.
		TOT0		Reload timer output pin. This function is applied when the output for reload timer 0 is enabled.
		IN3		Trigger inputs for input capture channel 3.
71, 72	69, 70	P94, P95	F (CMOS/H)	General-purpose I/O port.
		TOT1, TOT2		Reload timer output pins. This function is applied when the output for reload timer 1 and 2 are enabled.
		OUT0, OUT1		Event output for channel 0 and 1 of the output compare
73	71	P96	F (CMOS/H)	General-purpose I/O port.
		PWC		This pin serves as the PWC input with the PWC timer enabled.

*1: FPT-100P-M06

*2: FPT-100P-M05

*3: N.C. pin on the MB90587C/CA.

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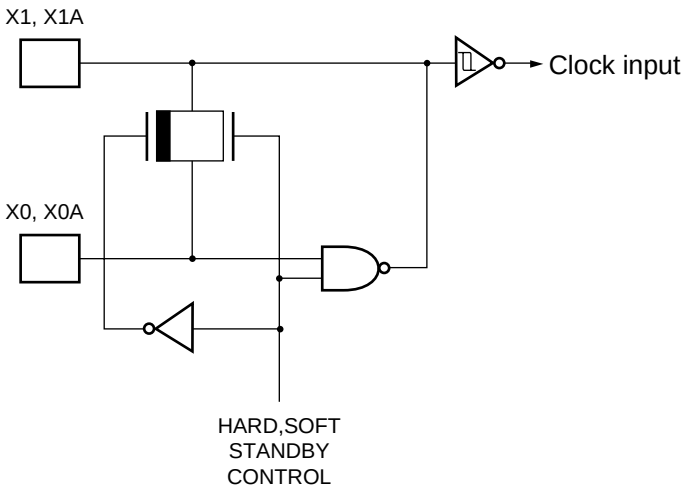
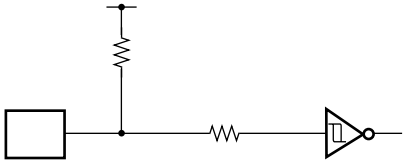
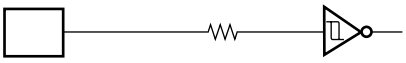
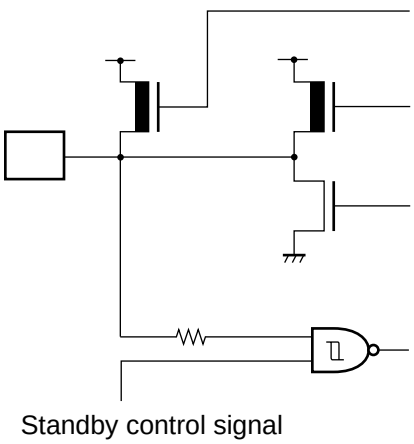
Pin no.		Pin name	Circuit type	Function
QFP*1	LQFP*2			
74	72	P97	F (CMOS/H)	General-purpose I/O port.
		POT		This pin serves as the PWC output with the PWC timer enabled.
75, 76	73, 74	PA0, PA1	F (CMOS/H)	General-purpose I/O port.
78	76	PA2	F (CMOS/H)	General-purpose I/O port.
79	77	X1A	A	Oscillation input pin. Leave the terminal open for the one clock system parts.
80	78	X0A	A	Oscillation input pin. Pull-down the terminal externally for the one clock system parts.
34	32	AV_{CC}	—	A/D converter power supply pin.
37	35	AV_{SS}	—	A/D converter power supply pin.
35	33	AVRH	—	A/D converter external reference power supply pin.
36	34	AVRL	—	A/D converter external reference power supply pin.
30	28	DVRH	—	D/A converter external reference power supply pin.
31	29	DV_{SS}	—	D/A converter power supply pin.
49 to 51	47 to 49	MD0 to MD2	C	Input pin for specifying the operation mode. Connect these pins directly to Vcc or Vss.
23, 84	21, 82	V_{CC}	—	Power supply (5 V) input pin.
11, 42, 81	9, 40, 79	V_{SS}	—	Power supply (0 V) input pin.

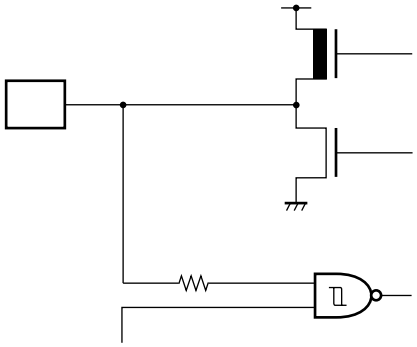
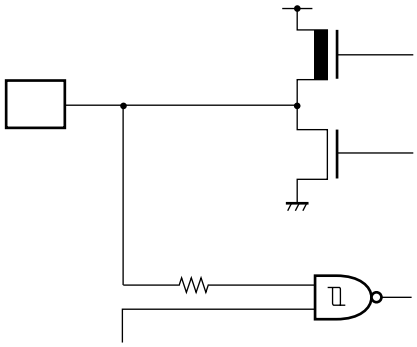
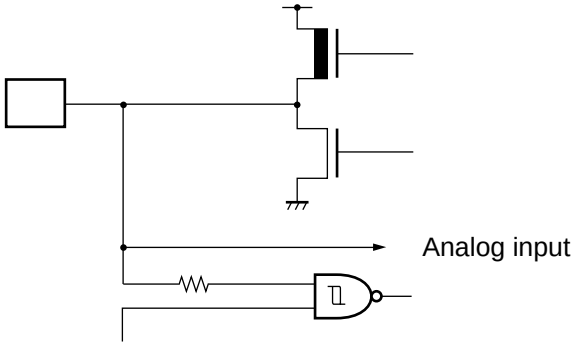
*1: FPT-100P-M06

*2: FPT-100P-M05

■ I/O CIRCUIT TYPE

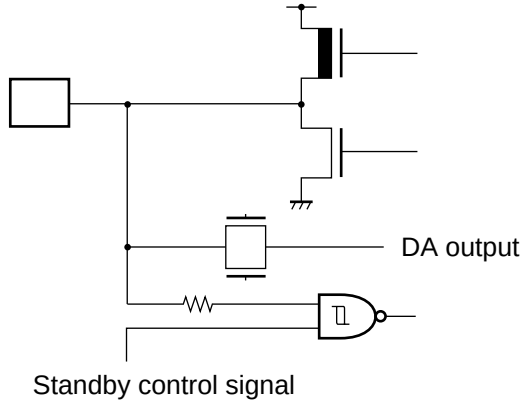
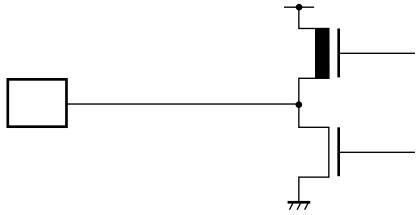
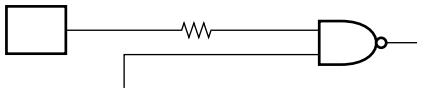
Type	Circuit	Remarks
A		• Oscillation feedback resistance : Approx. 1 MΩ
B		• Hysteresis input with pull-up Resistance approx. 50 kΩ
C		• Hysteresis input
D		• Incorporates pull-up resistor control (for input) • CMOS level output • Hysteresis input with standby control Resistance approx. 50 kΩ

(Continued)

Type	Circuit	Remarks
E		• CMOS level output • Hysteresis input with standby control • Incorporates open-drain control
F		• CMOS level output • Hysteresis input with standby control
G		• CMOS level output • Hysteresis input with standby control • Analog input

(Continued)

(Continued)

Type	Circuit	Remarks
H		• CMOS level output • Hysteresis input with standby control • DA output
I		• CMOS level output
J		• CMOS input with standby control

■ HANDLING DEVICES

1. Preventing Latchup

CMOS ICs may cause latchup in the following situations:

- When a voltage higher than Vcc or lower than Vss is applied to input or output pins.
- When a voltage exceeding the rating is applied between Vcc and Vss.
- When AVcc power is supplied prior to the Vcc voltage.

If latchup occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let it occur.

For the same reason, also be careful not to let the analog power-supply voltage exceed the digital power-supply voltage.

2. Handling unused input pins

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.

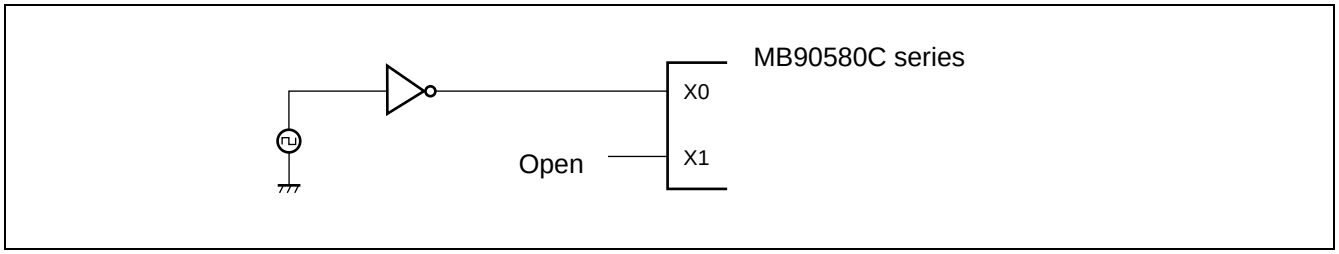
Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

3. Treatment of the TX and RX pins with the IEBus™ unused

When the IEBus is not used, connect a pull-down resistor to the TX pin and a pull-down/pull-up resistor to the RX pin.

4. Use of the external clock

When the device uses an external clock, drive only the X0 pin while leaving the X1 pin open (See the illustration below).

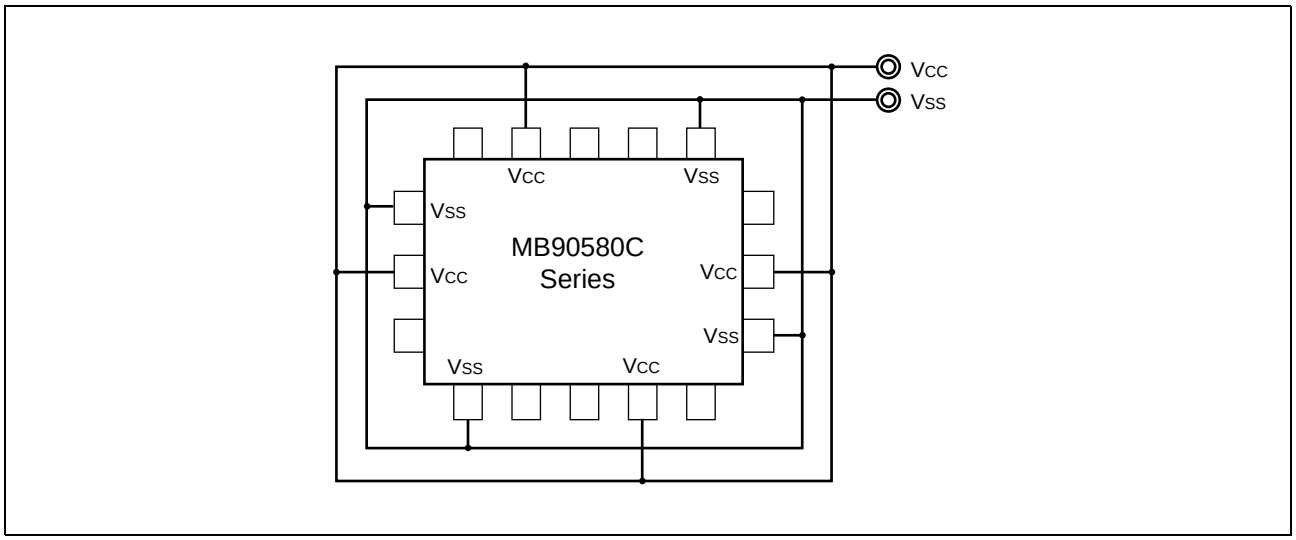


5. Power Supply Pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 µF between V_{CC} and V_{SS} pin near the device.



6. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with an grand area for stabilizing the operation.

7. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AV_{SS}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage of AVRH dose not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

8. Connection of Unused Pins of A/D Converter

Connect unused pin of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

9. Connection of Unused Pins of D/A Converter

Connect unused pin of D/A converter to $DVRH = V_{SS}$, $DV_{SS} = V_{SS}$.

10. N.C. Pin

The N.C. (internally connected) pin must be opened for use.

11. Notes on Energization

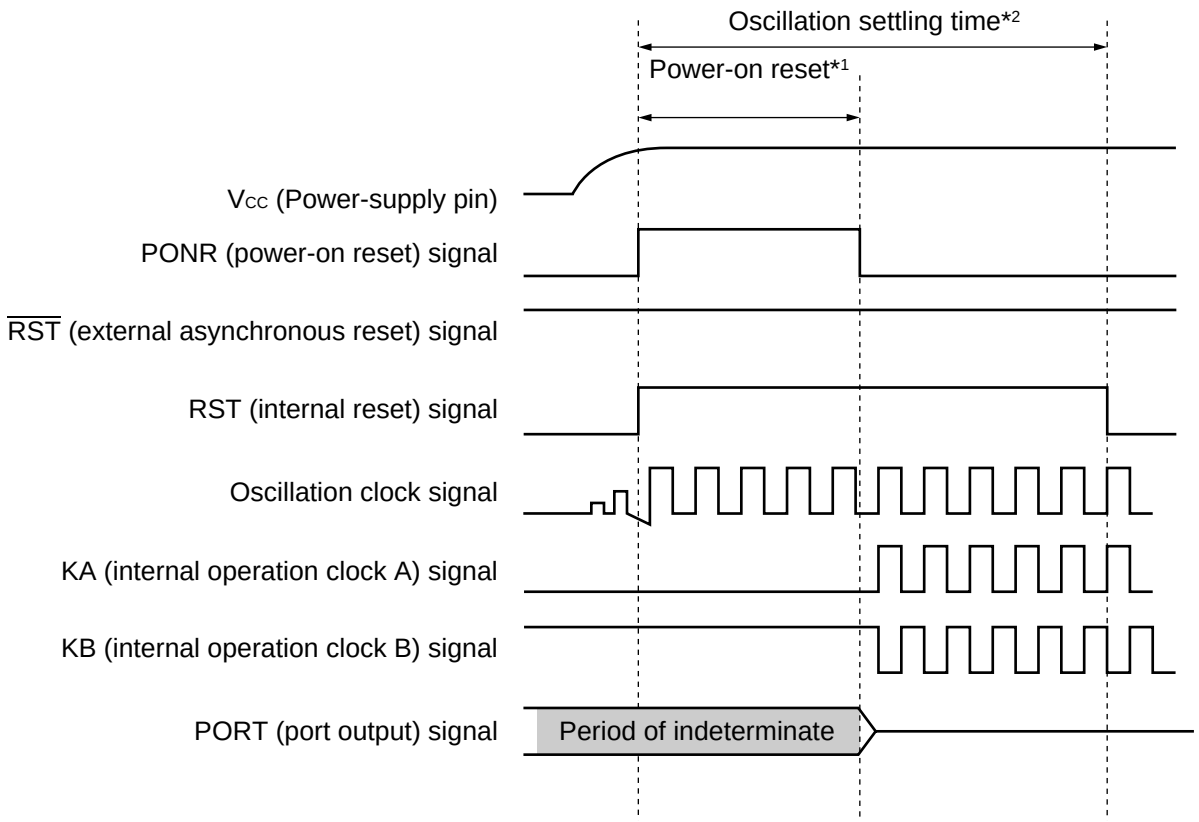
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

12. Use of the sub-clock

Use the one clock system parts when the sub-clock is not used. Connected the oscillator under 32 kHz to the both terminals XA0 and X1A for the two clocks system parts. Pull-down the terminal X0A and leave the terminal X0A open for the one clock system parts.

13. Indeterminate outputs from ports 0 and 1

The outputs from ports 0 and 1 become indeterminate during a power-on reset after the power is turned on. Pay attention to the port output timing shown as follow.



*1: Power-on reset time: Period of “clock frequency x 2^{17}” (Clock frequency of 16 MHz: 8.192 ms)
*2: Oscillation settling time: Period of “clock frequency x 2^{18}” (Clock frequency of 16 MHz: 16.384 ms)

14. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers turning on the power again.

15. Return from standby state

If the power-supply voltage goes below the standby RAM holding voltage in the standby state, the device may fail to return from the standby state. In this case, reset the device via the external reset pin to return to the normal state.

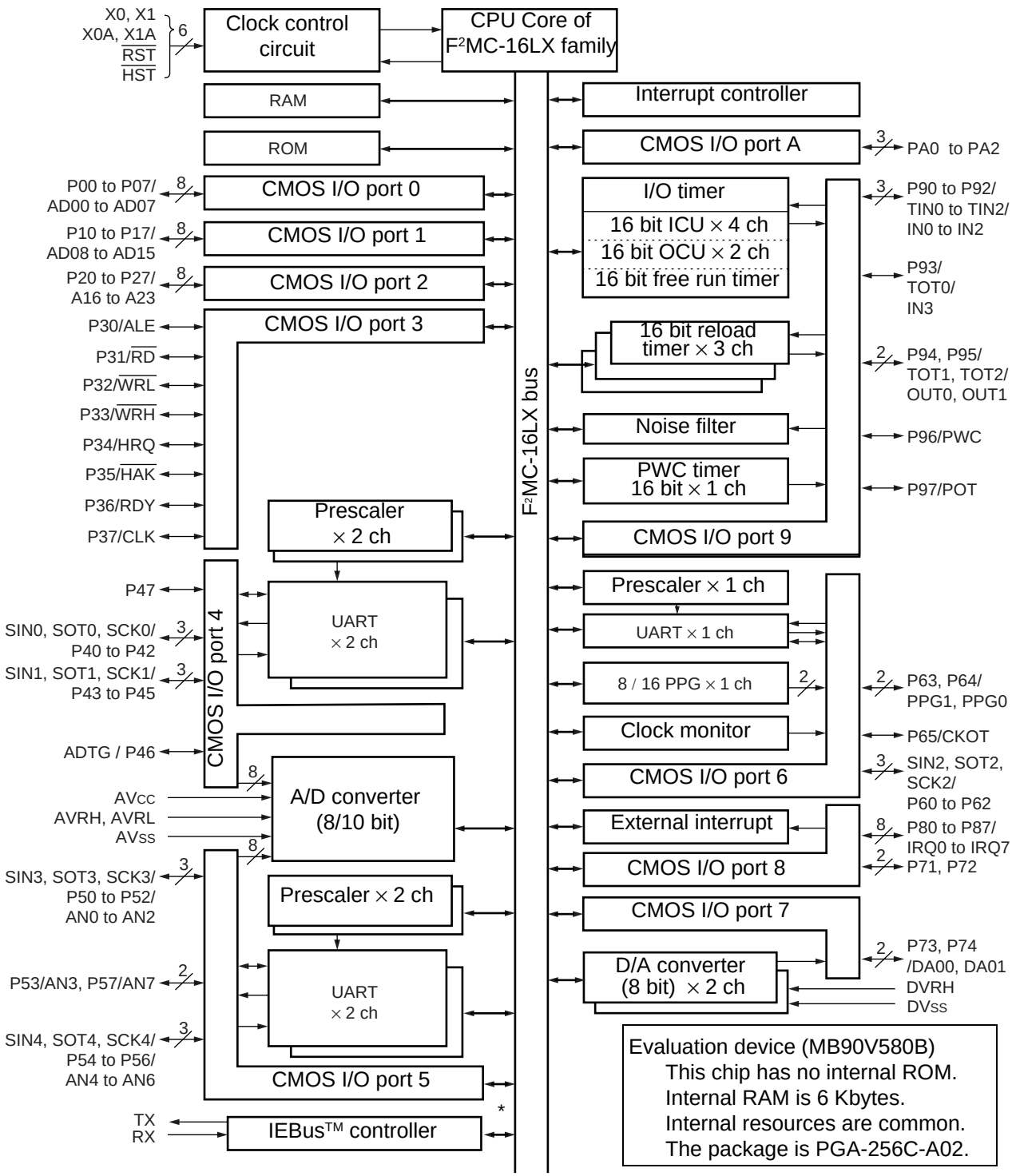
16. Precautions for Use of ’DIV A, Ri,’ and ’DIVW A, RWi’ Instructions

The signed multiplication-division instructions ’DIV A, Ri,’ and ’DIVW A, RWi’ should be used when the corresponding bank registers (DTB, ADB, USB, SSB) are set to value ’00h.’ If the corresponding bank registers (DTB, ADB, USB, SSB) are set to a value other than ’00h,’ then the remainder obtained after the execution of the instruction will not be placed in the instruction operand register.

17. Precautions for Use of REALOS

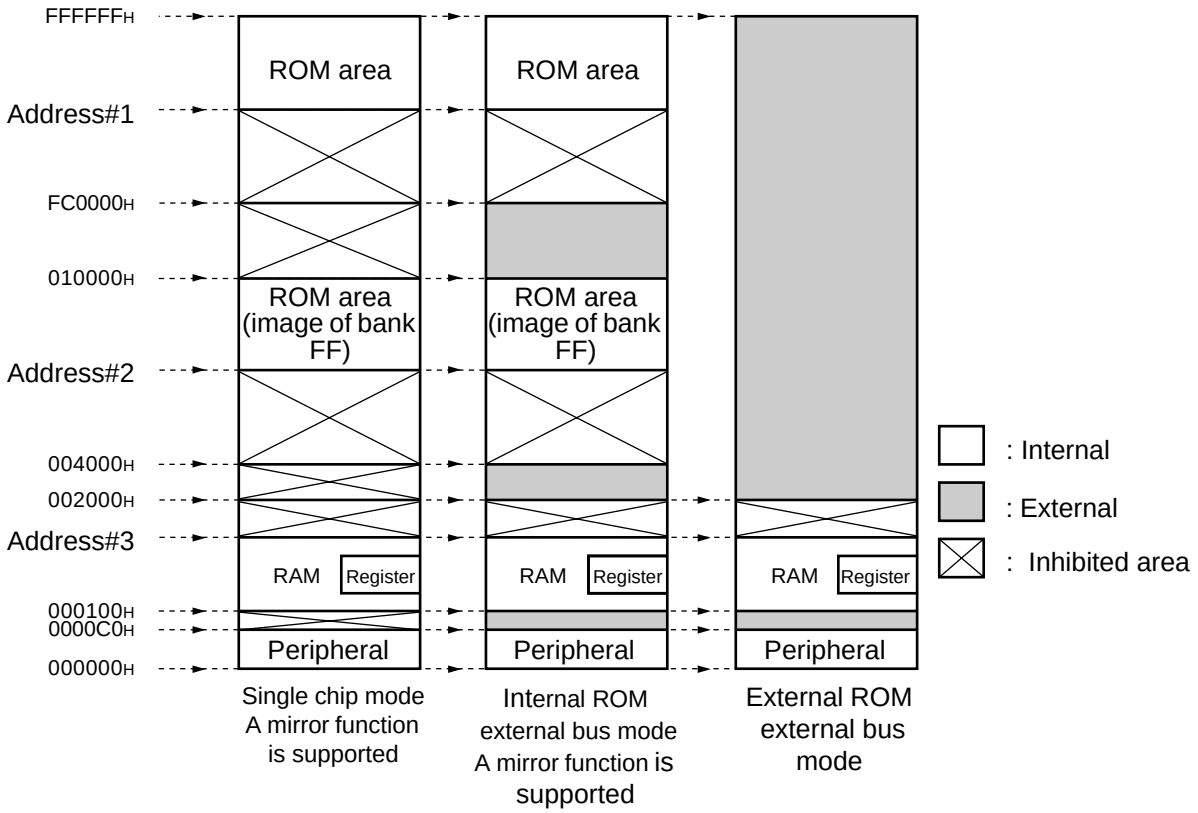
Extended intelligent I/O service (EI^{2}OS) cannot be used, when REALOS is used.

■ BLOCK DIAGRAM



P00 to 07 (8 channels): Provided with a register available as an input pull-up resistor.
P10 to 17(8 channels): Provided with a register available as an input pull-up resistor.
P60 to 65(6 channels): Provided with a register available as an input pull-up resistor.
P40 to 47 (8 channels): Provided with a register available as an open drain.
*: The MB90587C/CA has no IEBus™ controller. The TX and RX pins are N.C. pins.

■ MEMORY MAP

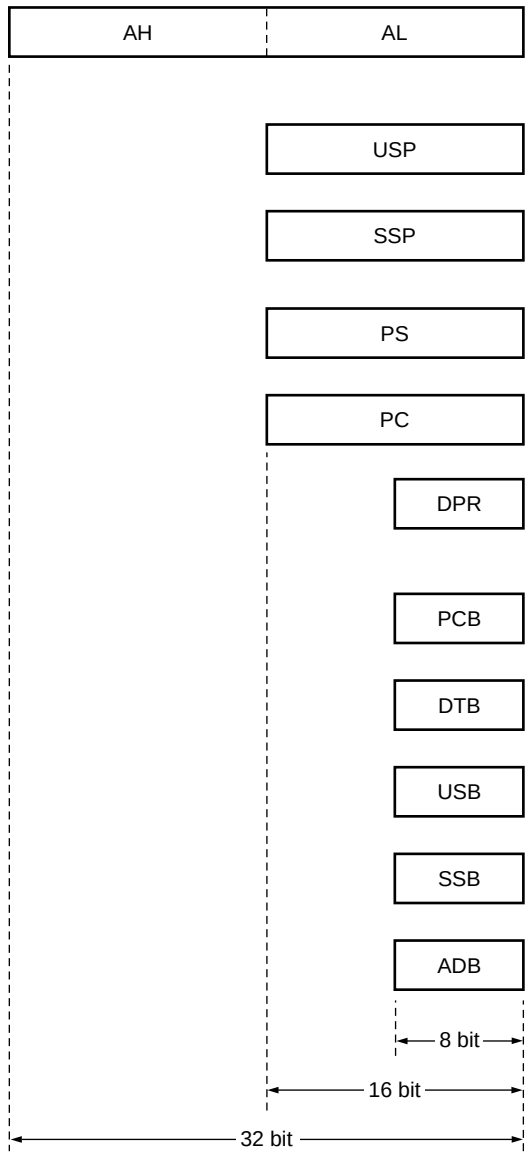


Parts No.	Address#1	Address#2	Address#3
MB90583C/CA	FE0000H	004000H	001900H
MB90F583C/CA	FE0000H	004000H	001900H
MB90587C/CA	FF0000H	004000H	001100H
MB90V580B	(FE0000H)	004000H	001900H

Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit is assigned to the same address, enabling reference of the table on the ROM without stating “far”. For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed actually. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 00400H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

■ F²MC-16LX CPU PROGRAMMING MODEL

• Dedicated registers



: Accumulator (A)
Dual 16-bit register used for storing results of calculation etc. The two 16-bit registers can be combined to be used as a 32-bit register.

: User stack pointer (USP)
The 16-bit pointer indicating a user stack address.

: System stack pointer (SSP)
The 16-bit pointer indicating the status of the system stack address.

: Processor status (PS)
The 16-bit register indicating the system status.

: Program counter (PC)
The 16-bit register indicating storing location of the current instruction code.

: Direct page register (DPR)
The 8-bit register indicating bit 8 through 15 of the operand address in the short direct addressing mode.

: Program bank register (PCB)
The 8-bit register indicating the program space.

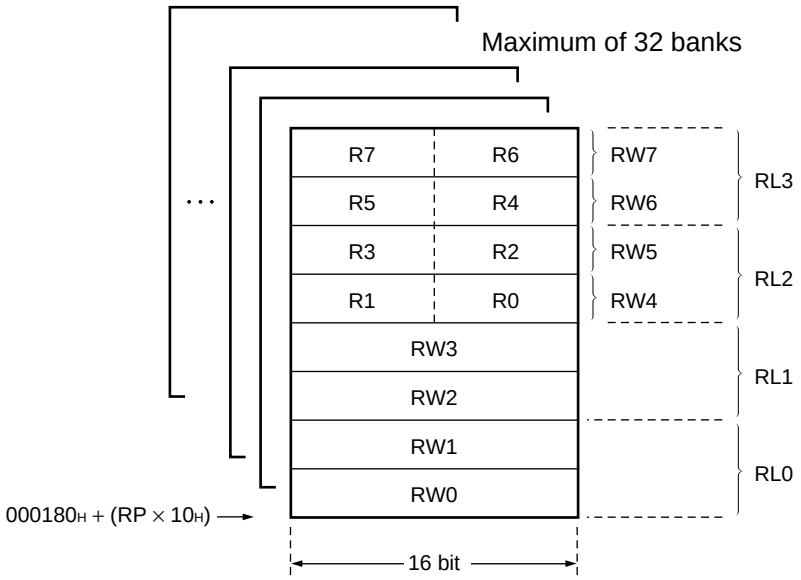
: Data bank register (DTB)
The 8-bit register indicating the data space.

: User stack bank register (USB)
The 8-bit register indicating the user stack space.

: System stack bank register (SSB)
The 8-bit register indicating the system stack space.

: Additional data bank register (ADB)
The 8-bit register indicating the additional data space.

• General-purpose registers



• Processor status (PS)

	ILM			RP					CCR							
	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PS	ILM2	ILM1	ILM0	B4	B3	B2	B1	B0	—	I	S	T	N	Z	V	C
Initial value	0	0	0	0	0	0	0	0	—	0	1	X	X	X	X	X

— : Unused
X : Undefined

■ I/O MAP

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
00_H	Port 0 data register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 data register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 data register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 data register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 data register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 data register	PDR5	R/W	Port 5	11111111_B
06_H	Port 6 data register	PDR6	R/W	Port 6	$--XXXXXX_B$
07_H	Port 7 data register	PDR7	R/W	Port 7	$---XXXX-_B$
08_H	Port 8 data register	PDR8	R/W	Port 8	$XXXXXXXX_B$
09_H	Port 9 data register	PDR9	R/W	Port 9	$XXXXXXXX_B$
$0A_H$	Port A data register	PDRA	R/W	Port A	$-----XXX_B$
$0B_H$ to $0F_H$	(Disabled)				
10_H	Port 0 direction register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 direction register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 direction register	DDR2	R/W	Port 2	00000000_B
13_H	Port 3 direction register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 direction register	DDR4	R/W	Port 4	00000000_B
15_H	Port 5 direction register	DDR5	R/W	Port 5	00000000_B
16_H	Port 6 direction register	DDR6	R/W	Port 6	$--0000000_B$
17_H	Port 7 direction register	DDR7	R/W	Port 7	$---0000-_B$
18_H	Port 8 direction register	DDR8	R/W	Port 8	00000000_B
19_H	Port 9 direction register	DDR9	R/W	Port 9	00000000_B
$1A_H$	Port A direction register	DDRA	R/W	Port A	$-----000_B$
$1B_H$	Port 4 output pin register	ODR4	R/W	Port 4	00000000_B
$1C_H$	Port 5 analog input enable register	ADER	R/W	Port 4, A/D	11111111_B
$1D_H$ to $1F_H$	(Disabled)				
20_H	Serial mode register 0	SMR0	R/W	UART0	00000000_B
21_H	Serial control register 0	SCR0	R/W		00000100_B
22_H	Serial input data register 0/ serial output data register 0	SIDR0/ SODR0	R/W		$XXXXXXXX_B$
23_H	Serial status register 0	SSR0	R/W		$00001-00_B$

(Continued)

Address	Register name	Abbreviated register name	Read/ write	Resource name	Initial value
24H	Serial mode register 1	SMR1	R/W	UART1	00000000B
25H	Serial control register 1	SCR1	R/W		00000100B
26H	Serial input data register 1/ serial output data register 1	SIDR1/ SODR1	R/W		XXXXXXXXB
27H	Serial status register 1	SSR1	R/W		00001–00B
28H	Serial mode register 2	SMR2	R/W	UART2	00000000B
29H	Serial control register 2	SCR2	R/W		00000100B
2AH	Serial input data register 2/ serial output data register 2	SIDR2/ SODR2	R/W		XXXXXXXXB
2BH	Serial status register 2	SSR2	R/W		00001–00B
2CH	Clock division control register 0	CDCR0	R/W	Communications prescaler 0	0–––1111B
2DH	(Disabled)				
2EH	Clock division control register 1	CDCR1	R/W	Communications prescaler 1	0–––1111B
2FH	(Disabled)				
30H	DTP/interrupt enable register	ENIR	R/W	DTP/external interrupt	00000000B
31H	DTP/interrupt factor register	EIRR	R/W		XXXXXXXXB
32H	Request level setting register lower	ELVR	R/W		00000000B
33H	Request level setting register upper				00000000B
34H	Clock division control register 2	CDCR2	R/W	Communications prescaler 2	0–––1111B
35H	(Disabled)				
36H	Control status register lower	ADCS1	R/W	A/D converter	00000000B
37H	Control status register upper	ADCS2	R/W		00000000B
38H	Data register lower	ADCR1	R		XXXXXXXXB
39H	Data register upper	ADCR2	R or W		00001–XXB
3AH	D/A converter data register 0	DAT0	R/W	D/A converter	00000000B
3BH	D/A converter data register 1	DAT1	R/W		00000000B
3CH	D/A control register 0	DACR0	R/W		–––––––0B
3DH	D/A control register 1	DACR1	R/W		–––––––0B
3EH	Clock output enable register	CLKR	R/W	Clock monitor function	––––0000B
3FH	(Disabled)				

(Continued)

Address	Register name	Abbreviated register name	Read/ write	Resource name	Initial value
40H	Reload register L (ch.0)	PRLL0	R/W	8/16 bit PPG0/1	XXXXXXXXB
41H	Reload register H (ch.0)	PRLH0	R/W		XXXXXXXXB
42H	Reload register L (ch.1)	PRLL1	R/W		XXXXXXXXB
43H	Reload register H (ch.1)	PRLH1	R/W		XXXXXXXXB
44H	PPG0 operating mode control register	PPGC0	R/W		0X000XX1B
45H	PPG1 operating mode control register	PPGC1	R/W		0X000001B
46H	PPG0 and 1 operating output control registers	PPGOE	R/W		00000000B
47H	(Disabled)				
48H	Timer control status register lower	TMCSR0	R/W	16 bit reload timer 0	00000000B
49H	Timer control status register upper				----0000B
4AH	16 bit timer register lower/ 16 bit reload register lower	TMR0/ TMRLR0	R/W		XXXXXXXXB
4BH	16 bit timer register upper/ 16 bit reload register upper				XXXXXXXXB
4CH	Timer control status register lower	TMCSR1	R/W	16 bit reload timer 1	00000000B
4DH	Timer control status register upper				----0000B
4EH	16bit timer register lower/ 16 bit reload register lower	TMR1/ TMRLR1	R/W		XXXXXXXXB
4FH	16 bit timer register upper/ 16 bit reload register upper				XXXXXXXXB
50H	Timer control status register lower	TMCSR2	R/W	16 bit reload timer 2	00000000B
51H	Timer control status register upper				----0000B
52H	16 bit timer register lower/ 16 bit reload register lower	TMR2/ TMRLR2	R/W		XXXXXXXXB
53H	16 bit timer register upper/ 16 bit reload register upper				XXXXXXXXB
54H	PWC control status register lower	PWCSR	R/W or R	16 bit PWC timer	00000000B
55H	PWC control status register upper				00000000B
56H	PWC data buffer register lower	PWCR	R/W		XXXXXXXXB
57H	PWC data buffer register upper				XXXXXXXXB
58H	Divide ratio control register	DIVR	R/W		------00B
59H	(Disabled)				

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
5A$_H$	Compare register lower	OCCP0	R/W	Output compare (ch.0)	XXXXXXXX$_B$
5B$_H$	Compare register upper				XXXXXXXX$_B$
5C$_H$	Compare register lower	OCCP1	R/W	Output compare (ch.1)	XXXXXXXX$_B$
5D$_H$	Compare register upper				XXXXXXXX$_B$
5E$_H$	Compare control status register 0	OCS0	R/W	Output compare (ch.0)	0000––00$_B$
5F$_H$	Compare control status register 1	OCS1	R/W	Output compare (ch.1)	–––00000$_B$
60$_H$	Input capture register lower	IPCP0	R	Input capture (ch.0)	XXXXXXXX$_B$
61$_H$	Input capture register upper				XXXXXXXX$_B$
62$_H$	Input capture register lower	IPCP1	R	Input capture (ch.1)	XXXXXXXX$_B$
63$_H$	Input capture register upper				XXXXXXXX$_B$
64$_H$	Input capture register lower	IPCP2	R	Input capture (ch.2)	XXXXXXXX$_B$
65$_H$	Input capture register upper				XXXXXXXX$_B$
66$_H$	Input capture register lower	IPCP3	R	Input capture (ch.3)	XXXXXXXX$_B$
67$_H$	Input capture register upper				XXXXXXXX$_B$
68$_H$	Input capture control status register 01	ICS01	R/W	Input capture (ch.0, ch.1)	00000000$_B$
69$_H$	(Disabled)				
6A$_H$	Input capture control status register 23	ICS23	R/W	Input capture (ch.2, ch.3)	00000000$_B$
6B$_H$	(Disabled)				
6C$_H$	Timer data register lower	TCDTL	R/W	Free-run timer	00000000$_B$
6D$_H$	Timer data register upper	TCDTH	R/W		00000000$_B$
6E$_H$	Timer control status register	TCCS	R/W		00000000$_B$
6F$_H$	ROM mirroring function selection register	ROMM	W	ROM mirror function	–––––––1$_B$
70$_H$	Local-office address setting register L	MAWL	R/W	IEBus™ controller	XXXXXXXX$_B$
71$_H$	Local-office address setting register H	MAWH	R/W		XXXXXXXX$_B$
72$_H$	Slave address setting register L	SAWL	R/W		XXXXXXXX$_B$
73$_H$	Slave address setting register H	SAWH	R/W		XXXXXXXX$_B$
74$_H$	Message length bit setting register	DEWR	R/W		00000000$_B$
75$_H$	Broadcast control bit setting register	DCWR	R/W		00000000$_B$

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
76H	Command register L	CMRL	R/W	IEBus™ controller	11000000B
77H	Command register H	CMRH	R/W		0000000XB
78H	Status register L	STRL	R		0011XXXXB
79H	Status register H	STRH	R/W or R		00XX0000B
7AH	Lock read register L	LRRL	R		XXXXXXXXB
7BH	Lock read register H	LRRH	R/W or R		1110XXXXB
7CH	Master address read register L	MARL	R		XXXXXXXXB
7DH	Master address read register H	MARH	R		1111XXXXB
7EH	Message length bit read register	DERR	R		XXXXXXXXB
7FH	Broadcast control bit read register	DCRR	R		000XXXXXB
80H	Write data buffer	WDB	W		XXXXXXXXB
81H	Read data buffer	RDB	R		XXXXXXXXB
82H	Serial mode register 3	SMR3	R/W	UART3	00000000B
83H	Serial control register 3	SCR3	R/W		00000100B
84H	Serial input register 3/ serial output register 3	SIDR3/ SODR3	R/W		XXXXXXXXB
85H	Serial status register 3	SSR3	R/W		00001–00B
86H	PWC noise filter register	RNCR	R/W	PWC noisefilter	–––––000B
87H	Clock division control register 3	CDCR3	R/W	Communications prescaler 3	0–––1111B
88H	Serial mode register 4	SMR4	R/W	UART4	00000000B
89H	Serial control register 4	SCR4	R/W		00000100B
8AH	Serial input register 4/ serial output register 4	SIDR4/ SODR4	R/W		XXXXXXXXB
8BH	Serial status register 4	SSR4	R/W		00001–00B
8CH	Port 0 input pull-up resistor setup register	RDR0	R/W	Port 0	00000000B
8DH	Port 1 input pull-up resistor setup register	RDR1	R/W	Port 1	00000000B
8EH	Port 6 input pull-up resistor setup register	RDR6	R/W	Port 6	––000000B
8FH	Clock division control register 4	CDCR4	R/W	Communications prescaler 4	0–––1111B
90H to 9DH	(Disabled)				

(Continued)

Address	Register name	Abbreviated register name	Read/ write	Resource name	Initial value
9E$_H$	Program address detection control/ status register	PACSR	R/W	Address match detection function	00000000$_B$
9F$_H$	Delayed interrupt generation/release register	DIRR	R/W	Delayed interrupt generation module	–––––––0$_B$
A0$_H$	Low-power consumption mode control register	LPMCR	R/W or W	Low-power consumption mode	0001100–$_B$
A1$_H$	Clock selection register	CKSCR	R/W or R		11111100$_B$
A2$_H$ to A4$_H$	(Disabled)				
A5$_H$	Auto-ready function selection register	ARSR	W	External bus pin control circuit	0011––00$_B$
A6$_H$	External address output control register	HACR	W		00000000$_B$
A7$_H$	Bus control signal selection register	ECSR	W		0000000–$_B$
A8$_H$	Watch dog timer control register	WDTC	R or W	Watch dog timer	XXXXX111$_B$
A9$_H$	Time-base timer control register	TBTC	R/W, W	Timebase timer	1––00100$_B$
AA$_H$	Clock timer control register	WTC	R/W or R	Clock timer	1X000000$_B$
AB$_H$ to AD$_H$	(Disabled)				
AE$_H$	Flash memory control status register	FMCS	R/W or R or W	Flash interface	000X0000$_B$
AF$_H$	(Disabled)				
B0$_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111$_B$
B1$_H$	Interrupt control register 01	ICR01	R/W		00000111$_B$
B2$_H$	Interrupt control register 02	ICR02	R/W		00000111$_B$
B3$_H$	Interrupt control register 03	ICR03	R/W		00000111$_B$
B4$_H$	Interrupt control register 04	ICR04	R/W		00000111$_B$
B5$_H$	Interrupt control register 05	ICR05	R/W		00000111$_B$
B6$_H$	Interrupt control register 06	ICR06	R/W		00000111$_B$
B7$_H$	Interrupt control register 07	ICR07	R/W		00000111$_B$
B8$_H$	Interrupt control register 08	ICR08	R/W		00000111$_B$
B9$_H$	Interrupt control register 09	ICR09	R/W		00000111$_B$
BA$_H$	Interrupt control register 10	ICR10	R/W		00000111$_B$
BB$_H$	Interrupt control register 11	ICR11	R/W		00000111$_B$
BC$_H$	Interrupt control register 12	ICR12	R/W		00000111$_B$
BD$_H$	Interrupt control register 13	ICR13	R/W		00000111$_B$
BE$_H$	Interrupt control register 14	ICR14	R/W		00000111$_B$
BF$_H$	Interrupt control register 15	ICR15	R/W		00000111$_B$

(Continued)

(Continued)

Address	Register name	Abbreviated register name	Read/write	Resource name	Initial value
C0H to FFH	(External area)				
100H to #H	(RAM area)				
#H to 1FEFH	(Reserved area)				
1FF0H	Program address detection register 0 (lower)	PADR0	R/W	Address match detection function	XXXXXXXXB
1FF1H	Program address detection register 0 (middle)		R/W		XXXXXXXXB
1FF2H	Program address detection register 0 (upper)		R/W		XXXXXXXXB
1FF3H	Program address detection register 1 (lower)	PADR1	R/W		XXXXXXXXB
1FF4H	Program address detection register 1 (middle)		R/W		XXXXXXXXB
1FF5H	Program address detection register 1 (upper)		R/W		XXXXXXXXB
1FF6H to 1FFFH	(Reserved area)				

- Explanation of initial values→“0” : initial value“0” / “1” : initial value“1” / “X” : undefined / “–” : undefined (not used)
- The addresses following 00FFH are reserved. No external bus access signal is generated.
- Boundary #H between the RAM area and the reserved area varies with the product model.

Note: For bits that is initialized by an reset operation, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results. For LPMCR/CKSCR/WDTC, there are cases where initialization is performed or not performed, depending on the types of the reset. However initial value for resets that initializes the value are listed.

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt source	EI²OS support	Interrupt vector		Interrupt control register		Priority
		No.	Address	ICR	Address	
Reset	×	#08	FFFFDC$_H$	—	—	High
INT9 instruction	×	#09	FFFFD8$_H$	—	—	
Exception	×	#10	FFFFD4$_H$	—	—	
A/D converter	○	#11	FFFFD0$_H$	ICR00	0000B0$_H$	
Timebase timer	×	#12	FFFFCC$_H$			
DTP0 (external interrupt #0) /UART3 reception complete	○	#13	FFFFC8$_H$	ICR01	0000B1$_H$	
DTP1 (external interrupt #1) /UART4 reception complete	○	#14	FFFFC4$_H$			
DTP2 (external interrupt #2) /UART3 transmission complete	○	#15	FFFFC0$_H$	ICR02	0000B2$_H$	
DTP3 (external interrupt #3) /UART4 transmission complete	○	#16	FFFFBC$_H$			
DTP4 to 7 (external interrupt #4 to #7)	○	#17	FFFFB8$_H$	ICR03	0000B3$_H$	
Output compare (ch.1) match (I/O timer)	○	#18	FFFFB4$_H$			
UART2 reception complete	○	#19	FFFFB0$_H$	ICR04	0000B4$_H$	
UART1 reception complete	○	#20	FFFFAC$_H$			
Input capture (ch.3) include (I/O timer)	○	#21	FFFFA8$_H$	ICR05	0000B5$_H$	
Input capture (ch.2) include (I/O timer)	○	#22	FFFFA4$_H$			
Input capture (ch.1) include (I/O timer)	○	#23	FFFFA0$_H$	ICR06	0000B6$_H$	
Input capture (ch.0) include (I/O timer)	○	#24	FFFF9C$_H$			
8/16 bit PPG0 counter borrow	×	#25	FFFF98$_H$	ICR07	0000B7$_H$	
16 bit reload timer 2 to 0	○	#26	FFFF94$_H$			
Clock prescaler	×	#27	FFFF90$_H$	ICR08	0000B8$_H$	
Output compare (ch.0) match (I/O timer)	○	#28	FFFF8C$_H$			
UART2 transmission complete	○	#29	FFFF88$_H$	ICR09	0000B9$_H$	
PWC timer measurement complete / over flow	○	#30	FFFF84$_H$			
UART1 transmission complete	○	#31	FFFF80$_H$	ICR10	0000BA$_H$	
16-bit free run timer (I/O timer) over flow	○	#32	FFFF7C$_H$			
UART0 transmission complete	○	#33	FFFF78$_H$	ICR11	0000BB$_H$	
8/16 bit PPG1 counter borrow	×	#34	FFFF74$_H$			
IEBus reception complete	◎	#35	FFFF70$_H$	ICR12	0000BC$_H$	
IEBus transmission start	◎	#37	FFFF68$_H$	ICR13	0000BD$_H$	
UART0 reception complete	◎	#39	FFFF60$_H$	ICR14	0000BE$_H$	
Flash memory status	×	#41	FFFF58$_H$	ICR15	0000BF$_H$	
Delayed interrupt	×	#42	FFFF54$_H$			Low

◎ : Indicates that the interrupt request flag is cleared by the EI²OS interrupt clear signal (stop request present).
○ : Indicates that the interrupt request flag is cleared by the EI²OS interrupt clear signal.
× : Indicates that the interrupt request flag is not cleared by the EI²OS interrupt clear signal.

■ PERIPHERAL RESOURCES

1. I/O Ports

(1) Outline of I/O ports

When a data register serving for control output is read, the data output from it as a control output is read regardless of the value in the direction register. Note that, if a read modify write instruction (such as a bit set instruction) is used to preset output data in the data register when changing its setting from input to output, the data read is not the data register latched value but the input data from the pin.

Ports 0 to 4 and 6 to A are input/output ports which serve as inputs when the direction register value is “0” or as outputs when the value is “1”.

On the MB90580C series, ports 0 to 3 also serve as external bus pins. When the device is used in external bus mode, therefore, these ports are restricted on use.

Ports 2 and 3 can be used as ports even in external bus mode depending on the setting of the corresponding function select bit.

(2) Register configuration

• Port 0 data register (PDR0)

bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 000000H	(PDR1)	P07	P06	P05	P04	P03	P02	P01	P00
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

• Port 1 data register (PDR1)

bit	15	14	13	12	11	10	9	8	7 ····· 0
Address : 000001H	P17	P16	P15	P14	P13	P12	P11	P10	(PDR0)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Port 2 data register (PDR2)

bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 000002H	(PDR3)	P27	P26	P25	P24	P23	P22	P21	P20
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

• Port 3 data register (PDR3)

bit	15	14	13	12	11	10	9	8	7 ····· 0
Address : 000003H	P37	P36	P35	P34	P33	P32	P31	P30	(PDR2)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Port 4 data register (PDR4)

bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 000004H	(PDR5)	P47	P46	P45	P44	P43	P42	P41	P40
Access		(R/W)	(RW)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

(Continued)

(Continued)

• Port 5 data register (PDR5)

Address : 000005H

bit	15	14	13	12	11	10	9	8	7 ····· 0
	P57	P56	P55	P54	P53	P52	P51	P50	(PDR4)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	

• Port 6 data register (PDR6)

Address : 000006H

bit	15 ····· 8	7	6	5	4	3	2	1	0
	(PDR7)	—	—	P65	P64	P63	P62	P61	P60
Access		(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(—)	(—)	(X)	(X)	(X)	(X)	(X)	(X)

• Port 7 data register (PDR7)

Address : 000007H

bit	15	14	13	12	11	10	9	8	7 ····· 0
	—	—	—	P74	P73	P72	P71	—	(PDR6)
Access	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	
Initial value	(—)	(—)	(—)	(X)	(X)	(X)	(X)	(—)	

• Port 8 data register (PDR8)

Address : 000008H

bit	15 ····· 8	7	6	5	4	3	2	1	0
	(PDR9)	P87	P86	P85	P84	P83	P82	P81	P80
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

• Port 9 data register (PDR9)

Address : 000009H

bit	15	14	13	12	11	10	9	8	7 ····· 0
	P97	P96	P95	P94	P93	P92	P91	P90	(PDR8)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Port A data register (PDRA)

Address : 00000AH

bit	15 ····· 8	7	6	5	4	3	2	1	0
	(Disabled)	—	—	—	—	—	PA2	PA1	PA0
Access		(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)
Initial value		(—)	(—)	(—)	(—)	(—)	(X)	(X)	(X)

• Port 0 direction register (DDR0)

Address : 000010H

bit	15 ····· 8	7	6	5	4	3	2	1	0
	(DDR1)	D07	D06	D05	D04	D03	D02	D01	D00
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

(Continued)

(Continued)

• Port 1 direction register (DDR1)

Address : 000011H

bit	15	14	13	12	11	10	9	8	7 ····· 0
	D17	D16	D15	D14	D13	D12	D11	D10	(DDR0)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Port 2 direction register (DDR2)

Address : 000012H

bit	15 ····· 8	7	6	5	4	3	2	1	0
	(DDR3)	D27	D26	D25	D24	D23	D22	D21	D20
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

• Port 3 direction register (DDR3)

Address : 000013H

bit	15	14	13	12	11	10	9	8	7 ····· 0
	D37	P36	P35	P34	P33	P32	P31	P30	(DDR2)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Port 4 direction register (DDR4)

Address : 000014H

bit	15 ····· 8	7	6	5	4	3	2	1	0
	(DDR5)	D47	D46	D45	D44	D43	D42	D41	D40
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

• Port 5 direction register (DDR5)

Address : 000015H

bit	15	14	13	12	11	10	9	8	7 ····· 0
	D57	D56	D55	D54	D53	D52	D51	D50	(DDR4)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Port 6 direction register (DDR6)

Address : 000016H

bit	15 ····· 8	7	6	5	4	3	2	1	0
	(DDR7)	—	—	D65	D64	D63	D62	D61	D60
Access		(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(—)	(—)	(0)	(0)	(0)	(0)	(0)	(0)

• Port 7 direction register (DDR7)

Address : 000017H

bit	15	14	13	12	11	10	9	8	7 ····· 0
	—	—	—	D74	D73	D72	D71	—	(DDR6)
Access	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	
Initial value	(—)	(—)	(—)	(0)	(0)	(0)	(0)	(—)	

(Continued)

• Port 8 direction register (DDR8)

bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 000018H	(DDR9)	D87	D86	D85	D84	D83	D82	D81	D80
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

• Port 9 direction register (DDR9)

bit	15	14	13	12	11	10	9	8	7 ····· 0
Address : 000019H	D97	D96	D95	D94	D93	D92	D91	D90	(DDR8)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Port A direction register (DDRA)

bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 00001AH	(ODR4)	—	—	—	—	—	DA2	DA1	DA0
Access		(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)
Initial value		(—)	(—)	(—)	(—)	(—)	(0)	(0)	(0)

• Port 4 output pin register (ODR4)

bit	15	14	13	12	11	10	9	8	7 ····· 0
Address : 00001BH	OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40	(DDRA)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Port 5 analog input enable register (ADER)

bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 00001CH		ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)

• Port 0 input pull-up resistor setup register (RDR0)

bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 00008CH	(RDR1)	RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00
Access		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

• Port 1 input pull-up resistor setup register (RDR1)

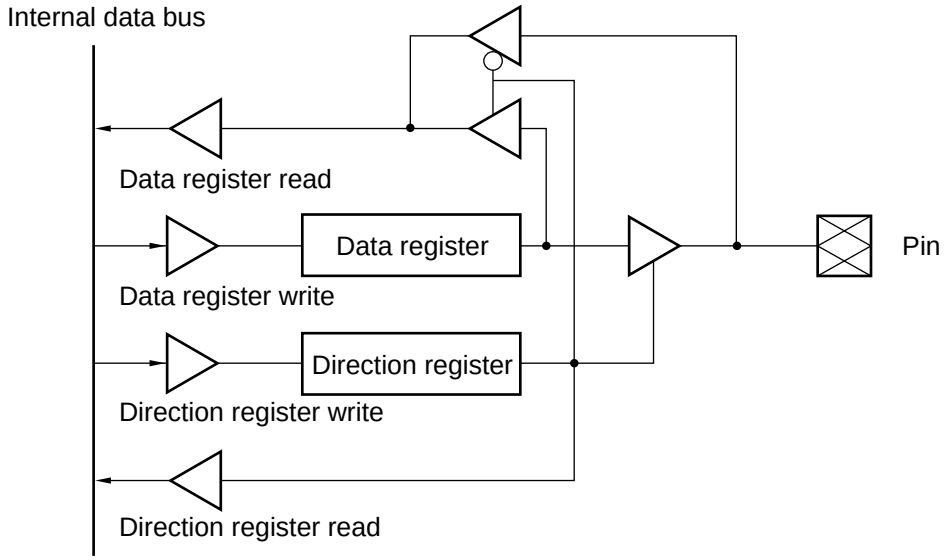
bit	15	14	13	12	11	10	9	8	7 ····· 0
Address : 00008DH	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	(RDR0)
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Port 6 input pull-up resistor setup register (RDR6)

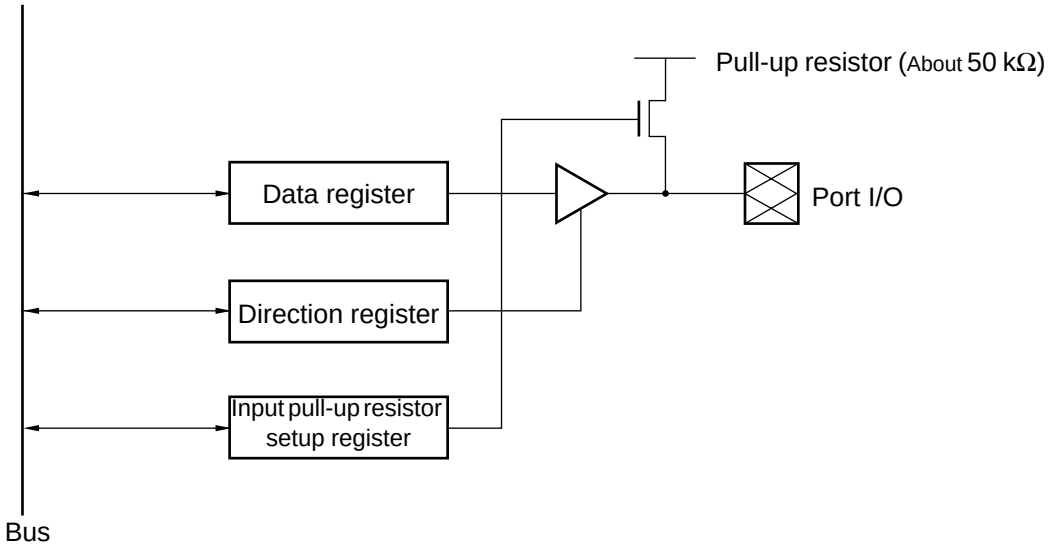
bit	15 ····· 8	7	6	5	4	3	2	1	0
Address : 00008EH	(CDCR4)	—	—	RD65	RD64	RD63	RD62	RD61	RD60
Access		(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value		(—)	(—)	(0)	(0)	(0)	(0)	(0)	(0)

(3) Block Diagram

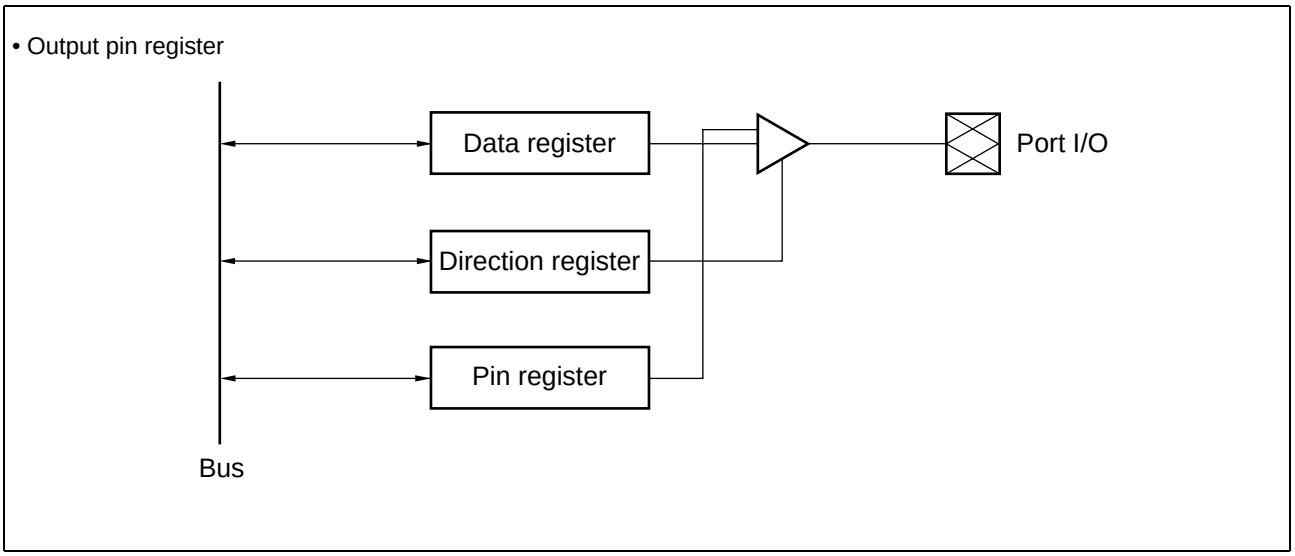
• Input/output port



• Input pull-up resistor setup register



• Output pin register



2. Timebase Timer

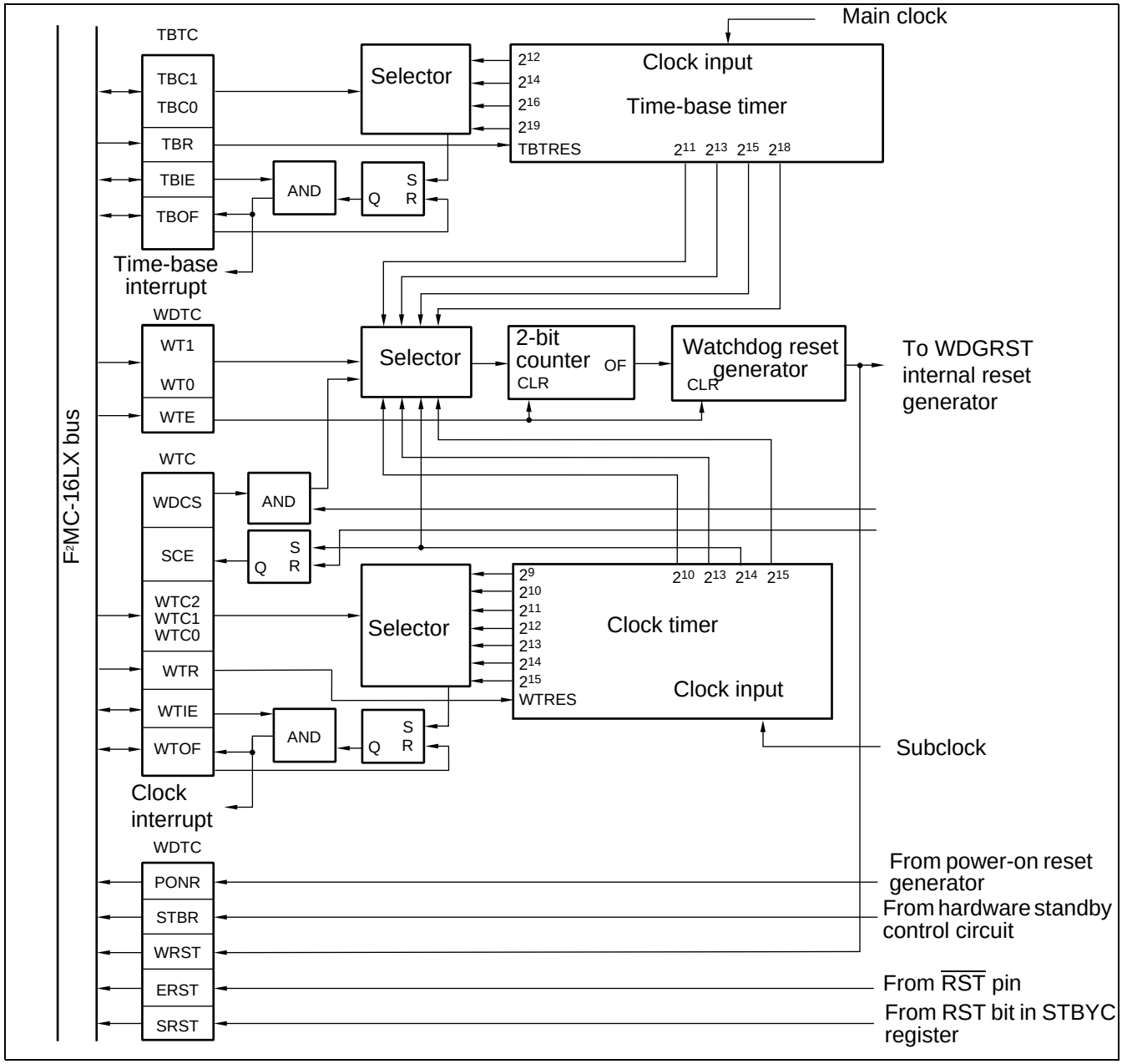
The time-base timer consists of a 18-bit timer and an interval interrupt control circuit. Note that the time-base timer uses the oscillation clock regardless of the setting of the MCS bit in the CKSCR.

(1) Register configuration

• Timebase timer control register

bit	15	14	13	12	11	10	9	8	
Address : 0000A9H	Reserved	—	—	TBIE	TBOF	TBR	TBC1	TBC0	TBTC
Access	(R/W)	(—)	(—)	(R/W)	(R/W)	(W)	(R/W)	(R/W)	
Initial value	(1)	(—)	(—)	(0)	(0)	(1)	(0)	(0)	

(2) Block Diagram



3. Watchdog Timer

The watchdog timer consists of a 2-bit watchdog counter using carry signals from the 18-bit time-base timer as the clock source, a control register, and a watchdog reset control section.

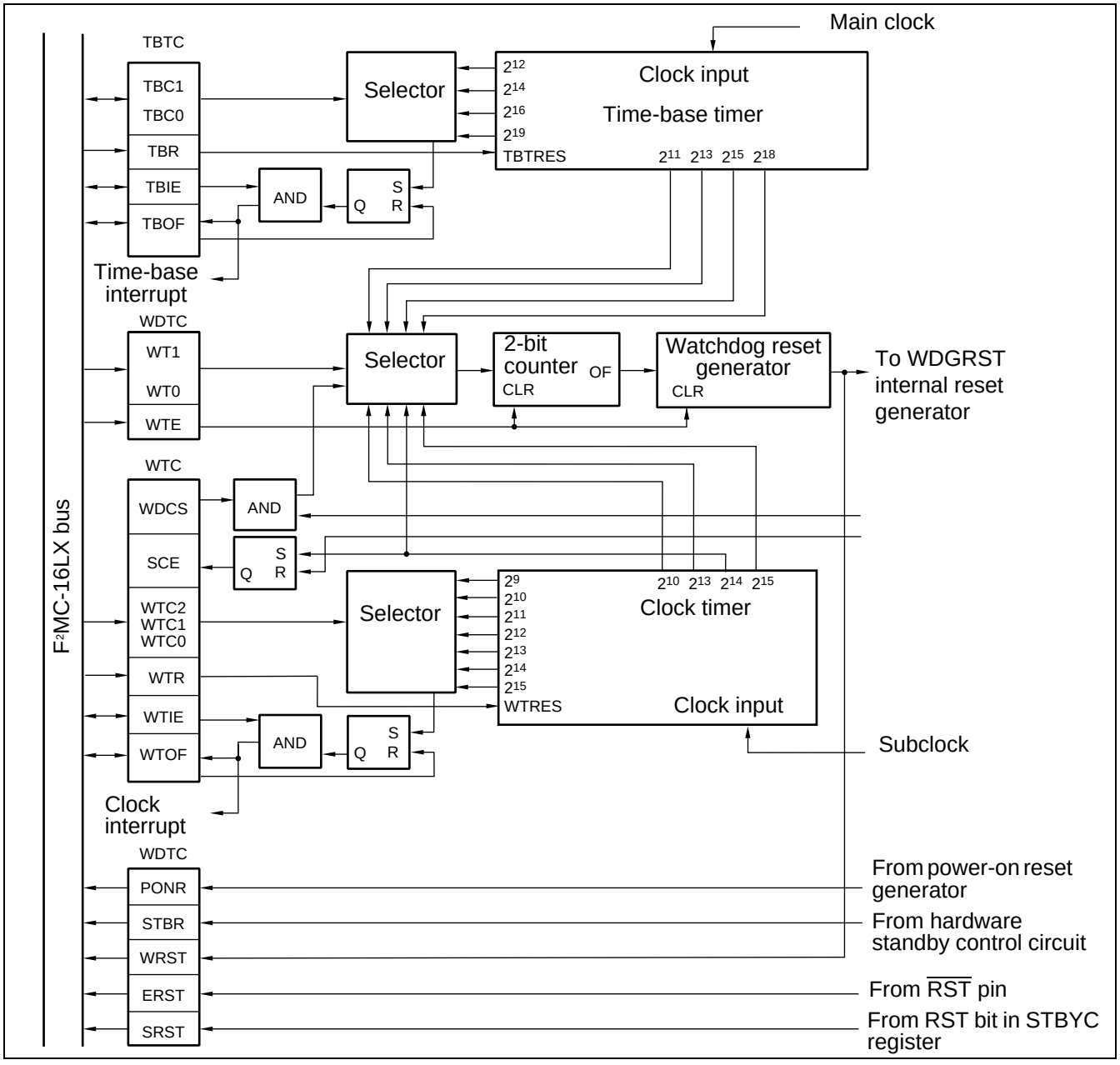
(1) Register configuration

• Watchdog timer control register

Address : 0000A8H

bit	7	6	5	4	3	2	1	0	
	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	WDTC
Access	(R)	(R)	(R)	(R)	(R)	(W)	(W)	(W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(1)	(1)	(1)	

(2) Block Diagram



4. Clock timer

The clock timer has the functions of a watchdog timer clock source, a subclock oscillation settling time wait timer, and of a periodically interrupt generating interval timer.

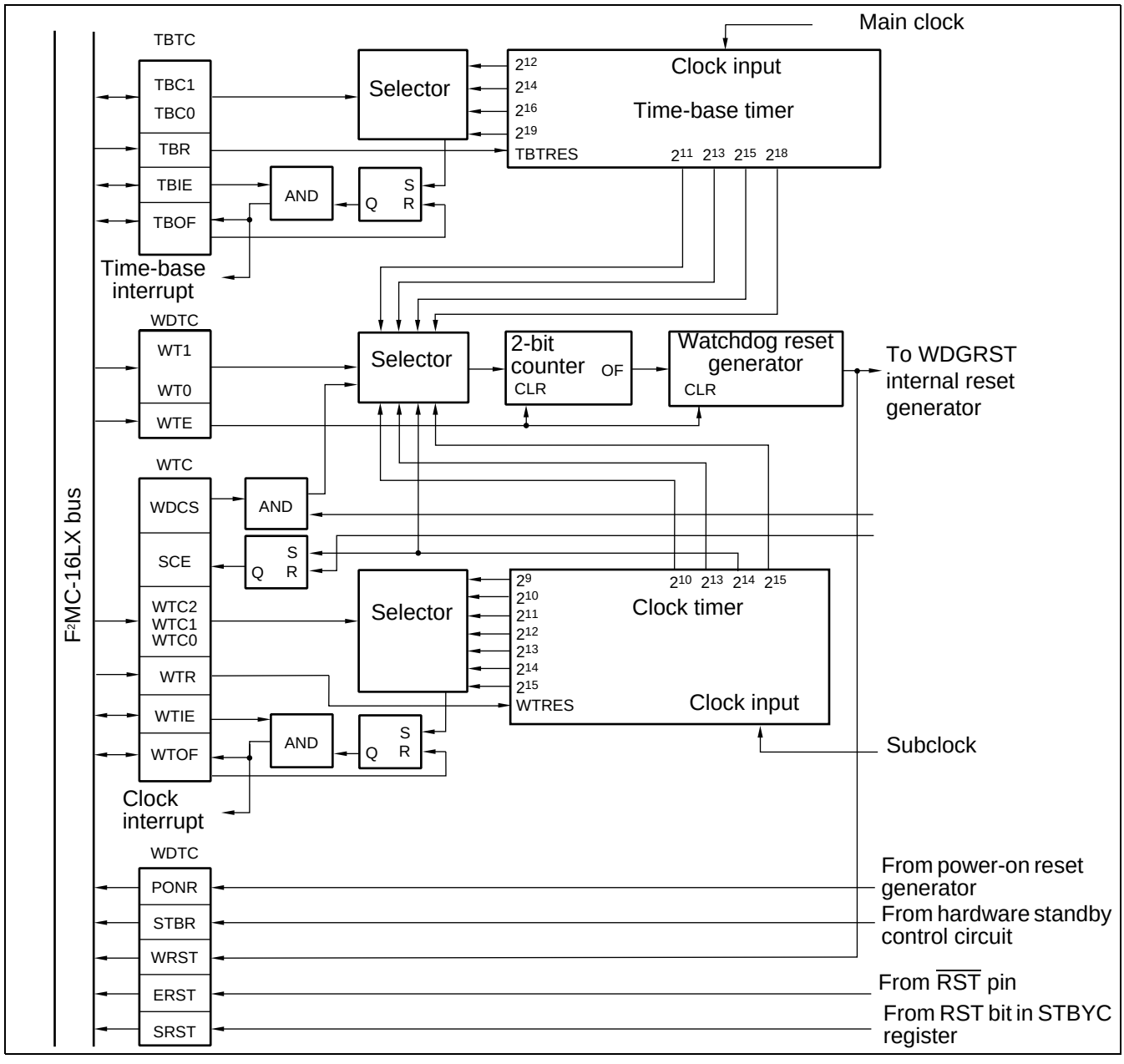
(1) Register configuration

• Clock timer control register

Address : 0000AA$_H$ WTC

bit	7	6	5	4	3	2	1	0
	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0
Access	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value	(1)	(X)	(0)	(0)	(0)	(0)	(0)	(0)

(2) Block Diagram



5. External Memory Access (External Bus Pin Control Circuit)

The external bus pin control circuit controls external bus pins used to expand the address/data buses of the CPU outside.

(1) Register configuration

• Automatic ready function selection register

Address : 0000A5H

bit	15	14	13	12	11	10	9	8	
	IOR1	IOR0	HMR1	HMR0	—	—	LMR1	LMR0	ARSR
Access	(W)	(W)	(W)	(W)	(—)	(—)	(W)	(W)	
Initial value	(0)	(0)	(1)	(1)	(—)	(—)	(0)	(0)	

• External address output control register

Address : 0000A6H

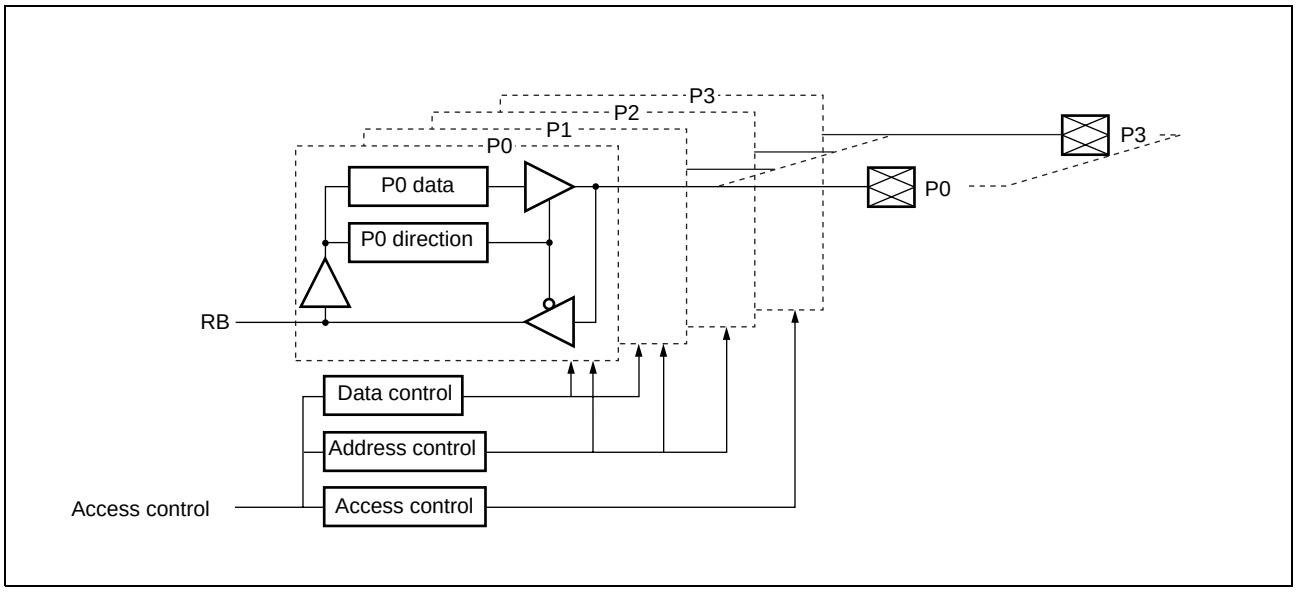
bit	7	6	5	4	3	2	1	0	
	E23	E22	E21	E20	E19	E18	E17	E16	HACR
Access	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Bus control signal selection register

Address : 0000A7H

bit	15	14	13	12	11	10	9	8	
	CKE	RYE	HDE	IOBS	HMBS	WRE	LMBS	—	ECSR
Access	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(—)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(—)	

(2) Block Diagram



6. PWC Timer

The PWC (pulse width count) timer is a 16-bit multifunction up-counter with reload timer functions and input-signal pulse-width count functions as well.

The PWC timer consists of a 16-bit counter, a input pulse divider, a divide ratio control register, a count input pin, a pulse output pin, and a 16-bit control register.

(1) Features of the PWC timer

The PWC timer has the following features:

- Timer functions
  Generates an interrupt request at set time intervals.
  Outputs pulse signals synchronized with the timer cycle.
  Selects the counter clock from among three internal clocks.
- Pulse-width count functions
  Counts the time between external pulse input events.
  Selects the counter clock from among three internal clocks.
  Count mode
  - H pulse width (rising edge to falling edge)/L pulse width (falling edge to rising edge)
  - Rising-edge cycle (rising edge to falling edge)/Falling-edge cycle (falling edge to rising edge)
  - Count between edges (rising or falling edge to falling or rising edge)

  Capable of counting cycles by dividing input pulses by 2^2, 2^4, 2^6, 2^8 using an 8-bit input divider.
  Generates an interrupt request upon the completion of count operation.
  Selects single or consecutive count operation.

(2) Register configuration

• PWC control status register Upper

bit	15	14	13	12	11	10	9	8	
Address : 000055H	STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	POUT	PWCSR upper
Access	(R/W)	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• PWC control status register Lower

bit	7	6	5	4	3	2	1	0	
Address : 000054H	CKS1	CKS0	Reserved	Reserved	S/C	MOD2	MOD1	MOD0	PWCSR lower
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• PWC data buffer register Upper

bit	15	14	13	12	11	10	9	8	
Address : 000057H									PWCR upper
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• PWC data buffer register Lower

bit	7	6	5	4	3	2	1	0	
Address : 000056H									PWCR lower
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

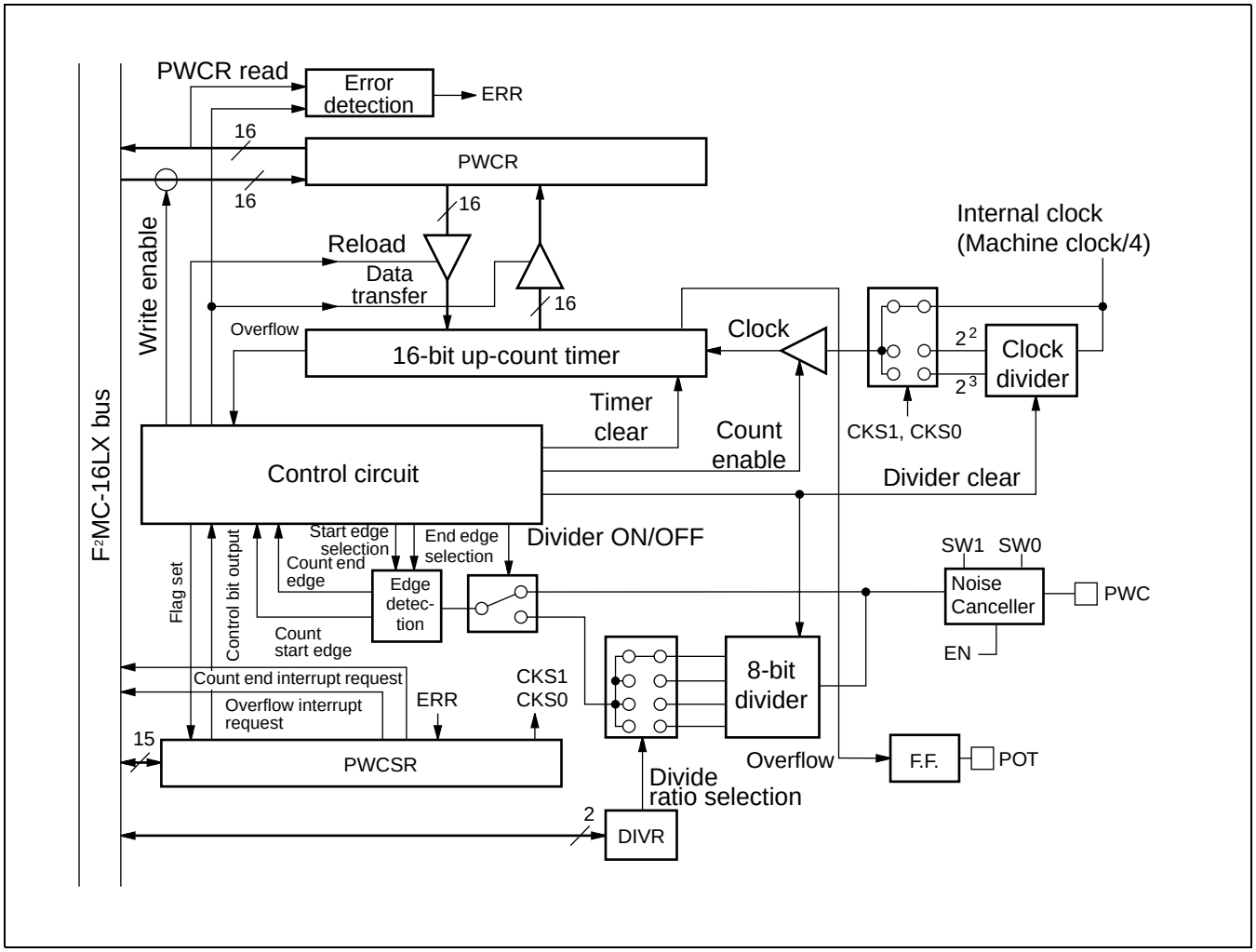
• Divide ratio control register

bit	7	6	5	4	3	2	1	0	
Address : 000058H	—	—	—	—	—	—	DIV1	DIV0	DIVR
Access	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	
Initial value	(—)	(—)	(—)	(—)	(—)	(—)	(0)	(0)	

• PWC noise filter register

bit	7	6	5	4	3	2	1	0	
Address : 000086H	—	—	—	—	—	SW1	SW0	EN	RNCR
Access	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	
Initial value	(—)	(—)	(—)	(—)	(—)	(0)	(0)	(0)	

(3) Block Diagram



7. 16-bit I/O timer

The 16-bit I/O timer module consists of one 16-bit free run timer, four input capture circuits, and two output comparators. This module allows two independent waveforms to be output on the basis of the 16-bit free run timer. Input pulse width and external clock periods can, therefore, be measured.

(1) 16-bit free-run timer (1 channel)

The 16-bit free run timer consists of a 16-bit up-counter, a control register, and a prescaler. The value output from this timer/counter is used as the base time for the input capture and output compare modules.

- Counter operation clock (Selectable from among the following four)
  Four internal clock cycles: $\phi/4$, $\phi/16$, $\phi/64$, $\phi/256$
  ϕ: Machine clock
- Interrupts
  An interrupt can be generated when the 16-bit free-run timer causes a counter overflow or by compare/match operation with compare register 0. (The compare/match operation requires the mode setting).
- Counter value
  An interrupt can be generated when the 16-bit free-run timer causes a counter overflow or when a match with compare register 0 occurs (The compare/match function can be used by the appropriate mode setting).
- Initialization
  The counter value can be initialized to "0000_H" at a reset, soft clear operation, or a match with compare register 0.

(2) Output compare module (2 channels)

The output compare module consists of two 16-bit compare registers, compare output latches, and control registers. When the 16-bit free-run timer value matches the compare register value, this module generates an interrupt while inverting the output level.

- Two compare registers can operate independently.
  Output pin and interrupt flag for each compare register
- A pair of compare registers can be used to control the output pin.
  Two compare registers can be used to invert the output pin polarity.
- The initial value for each output pin can be set.
- An interrupt can be generated by compare/match operation.

(3) Input capture module (4 channels)

The input capture module consists of capture registers and control registers respectively associated with four independent external input pins. This module can hold the 16-bit free run timer value in the capture register. In addition, it can detect an arbitrary edge of the signal input from each external input pin to generate an interrupt.

- The external input signal edge to be detected can be selected.
  One or both of the rising and falling edges can be selected.
- Four input capture channels can operate independently.
- An interrupt can be generated at a valid edge of the external input signal.
  The extended intelligent I/O service can be activated by the interrupt by the input capture module.

(4) Register configuration

• Timer data register (upper)

bit	15	14	13	12	11	10	9	8	
Address : 00006DH	T15	T14	T13	T12	T11	T10	T09	T08	TCDTH
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Timer data register (lower)

bit	7	6	5	4	3	2	1	0	
Address : 00006CH	T07	T06	T05	T04	T03	T02	T01	T00	TCDTL
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Timer control status register

bit	7	6	5	4	3	2	1	0	
Address : 00006EH	Re-served	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0	TCCS
Access	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Compare register (upper)

bit	15	14	13	12	11	10	9	8	
Address : ch0 00005BH : ch1 00005DH	C15	C14	C13	C12	C11	C10	C09	C08	OCCP0 OCCP1
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Compare register (lower)

bit	7	6	5	4	3	2	1	0	
Address : ch0 00005AH : ch1 00005CH	C07	C06	C05	C04	C03	C02	C01	C00	OCCP0 OCCP1
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Compare control status register 1

bit	15	14	13	12	11	10	9	8	
Address : ch1 00005FH	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	OCS1
Access	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(—)	(—)	(—)	(0)	(0)	(0)	(0)	(0)	

• Compare control status register 0

bit	7	6	5	4	3	2	1	0	
Address : ch0 00005EH	ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0	OCS0
Access	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(—)	(—)	(0)	(0)	

(Continued)

(Continued)

• Input capture register (upper)

bit	15	14	13	12	11	10	9	8	
Address : ch0 000061H	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	IPCP0 upper
: ch1 000063H									IPCP1 upper
: ch2 000065H									IPCP2 upper
: ch3 000067H									IPCP3 upper
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Input capture register (lower)

bit	7	6	5	4	3	2	1	0	
Address : ch0 000060H	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	IPCP0 lower
: ch1 000062H									IPCP1 lower
: ch2 000064H									IPCP2 lower
: ch3 000066H									IPCP3 lower
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

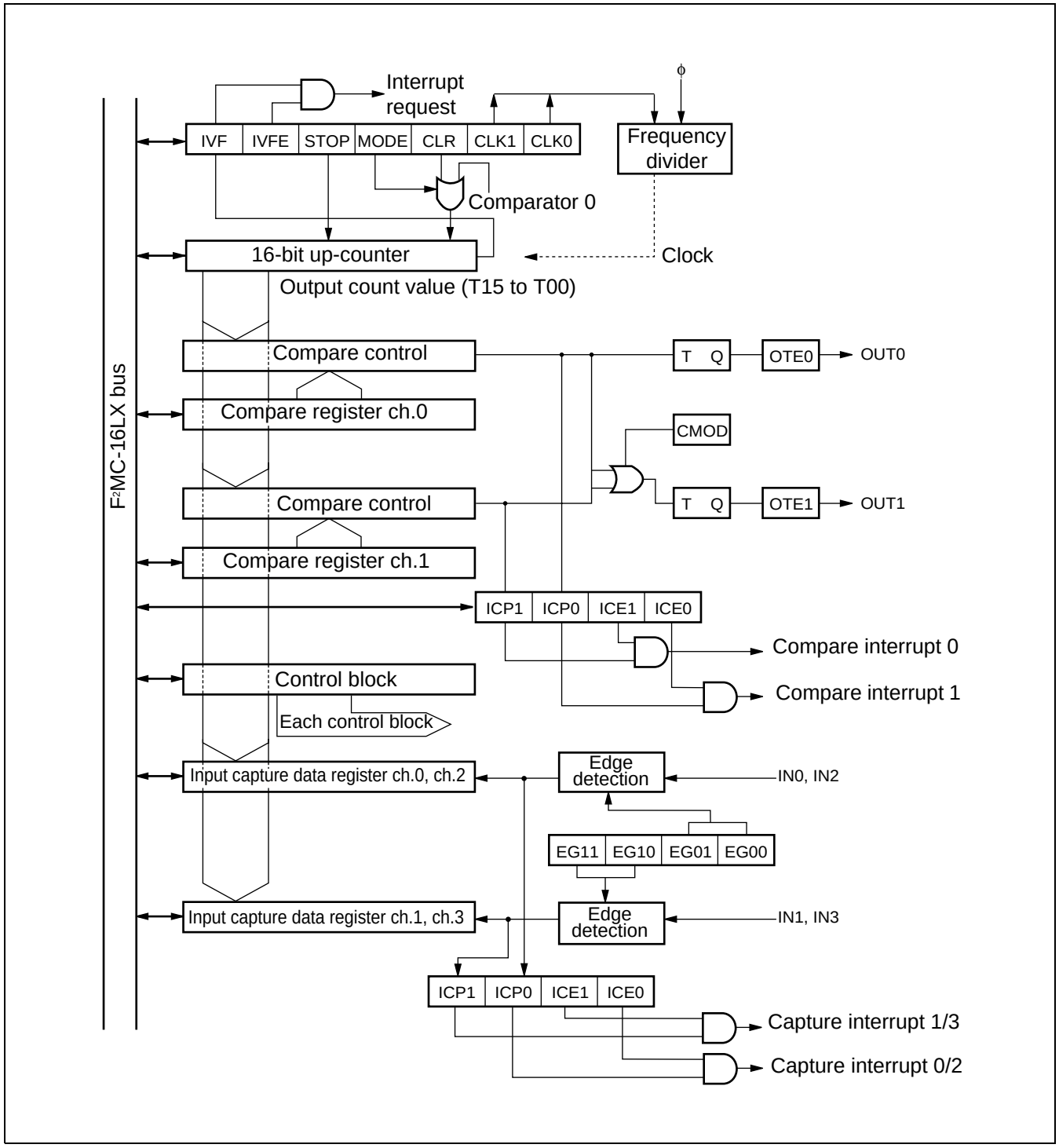
• Input capture control status register 01

bit	7	6	5	4	3	2	1	0	
Address : 000068H	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	ICS01
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Input capture control status register 23

bit	7	6	5	4	3	2	1	0	
Address : 00006AH	ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20	ICS23
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

(5) Block Diagram



8. 16-bit Reload Timer

The 16-bit reload timer has three channels, each of which consists of a 16-bit down counter, a 16-bit reload register, an input pin (TIN), an output pin (TOT), and a control register. The input clock can be selected from among three internal clocks and one external clock.

(1) Register configuration

• Timer control status register (upper)

bit	15	14	13	12	11	10	9	8	
Address : ch0 000049H									TMCSR0 upper
: ch1 00004DH	—	—	—	—	CSL1	CSL0	MOD2	MOD1	TMCSR1 upper
: ch2 000051H									TMCSR2 upper
Access	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)	

• Timer control status register (lower)

bit	7	6	5	4	3	2	1	0	
Address : ch0 000048H									TMCSR0 lower
: ch1 00004CH	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	TMCSR1 lower
: ch2 000050H									TMCSR2 lower
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

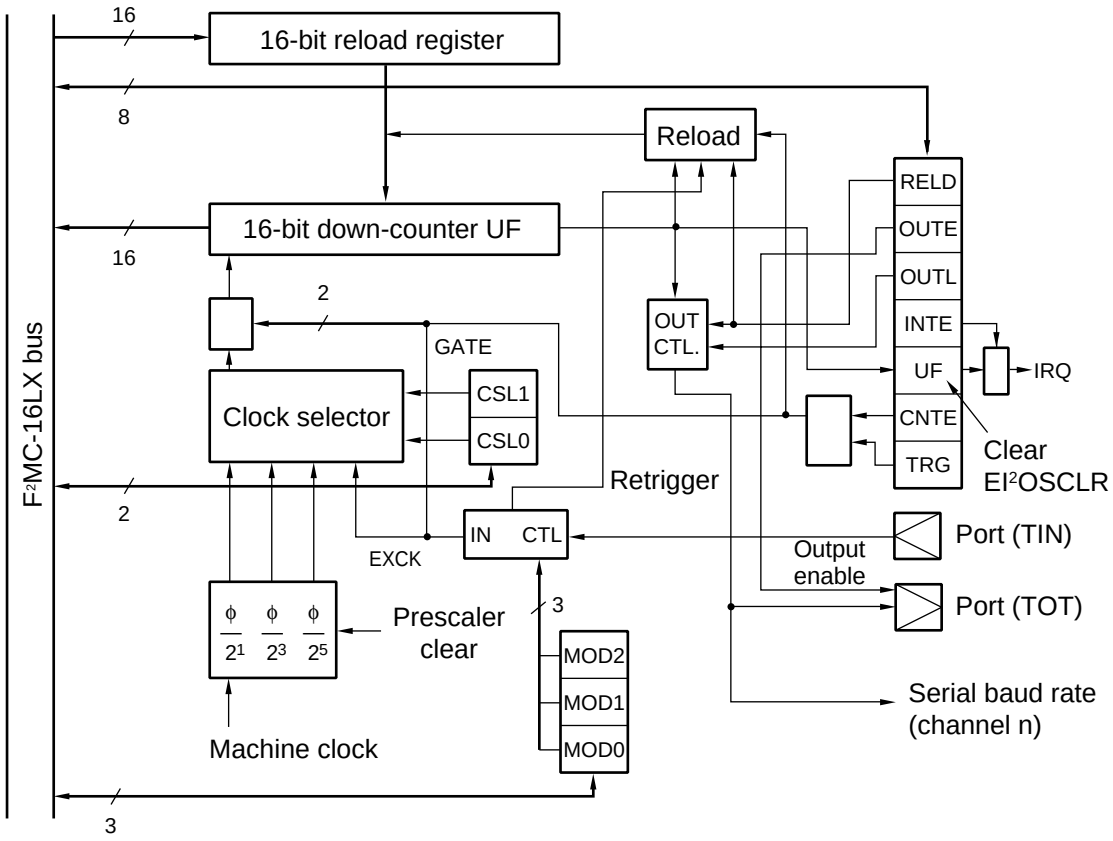
• 16-bit timer register (upper) /16 bit reload register (upper)

bit	15	14	13	12	11	10	9	8	(read)
Address : ch0 00004BH									TMR0 upper
: ch1 00004FH									TMR1 upper
: ch2 000053H									TMR2 upper
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(write)
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	TMRLR0 upper
									TMRLR1 upper
									TMRLR2 upper

• 16-bit timer register (lower) /16 bit reload register (lower)

bit	7	6	5	4	3	2	1	0	(read)
Address : ch0 00004AH									TMR0 lower
: ch1 00004EH									TMR1 lower
: ch2 000052H									TMR2 lower
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(write)
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	TMRLR0 lower
									TMRLR1 lower
									TMRLR2 lower

(2) Block Diagram



Note: Reload timer channels and UART channels are connected as follows

- Reload timer channel 0 : UART0, UART3
- Reload timer channel 1 : UART1, UART4
- Reload timer channel 2 : UART2

9. 8/16-bit PPG

8/16-bit PPG is an 8/16-bit reload timer module. The block performs PPG output in which the pulse output is controlled by the operation of the timer.
The hardware consists of two 8-bit down-counters, four 8-bit reload registers, one 16-bit control register, two external pulse output pins, and two interrupt outputs. The PPG has the following functions.

- 8-bit PPG output in two channels independent operation mode:
  Two independent PPG output channels are available.
- 16-bit PPG output operation mode :
  One 16-bit PPG output channel is available.
- 8 + 8-bit PPG output operation mode :
  Variable-period 8-bit PPG output operation is available by using the output of channel 0 as the clock input to channel 1.
- PPG output operation :
  Outputs pulse waveforms with variable period and duty ratio. Can be used as a D/A converter in conjunction with an external circuit.

(1) Register configuration

• PPG0 operating mode control register

bit	7	6	5	4	3	2	1	0	
Address : ch0 0000044H	PEN0	—	POE0	PIE0	PUF0	—	—	Reserved	PPGC0
Access	(R/W)	(—)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	
Initial value	(0)	(X)	(0)	(0)	(0)	(X)	(X)	(1)	

• PPG1 operating mode control register

bit	15	14	13	12	11	10	9	8	
Address : ch1 0000045H	PEN1	—	POE1	PIE1	PUF1	MD1	MD0	Reserved	PPGC1
Access	(R/W)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(X)	(0)	(0)	(0)	(0)	(0)	(1)	

• PPG0 and 1 output control registers

bit	7	6	5	4	3	2	1	0	
Address : ch0, 1 0000046H	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	Reserved	Reserved	PPGOE
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Reload register H

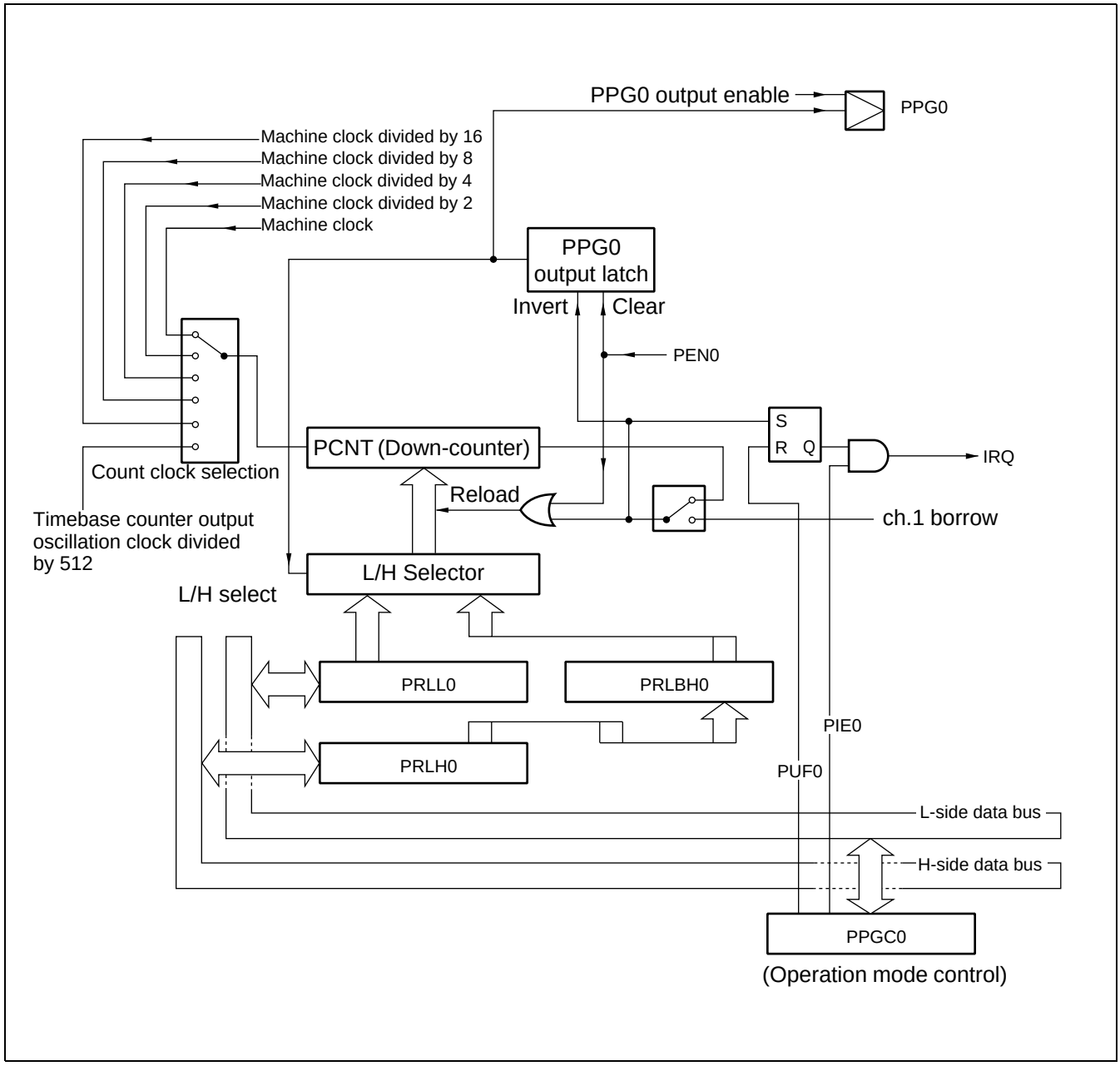
bit	15	14	13	12	11	10	9	8	
Address : ch0 000041H									PRLH0
: ch1 000043H									PRLH1
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Reload register L

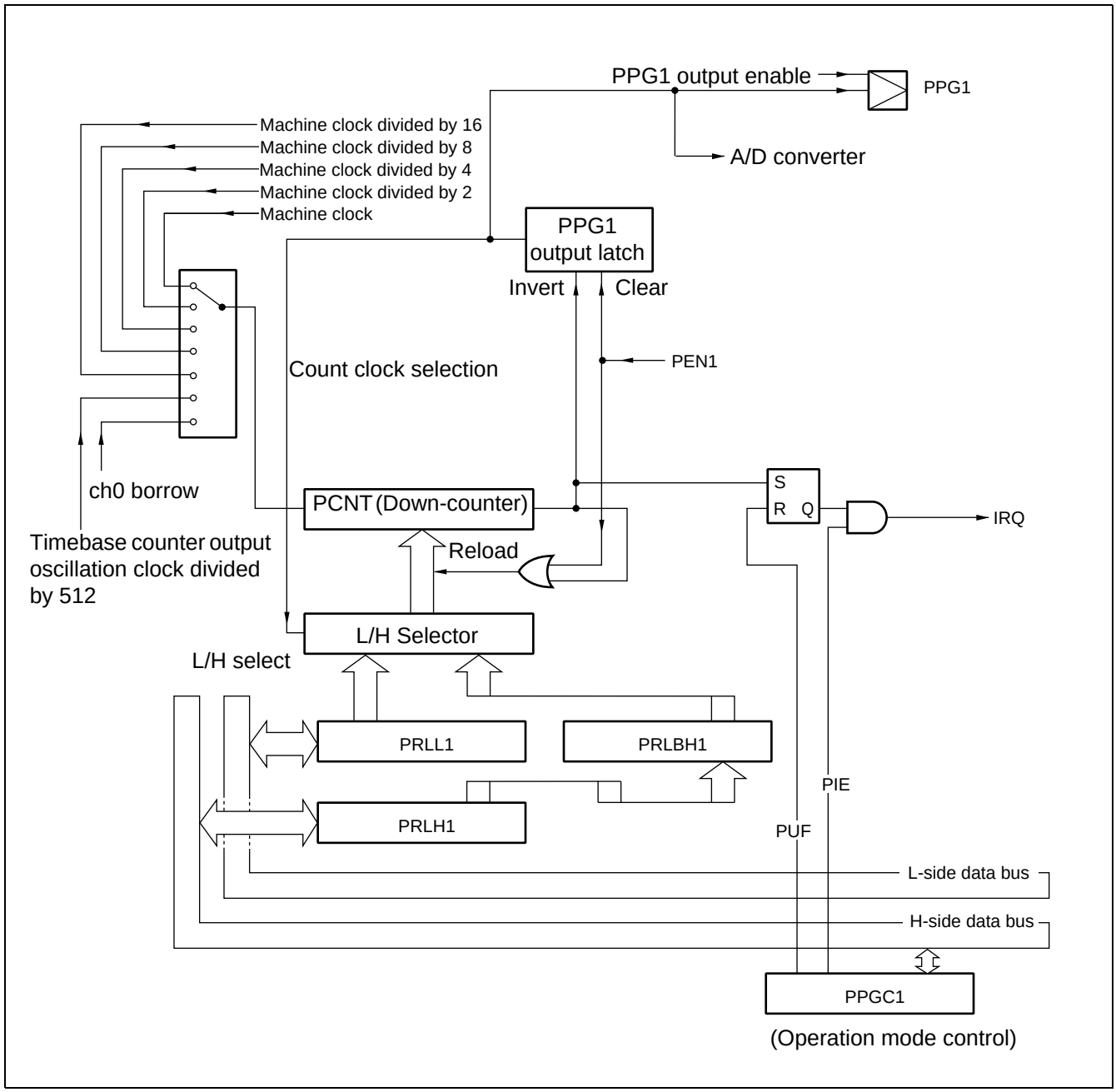
bit	7	6	5	4	3	2	1	0	
Address : ch0 000040H									PRLL0
: ch1 000042H									PRLL1
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram

• Block diagram (8 bit PPG (ch.0))



• Block Diagram (8/16 bit PPG (ch.1))



10. DTP/External Interrupts

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F²MC-16LX CPU. The DTP receives DMA and interrupt processing requests from external peripherals and passes the requests to the F²MC-16LX CPU to activate the intelligent I/O service or interrupt processing. Two request levels (“H” and “L”) are provided for the intelligent I/O service. For external interrupt requests, generation of interrupts on a rising or falling edge as well as on “H” and “L” levels can be selected, giving a total of four types.

(1) Register configuration

• Interrupt/DTP enable register

	bit	7	6	5	4	3	2	1	0	
Address : 0000030H		EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	ENIR
	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Interrupt/DTP source register

	bit	15	14	13	12	11	10	9	8	
Address : 0000031H		ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EIRR
	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

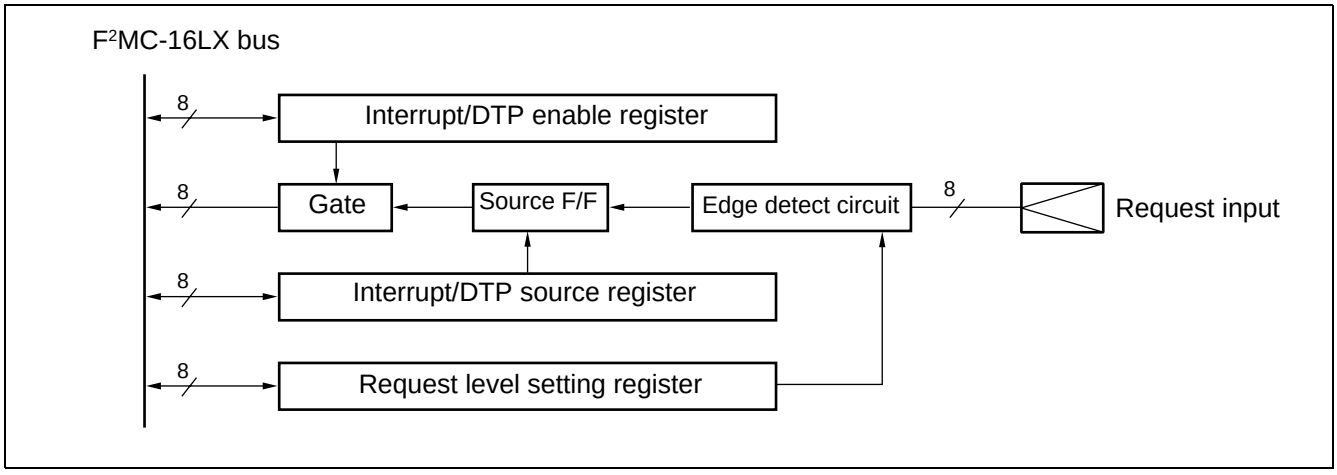
• Request level setting register (lower)

	bit	7	6	5	4	3	2	1	0	
Address : 0000032H		LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	ELVR lower
	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Request level setting register (upper)

	bit	15	14	13	12	11	10	9	8	
Address : 0000033H		LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	ELVR upper
	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

(2) Block Diagram



11. Delayed Interrupt Generation Module

The delayed interrupt generation module is used to generate the task switching interrupt. Interrupt requests to the F²MC-16LX CPU can be generated and cleared by software using this module.

(1) Register configuration

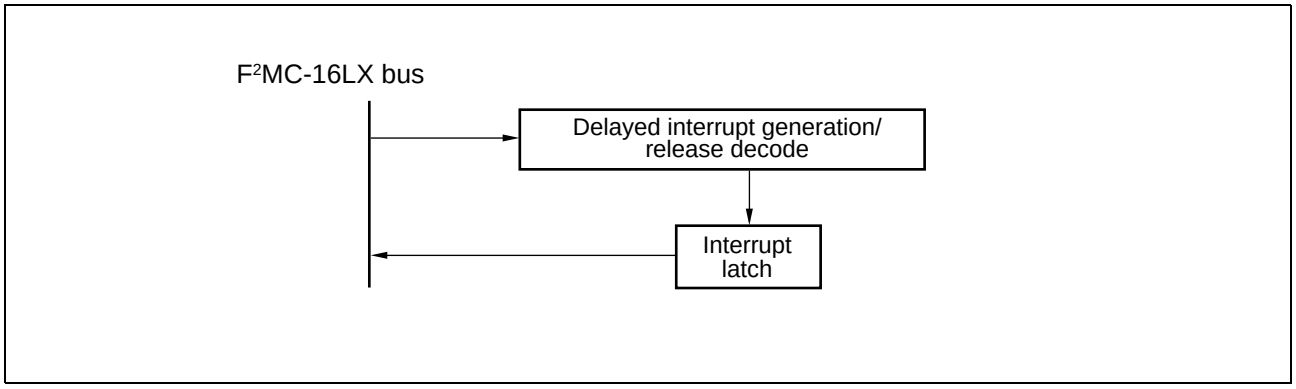
The DIRR register controls generation and clearing of delayed interrupt requests. Writing “1” to the register generates a delayed interrupt request. Writing “0” to the register clears the delayed interrupt request. The register is set to the interrupt cleared state by a reset. Either “0” or “1” can be written to the reserved bits. However, considering possible future extensions, it is recommended that the set bit and clear bit instructions are used for register access.

• Delayed interrupt generation/release register

Address : 00009F$_H$

bit	15	14	13	12	11	10	9	8	
	—	—	—	—	—	—	—	R0	DIRR
Access	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Initial value	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

(2) Block Diagram



12. A/D Converter

The A/D converter converts analog input voltages to digital values. The A/D converter has the following features.

- Conversion time: Minimum of 34.7 μs per channel (for a 12 MHz machine clock)
- Uses RC-type successive approximation conversion with a sample and hold circuit.
- 8/10-bit resolution
- Eight program-selectable analog input channels
  Single conversion mode: Selectively convert one channel.
  Scan conversion mode: Continuously convert multiple channels. Maximum of 8 program selectable channels.
  Continuous conversion mode : Repeatedly convert specified channels.
  Stop conversion mode:Convert one channel then halt until the next activation. (Enables synchronization of the conversion start timing.)
- An A/D conversion completion interrupt request.
  An A/D conversion completion interrupt request to the CPU can be generated on the completion of A/D conversion. This interrupt can activate EI^{2}OS to transfer the result of A/D conversion to memory and is suitable for continuous operation.
- Activation by software, external trigger (falling edge), or timer (rising edge) can be selected.

(1) Register configuration

• Control status register (upper)

bit	15	14	13	12	11	10	9	8	
Address : 000037H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Re-served	ADCS2
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Control status register (lower)

bit	7	6	5	4	3	2	1	0	
Address : 000036H	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	ADCS1
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

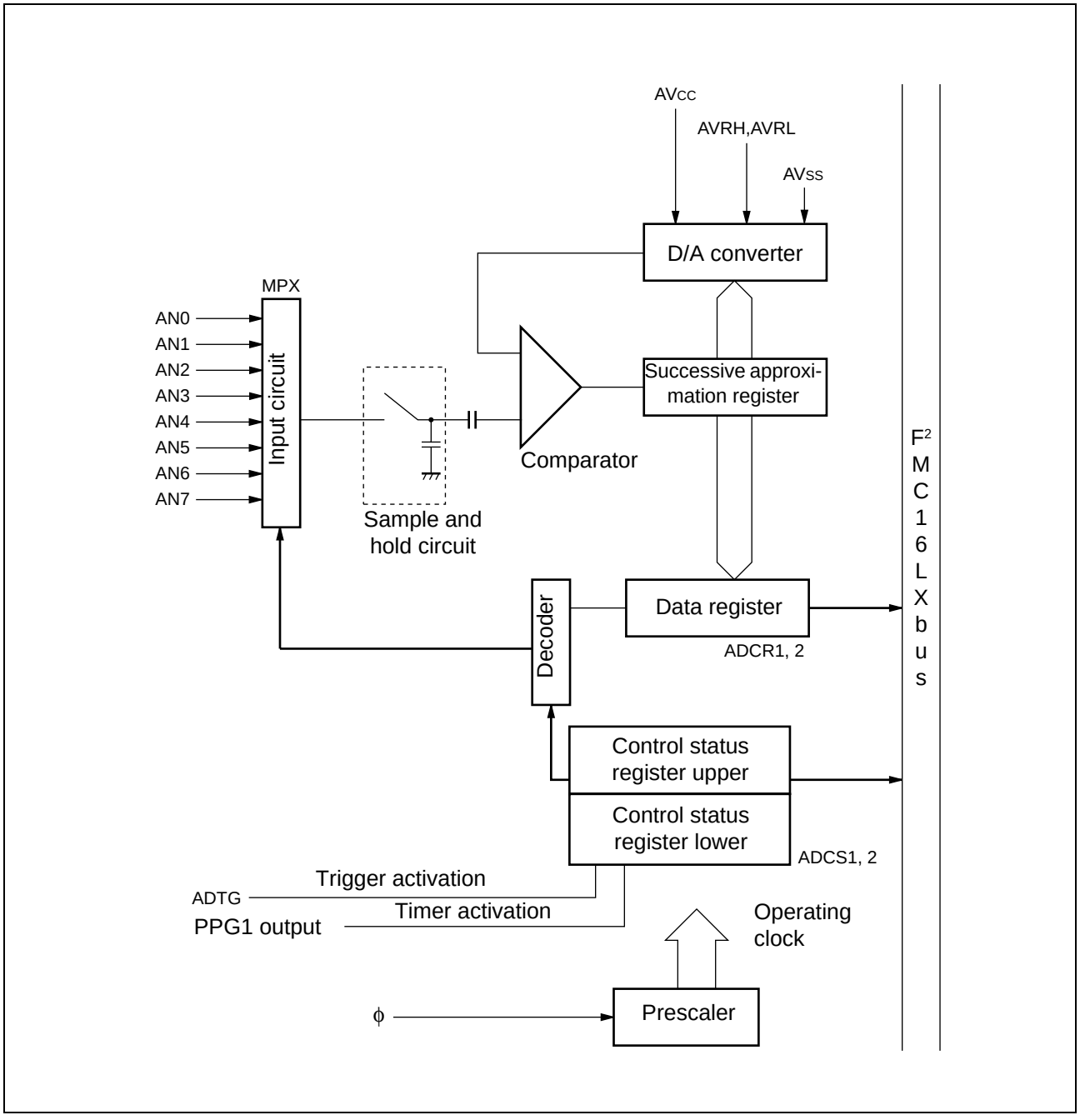
• Data register (upper)

bit	15	14	13	12	11	10	9	8	
Address : 000039H	SELB	ST1	ST0	CT1	CT0	—	D9	D8	ADCR2
Access	(W)	(W)	(W)	(W)	(W)	(—)	(R)	(R)	
Initial value	(0)	(0)	(0)	(0)	(1)	(—)	(X)	(X)	

• Data register (lower)

bit	7	6	5	4	3	2	1	0	
Address : 000038H	D7	D6	D5	D4	D3	D2	D1	D0	ADCR1
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



13. D/A Converter

D/A converter is an R-2R type D/A converter with 8-bit resolution. The device contains two D/A converters. The D/A control register controls the output of the two D/A converters independently.

(1) Register configuration

• D/A converter data register 1

bit	15	14	13	12	11	10	9	8	
Address : 00003B$_H$	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAT1
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• D/A converter data register 0

bit	7	6	5	4	3	2	1	0	
Address : 00003A$_H$	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00	DAT0
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

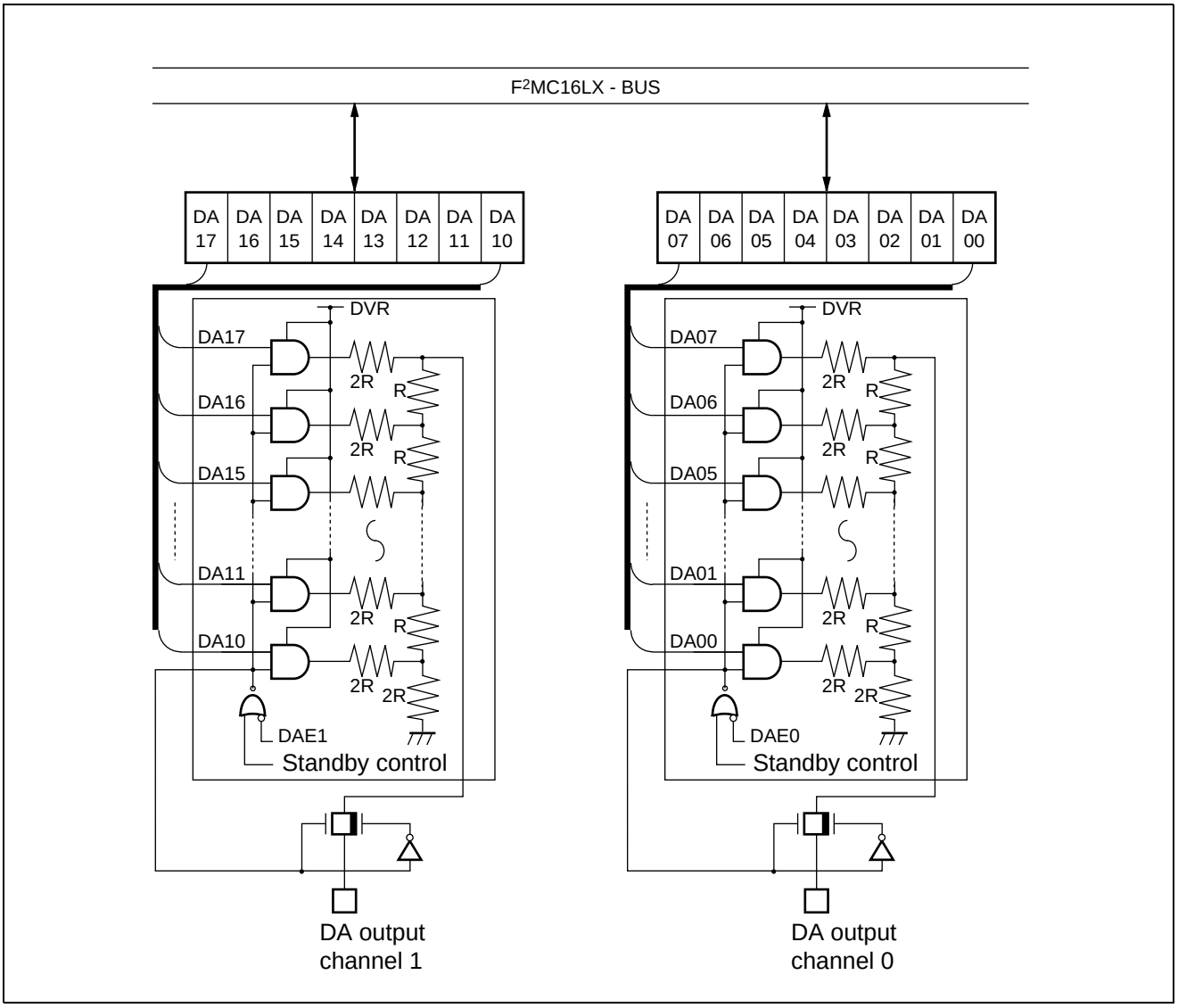
• D/A control register 1

bit	15	14	13	12	11	10	9	8	
Address : 00003D$_H$	—	—	—	—	—	—	—	DAE1	DACR1
Access	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Initial value	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

• D/A control register 0

bit	7	6	5	4	3	2	1	0	
Address : 00003C$_H$	—	—	—	—	—	—	—	DAE0	DACR0
Access	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Initial value	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

(2) Block Diagram



14. Communication Prescaler

The register (clock division control register) of the communication prescaler controls division of the machine clock frequency. It is designed to provide a fixed baud rate for a variety of machine clock frequencies depending on the user setting.
The output from the communication prescaler is used by the UARTs.

(1) Register configuration

• Clock division control registers 0 to 4

		bit	15	14	13	12	11	10	9	8	
Address :	00002C$_H$		MD	—	—	—	DIV3	DIV2	DIV1	DIV0	CDCR0
	00002E$_H$	Access	(R/W)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	CDCR1
	000034$_H$	Initial value	(0)	(—)	(—)	(—)	(1)	(1)	(1)	(1)	CDCR2
	000087$_H$										CDCR3
	00008F$_H$										CDCR4

15. UART

The UART is a serial I/O port for asynchronous (start-stop) communication or clock-synchronous communication.

The UART has the following features:

- Full-duplex double buffering
- Capable of asynchronous (start-stop) and CLK-synchronous communications
- Support for the multiprocessor mode
- Dedicated baud rate generator integratedBaud rate

Operation	Baud rate
Asynchronous	31250/9615/4808/2404/1202 bps
CLK synchronous	2 M/1 M/500 K/250 K/125 K/62.5 Kbps

* : Assuming internal machine clock frequencies of 6, 8, 10, 12, and 16 MHz

- Capable of setting an arbitrary baud rate using an external clock
- Error detection functions (parity, framing, overrun)
- HRz sign transfer signal

(1) Register configuration

• Serial mode register 0 to 4

Address	bit	7	6	5	4	3	2	1	0	
0000020H		MD1	MD0	CS2	CS1	CS0	Re-served	SCKE	SOE	SMR0
0000024H										SMR1
0000028H										SMR2
0000082H	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	SMR3
0000088H	Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	SMR4

• Serial control register 0 to 4

Address	bit	15	14	13	12	11	10	9	8	
0000021H		PEN	P	SBL	CL	A/D	REC	RXE	TXE	SCR0
0000025H										SCR1
0000029H										SCR2
0000083H	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	SCR3
0000089H	Initial value	(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)	SCR4

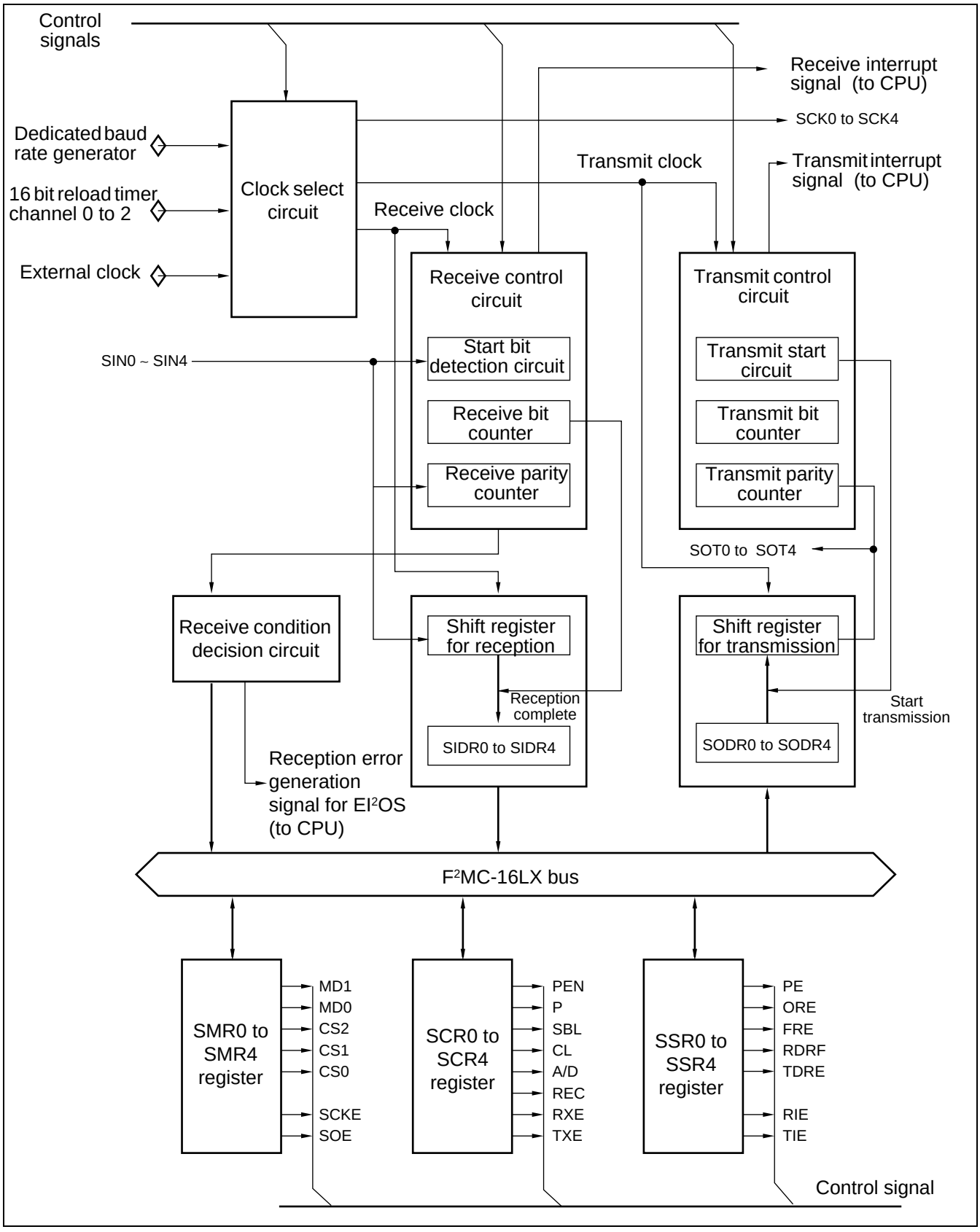
• Serial input register 0 to 4/serial output register 0 to 4

Address	bit	7	6	5	4	3	2	1	0	(read)	(write)
0000022H		D7	D6	D5	D4	D3	D2	D1	D0	SIDR0	SODR0
0000026H										SIDR1	SODR1
000002AH	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	SIDR2	SODR2
0000084H	Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	SIDR3	SODR3
000008AH										SIDR4	SODR4

• Serial status register 0 to 4

Address	bit	15	14	13	12	11	10	9	8	
0000023H		PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE	SSR0
0000027H										SSR1
000002BH										SSR2
0000085H	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(R/W)	(R/W)	SSR3
000008BH	Initial value	(0)	(0)	(0)	(0)	(1)	(—)	(0)	(0)	SSR4

(2) Block Diagram



16. IEBus™ Controller

The IEBus™ (Inter-Equipment Bus) is a small-scale, two-wire serial bus interface designed for data transfer between pieces of equipment.

This interface is applicable, for example, as a bus interface for controlling vehicle-mounted devices.

IEBus™ has the following features:

- Multitasking
  Any of the units connected to the IEBus™ can transmit data to another one.
- Broadcast function (Communication from one unit to multiple units)
  Group broadcast : Broadcast to a group of units
  All-unit broadcast : Broadcast to all units
- Three modes can be selected for different transmission speeds.

	IEBus™ internal frequency	
	6 MHz	6.29 MHz
Mode 0	About 3.9 Kbps	About 4.1 Kbps
Mode 1	About 17 Kbps	About 18 Kbps
Mode 2	About 26 Kbps	About 27 Kbps

- Data buffer for transmission
  8-byte FIFO buffer
- Data buffer for reception
  8-byte FIFO buffer
- CPU internal operating frequency (12 MHz, 12.58 MHz)
- Frequency tolerance
  In mode 0 or 1 : ±1.5%
  In mode 2 : ±0.5%

(1) Register configuration

• Local-office address setting register H

	bit	15	14	13	12	11	10	9	8	
Address : 000071H		Reserved	Reserved	Reserved	Reserved	MA11	MA10	MA09	MA08	MAWH
	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Local-office address setting register L

	bit	7	6	5	4	3	2	1	0	
Address : 000070H		MA07	MA06	MA05	MA04	MA03	MA02	MA01	MA00	MAWL
	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Slave address setting register H

	bit	15	14	13	12	11	10	9	8	
Address : 000073H		Reserved	Reserved	Reserved	Reserved	SA11	SA10	SA09	SA08	SAWH
	Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
	Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(Continued)

• Slave address setting register L

bit	7	6	5	4	3	2	1	0	
Address : 000072H	SA07	SA06	SA05	SA04	SA03	SA02	SA01	SA00	SAWL
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Broadcast control bit setting register

bit	15	14	13	12	11	10	9	8	
Address : 000075H	DO3	DO2	DO1	DO0	C3	C2	C1	C0	DCWR
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Broadcast control bit read register

bit	15	14	13	12	11	10	9	8	
Address : 00007FH	DO3	DO2	DO1	DO0	C3	C2	C1	C0	DCRR
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(0)	(0)	(0)	(X)	(X)	(X)	(X)	(X)	

• Message length bit setting register

bit	7	6	5	4	3	2	1	0	
Address : 000074H	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0	DEWR
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

• Message length bit read register

bit	7	6	5	4	3	2	1	0	
Address : 00007EH	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0	DERR
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Command register H

bit	15	14	13	12	11	10	9	8	
Address : 000077H	MD1	MD0	PCOM	RIE	TIE	GOTM	GOTS	Reserved	CMRH
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(X)	

• Command register L

bit	7	6	5	4	3	2	1	0	
Address : 000076H	RXS	TXS	TIT1	TIT0	CS1	CS0	RDBC	WDBC	CMRL
Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(1)	(1)	(0)	(0)	(0)	(0)	(0)	(0)	

• Status register H

bit	15	14	13	12	11	10	9	8	
Address : 000079H	COM	TE	PEF	ACK	RIF	TIF	TSL	EOD	STRH
Access	(R)	(R/W)	(R)	(R)	(R/W)	(R/W)	(R)	(R)	
Initial value	(0)	(0)	(X)	(X)	(0)	(0)	(0)	(0)	

(Continued)

(Continued)

• Status register L

bit	7	6	5	4	3	2	1	0	
Address : 000078H	WDBF	RDBF	WDBE	RDBE	ST3	ST2	ST1	ST0	STRL
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(0)	(0)	(1)	(1)	(X)	(X)	(X)	(X)	

• Lock read register H

bit	15	14	13	12	11	10	9	8	
Address : 00007BH	Reserved	Reserved	Reserved	LOC	LD11	LD10	LD09	LD08	LRRH
Access	(R)	(R)	(R)	(R/W)	(R)	(R)	(R)	(R)	
Initial value	(1)	(1)	(1)	(0)	(X)	(X)	(X)	(X)	

• Lock read register L

bit	7	6	5	4	3	2	1	0	
Address : 00007AH	LD07	LD06	LD05	LD04	LD03	LD02	LD01	LD00	LRRL
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Master address read register H

bit	15	14	13	12	11	10	9	8	
Address : 00007DH	Reserved	Reserved	Reserved	Reserved	MA11	MA10	MA09	MA08	MARH
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(1)	(1)	(1)	(1)	(X)	(X)	(X)	(X)	

• Master address read register L

bit	7	6	5	4	3	2	1	0	
Address : 00007CH	MA07	MA06	MA05	MA04	MA03	MA02	MA01	MA00	MARL
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

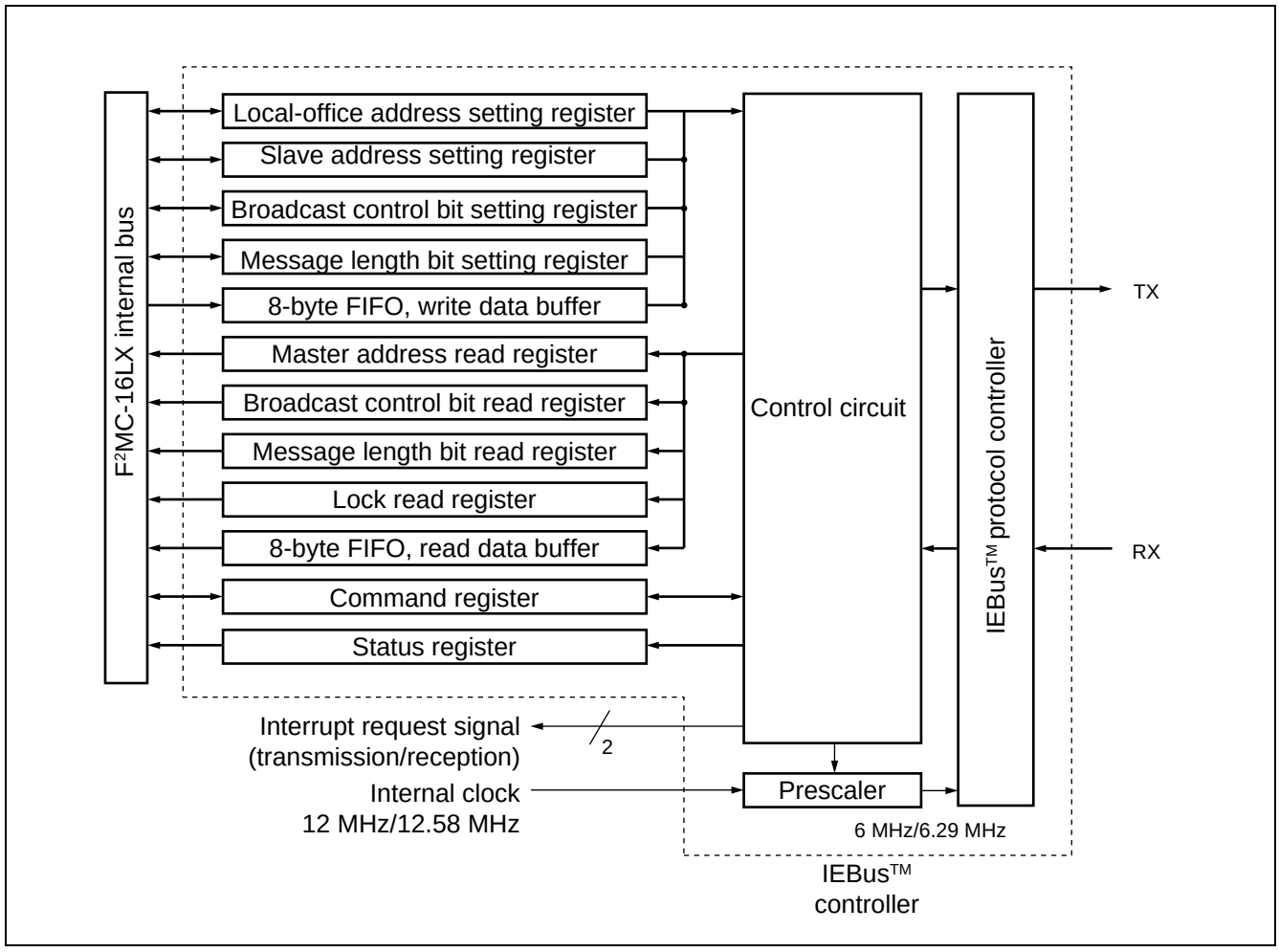
• Read data buffer

bit	15	14	13	12	11	10	9	8	
Address : 000081H	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	RDB
Access	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

• Write data buffer

bit	7	6	5	4	3	2	1	0	
Address : 000080H	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	WDB
Access	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



The control circuit in the IEBus™ controller executes the following control functions:

- Controls the number of bytes in data to be transmitted and received.
- Controls the maximum number of bytes transmitted.
- Detects the results of arbitration.
- Evaluates the return of acknowledgment of each field.
- Generates interrupt signals.

17. Clock Monitor Function

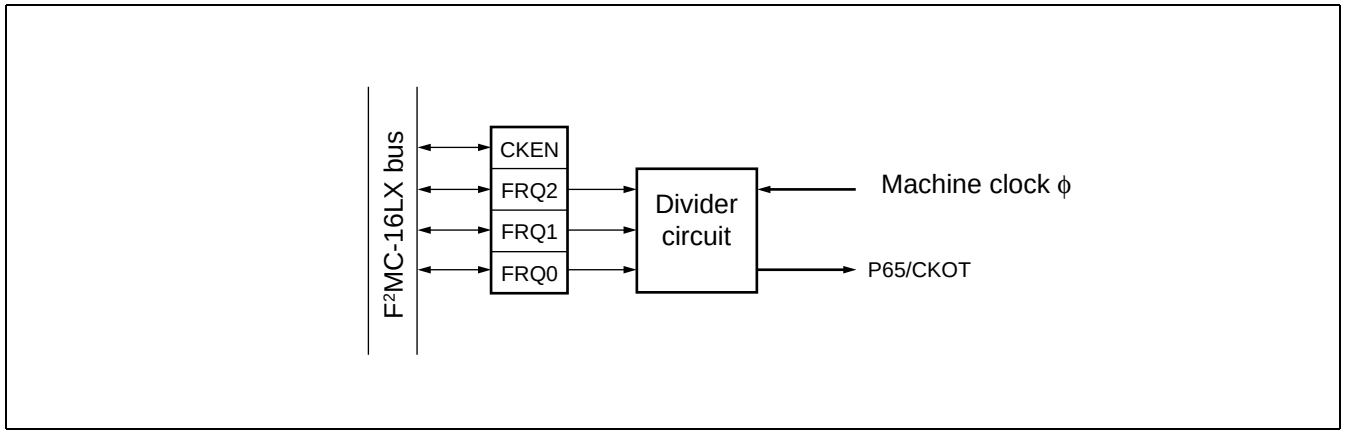
The clock monitor function outputs the frequency-divided machine clock signal (for monitoring purposes) from the CKOT pin.

(1) Register configuration

• Clock output enable register

bit	7	6	5	4	3	2	1	0	
Address : 00003E$_H$	—	—	—	—	CKEN	FRQ2	FRQ1	FRQ0	CLKR
Access	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)	

(2) Block Diagram



18. Address Match Detection Function

When an address matches the value set in the address detection register, the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code (01H). When executing a set instruction, the CPU executes the INT9 instruction. The address match detection function is implemented by processing using the INT9 interrupt routine.

The device contains two address detection registers, each provided with a compare enable bit. When the value set in the address detection register matches an address and the interrupt enable bit is “1”, the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code.

(1) Register configuration

• Program address detection register 0 to 2 (PADR0)

			bit	7	6	5	4	3	2	1	0
PADR0 (lower)	Address	: 001FF0H									
			Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
			Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

			bit	17	16	15	14	13	12	11	10
PADR0 (middle)	Address	: 001FF1H									
			Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
			Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

			bit	7	6	5	4	3	2	1	0
PADR0 (upper)	Address	: 001FF2H									
			Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
			Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

• Program address detection register 3 to 5 (PADR1)

			bit	17	16	15	14	13	12	11	10
PADR1 (lower)	Address	: 001FF3H									
			Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
			Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

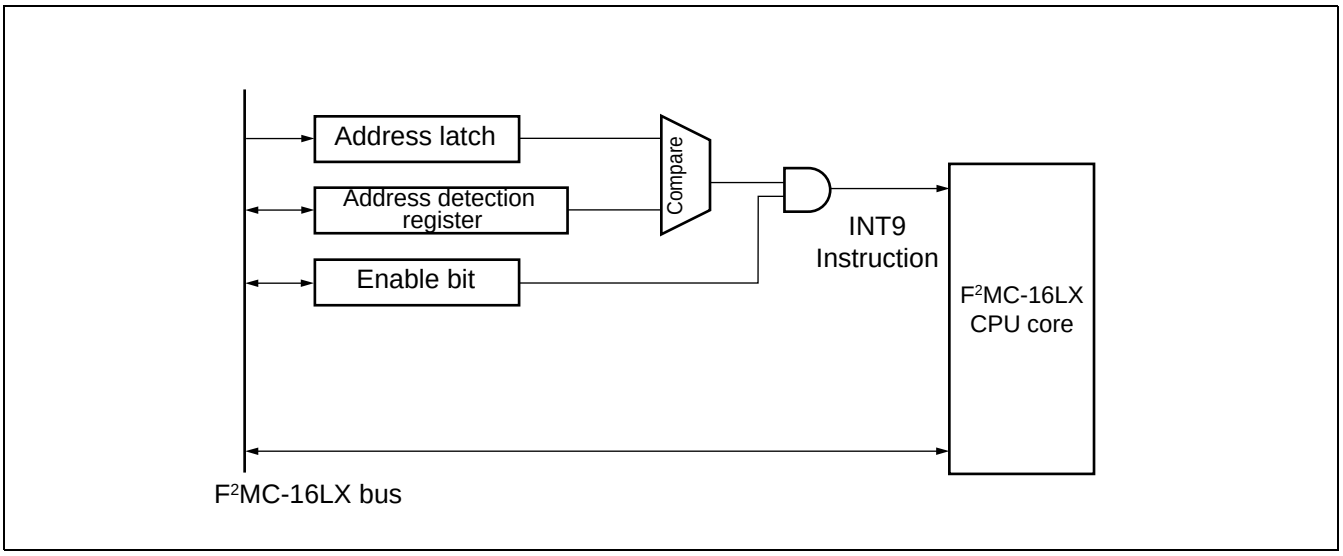
			bit	7	6	5	4	3	2	1	0
PADR1 (middle)	Address	: 001FF4H									
			Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
			Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

			bit	17	16	15	14	13	12	11	10
PADR1 (upper)	Address	: 001FF5H									
			Access	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
			Initial value	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

• Program address detection control/status register (PACSR)

		bit	7	6	5	4	3	2	1	0
Address	: 00009EH		Re-served	Re-served	Re-served	Re-served	AD1E	Re-served	AD0E	Re-served
		Access	(–)	(–)	(–)	(–)	(R/W)	(–)	(R/W)	(–)
		Initial value	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

(2) Block Diagram



19. ROM Mirroring Function Selection Module

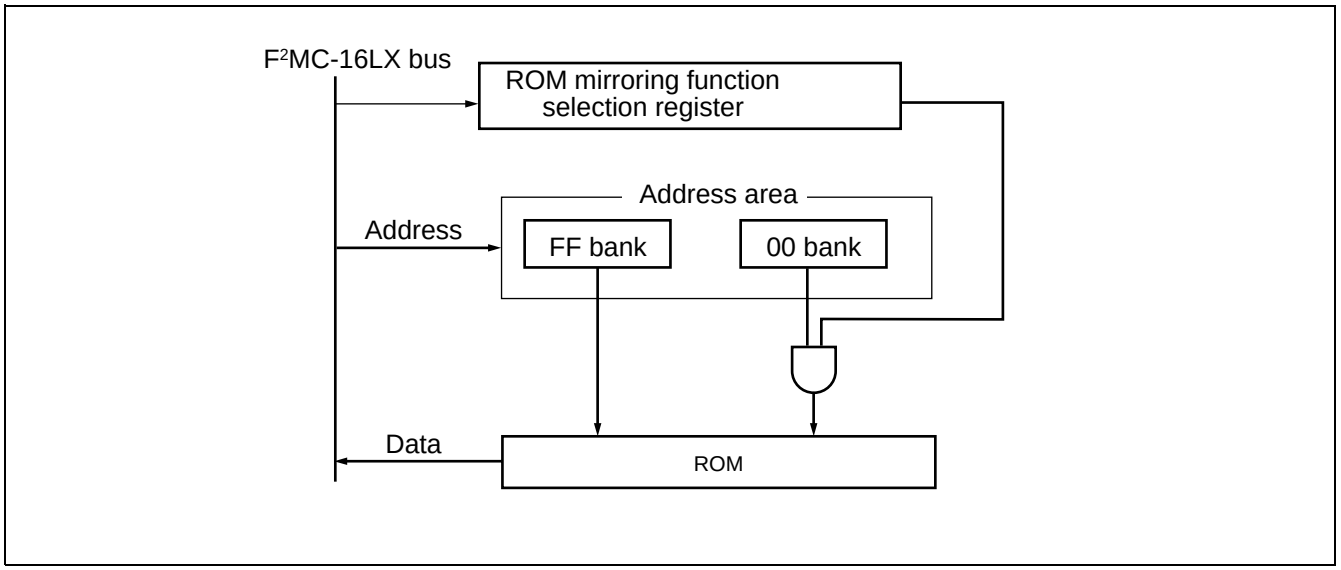
The ROM mirroring function selection module can select what the FF bank allocated the ROM sees through the 00 bank according to register settings.

(1) Register configuration

• ROM mirroring function selection register

bit	15	14	13	12	11	10	9	8	
Address : 00006F$_H$	—	—	—	—	—	—	—	MI	ROMM
Access	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(W)	

(2) Block Diagram



20. One-Megabit Flash Memory

The 1Mbit flash memory is allocated in the FE_H to FF_H banks on the CPU memory map. Like masked ROM, flash memory is read-accessible and program-accessible to the CPU using the flash memory interface circuit. The flash memory can be programmed/erased by the instruction from the CPU via the flash memory interface circuit. The flash memory can therefore be reprogrammed (updated) while still on the circuit board under integrated CPU control, allowing program code and data to be improved efficiently.
Note that sector operations such as “enable sector protect” cannot be used.

Features of 1Mbit flash memory

- 128K words x 8 bits or 64K words x 16 bits (16K + 512 x 2 + 7K + 8K + 32K + 64K) sector configuration
- Automatic program algorithm (Embedded Algorithm*: Same as the MBM29F400TA)
- Erasure suspend/resume function integrated
- Detection of programming/erasure completion using the data polling or toggle bit
- Detection of programming/erasure completion using CPU interrupts
- Compatible with JEDEC standard commands
- Capable of erasing data sector by sector (arbitrary combination of sectors)
- Minimum number of times of programming/erasure: 100,000

* : Embedded Algorithm is a trademark of Advanced Micro Devices, Inc.

(1) Register configuration

- Flash memory control status register

	bit	7	6	5	4	3	2	1	0	
Address	: 0000AE$_H$	INTE	RDY-INT	WE	RDY	Reserved	LPM1	Reserved	LPM0	FMCS
	Access	(R/W)	(R/W)	(R/W)	(R)	(W)	(R/W)	(W)	(R/W)	
	Initial value	(0)	(0)	(0)	(X)	(0)	(0)	(0)	(0)	

(2) Sector configuration of 1Mbit flash memory

The 1Mbit flash memory has the sector configuration illustrated below. The addresses in the illustration are the upper and lower addresses of each sector.
When accessed from the CPU, SA0 and SA1 to SA4 are allocated in the FE and FF bank registers, respectively.

Flash memory	CPU address	Programmer address *
SA4 (16 Kbytes)	$FFFFFF_H$	$7FFFF_H$
	$FFC000_H$	$7C000_H$
SA3 (8 Kbytes)	$FFBFFF_H$	$7BFFF_H$
	$FFA000_H$	$7A000_H$
SA2 (8 Kbytes)	$FF9FFF_H$	$79FFF_H$
	$FF8000_H$	78000_H
SA1 (32 Kbytes)	$FF7FFF_H$	$77FFF_H$
	$FF0000_H$	70000_H
SA0 (64 Kbytes)	$FEFFFF_H$	$6FFFF_H$
	$FE0000_H$	60000_H

* : Programmer addresses correspond to CPU addresses when data is programmed in flash memory by a parallel programmer. Programmer addresses are used to program/erase data using a general-purpose programmer.

21. Low-Power Consumption Control Circuit

The operation modes of the MB90580C series are the PLL clock, PLL sleep, watch, main clock, main sleep, stop, and hardware standby modes. The operation modes excluding the PLL clock mode are classified as low-power consumption modes.

The low power consumption circuit has the following functions.

- Main clock mode/Main sleep mode
  In either mode, the microcontroller operates only with the main clock (OSC oscillation clock), using the main clock as the operating clock while suspending the PLL clock (VCO oscillation clock).
- PLL sleep mode/Main sleep mode
  These modes stop only the operation clock of the CPU, leaving the other clocks active.
- Watch mode
  The watch mode allows only the time-base timer to operate.
- Stop mode/Hardware standby mode
  These modes stop oscillation while retaining data at the lowest power consumption. The CPU intermittent operation function causes the clock supplied to the CPU to operate intermittently when the CPU accesses a register, internal memory, internal resource, or external bus. This function saves power consumption by decreasing the execution speed of the CPU while providing high-speed clock signals to the internal resources.
  The PLL clock multiplication factor can be selected from among 1, 2, 3, and 4 using the CS1 and CS0 bits in the clock selection register.
  The WS1 and WS0 bits can be used to set the oscillation settling time for the main clock, which is taken to wake up from the stop or hardware standby mode.

(1) Register configuration

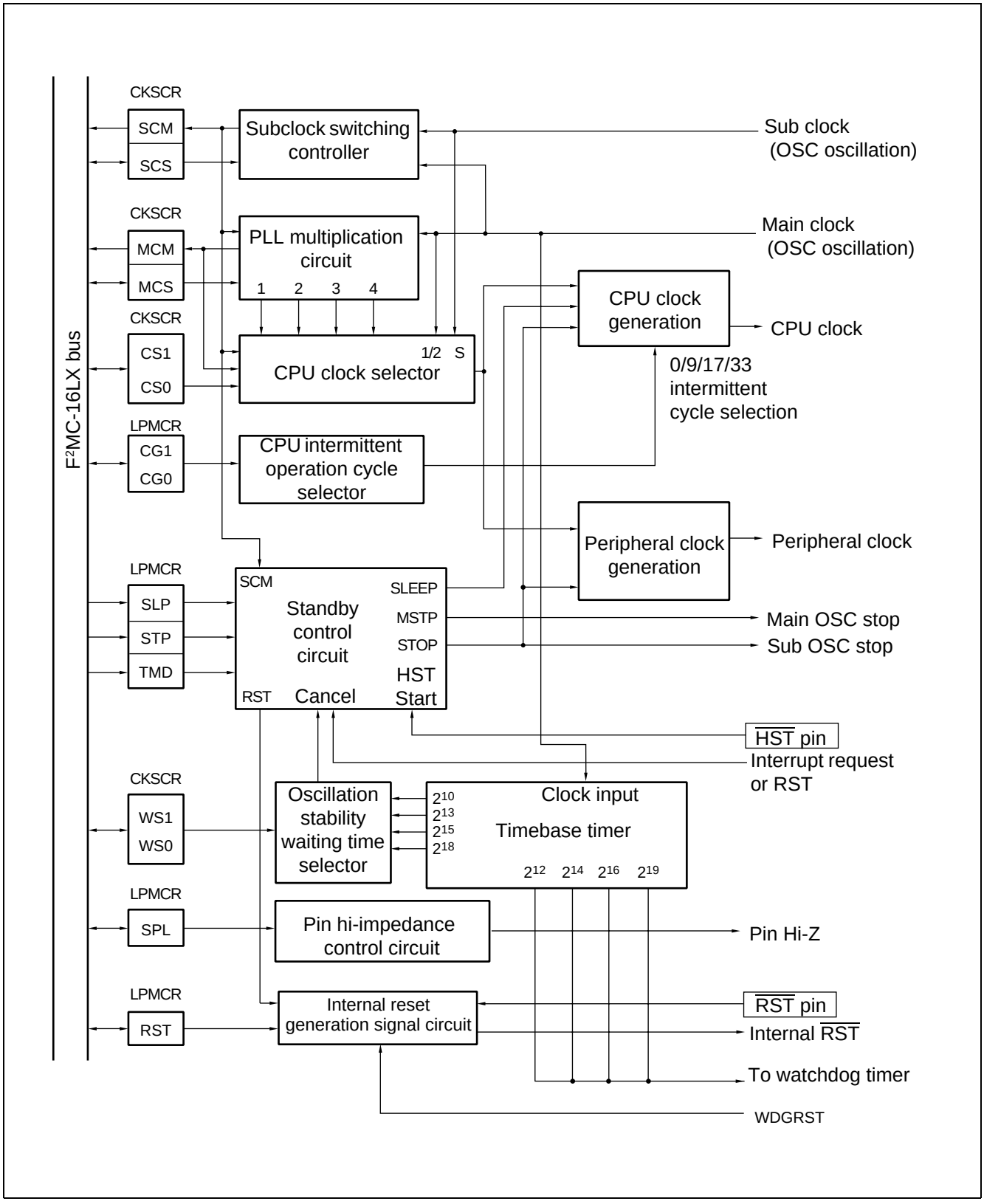
• Low-power consumption mode control register

bit	7	6	5	4	3	2	1	0	
Address : 0000A0H	STP	SLP	SPL	RST	TMD	CG1	CG0	—	LPMCR
Access	(W)	(W)	(R/W)	(W)	(—)	(R/W)	(R/W)	(—)	
Initial value	(0)	(0)	(0)	(1)	(1)	(0)	(0)	(—)	

• Clock selection register

bit	15	14	13	12	11	10	9	8	
Address : 0000A1H	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	CKSCR
Access	(R)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value	(1)	(1)	(1)	(1)	(1)	(1)	(0)	(0)	

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} \geq AV_{CC}$ *1
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH/L, AVRH ≥ AVRL
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} \geq DV_{CC}$
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
“L” level maximum output current	I_{OL}	—	15	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	Average output current = operating current × operating efficiency
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Average output current = operating current × operating efficiency
“H” level maximum output current	I_{OH}	—	–15	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	Average output current = operating current × operating efficiency
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Average output current = operating current × operating efficiency
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : AV_{CC} shall never exceed V_{CC} when power on.

*2 : V_I and V_O shall never exceed V_{CC} + 0.3 V.

*3 : The maximum output current is a peak value for a corresponding pin.

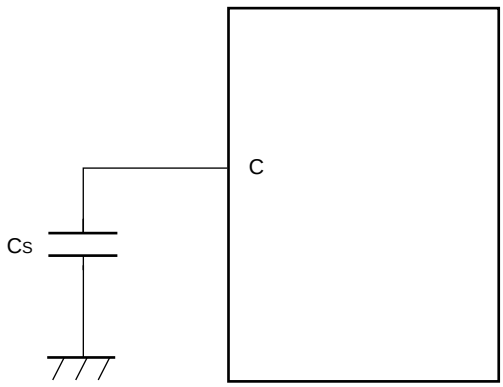
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	5.5	V	Normal operation (MB90583C/CA, MB90587C/CA, MB90V580B)
		4.5	5.5	V	Normal operation (MB90F583C/CA)
	V_{CC}	3.0	5.5	V	Retains status at the time of operation stop
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC}+0.3	V	CMOS input pin
	V_{IHS}	0.8 V_{CC}	V_{CC}+0.3	V	CMOS hysteresis input pin
	V_{IHM}	V_{CC} – 0.3	V_{CC}+0.3	V	MD pin input
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	V_{SS} – 0.3	V_{SS}+0.3	V	MD pin input
Smoothing capacitor	C_S	0.1	1.0	µF	Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.
Operating temperature	T_A	–40	+85	°C	

• C pin connection circuit



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = –2.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 4.5 V, I_{OL} = 2.0 mA	—	—	0.4	V	
Input leakage current	I_{IL}	All input pins	V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal operation at 16 MHz, Normal operation	—	27	33	mA	MB90583C/CA, MB90587C/CA
				—	40	50	mA	MB90F583C/CA
			V_{CC} = 5.0 V, Internal operation at 12.58 MHz, Normal operation	—	22	26	mA	MB90583C/CA
				—	35	45	mA	MB90F583C/CA
			V_{CC} = 5.0 V, Internal operation at 16 MHz, When data written in flash mode pro-gramming of erasing	—	45	60	mA	MB90F583C/CA
			V_{CC} = 5.0 V, Internal operation at 12.58 MHz, When data written in flash mode pro-gramming of erasing	—	40	50	mA	
	I_{CCS}		V_{CC} = 5.0 V, Internal operation at 16 MHz, In sleep mode	—	7	12	mA	MB90587C/CA
				—	15	20	mA	MB90583C/CA, MB90F583C /CA
			V_{CC} = 5.0 V Internal operation at 12.58 MHz, In sleep mode	—	6	10	mA	MB90587C/CA
				—	12	18	mA	MB90583C/CA, MB90F583C/CA
	I_{CCL}		V_{CC} = 5.0 V, Internal operation at 8 kHz, Subsystem operatin, T_A = 25 °C	—	0.1	1.0	mA	MB90583C, MB90587C
				—	4	7	mA	MB90F583C

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*	I_{CCLS}	V_{CC}	V_{CC} = 5.0 V, Internal operation at 8 kHz, In subsleep mode, T_A = 25 °C	—	30	50	µA	MB90583C, MB90587C, MB90F583C
	I_{CCT}		V_{CC} = 5.0 V, Internal operation at 8 kHz, In clock mode, T_A = 25 °C	—	15	30	µA	MB90583C, MB90587C, MB90F583C
	I_{CCH}		In stop mode, T_A = 25 °C	—	5	20	µA	MB90583C/CA MB90587C/CA, MB90F583C/CA
Input capacitance	C_{IN}	Except AV_{CC}, AV_{SS}, C, V_{CC} and V_{SS}	—	—	10	80	pF	
Open-drain output leakage current	I_{leak}	P40 to P47	—	—	0.1	5	µA	Open-drain output setting
Pull-up resistance	R_{UP}	P00 to P07 P10 to P17 P60 to P65 $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

* : The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice. The power supply current is measured with an external clock.

4. AC Characteristics

(1) Clock Timings

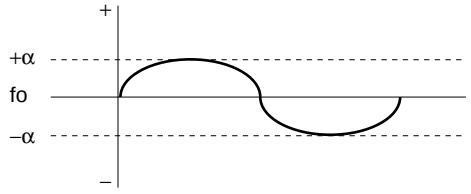
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	f_C	X0, X1	—	3	—	16	MHz	
	f_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		62.5	—	333	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Frequency fluctuation rate locked*	Δf	—		—	—	5	%	
Input clock pulse width	P_{WH} P_{WL}	X0		10	—	—	ns	Recommened duty ratio of 30% to 70%
	P_{WLH} P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise/fall time	t_{CR} t_{CF}	X0		—	—	5	ns	External clock operation
Internal operating clock frequency	f_{CP}	—		1.5	—	16	MHz	Main clock operation
	f_{LCP}	—		—	8.192	—	kHz	Subclock operation
Internal operating clock cycle time	t_{CP}	—		62.5	—	666	ns	Main clock operation
	t_{LCP}	—		—	122.1	—	µs	Subclock operation

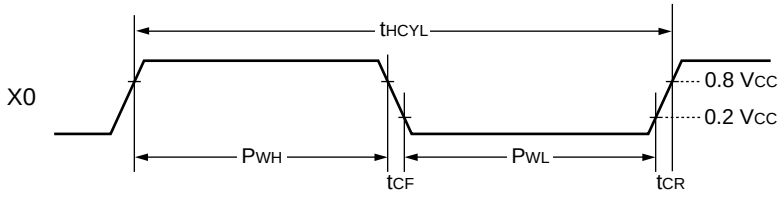
*: The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

$$\Delta f = \frac{|\alpha|}{fo} \times 100\ (\%)$$

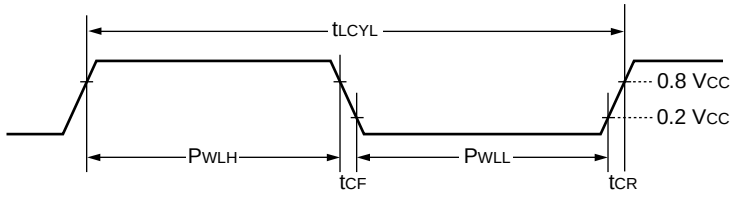
Center frequency



• X0, X1 clock timing

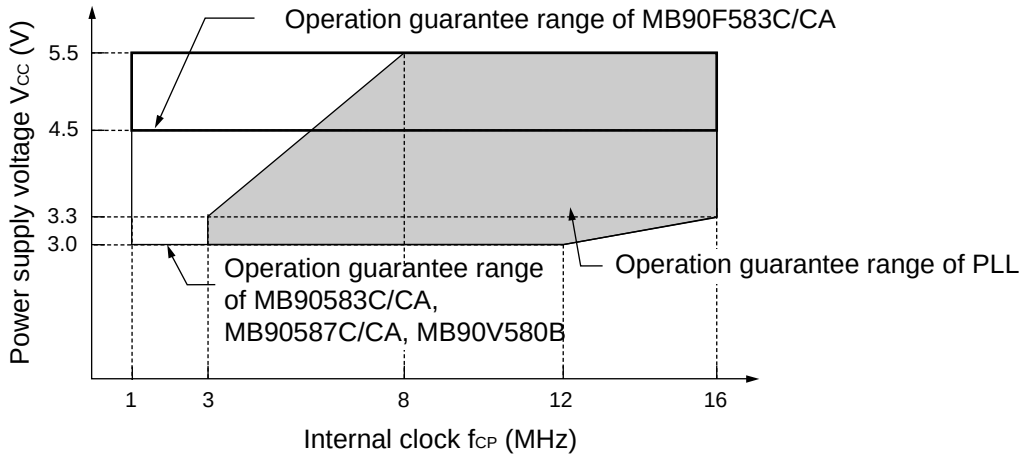


• X0A, X1A clock timing

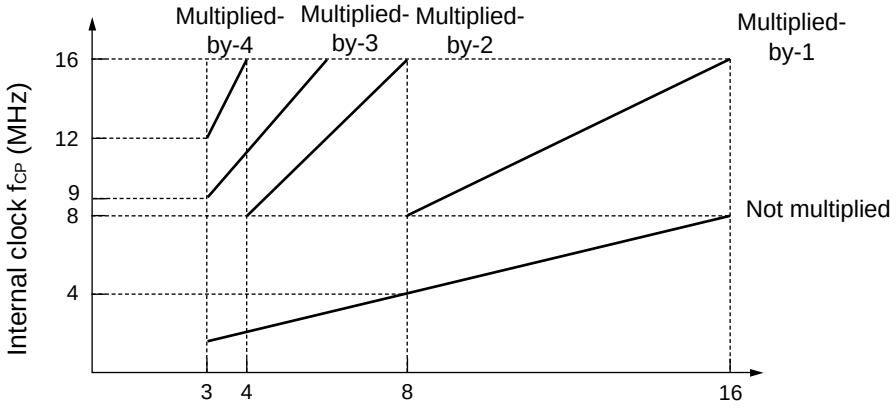


• PLL operation guarantee range

Relationship between internal operating clock frequency and power supply voltage



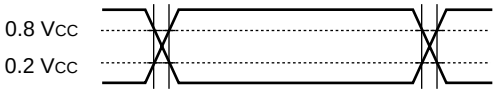
Relationship between oscillating frequency and internal operating clock frequency



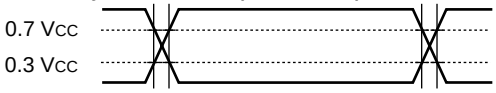
The AC ratings are measured for the following measurement reference voltages

• Input signal waveform

Hystheresis input pin

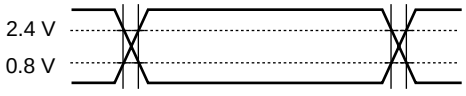


Pins other than hystheresis input/MD input



• Output signal waveform

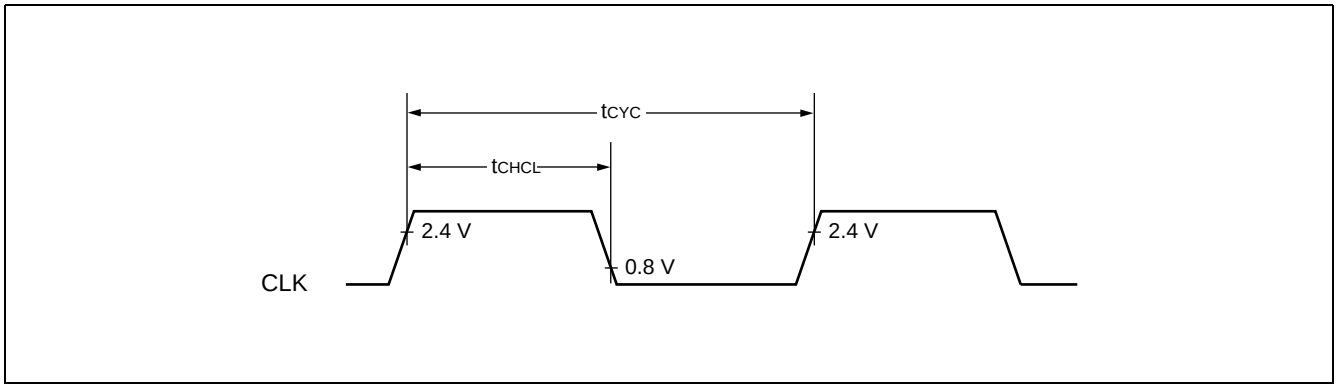
Output pin



(2) Clock Output Timings

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

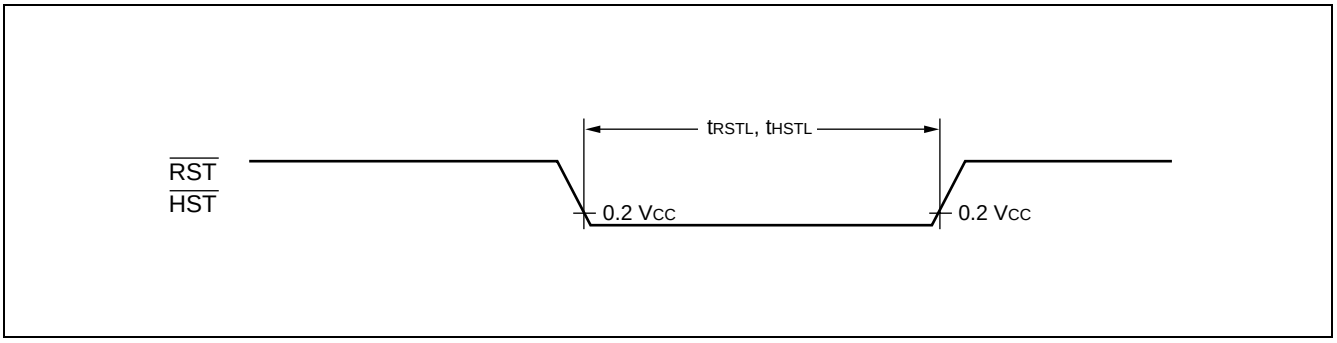
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock cycle time	t_{CYC}	CLK	V_{CC} = 5 V ± 10%	62.5	—	ns	
CLK↑ → CLK↓	t_{CHCL}			20	—	ns	



(3) Reset, Hardware Standby Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	4 t_{CP}	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$		4 t_{CP}	—	ns	



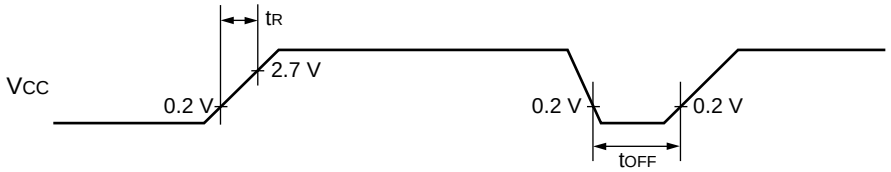
(4) Power-on Reset

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

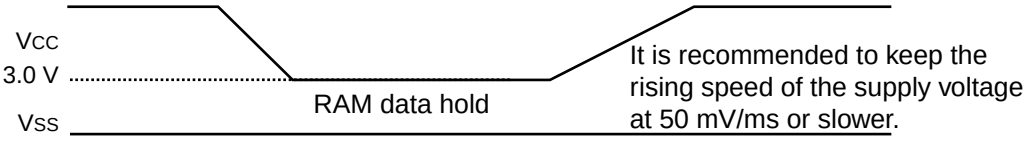
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	0.05	30	ms	
Power supply cut-off time	t_{OFF}	V_{CC}		4	—	ms	Due to repeated operations

* : VCC must be kept lower than 0.2 V before power-on.

Note The above values are used for causing a power-on reset.
If $\overline{HST}$ = “L”, be sure to turn the power supply on using the above values to cause a power-on reset whether or not the power-on reset is required.
Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 mV or fewer per second, however, you can use the PLL clock.

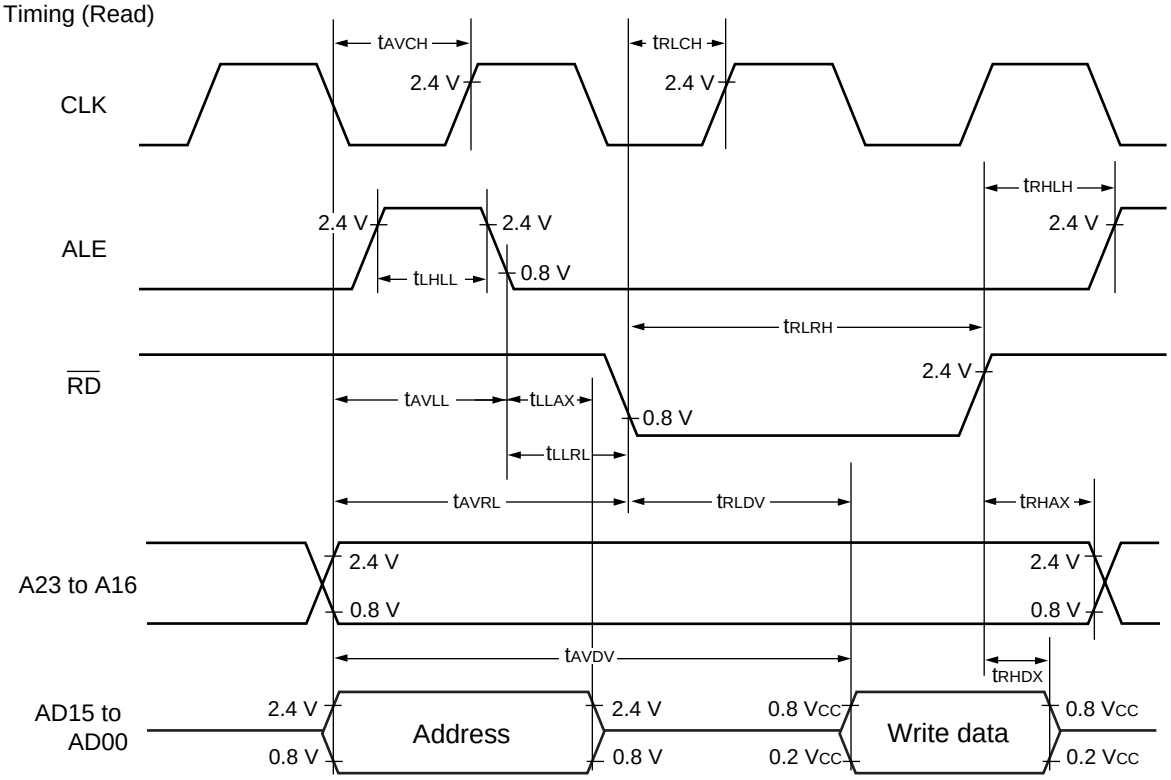


(5) Bus Timing (Read)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$	—	ns	
Effective address → ALE ↓ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE ↓ → address effective time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Effective address → $\overline{RD}$ ↓ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Effective address → valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5\,t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$3\,t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$3\,t_{CP}/2 - 60$	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ → address effective time	t_{RHAX}	ALE, A23 to A16		$t_{CP}/2 - 10$	—	ns	
Effective address → CLK ↑ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	—	ns	
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

• Bus Timing (Read)

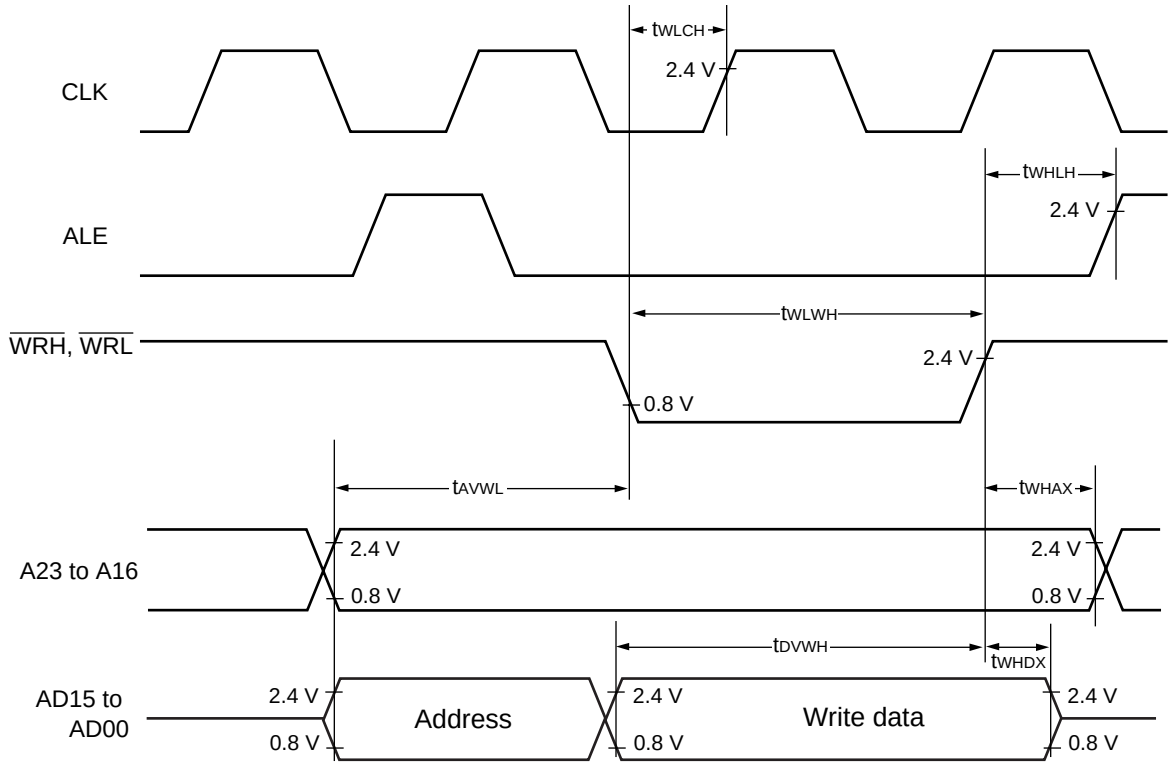


(6) Bus Timing (Write)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Effective address → $\overline{WRH}$, $\overline{WRL}$↓ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WRH}$, $\overline{WRL}$	—	t_{CP} – 15	—	ns	
$\overline{WRH}$, $\overline{WRL}$ pulse width	t_{WLWH}	$\overline{WRH}$, $\overline{WRL}$		3 t_{CP}/2 – 20	—	ns	
Effective data output → $\overline{WRH}$, $\overline{WRL}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WRH}$, $\overline{WRL}$		3 t_{CP}/2 – 20	—	ns	
$\overline{WRH}$, $\overline{WRL}$ ↑ → data hold time	t_{WHDX}	$\overline{WRH}$, $\overline{WRL}$, AD15 to AD00		20	—	ns	
$\overline{WRH}$, $\overline{WRL}$ ↑ → address effective time	t_{WHAX}	$\overline{WRH}$, $\overline{WRL}$, A23 to A16		t_{CP}/2 – 10	—	ns	
$\overline{WRH}$, $\overline{WRL}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WRH}$, $\overline{WRL}$, ALE		t_{CP}/2 – 15	—	ns	
$\overline{WRH}$, $\overline{WRL}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WRH}$, $\overline{WRL}$, CLK		t_{CP}/2 – 20	—	ns	

• Bus Timing (Write)

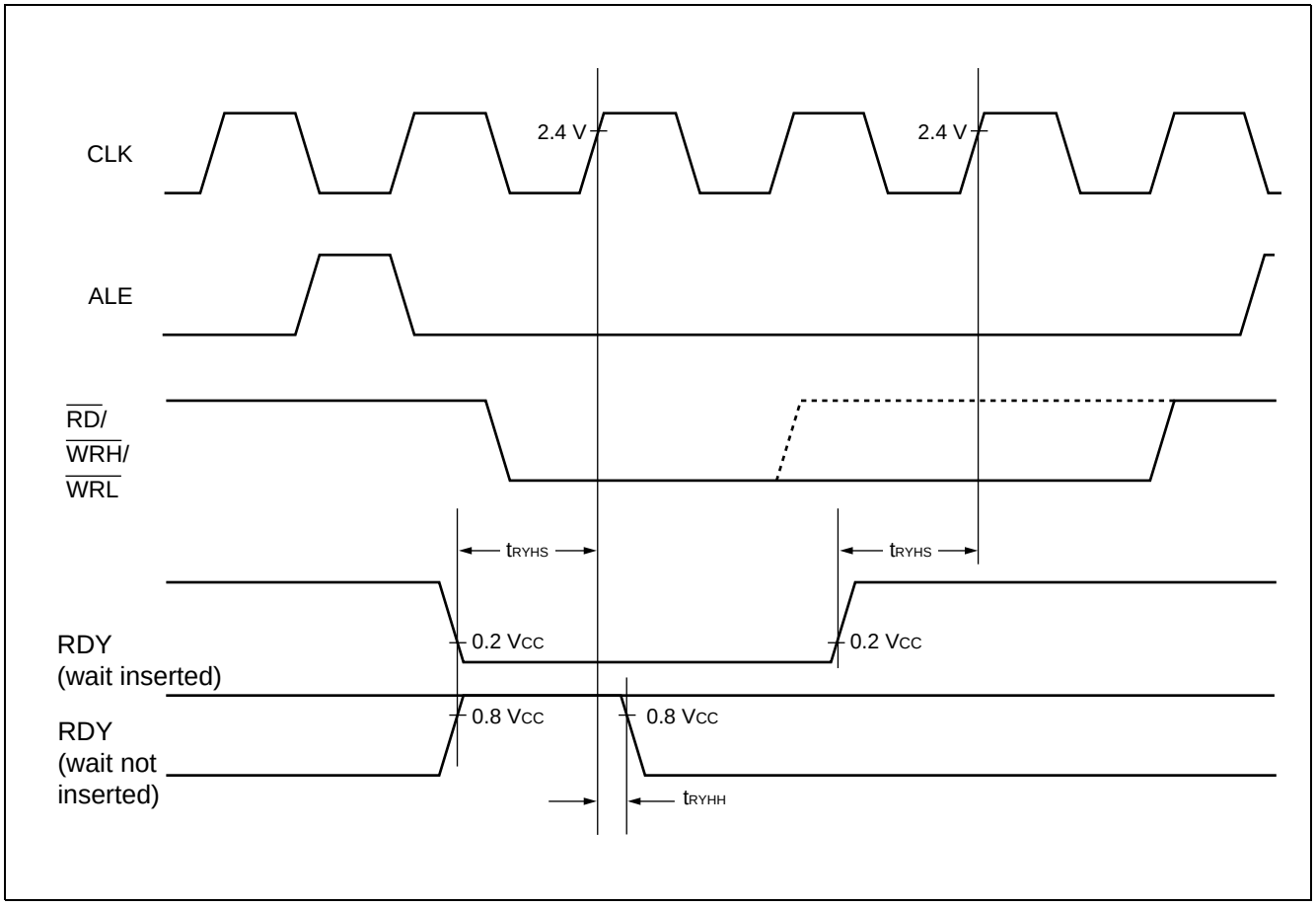


(7) Ready Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}		—	0	—	ns	

Note: Use the automatic ready function when the setup time for the rising edge of the RDY signal is not sufficient.

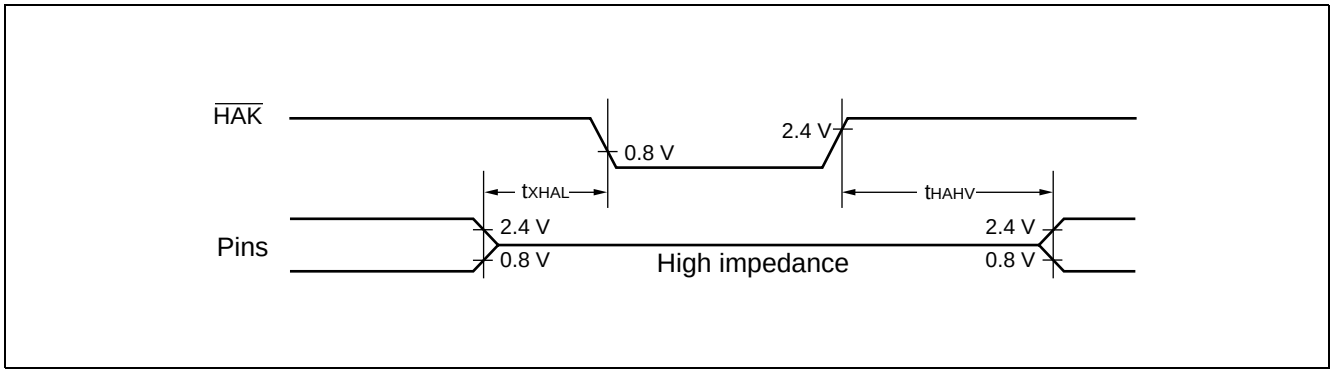


(8) Hold Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Pins in floating status → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↑ → pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Note: More than 1 machine cycle is needed before $\overline{HAK}$ changes after HRQ pin is fetched.



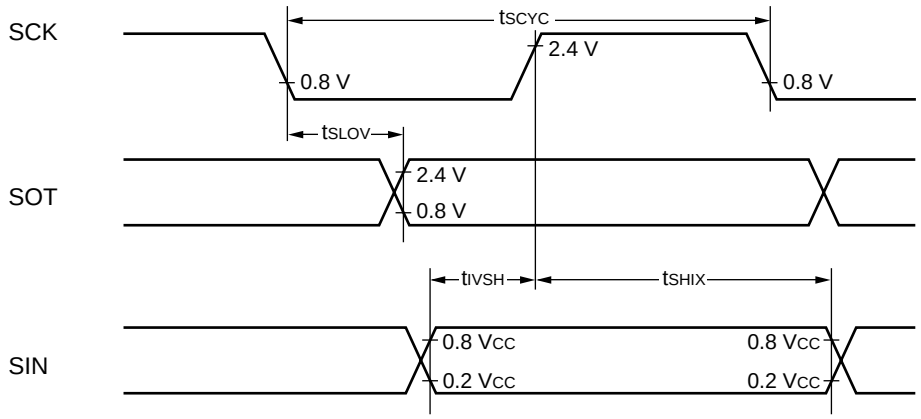
(9) UART0 to UART4

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

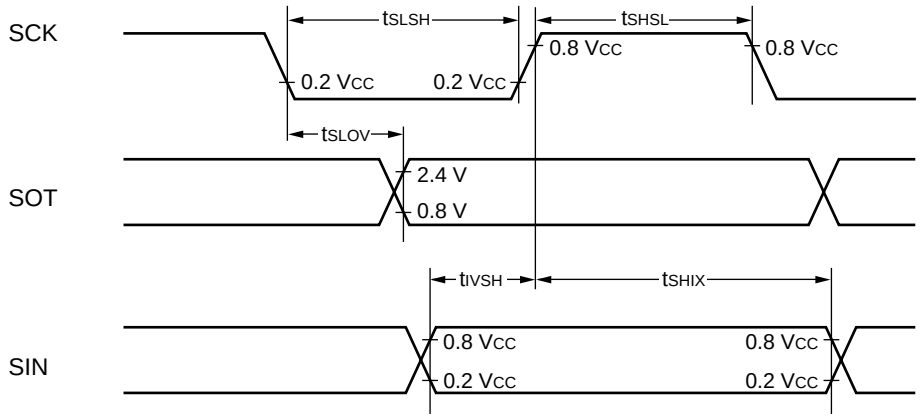
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	C_L = 80 pF + 1 TTL for an output pin of internal shift clock mode	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK4	C_L = 80 pF + 1 TTL for an output pin of external shift clock mode	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK4		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	

Note : • These are AC ratings in the CLK synchronous mode.
• CL is the load capacitance value connected to pins while testing.
• t_{CP} is machine cycle time (unit:ns).

• Internal shift clock mode



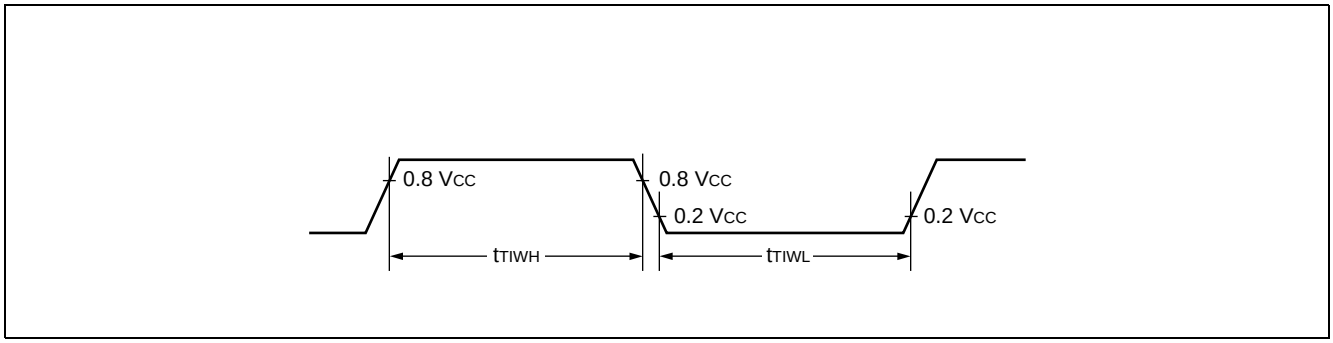
• External shift clock mode



(10)Timer Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

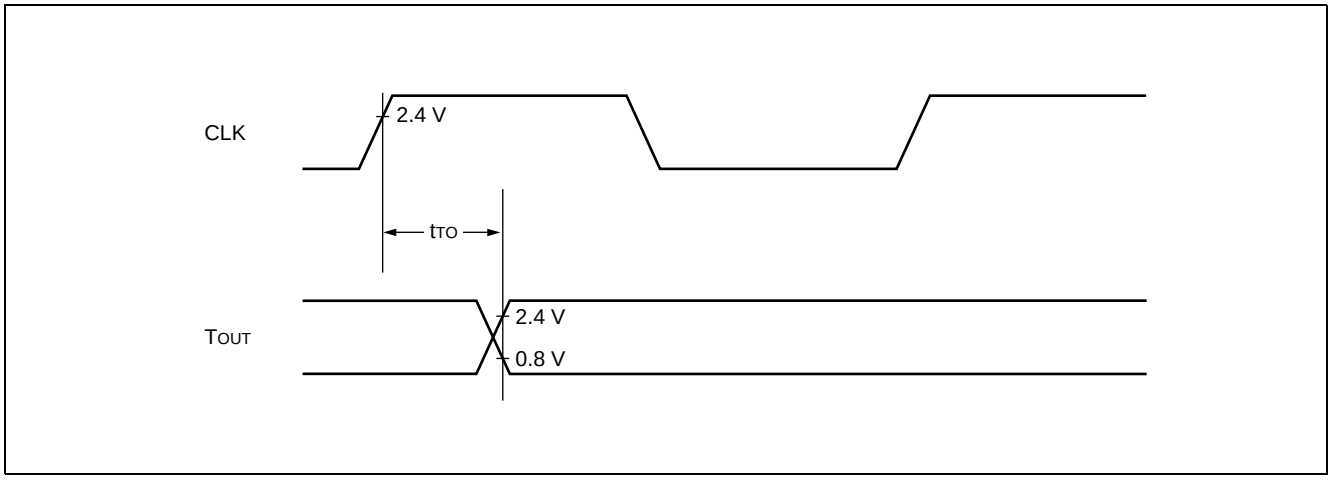
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	IN0 to IN3, TIN0 to TIN2	—	4 t_{CP}	—	ns	



(11) Timer Output Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

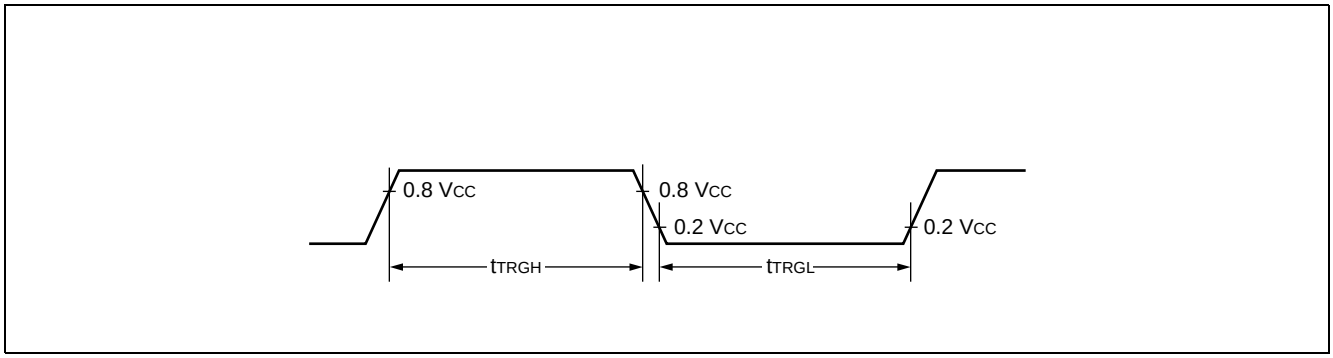
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK↑→T_{OUT} transition time	t_{TO}	OUT0, OUT1, PPG0, PPG1, TOT0 to TOT2	—	30	—	ns	



(12) Trigger Input Timimg

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

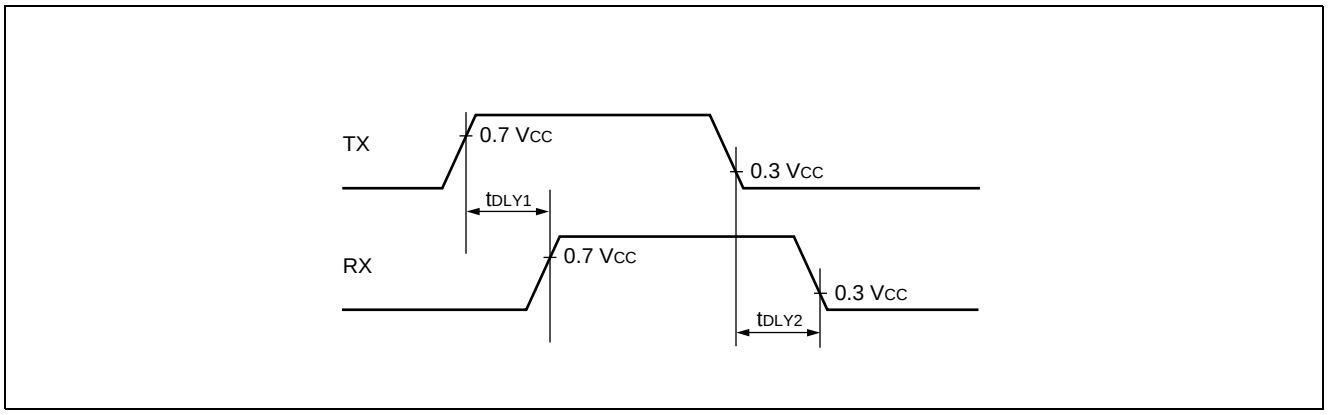
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGH} t_{TRGL}	IRQ0 to IRQ7, ADTG	—	5 t_{CP}	—	ns	

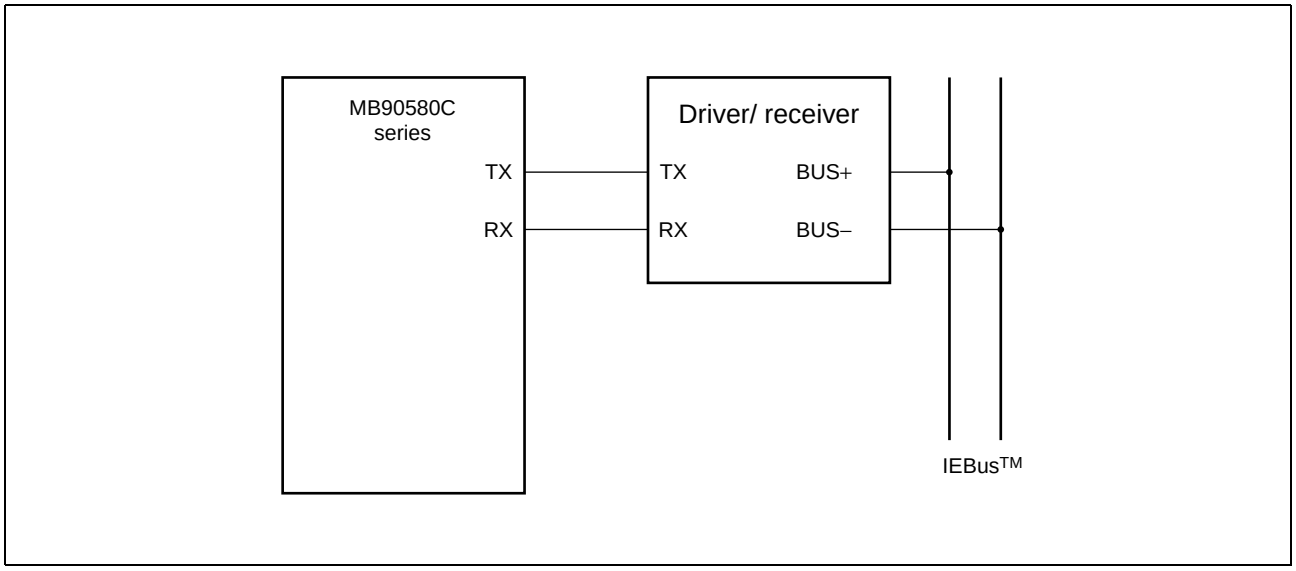


(13) IEBus™ Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
TX → RX delay time (rise)	t_{DLY1}	TX, RX	—	0	1000	ns	
TX → RX delay time (fall)	t_{DLY2}	TX, RX		0	1000	ns	





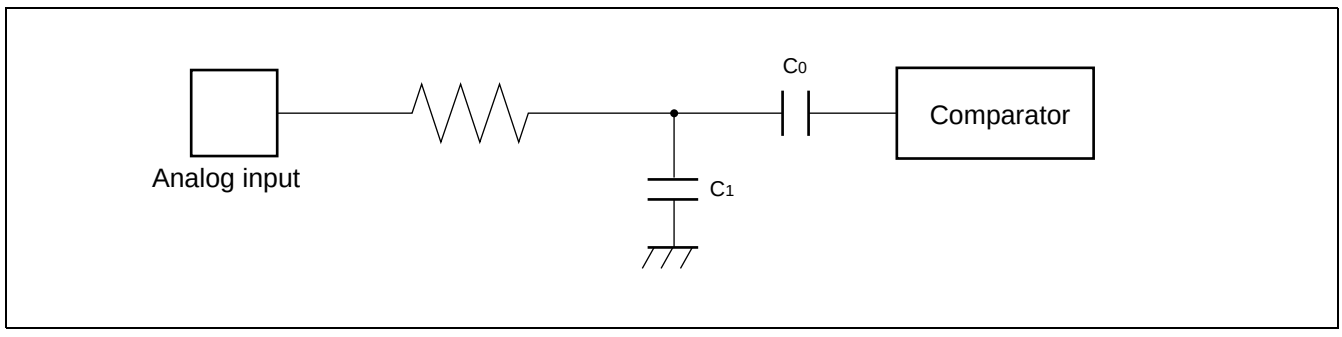
5. A/D Converter Electrical Characteristics

(3.0 V ≤ AVRH – AVRL, V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	—	bit	
Total error	—	—	—	—	±5.0	LSB	
Non-linear error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 3.5	+0.5	AV_{SS} + 4.5	mV	
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 6.5	AVRH – 1.5	AVRH + 1.5	mV	
Conversion time	—	—	—	176 t_{CP}	—	ns	
Sampling period	—	—	—	64 t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH – 2.7	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	400	—	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between channels	—	AN0 to AN7	—	—	4	LSB	

* : The current when the A/D converter is not operating or the CPU is in stop mode (for V_{CC} = AV_{CC} = AVRH = 5.0 V)

Note: • The error increases proportionally as |AVRH - AVRL| decreases.
- The output impedance of the external circuits connected to the analog inputs should be in the following range.
- The output impedance of the external circuit : 15.5 kΩ (Max.) (Sampling time = 4.0 µs)
- If the output impedance of the external circuit is too high, the sampling time might be insufficient.



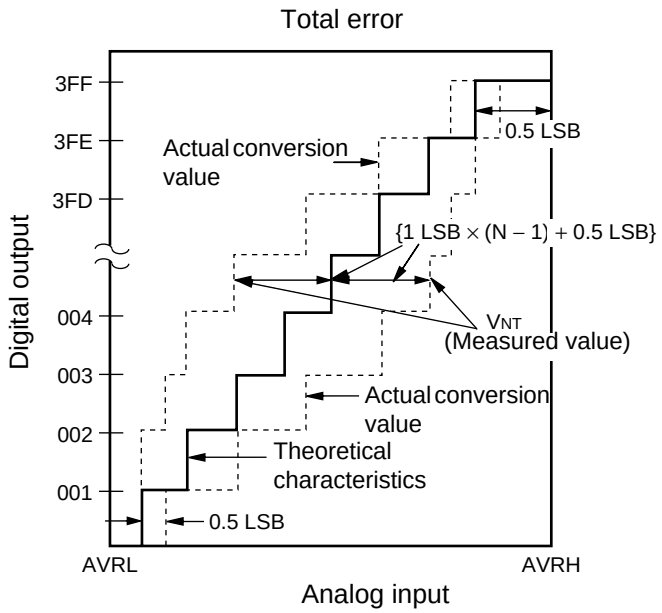
6. A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Theoretical value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

V_{OT}(Theoretical value) = AVRL + 0.5 LSB [V]

V_{FST}(Theoretical value) = AVRH – 1.5 LSB [V]

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

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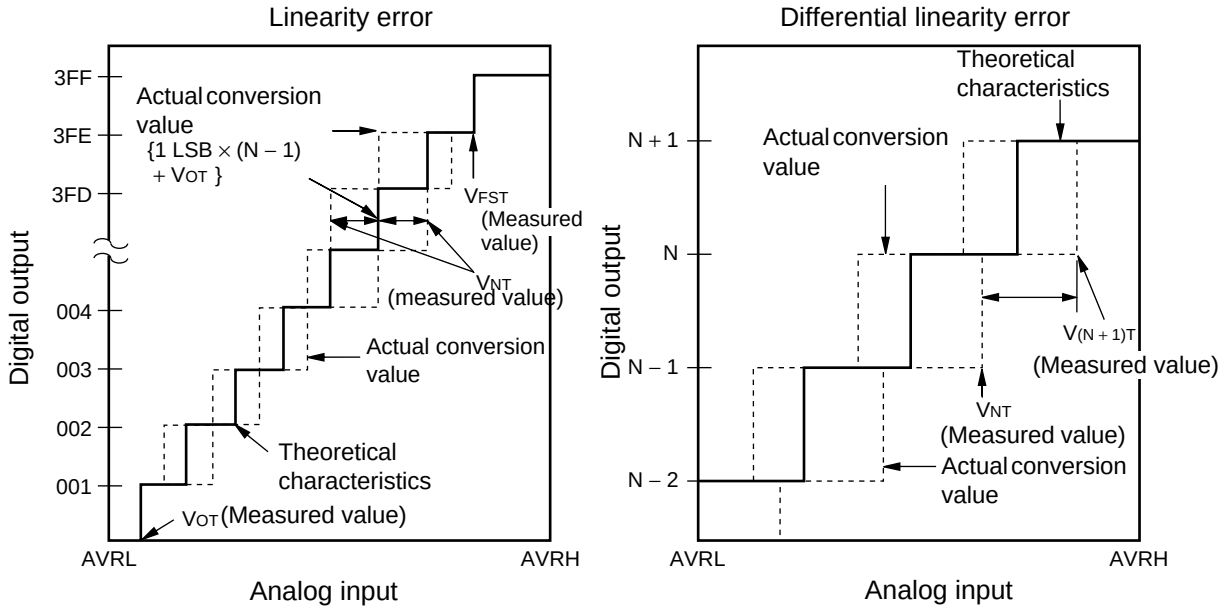


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}[\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from “000_H” to “001_H”
V_{FST} : Voltage at transition of digital output from “$3FE_H$” to “$3FF_H$”

7. Notes on Using A/D Converter

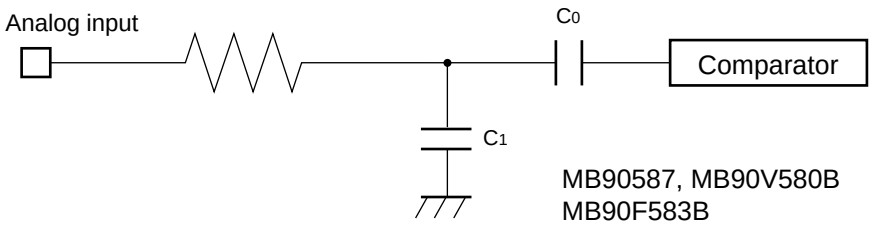
Select the output impedance value for the external circuit of analog input according to the following conditions.

Output impedance values of the external circuit of 7 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 µs @machine clock of 16 MHz)

• Equipment of analog input circuit model



MB90587, MB90V580B	R ≅ 1.5 kΩ, C ≅ 30 pF
MB90F583B	R ≅ 3.0 kΩ, C ≅ 65 pF
MB90583B	R ≅ 2.2 kΩ, C ≅ 45 pF

Note: Listed values must be considered as standards.

• Error

The smaller the | AVRH - AVRL |, the greater the error would become relatively.

8. D/A Converter Electrical Characteristics

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	8	—	bit	
Differential linearity error	—	—	—	—	±0.9	LSB	
Absolute accuracy	—	—	—	—	±1.2	%	
Linearity error	—	—	—	—	±1.5	LSB	
Conversion time	—	—	—	10	20	µs	*1
Analog reference voltage	—	DVRH	V_{SS} + 3.0	—	AV_{CC}	V	
Reference voltage supply current	I_{DVR}	DVRH	—	120	300	µA	
	I_{DVRS}		—	—	10	µA	*2
Analog output impedance	—	—	—	20	—	kΩ	

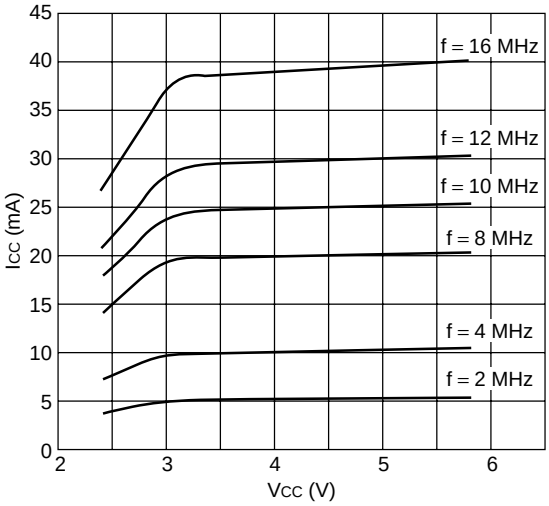
*1 : Load capacitance: 20 pF

*2 : In sleep mode

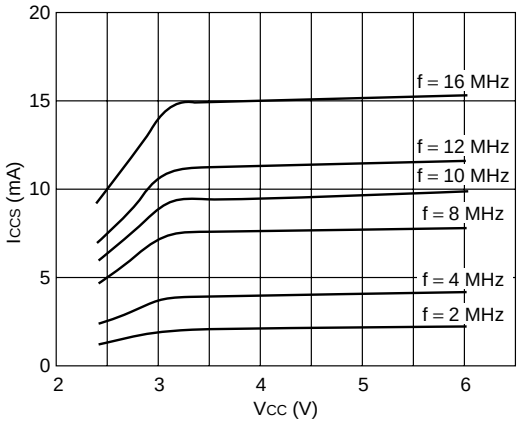
■ EXAMPLE CHARACTERISTICS

• Power Suppy Current of MB90F583C/CA

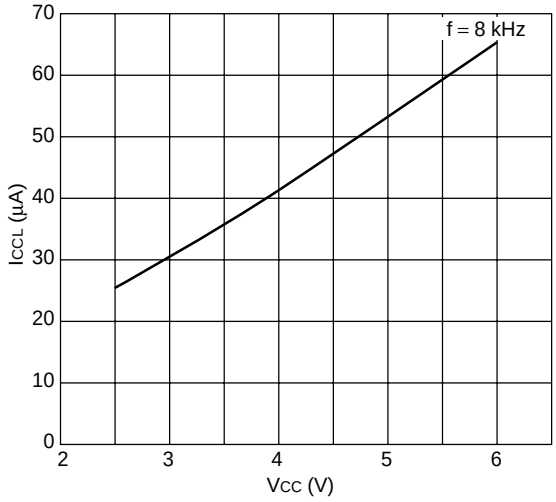
I_{CC} vs. V_{CC}
T_A = 25 °C, external clock input



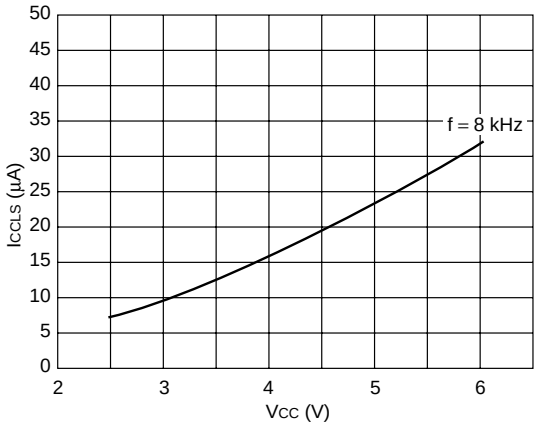
I_{CCS} vs. V_{CC}
T_A = 25 °C, external clock input



I_{CCL} vs. V_{CC}
T_A = 25 °C, external clock input
(MB90F583C only)



I_{CCLS} vs. V_{CC}
T_A = 25 °C, external clock input
(MB90F583C only)



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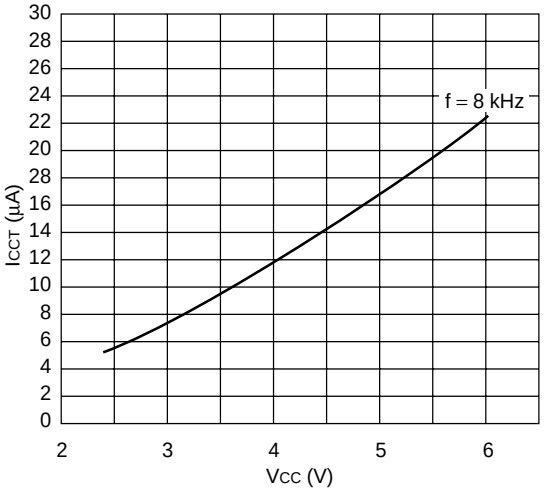
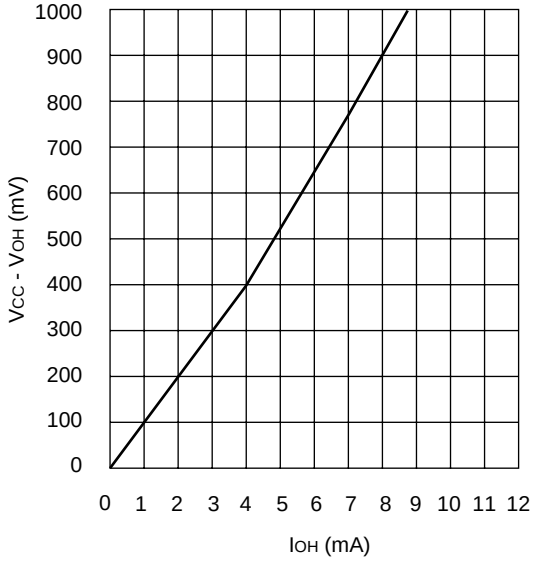
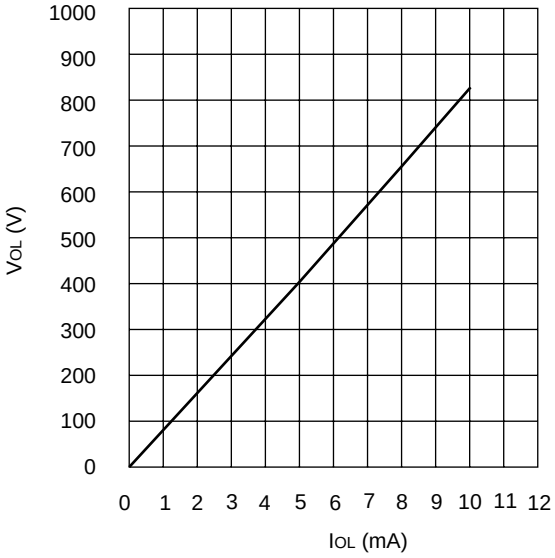
I_{CCT} vs. V_{CC}
T_A = 25 °C, external clock input
(MB90F583C only)



V_{OH} vs. I_{OH}
T_A = 25 °C, V_{CC} = 4.5 V

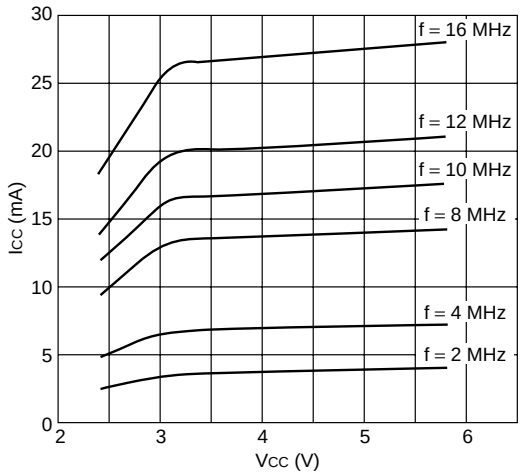


V_{OL} vs. I_{OL}
T_A = 25 °C, V_{CC} = 4.5 V

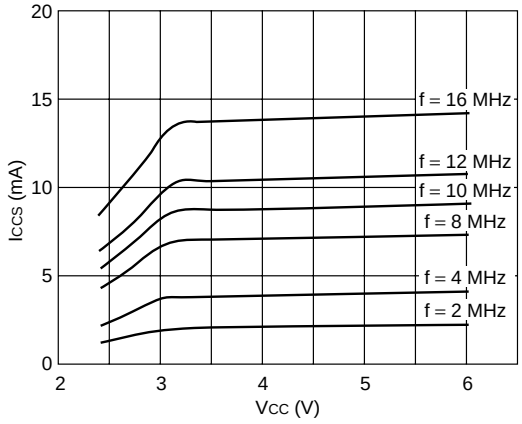


Power Suppy Current of MB90583C/CA

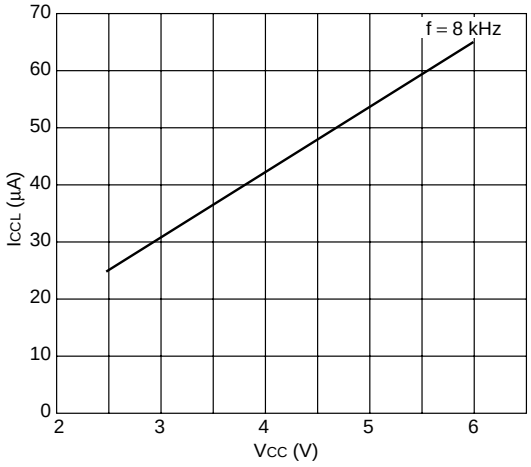
I_{CC} vs. V_{CC}
T_A = 25 °C, external clock input



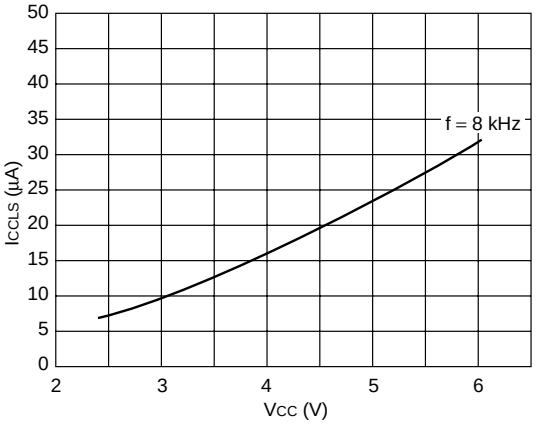
I_{CCS} vs. V_{CC}
T_A = 25 °C, external clock input



I_{CCL} vs. V_{CC}
T_A = 25 °C, external clock input
(MB90583C only)



I_{CCLS} vs. V_{CC}
T_A = 25 °C, external clock input
(MB90583C only)



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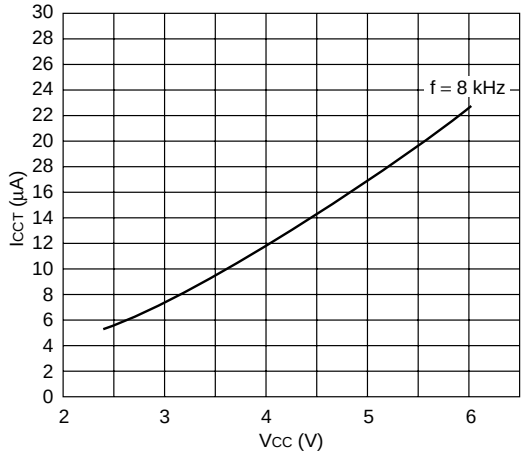
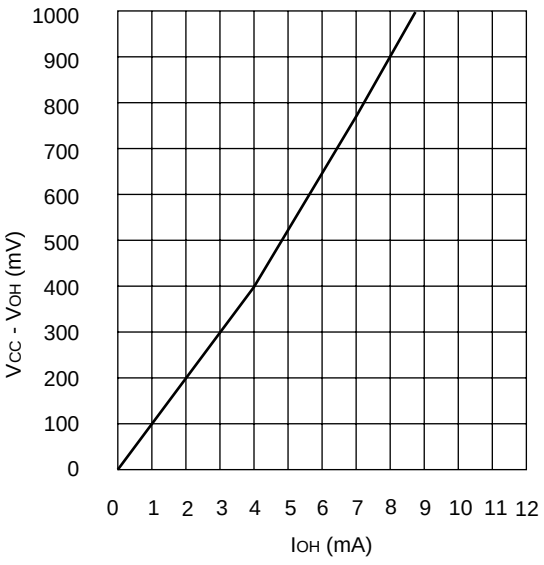
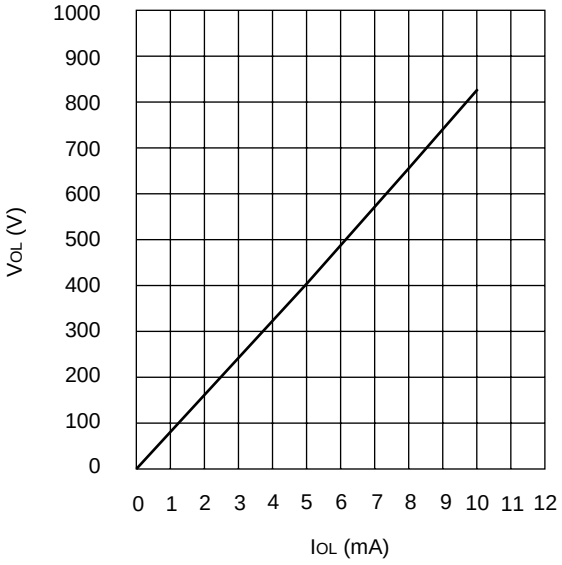
I_{CCT} vs. V_{CC}
T_A = 25 °C, external clock input
(MB90583C only)



V_{OH} vs. I_{OH}
T_A = 25 °C, V_{CC} = 4.5 V



V_{OL} vs. I_{OL}
T_A = 25 °C, V_{CC} = 4.5 V



■ INSTRUCTIONS (351 INSTRUCTIONS)

Table 1 Explanation of Items in Tables of Instructions

Item	Meaning
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler. Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction code.
#	Indicates the number of bytes.
~	Indicates the number of cycles. m : When branching n : When not branching See Table 4 for details about meanings of other letters in items.
RG	Indicates the number of accesses to the register during execution of the instruction. It is used calculate a correction value for intermittent operation of CPU.
B	Indicates the correction value for calculating the number of actual cycles during execution of the instruction. (Table 5) The number of actual cycles during execution of the instruction is the correction value summed with the value in the “~” column.
Operation	Indicates the operation of instruction.
LH	Indicates special operations involving the upper 8 bits of the lower 16 bits of the accumulator. Z : Transfers “0”. X : Extends with a sign before transferring. – : Transfers nothing.
AH	Indicates special operations involving the upper 16 bits in the accumulator. * : Transfers from AL to AH. – : No transfer. Z : Transfers 00_H to AH. X : Transfers 00_H or FF_H to AH by signing and extending AL.
I S T N Z V C	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). * : Changes due to execution of instruction. – : No change. S : Set by execution of instruction. R : Reset by execution of instruction.
RMW	Indicates whether the instruction is a read-modify-write instruction. (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.) * : Instruction is a read-modify-write instruction. – : Instruction is not a read-modify-write instruction. Note: A read-modify-write instruction cannot be used on addresses that have different meanings depending on whether they are read or written.

- **Number of execution cycles**

  The number of cycles required for instruction execution is acquired by adding the number of cycles for each instruction, a corrective value depending on the condition, and the number of cycles required for program fetch. Whenever the instruction being executed exceeds the two-byte (word) boundary, a program on an internal ROM connected to a 16-bit bus is fetched. If data access is interfered with, therefore, the number of execution cycles is increased.

  For each byte of the instruction being executed, a program on a memory connected to an 8-bit external data bus is fetched. If data access in interfered with, therefore, the number of execution cycles is increased. When a general-purpose register, an internal ROM, an internal RAM, an internal I/O device, or an external bus is accessed during intermittent CPU operation, the CPU clock is suspended by the number of cycles specified by the CG1/0 bit of the low-power consumption mode control register. When determining the number of cycles required for instruction execution during intermittent CPU operation, therefore, add the value of the number of times access is done × the number of cycles suspended as the corrective value to the number of ordinary execution cycles.

Table 2 Explanation of Symbols in Tables of Instructions

Symbol	Meaning
A	32-bit accumulator The bit length varies according to the instruction. Byte : Lower 8 bits of AL Word : 16 bits of AL Long : 32 bits of AL and AH
AH AL	Upper 16 bits of A Lower 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir	Compact direct addressing
addr16 addr24 ad24 0 to 15 ad24 16 to 23	Direct addressing Physical direct addressing Bit 0 to bit 15 of addr24 Bit 16 to bit 23 of addr24
io	I/O area (000000_H to $0000FF_H$)
imm4 imm8 imm16 imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
( )b	Bit address
rel	PC relative addressing
ear eam	Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

Table 3 Effective Address Fields

Code	Notation			Address format	Number of bytes in address extension *
00 01 02 03 04 05 06 07	R0 R1 R2 R3 R4 R5 R6 R7	RW0 RW1 RW2 RW3 RW4 RW5 RW6 RW7	RL0 (RL0) RL1 (RL1) RL2 (RL2) RL3 (RL3)	Register direct “ea” corresponds to byte, word, and long-word types, starting from the left	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3			Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +			Register indirect with post-increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8			Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16			Register indirect with 16-bit displacement	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16			Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

Note : The number of bytes in the address extension is indicated by the “+” symbol in the “#” (number of bytes) column in the tables of instructions.

Table 4 Number of Execution Cycles for Each Type of Addressing

Code	Operand	(a) Number of execution cycles for each type of addressing	Number of register accesses for each type of addressing
00 to 07	Ri RWi RLi	Listed in tables of instructions	Listed in tables of instructions
08 to 0B	@RWj	2	1
0C to 0F	@RWj +	4	2
10 to 17	@RWi + disp8	2	1
18 to 1B	@RWj + disp16	2	1
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	4 4 2 1	2 2 0 0

Note : “(a)” is used in the “~” (number of states) column and column B (correction value) in the tables of instructions.

Table 5 Compensation Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b) byte		(c) word		(d) long	
	Cycles	Access	Cycles	Access	Cycles	Access
Internal register	+0	1	+0	1	+0	2
Internal memory even address Internal memory odd address	+0 +0	1 1	+0 +2	1 2	+0 +4	2 4
Even address on external data bus (16 bits) Odd address on external data bus (16 bits)	+1 +1	1 1	+1 +4	1 2	+2 +8	2 4
External data bus (8 bits)	+1	1	+4	2	+8	4

Notes: • “(b)”, “(c)”, and “(d)” are used in the “~” (number of states) column and column B (correction value) in the tables of instructions.
• When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

Table 6 Correction Values for Number of Cycles Used to Calculate Number of Program Fetch Cycles

Instruction	Byte boundary	Word boundary
Internal memory	—	+2
External data bus (16 bits)	—	+3
External data bus (8 bits)	+3	—

Notes: • When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.
• Because instruction execution is not slowed down by all program fetches in actuality, these correction values should be used for “worst case” calculations.

Table 7 Transfer Instructions (Byte) [41 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOV	A, dir	2	3	0	(b)	byte (A) ← (dir)	Z	*	–	–	–	*	*	–	–	–
MOV	A, addr16	3	4	0	(b)	byte (A) ← (addr16)	Z	*	–	–	–	*	*	–	–	–
MOV	A, Ri	1	2	1	0	byte (A) ← (Ri)	Z	*	–	–	–	*	*	–	–	–
MOV	A, ear	2	2	1	0	byte (A) ← (ear)	Z	*	–	–	–	*	*	–	–	–
MOV	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	Z	*	–	–	–	*	*	–	–	–
MOV	A, io	2	3	0	(b)	byte (A) ← (io)	Z	*	–	–	–	*	*	–	–	–
MOV	A, #imm8	2	2	0	0	byte (A) ← imm8	Z	*	–	–	–	*	*	–	–	–
MOV	A, @A	2	3	0	(b)	byte (A) ← ((A))	Z	–	–	–	–	*	*	–	–	–
MOV	A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	Z	*	–	–	–	*	*	–	–	–
MOVN	A, #imm4	1	1	0	0	byte (A) ← imm4	Z	*	–	–	–	R	*	–	–	–
MOVX	A, dir	2	3	0	(b)	byte (A) ← (dir)	X	*	–	–	–	*	*	–	–	–
MOVX	A, addr16	3	4	0	(b)	byte (A) ← (addr16)	X	*	–	–	–	*	*	–	–	–
MOVX	A, Ri	2	2	1	0	byte (A) ← (Ri)	X	*	–	–	–	*	*	–	–	–
MOVX	A, ear	2	2	1	0	byte (A) ← (ear)	X	*	–	–	–	*	*	–	–	–
MOVX	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	X	*	–	–	–	*	*	–	–	–
MOVX	A, io	2	3	0	(b)	byte (A) ← (io)	X	*	–	–	–	*	*	–	–	–
MOVX	A, #imm8	2	2	0	0	byte (A) ← imm8	X	*	–	–	–	*	*	–	–	–
MOVX	A, @A	2	3	0	(b)	byte (A) ← ((A))	X	–	–	–	–	*	*	–	–	–
MOVX	A,@RWi+disp8	2	5	1	(b)	byte (A) ← ((RWi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOVX	A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOV	dir, A	2	3	0	(b)	byte (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	addr16, A	3	4	0	(b)	byte (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, A	1	2	1	0	byte (Ri) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	ear, A	2	2	1	0	byte (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	eam, A	2+	3+ (a)	0	(b)	byte (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	io, A	2	3	0	(b)	byte (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	@RLi+disp8, A	3	10	2	(b)	byte ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, ear	2	3	2	0	byte (Ri) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, eam	2+	4+ (a)	1	(b)	byte (Ri) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOV	ear, Ri	2	4	2	0	byte (ear) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV	eam, Ri	2+	5+ (a)	1	(b)	byte (eam) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, #imm8	2	2	1	0	byte (Ri) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV	io, #imm8	3	5	0	(b)	byte (io) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	dir, #imm8	3	5	0	(b)	byte (dir) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	ear, #imm8	3	2	1	0	byte (ear) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV	eam, #imm8	3+	4+ (a)	0	(b)	byte (eam) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	@AL, AH															
/MOV	@A, T	2	3	0	(b)	byte ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCH	A, ear	2	4	2	0	byte (A) ↔ (ear)	Z	–	–	–	–	–	–	–	–	–
XCH	A, eam	2+	5+ (a)	0	2× (b)	byte (A) ↔ (eam)	Z	–	–	–	–	–	–	–	–	–
XCH	Ri, ear	2	7	4	0	byte (Ri) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCH	Ri, eam	2+	9+ (a)	2	2× (b)	byte (Ri) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 8 Transfer Instructions (Word/Long Word) [38 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	3	0	(c)	word (A) ← (dir)	–	*	–	–	–	*	*	–	–	–
MOVW A, addr16	3	4	0	(c)	word (A) ← (addr16)	–	*	–	–	–	*	*	–	–	–
MOVW A, SP	1	1	0	0	word (A) ← (SP)	–	*	–	–	–	*	*	–	–	–
MOVW A, RWi	1	2	1	0	word (A) ← (RWi)	–	*	–	–	–	*	*	–	–	–
MOVW A, ear	2	2	1	0	word (A) ← (ear)	–	*	–	–	–	*	*	–	–	–
MOVW A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	*	–	–	–	*	*	–	–	–
MOVW A, io	2	3	0	(c)	word (A) ← (io)	–	*	–	–	–	*	*	–	–	–
MOVW A, @A	2	3	0	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW A, #imm16	3	2	0	0	word (A) ← imm16	–	*	–	–	–	*	*	–	–	–
MOVW A, @RWi+disp8	2	5	1	(c)	word (A) ← ((RWi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @RLi+disp8	3	10	2	(c)	word (A) ← ((RLi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW dir, A	2	3	0	(c)	word (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW addr16, A	3	4	0	(c)	word (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW SP, A	1	1	0	0	word (SP) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, A	1	2	1	0	word (RWi) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW ear, A	2	2	1	0	word (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW eam, A	2+	3+ (a)	0	(c)	word (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW io, A	2	3	0	(c)	word (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RWi+disp8, A	2	5	1	(c)	word ((RWi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RLi+disp8, A	3	10	2	(c)	word ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, ear	2	3	2	(0)	word (RWi) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, eam	2+	4+ (a)	1	(c)	word (RWi) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVW ear, RWi	2	4	2	0	word (ear) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW eam, RWi	2+	5+ (a)	1	(c)	word (eam) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, #imm16	3	2	1	0	word (RWi) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW io, #imm16	4	5	0	(c)	word (io) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW ear, #imm16	4	2	1	0	word (ear) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW eam, #imm16	4+	4+ (a)	0	(c)	word (eam) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW @AL, AH /MOVW@A, T	2	3	0	(c)	word ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCHW A, ear	2	4	2	0	word (A) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW A, eam	2+	5+ (a)	0	2× (c)	word (A) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, ear	2	7	4	0	word (RWi) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, eam	2+	9+ (a)	2	2× (c)	word (RWi) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
MOVL A, ear	2	4	2	0	long (A) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVL A, eam	2+	5+ (a)	0	(d)	long (A) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVL A, #imm32	5	3	0	0	long (A) ← imm32	–	–	–	–	–	*	*	–	–	–
MOVL ear, A	2	4	2	0	long (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL eam, A	2+	5+ (a)	0	(d)	long (eam) ← (A)	–	–	–	–	–	*	*	–	–	–

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD	A,#imm8	2	2	0	0	byte (A) ← (A) +imm8	Z	–	–	–	–	*	*	*	*	–
ADD	A, dir	2	5	0	(b)	byte (A) ← (A) +(dir)	Z	–	–	–	–	*	*	*	*	–
ADD	A, ear	2	3	1	0	byte (A) ← (A) +(ear)	Z	–	–	–	–	*	*	*	*	–
ADD	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) +(eam)	Z	–	–	–	–	*	*	*	*	–
ADD	ear, A	2	3	2	0	byte (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADD	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) + (A)	Z	–	–	–	–	*	*	*	*	*
ADDC	A	1	2	0	0	byte (A) ← (AH) + (AL) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC	A, ear	2	3	1	0	byte (A) ← (A) + (ear) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) + (eam) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDDC	A	1	3	0	0	byte (A) ← (AH) + (AL) + (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
SUB	A, #imm8	2	2	0	0	byte (A) ← (A) –imm8	Z	–	–	–	–	*	*	*	*	–
SUB	A, dir	2	5	0	(b)	byte (A) ← (A) – (dir)	Z	–	–	–	–	*	*	*	*	–
SUB	A, ear	2	3	1	0	byte (A) ← (A) – (ear)	Z	–	–	–	–	*	*	*	*	–
SUB	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam)	Z	–	–	–	–	*	*	*	*	–
SUB	ear, A	2	3	2	0	byte (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUB	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBC	A	1	2	0	0	byte (A) ← (AH) – (AL) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC	A, ear	2	3	1	0	byte (A) ← (A) – (ear) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBDC	A	1	3	0	0	byte (A) ← (AH) – (AL) – (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
ADDW	A	1	2	0	0	word (A) ← (AH) + (AL)	–	–	–	–	–	*	*	*	*	–
ADDW	A, ear	2	3	1	0	word (A) ← (A) +(ear)	–	–	–	–	–	*	*	*	*	–
ADDW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) +(eam)	–	–	–	–	–	*	*	*	*	–
ADDW	A, #imm16	3	2	0	0	word (A) ← (A) +imm16	–	–	–	–	–	*	*	*	*	–
ADDW	ear, A	2	3	2	0	word (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADDW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) + (A)	–	–	–	–	–	*	*	*	*	*
ADDCW	A, ear	2	3	1	0	word (A) ← (A) + (ear) + (C)	–	–	–	–	–	*	*	*	*	–
ADDCW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) + (eam) + (C)	–	–	–	–	–	*	*	*	*	–
SUBW	A	1	2	0	0	word (A) ← (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
SUBW	A, ear	2	3	1	0	word (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBW	A, #imm16	3	2	0	0	word (A) ← (A) –imm16	–	–	–	–	–	*	*	*	*	–
SUBW	ear, A	2	3	2	0	word (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUBW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBCW	A, ear	2	3	1	0	word (A) ← (A) – (ear) – (C)	–	–	–	–	–	*	*	*	*	–
SUBCW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam) – (C)	–	–	–	–	–	*	*	*	*	–
ADDL	A, ear	2	6	2	0	long (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDL	A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDL	A, #imm32	5	4	0	0	long (A) ← (A) +imm32	–	–	–	–	–	*	*	*	*	–
SUBL	A, ear	2	6	2	0	long (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBL	A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBL	A, #imm32	5	4	0	0	long (A) ← (A) –imm32	–	–	–	–	–	*	*	*	*	–

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC	ear	2	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC	ear	2	3	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DEC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW	ear	2	3	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW	ear	2	3	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL	ear	2	7	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL	ear	2	7	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP	A	1	1	0	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP	A, ear	2	2	1	0	byte (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMP	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMP	A, #imm8	2	2	0	0	byte (A) ← imm8	–	–	–	–	–	*	*	*	*	–
CMPW	A	1	1	0	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW	A, ear	2	2	1	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPW	A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPW	A, #imm16	3	2	0	0	word (A) ← imm16	–	–	–	–	–	*	*	*	*	–
CMPL	A, ear	2	6	2	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPL	A, eam	2+	7+ (a)	0	(d)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPL	A, #imm32	5	3	0	0	word (A) ← imm32	–	–	–	–	–	*	*	*	*	–

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 12 Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIVU	A	1	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	–	–	–	–	–	–	–	*	*	–
DIVU	A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	–	–	–	–	–	–	–	*	*	–
DIVU	A, eam	2+	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU	A	1	*8	0	0	byte (AH) *byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, eam	2+	*10	0	(b)	byte (A) *byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A	1	*11	0	0	word (AH) *word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, eam	2+	*13	0	(c)	word (A) *word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

*1: 3 when the result is zero, 7 when an overflow occurs, and 15 normally.
*2: 4 when the result is zero, 8 when an overflow occurs, and 16 normally.
*3: 6 + (a) when the result is zero, 9 + (a) when an overflow occurs, and 19 + (a) normally.
*4: 4 when the result is zero, 7 when an overflow occurs, and 22 normally.
*5: 6 + (a) when the result is zero, 8 + (a) when an overflow occurs, and 26 + (a) normally.
*6: (b) when the result is zero or when an overflow occurs, and 2 × (b) normally.
*7: (c) when the result is zero or when an overflow occurs, and 2 × (c) normally.
*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not zero.
*9: 4 when byte (ear) is zero, and 8 when byte (ear) is not zero.
*10: 5 + (a) when byte (eam) is zero, and 9 + (a) when byte (eam) is not 0.
*11: 3 when word (AH) is zero, and 11 when word (AH) is not zero.
*12: 4 when word (ear) is zero, and 12 when word (ear) is not zero.
*13: 5 + (a) when word (eam) is zero, and 13 + (a) when word (eam) is not zero.

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 13 Signed Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIV	A	2	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	Z	–	–	–	–	–	–	*	*	–
DIV	A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	Z	–	–	–	–	–	–	*	*	–
DIV	A, eam	2 +	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	Z	–	–	–	–	–	–	*	*	–
DIVW	A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVW	A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU	A	2	*8	0	0	byte (AH) *byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, eam	2 +	*10	0	(b)	byte (A) *byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A	2	*11	0	0	word (AH) *word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, eam	2 +	*13	0	(c)	word (A) *word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

*1: Set to 3 when the division-by-0, 8 or 18 for an overflow, and 18 for normal operation.
*2: Set to 3 when the division-by-0, 10 or 21 for an overflow, and 22 for normal operation.
*3: Set to 4 + (a) when the division-by-0, 11 + (a) or 22 + (a) for an overflow, and 23 + (a) for normal operation.
*4: Positive dividend: Set to 4 when the division-by-0, 10 or 29 for an overflow, and 30 for normal operation.
Negative dividend: Set to 4 when the division-by-0, 11 or 30 for an overflow and 31 for normal operation.
*5: Positive dividend: Set to 4 + (a) when the division-by-0, 11 + (a) or 30 + (a) for an overflow, and 31 + (a) for normal operation.
Negative dividend: Set to 4 + (a) when the division-by-0, 12 + (a) or 31 + (a) for an overflow, and 32 + (a) for normal operation.
*6: When the division-by-0, (b) for an overflow, and 2 × (b) for normal operation.
*7: When the division-by-0, (c) for an overflow, and 2 × (c) for normal operation.
*8: Set to 3 when byte (AH) is zero, 12 when the result is positive, and 13 when the result is negative.
*9: Set to 3 when byte (ear) is zero, 12 when the result is positive, and 13 when the result is negative.
*10: Set to 4 + (a) when byte (eam) is zero, 13 + (a) when the result is positive, and 14 + (a) when the result is negative.
*11: Set to 3 when word (AH) is zero, 12 when the result is positive, and 13 when the result is negative.
*12: Set to 3 when word (ear) is zero, 16 when the result is positive, and 19 when the result is negative.
*13: Set to 4 + (a) when word (eam) is zero, 17 + (a) when the result is positive, and 20 + (a) when the result is negative.

Notes:
- When overflow occurs during DIV or DIVW instruction execution, the number of execution cycles takes two values because of detection before and after an operation.
- When overflow occurs during DIV or DIVW instruction execution, the contents of AL are destroyed.
- For (a) to (d), refer to “Table 4 Number of Execution Cycles for Effective Address in Addressing Modes” and “Table 5 Correction Values for Number of Cycles for Calculating Actual Number of Cycles.”

Table 14 Logical 1 Instructions (Byte/Word) [39 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
AND	A, #imm8	2	2	0	0	byte (A) ← (A) and imm8	–	–	–	–	–	*	*	R	–	–
AND	A, ear	2	3	1	0	byte (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
AND	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
AND	ear, A	2	3	2	0	byte (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
AND	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
OR	A, #imm8	2	2	0	0	byte (A) ← (A) or imm8	–	–	–	–	–	*	*	R	–	–
OR	A, ear	2	3	1	0	byte (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
OR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
OR	ear, A	2	3	2	0	byte (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
OR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XOR	A, #imm8	2	2	0	0	byte (A) ← (A) xor imm8	–	–	–	–	–	*	*	R	–	–
XOR	A, ear	2	3	1	0	byte (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XOR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XOR	ear, A	2	3	2	0	byte (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XOR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOT	A	1	2	0	0	byte (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOT	ear	2	3	2	0	byte (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOT	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*
ANDW	A	1	2	0	0	word (A) ← (AH) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	A, #imm16	3	2	0	0	word (A) ← (A) and imm16	–	–	–	–	–	*	*	R	–	–
ANDW	A, ear	2	3	1	0	word (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ANDW	ear, A	2	3	2	0	word (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
ORW	A	1	2	0	0	word (A) ← (AH) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	A, #imm16	3	2	0	0	word (A) ← (A) or imm16	–	–	–	–	–	*	*	R	–	–
ORW	A, ear	2	3	1	0	word (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
ORW	ear, A	2	3	2	0	word (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XORW	A	1	2	0	0	word (A) ← (AH) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	A, #imm16	3	2	0	0	word (A) ← (A) xor imm16	–	–	–	–	–	*	*	R	–	–
XORW	A, ear	2	3	1	0	word (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XORW	ear, A	2	3	2	0	word (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOTW	A	1	2	0	0	word (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOTW	ear	2	3	2	0	word (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOTW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 15 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	6	2	0	long (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ORL A, ear	2	6	2	0	long (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
XORL A, ea	2	6	2	0	long (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 16 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	0	byte (A) ← 0 – (A)	X	–	–	–	–	*	*	*	*	–
NEG ear	2	3	2	0	byte (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEG eam	2+	5+ (a)	0	2× (b)	byte (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*
NEGW A	1	2	0	0	word (A) ← 0 – (A)	–	–	–	–	–	*	*	*	*	–
NEGW ear	2	3	2	0	word (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEGW eam	2+	5+ (a)	0	2× (c)	word (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 17 Normalize Instruction (Long Word) [1 Instruction]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*1	1	0	long (A) ← Shift until first digit is “1” byte (R0) ← Current shift count	–	–	–	–	–	–	*	–	–	–

*1: 4 when the contents of the accumulator are all zeroes, 6 + (R0) in all other cases (shift count).

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 18 Shift Instructions (Byte/Word/Long Word) [18 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
RORC A	2	2	0	0	byte (A) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC A	2	2	0	0	byte (A) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC ear	2	3	2	0	byte (ear) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	*
ROLC ear	2	3	2	0	byte (ear) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	*
ASR A, R0	2	*1	1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSR A, R0	2	*1	1	0	byte (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSL A, R0	2	*1	1	0	byte (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRW A	1	2	0	0	word (A) ← Arithmetic right shift (A, 1 bit)	–	–	–	–	*	*	*	–	*	–
LSRW A/SHRW A	1	2	0	0	word (A) ← Logical right shift (A, 1 bit)	–	–	–	–	*	R	*	–	*	–
LSLW A/SHLW A	1	2	0	0	word (A) ← Logical left shift (A, 1 bit)	–	–	–	–	–	*	*	–	*	–
ASRW A, R0	2	*1	1	0	word (A) ← Arithmetic right barrel shift (A,	–	–	–	–	*	*	*	–	*	–
LSRW A, R0	2	*1	1	0	R0)	–	–	–	–	*	*	*	–	*	–
LSLW A, R0	2	*1	1	0	word (A) ← Logical right barrel shift (A, R0) word (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRL A, R0	2	*2	1	0	long (A) ← Arithmetic right shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRL A, R0	2	*2	1	0	long (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLL A, R0	2	*2	1	0	long (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–

*1: 6 when R0 is 0, 5 + (R0) in all other cases.
*2: 6 when R0 is 0, 6 + (R0) in all other cases.

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 19 Branch 1 Instructions [31 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
BZ/BEQ rel	2	*1	0	0	Branch when (Z) = 1	–	–	–	–	–	–	–	–	–	–
BNZ/BNE rel	2	*1	0	0	Branch when (Z) = 0	–	–	–	–	–	–	–	–	–	–
BC/BLO rel	2	*1	0	0	Branch when (C) = 1	–	–	–	–	–	–	–	–	–	–
BNC/BHS rel	2	*1	0	0	Branch when (C) = 0	–	–	–	–	–	–	–	–	–	–
BN rel	2	*1	0	0	Branch when (N) = 1	–	–	–	–	–	–	–	–	–	–
BP rel	2	*1	0	0	Branch when (N) = 0	–	–	–	–	–	–	–	–	–	–
BV rel	2	*1	0	0	Branch when (V) = 1	–	–	–	–	–	–	–	–	–	–
BNV rel	2	*1	0	0	Branch when (V) = 0	–	–	–	–	–	–	–	–	–	–
BT rel	2	*1	0	0	Branch when (T) = 1	–	–	–	–	–	–	–	–	–	–
BNT rel	2	*1	0	0	Branch when (T) = 0	–	–	–	–	–	–	–	–	–	–
BLT rel	2	*1	0	0	Branch when (V) xor (N) = 1	–	–	–	–	–	–	–	–	–	–
BGE rel	2	*1	0	0	Branch when (V) xor (N) = 0	–	–	–	–	–	–	–	–	–	–
BLE rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BGT rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BLS rel	2	*1	0	0	Branch when (C) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BHI rel	2	*1	0	0	Branch when (C) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BRA rel	2	*1	0	0	Branch unconditionally	–	–	–	–	–	–	–	–	–	–
JMP @A	1	2	0	0	word (PC) ← (A)	–	–	–	–	–	–	–	–	–	–
JMP addr16	3	3	0	0	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
JMP @ear	2	3	1	0	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
JMP @eam	2+	4+ (a)	0	(c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
JMPP @ear *3	2	5	2	0	word (PC) ← (ear), (PCB) ← (ear +2)	–	–	–	–	–	–	–	–	–	–
JMPP @eam *3	2+	6+ (a)	0	(d)	word (PC) ← (eam), (PCB) ← (eam +2)	–	–	–	–	–	–	–	–	–	–
JMPP addr24	4	4	0	0	word (PC) ← ad24 0 to 15, (PCB) ← ad24 16 to 23	–	–	–	–	–	–	–	–	–	–
CALL @ear *4	2	6	1	(c)	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
CALL @eam *4	2+	7+ (a)	0	2× (c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
CALL addr16 *5	3	6	0	(c)	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
CALLV #vct4 *5	1	7	0	2× (c)	Vector call instruction	–	–	–	–	–	–	–	–	–	–
CALLP @ear *6	2	10	2	2× (c)	word (PC) ← (ear) 0 to 15, (PCB) ← (ear) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP @eam *6	2+	11+ (a)	0	*2	word (PC) ← (eam) 0 to 15, (PCB) ← (eam) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP addr24 *7	4	10	0	2× (c)	word (PC) ← addr0 to 15, (PCB) ← addr16 to 23	–	–	–	–	–	–	–	–	–	–

*1: 4 when branching, 3 when not branching.
*2: (b) + 3 × (c)
*3: Read (word) branch address.
*4: W: Save (word) to stack; R: read (word) branch address.
*5: Save (word) to stack.
*6: W: Save (long word) to W stack; R: read (long word) R branch address.
*7: Save (long word) to stack.

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 20 Branch 2 Instructions [19 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CBNE A, #imm8, rel	3	*1	0	0	Branch when byte (A) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE A, #imm16, rel	4	*1	0	0	Branch when word (A) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CBNE ear, #imm8, rel	4	*2	1	0	Branch when byte (ear) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CBNE eam, #imm8, rel*10	4+	*3	0	(b)	Branch when byte (eam) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE ear, #imm16, rel	5	*4	1	0	Branch when word (ear) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CWBNE eam, #imm16, rel*10	5+	*3	0	(c)	Branch when word (eam) ≠ imm16	–	–	–	–	–	*	*	*	*	–
DBNZ ear, rel	3	*5	2	0	Branch when byte (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DBNZ eam, rel	3+	*6	2	2× (b)	Branch when byte (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
DWBNZ ear, rel	3	*5	2	0	Branch when word (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DWBNZ eam, rel	3+	*6	2	2× (c)	Branch when word (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
INT #vct8	2	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT addr16	3	16	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INTP addr24	4	17	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT9	1	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
RETI	1	15	0	*7	Return from interrupt	–	–	*	*	*	*	*	*	*	–
LINK #imm8	2	6	0	(c)	At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area	–	–	–	–	–	–	–	–	–	–
UNLINK	1	5	0	(c)	At constant entry, retrieve old frame pointer from stack.	–	–	–	–	–	–	–	–	–	–
RET *8	1	4	0	(c)	Return from subroutine	–	–	–	–	–	–	–	–	–	–
RETP *9	1	6	0	(d)	Return from subroutine	–	–	–	–	–	–	–	–	–	–

*1: 5 when branching, 4 when not branching
*2: 13 when branching, 12 when not branching
*3: 7 + (a) when branching, 6 + (a) when not branching
*4: 8 when branching, 7 when not branching
*5: 7 when branching, 6 when not branching
*6: 8 + (a) when branching, 7 + (a) when not branching
*7: Set to 3 × (b) + 2 × (c) when an interrupt request occurs, and 6 × (c) for return.
*8: Retrieve (word) from stack
*9: Retrieve (long word) from stack
*10: In the CBNE/CWBNE instruction, do not use the RWj+ addressing mode.

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 21 Other Control Instructions (Byte/Word/Long Word) [28 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW A	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (A)	–	–	–	–	–	–	–	–	–	–
PUSHW AH	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (AH)	–	–	–	–	–	–	–	–	–	–
PUSHW PS	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (PS)	–	–	–	–	–	–	–	–	–	–
PUSHW rlst	2	*3	*5	*4	(SP) ← (SP) –2n, ((SP)) ← (rlst)	–	–	–	–	–	–	–	–	–	–
POPW A	1	3	0	(c)	word (A) ← ((SP)), (SP) ← (SP) +2	–	*	–	–	–	–	–	–	–	–
POPW AH	1	3	0	(c)	word (AH) ← ((SP)), (SP) ← (SP) +2	–	–	–	–	–	–	–	–	–	–
POPW PS	1	4	0	(c)	word (PS) ← ((SP)), (SP) ← (SP) +2	–	–	*	*	*	*	*	*	*	–
POPW rlst	2	*2	*5	*4	(rlst) ← ((SP)), (SP) ← (SP) +2n	–	–	–	–	–	–	–	–	–	–
JCTX @A	1	14	0	6× (c)	Context switch instruction	–	–	*	*	*	*	*	*	*	–
AND CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) and imm8	–	–	*	*	*	*	*	*	*	–
OR CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) or imm8	–	–	*	*	*	*	*	*	*	–
MOV RP, #imm8	2	2	0	0	byte (RP) ←imm8	–	–	–	–	–	–	–	–	–	–
MOV ILM, #imm8	2	2	0	0	byte (ILM) ←imm8	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, ear	2	3	1	0	word (RWi) ←ear	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, eam	2+	2+ (a)	1	0	word (RWi) ←eam	–	–	–	–	–	–	–	–	–	–
MOVEA A, ear	2	1	0	0	word(A) ←ear	–	*	–	–	–	–	–	–	–	–
MOVEA A, eam	2+	1+ (a)	0	0	word (A) ←eam	–	*	–	–	–	–	–	–	–	–
ADDSP #imm8	2	3	0	0	word (SP) ← (SP) +ext (imm8)	–	–	–	–	–	–	–	–	–	–
ADDSP #imm16	3	3	0	0	word (SP) ← (SP) +imm16	–	–	–	–	–	–	–	–	–	–
MOV A, brgl	2	*1	0	0	byte (A) ← (brgl)	Z	*	–	–	–	*	*	–	–	–
MOV brg2, A	2	1	0	0	byte (brg2) ← (A)	–	–	–	–	–	*	*	–	–	–
NOP	1	1	0	0	No operation	–	–	–	–	–	–	–	–	–	–
ADB	1	1	0	0	Prefix code for accessing AD space	–	–	–	–	–	–	–	–	–	–
DTB	1	1	0	0	Prefix code for accessing DT space	–	–	–	–	–	–	–	–	–	–
PCB	1	1	0	0	Prefix code for accessing PC space	–	–	–	–	–	–	–	–	–	–
SPB	1	1	0	0	Prefix code for accessing SP space	–	–	–	–	–	–	–	–	–	–
NCC	1	1	0	0	Prefix code for no flag change	–	–	–	–	–	–	–	–	–	–
CMR	1	1	0	0	Prefix code for common register bank	–	–	–	–	–	–	–	–	–	–

*1: PCB, ADB, SSB, USB, and SPB : 1 state
DTB, DPR : 2 states
*2: 7 + 3 × (pop count) + 2 × (last register number to be popped), 7 when rlst = 0 (no transfer register)
*3: 29 +3 × (push count) – 3 × (last register number to be pushed), 8 when rlst = 0 (no transfer register)
*4: Pop count × (c), or push count × (c)
*5: Pop count or push count.

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 22 Bit Manipulation Instructions [21 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVB A, dir:bp	3	5	0	(b)	byte (A) ← (dir:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB A, addr16:bp	4	5	0	(b)	byte (A) ← (addr16:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB A, io:bp	3	4	0	(b)	byte (A) ← (io:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB dir:bp, A	3	7	0	2× (b)	bit (dir:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB addr16:bp, A	4	7	0	2× (b)	bit (addr16:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB io:bp, A	3	6	0	2× (b)	bit (io:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
SETB dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB io:bp	3	7	0	2× (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
CLRB dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB io:bp	3	7	0	2× (b)	bit (io:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
BBC dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBS dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 1	–	–	–	–	–	–	*	–	–	–
SBBS addr16:bp, rel	5	*3	0	2× (b)	Branch when (addr16:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
WBTS io:bp	3	*4	0	*5	Wait until (io:bp) b = 1	–	–	–	–	–	–	–	–	–	–
WBTC io:bp	3	*4	0	*5	Wait until (io:bp) b = 0	–	–	–	–	–	–	–	–	–	–

*1: 8 when branching, 7 when not branching
*2: 7 when branching, 6 when not branching
*3: 10 when condition is satisfied, 9 when not satisfied
*4: Undefined count
*5: Until condition is satisfied

Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 23 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
SWAP	1	3	0	0	byte (A) 0 to 7 ↔ (A) 8 to 15	–	–	–	–	–	–	–	–	–	–
SWAPW/XCHW A,T	1	2	0	0	word (AH) ↔ (AL)	–	*	–	–	–	–	–	–	–	–
EXT	1	1	0	0	byte sign extension	X	–	–	–	–	*	*	–	–	–
EXTW	1	2	0	0	word sign extension	–	X	–	–	–	*	*	–	–	–
ZEXT	1	1	0	0	byte zero extension	Z	–	–	–	–	R	*	–	–	–
ZEXTW	1	1	0	0	word zero extension	–	Z	–	–	–	R	*	–	–	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 24 String Instructions [10 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVS/MOVSI	2	*2	*5	*3	Byte transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSD	2	*2	*5	*3	Byte transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCEQ/SCEQI	2	*1	*5	*4	Byte retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCEQD	2	*1	*5	*4	Byte retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FISL/FILSI	2	6m +6	*5	*3	Byte filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–
MOVSW/MOVSWI	2	*2	*8	*6	Word transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSWD	2	*2	*8	*6	Word transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCWEQ/SCWEQI	2	*1	*8	*7	Word retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCWEQD	2	*1	*8	*7	Word retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FILSW/FILSWI	2	6m +6	*8	*6	Word filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–

m: RW0 value (counter value)
n: Loop count
*1: 5 when RW0 is 0, 4 + 7 × (RW0) for count out, and 7 × n + 5 when match occurs
*2: 5 when RW0 is 0, 4 + 8 × (RW0) in any other case
*3: (b) × (RW0) + (b) × (RW0) when accessing different areas for the source and destination, calculate (b) separately for each.
*4: (b) × n
*5: 2 × (RW0)
*6: (c) × (RW0) + (c) × (RW0) when accessing different areas for the source and destination, calculate (c) separately for each.
*7: (c) × n
*8: 2 × (RW0)

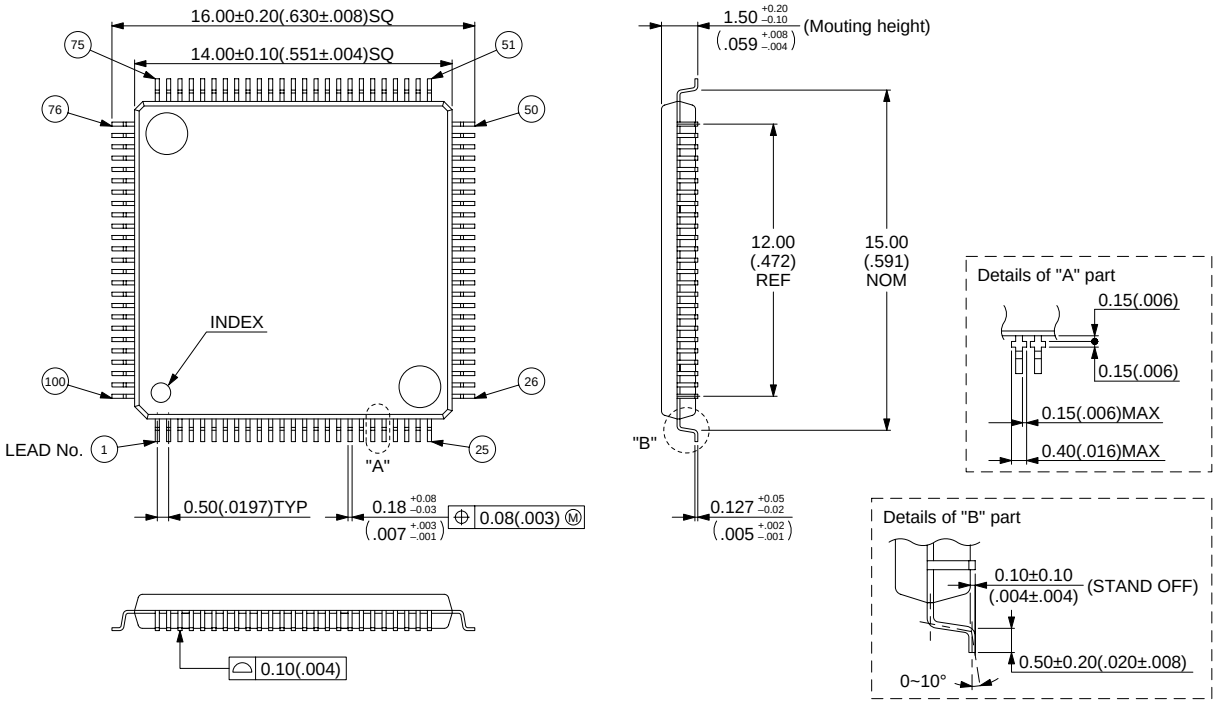
Note : For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F583CPFV MB90F583CAPFV MB90583CPFV MB90583CAPFV MB90587CPFV MB90587CAPFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F583CPF MB90F583CAPF MB90583CPF MB90583CAPF MB90587CPF MB90587CAPF	100-pin Plastic QFP (FPT-100P-M06)	

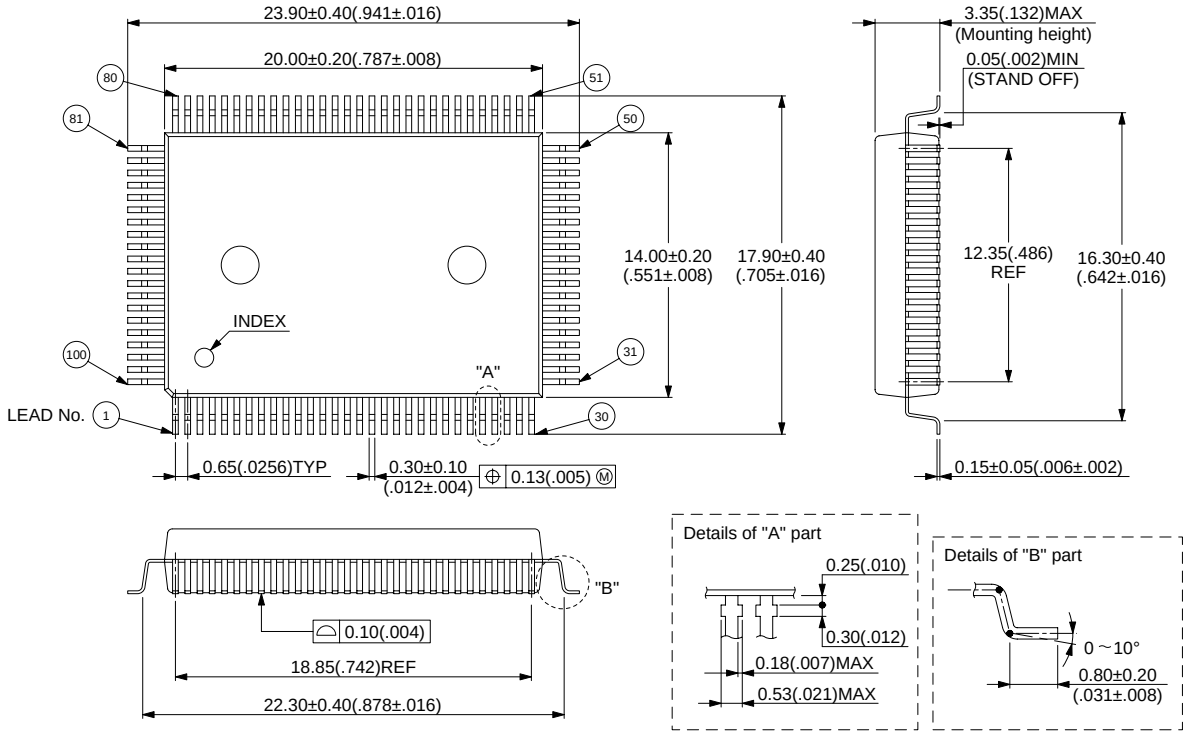
■ PACKAGE DIMENSIONS

100-pin plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches)

100-pin plastic QFP
(FPT-100P-M06)



Dimensions in mm (inches)

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