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KBA2338

3W Filterless Class-D Audio Power Amplifier

General Description

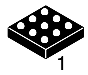
The kB2338A is a high efficiency, 3W mono class-D audio power amplifier. A low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplifying design.

Operating in a single 5V supply, kB2338A is capable of driving 4Ω speaker load at a continuous average output of 3W/10% THD+N or 2W/1% THD+N. The kB2338A has high efficiency with speaker load compared to a typical class AB amplifier. With a 3.6V supply driving an 8Ω speaker , the efficiency for a 400mW power level is 88%.

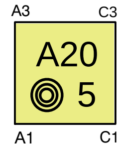
In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the kB2338A. The gain of kB2338A is externally configurable which allows independent gain control from multiple sources by summing signals from seperate sources.

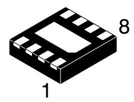
The kB2338A is available in space-saving WCSP and DFN packages.

MARKING DIAGRAMS

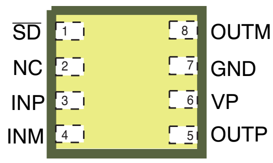


9–PIN FLIP–CHIP WCSP





8 PIN UDFN 2x2.2



Features

- Unique Modulation Scheme Reduces EMI Emissions
- Efficiency at 3.6V With an 8-Ω Speaker:
  - 88% at 400 mW
  - 80% at 100 mW
- Low 2.38-mA Quiescent Current and 0.5-µA Shutdown Current
- 2.5V to 6.0V Wide Supply Voltage
- Optimized PWM Output Stage Eliminates LC Output Filter
- Improved PSRR (−72 dB) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- Internally Generated 250-kHz Switching Frequency
- Integrated Pop and Click Suppression Circuitry
- 1.5mm × 1.5mm Wafer Chip Scale Package (WCSP) and 3mm × 3mm DFN-8 package
- RoHS compliant and 100% lead(Pb)-free

Applications

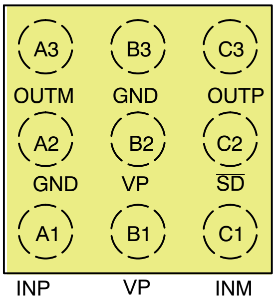
- Cellular Phone
- Portable Electronic Devices
- PDAs and Smart Phones
- Portable Computer

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
~~kBA2338B-UDFN~~	~~UDFN-8~~	~~xxxx~~	~~-40 °C to 85°C~~
kBA2338-WCSP	WCSP-9	A20 5	-40 °C to 85°C

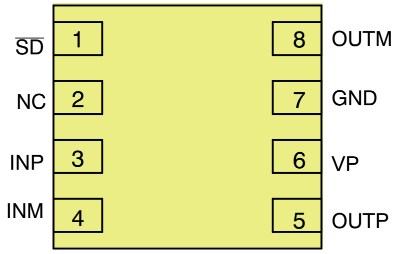
Pin Configuration

9–Pin Flip–Chip WCSP



(Top View)

UDFN8



(Top View)

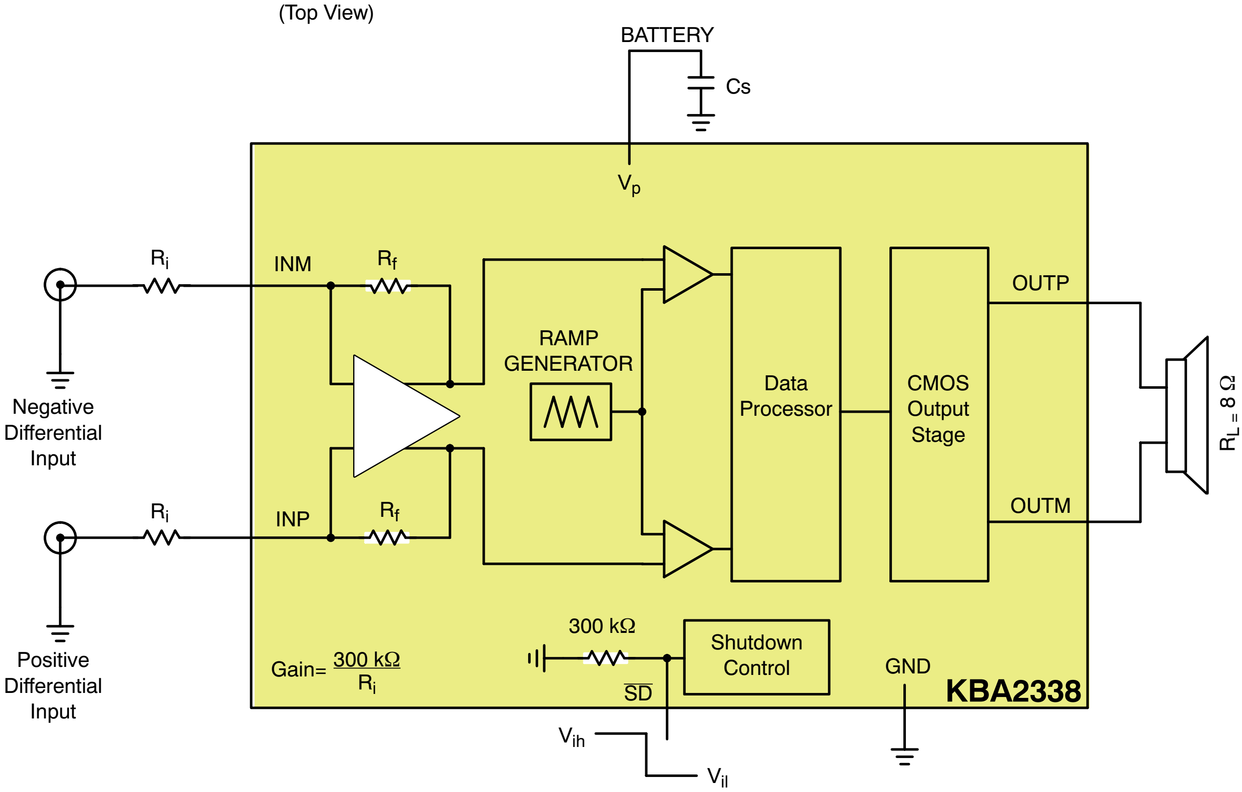


Figure 1. Typical Application

Pin Description

Pin No.		Symbol	Type	Description
WCSP	UDFN8			
A1	3	INP	I	Positive Differential Input.
A2	7	GND	I	Analog Ground.
A3	8	OUTM	O	Negative BTL Output.
B1		V_p	I	Analog Positive Supply. Range: 2.5 V – 6.0 V.
B2	6	V_p	I	Power Analog Positive Supply. Range: 2.5 V – 6.0 V.
B3	7	GND	I	Analog Ground.
C1	4	INM	I	Negative Differential Input.
C2	1	$\overline{SD}$	I	The device enters in Shutdown Mode when a low level is applied on this pin. An internal 300 kΩ resistor will force the device in shutdown mode if no signal is applied to this pin. It also helps to save space and cost.
C3	5	OUTP	O	Positive BTL Output.

Absolute Maximum Ratings

Symbol	Rating		Max	Unit
V_p	Supply Voltage	Active Mode Shutdown Mode	6.0 7.0	V
V_{in}	Input Voltage		−0.3 to V_{CC} +0.3	V
I_{out}	Max Output Current (Note 1)		1.5	A
P_d	Power Dissipation (Note 2)		Internally Limited	–
T_A	Operating Ambient Temperature		−40 to +85	°C
T_J	Max Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		−65 to +150	°C
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	9−Pin Flip−Chip UDFN8	90 (Note 3) 50	°C/W
 – –	ESD Protection Human Body Model (HBM) (Note 4) Machine Model (MM) (Note 5)		 > 2000 > 200	V
–	Latchup Current @ T_A = 85°C (Note 6)	9−Pin Flip−Chip UDFN8	±70 ±100	mA
MSL	Moisture Sensitivity (Note 7)		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The device is protected by a current breaker structure. See “Current Breaker Circuit” in the Description Information section for more information.
2. The thermal shutdown is set to 160°C (typical) avoiding irreversible damage to the device due to power dissipation.
3. For the 9−Pin Flip−Chip CSP package, the $R_{\theta JA}$ is highly dependent of the PCB Heatsink area. For example, $R_{\theta JA}$ can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 500 mm^2. When using ground and power planes, the value is around 90°C/W, as specified in table.
4. Human Body Model: 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114. On 9−Pin Flip−Chip, B2 Pin (V_P) is qualified at 1500 V.
5. Machine Model: 200 pF discharged through all pins following specification JESD22/A115.
6. Latchup Testing per JEDEC Standard JESD78.
7. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Electrical Characteristics

(Limits apply for T_A = +25°C unless otherwise noted) (WCSP)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	V_p	T_A = –40°C to +85°C	2.5	–	6.0	V
Supply Quiescent Current	I_{dd}	V_p = 3.6 V, R_L = 8.0 Ω V_p = 5.5 V, No Load V_p from 2.5 V to 5.5 V, No Load T_A = –40°C to +85°C	– – –	2.15 2.61 –	– – 4.6	mA
Shutdown Current	I_{sd}	V_p = 4.2 V T_A = +25°C T_A = +85°C	 – –	 0.42 0.45	 0.8 –	μA
		V_p = 5.5 V T_A = +25°C T_A = +85°C	 – –	 0.8 0.9	 1.5 –	μA
Shutdown Voltage High	V_{sdih}	–	1.2	–	–	V
Shutdown Voltage Low	V_{sdil}	–	–	–	0.4	V
Switching Frequency	F_{sw}	V_p from 2.5 V to 5.5 V T_A = –40°C to +85°C	190	250	310	kHz
Gain	G	R_L = 8.0 Ω	$\frac{285\ k\Omega}{R_i}$	$\frac{300\ k\Omega}{R_i}$	$\frac{315\ k\Omega}{R_i}$	$\frac{V}{V}$
Output Impedance in Shutdown Mode	Z_{SD}	–	–	300	–	Ω
Resistance from $\overline{SD}$ to GND	Rs	–	–	300	–	kΩ
Output Offset Voltage	Vos	V_p = 5.5 V	–	6.0	–	mV
Turn On Time	Ton	V_p from 2.5 V to 5.5 V	–	9.0	–	ms
Turn Off Time	Toff	V_p from 2.5 V to 5.5 V	–	5.0	–	ms
Thermal Shutdown Temperature	Tsd	–	–	160	–	°C
Output Noise Voltage	Vn	V_p = 3.6 V, f = 20 Hz to 20 kHz no weighting filter with A weighting filter	 – –	 65 42	 – –	μVrms
RMS Output Power	Po	R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 1% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.32 0.48 0.7 0.97 1.38	 – – – – –	W
		R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 10% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.4 0.59 0.87 1.19 1.7	 – – – – –	W
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 1% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.49 0.72 1.06 1.62 2.12	 – – – – –	W
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 10% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.6 0.9 1.33 2.0 2.63	 – – – – –	W

Electrical Characteristics

(Limits apply for T_A = +25°C unless otherwise noted) (WCSP)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Efficiency	–	R_L = 8.0 Ω, f = 1.0 kHz V_p = 5.0 V, P_{out} = 1.2 W V_p = 3.6 V, P_{out} = 0.6 W	 – –	 91 90	 – –	%
		R_L = 4.0 Ω, f = 1.0 kHz V_p = 5.0 V, P_{out} = 2.0 W V_p = 3.6 V, P_{out} = 1.0 W	 – –	 82 81	 – –	
Total Harmonic Distortion + Noise	THD+N	V_p = 5.0 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W V_p = 3.6 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W	 – –	 0.05 0.09	 – –	%
Common Mode Rejection Ratio	CMRR	V_p from 2.5 V to 5.5 V V_{ic} = 0.5 V to V_p – 0.8 V V_p = 3.6 V, V_{ic} = 1.0 V_{pp} f = 217 Hz f = 1.0 kHz	 – – –	 –62 –56 –57	 – – –	dB
Power Supply Rejection Ratio	PSRR	$V_{p\_ripple\_pk-pk}$ = 200 mV, R_L = 8.0 Ω, Inputs AC Grounded V_p = 3.6 V f = 217 kHz f = 1.0 kHz	 – –	 –62 –65	 – –	dB

Electrical Characteristics

(Limits apply for T_A = +25°C unless otherwise noted) (UDFN)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	V_p	T_A = –40°C to +85°C	2.5	–	6.0	V
Supply Quiescent Current	I_{dd}	V_p = 3.6 V, R_L = 8.0 Ω V_p = 5.5 V, No Load V_p from 2.5 V to 5.5 V, No Load T_A = –40°C to +85°C	– – –	2.15 2.61 –	– – 3.8	mA
Shutdown Current	I_{sd}	V_p = 4.2 V T_A = +25°C T_A = +85°C	 – –	 0.42 0.45	 0.8 2.0	µA
		V_p = 5.5 V T_A = +25°C T_A = +85°C	 – –	 0.8 0.9	 1.5 –	µA
Shutdown Voltage High	V_{sdih}	–	1.2	–	–	V
Shutdown Voltage Low	V_{sdil}	–	–	–	0.4	V
Switching Frequency	F_{sw}	V_p from 2.5 V to 5.5 V T_A = –40°C to +85°C	180	240	300	kHz
Gain	G	R_L = 8.0 Ω	$\frac{285\ k\Omega}{R_i}$	$\frac{300\ k\Omega}{R_i}$	$\frac{315\ k\Omega}{R_i}$	$\frac{V}{V}$
Output Impedance in Shutdown Mode	Z_{SD}	–	–	20	–	kΩ
Resistance from $\overline{SD}$ to GND	Rs	–	–	300	–	kΩ
Output Offset Voltage	Vos	V_p = 5.5 V	–	6.0	–	mV
Turn On Time	Ton	V_p from 2.5 V to 5.5 V	–	1.0	–	µs
Turn Off Time	Toff	V_p from 2.5 V to 5.5 V	–	1.0	–	µs
Thermal Shutdown Temperature	Tsd	–	–	160	–	°C
Output Noise Voltage	Vn	V_p = 3.6 V, f = 20 Hz to 20 kHz no weighting filter with A weighting filter	 – –	 65 42	 – –	µVrms

Electrical Characteristics

(Limits apply for T_A = +25°C unless otherwise noted) (UDFN)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
RMS Output Power	Po	R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 1% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.22 0.33 0.45 0.67 0.92	 – – – – –	W
		R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 10% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.36 0.53 0.76 1.07 1.49	 – – – – –	W
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 1% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.24 0.38 0.57 0.83 1.2	 – – – – –	W
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 10% V_p = 2.5 V V_p = 3.0 V V_p = 3.6 V V_p = 4.2 V V_p = 5.0 V	 – – – – –	 0.52 0.8 1.125 1.58 2.19	 – – – – –	W
Efficiency	–	R_L = 8.0 Ω, f = 1.0 kHz V_p = 5.0 V, P_{out} = 1.2 W V_p = 3.6 V, P_{out} = 0.6 W	 – –	 87 87	 – –	%
		R_L = 4.0 Ω, f = 1.0 kHz V_p = 5.0 V, P_{out} = 2.0 W V_p = 3.6 V, P_{out} = 1.0 W	 – –	 79 78	 – –	
Total Harmonic Distortion + Noise	THD+N	V_p = 5.0 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W V_p = 3.6 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W	 – –	 0.05 0.06	 – –	%
Common Mode Rejection Ratio	CMRR	V_p from 2.5 V to 5.5 V V_{ic} = 0.5 V to V_p – 0.8 V V_p = 3.6 V, V_{ic} = 1.0 V_{pp} f = 217 Hz f = 1.0 kHz	 – – –	 –62 –56 –57	 – – –	dB
Power Supply Rejection Ratio	PSRR	$V_{p\_ripple\_pk-pk}$ = 200 mV, R_L = 8.0 Ω, Inputs AC Grounded V_p = 3.6 V f = 217 kHz f = 1.0 kHz	 – –	 –62 –65	 – –	dB

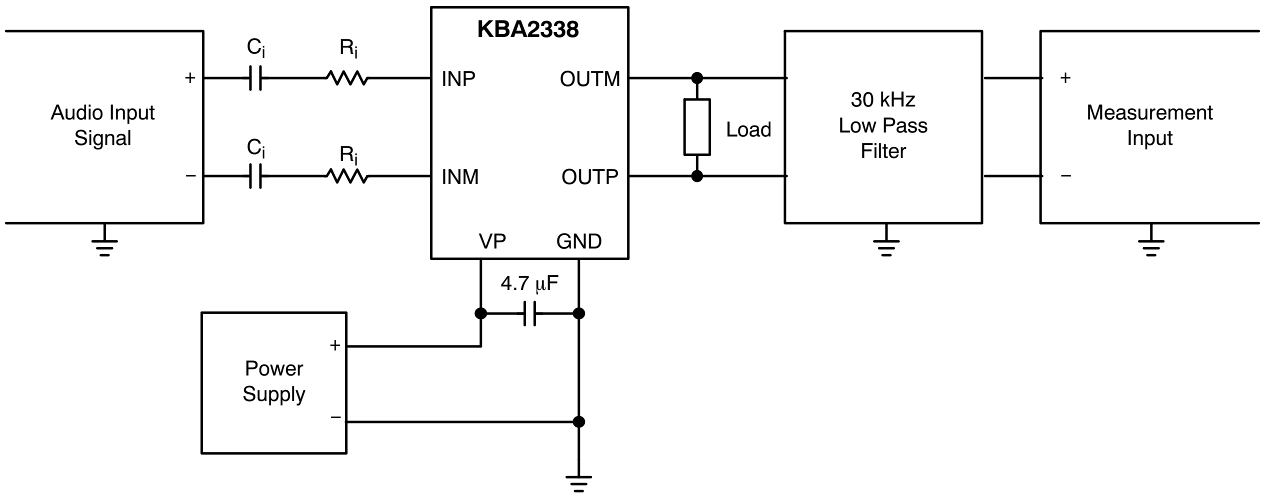


Figure 2. Test Setup for Graphs

NOTES:

1. Unless otherwise noted, C_i = 100 nF and R_i= 150 kΩ. Thus, the gain setting is 2 V/V and the cutoff frequency of the input high pass filter is set to 10 Hz. Input capacitors are shorted for CMRR measurements.
2. To closely reproduce a real application case, all measurements are performed using the following loads:
   R_L = 8 Ω means Load = 15 µH + 8 Ω + 15 µH
   R_L = 4 Ω means Load = 15 µH + 4 Ω + 15 µH
   Very low DCR 15 µH inductors (50 mΩ) have been used for the following graphs. Thus, the electrical load measurements are performed on the resistor (8 Ω or 4 Ω) in differential mode.
3. For Efficiency measurements, the optional 30 kHz filter is used. An RC low−pass filter is selected with (100 Ω, 47 nF) on each PWM output.

TYPICAL PERFORMANCE CHARACTERISTICS

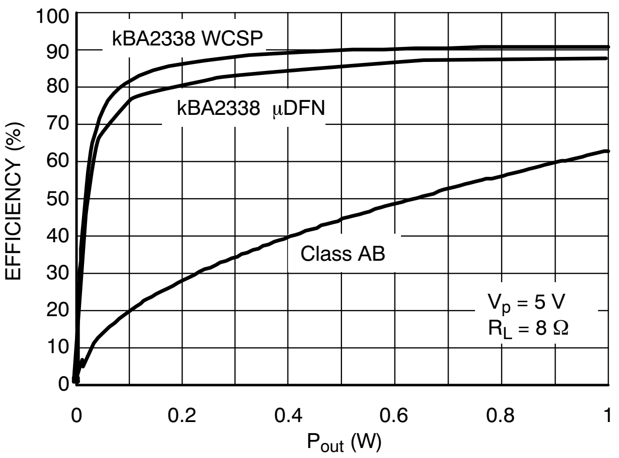


Figure 3. Efficiency vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz

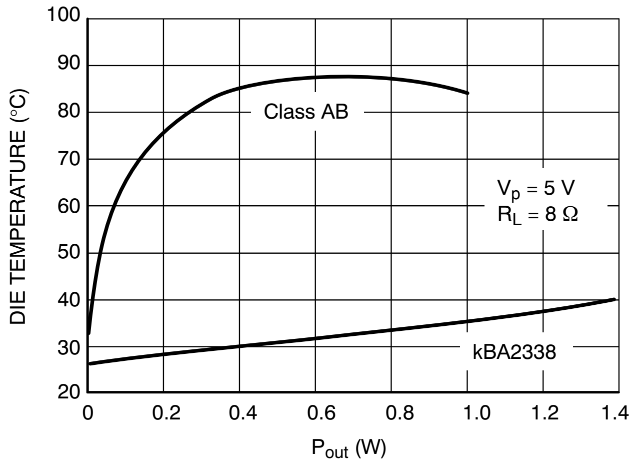


Figure 4. Die Temperature vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz @ T_A = +25°C

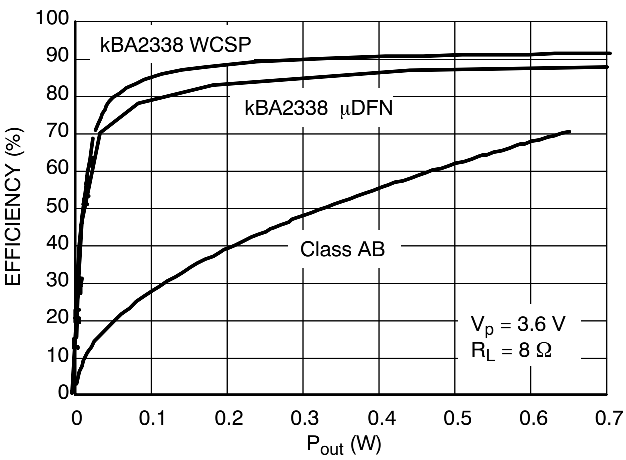


Figure 5. Efficiency vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz

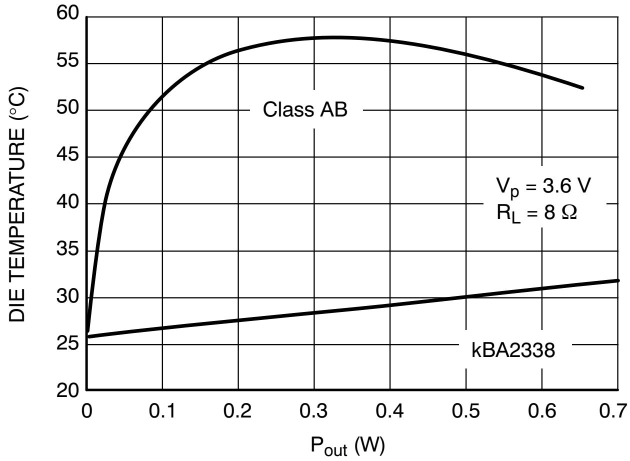


Figure 8. Die Temperature vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz @ T_A = +25°C

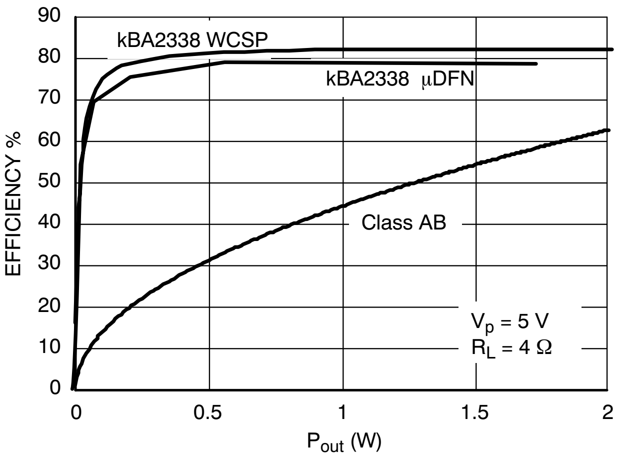


Figure 6. Efficiency vs. P_{out}
V_p = 5 V, R_L = 4 Ω, f = 1 kHz

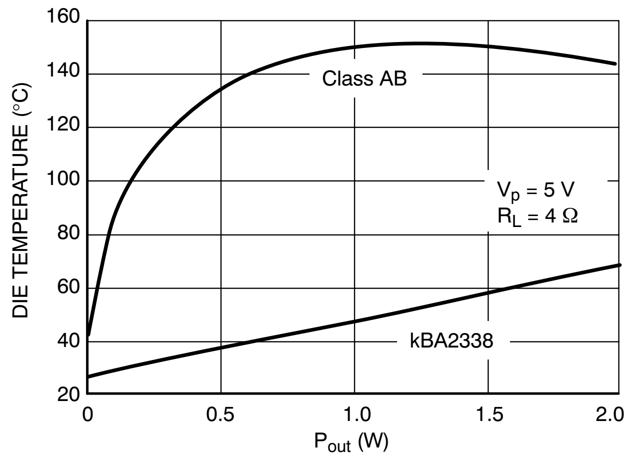


Figure 7. Die Temperature vs. P_{out}
V_p = 5 V, R_L = 4 Ω, f = 1 kHz @ T_A = +25°C

TYPICAL PERFORMANCE CHARACTERISTICS

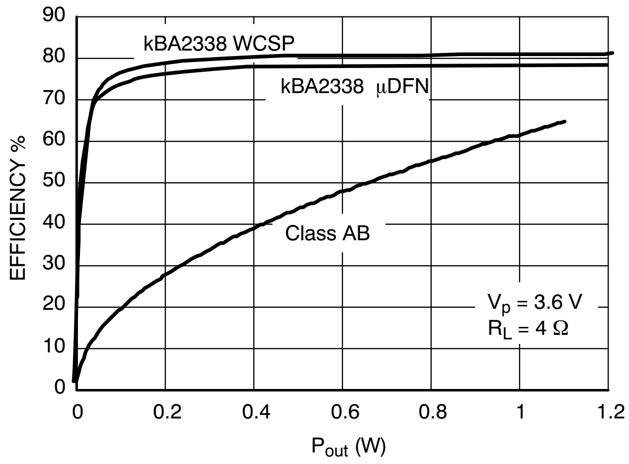


Figure 9. Efficiency vs. P_{out}
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz

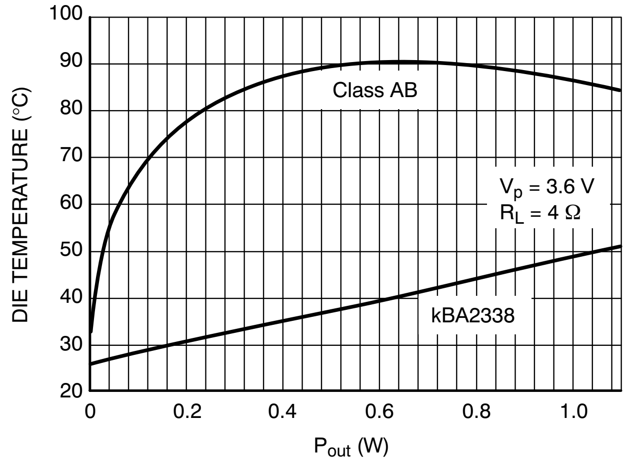


Figure 10. Die Temperature vs. P_{out}
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz @ T_A = +25°C

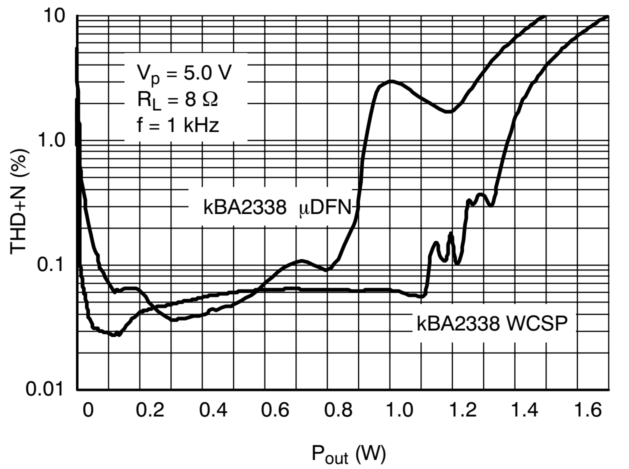


Figure 11. THD+N vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz

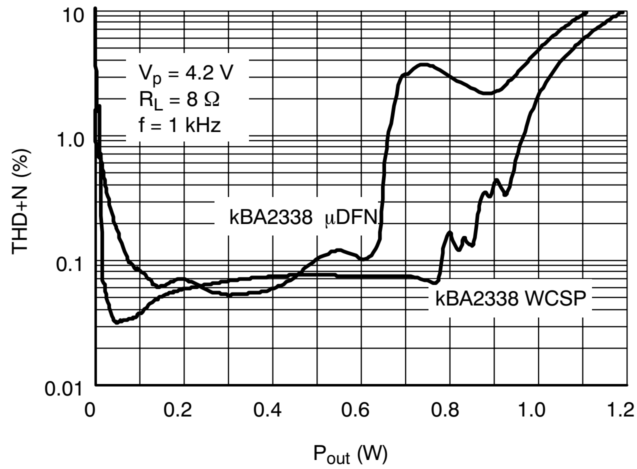


Figure 12. THD+N vs. P_{out}
V_p = 4.2 V, R_L = 8 Ω, f = 1 kHz

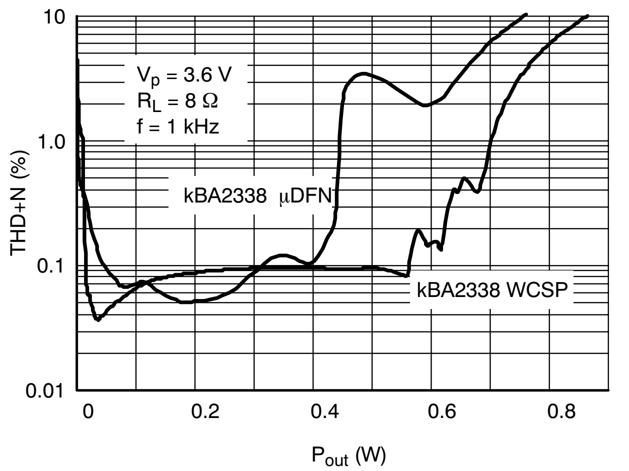


Figure 13. THD+N vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz

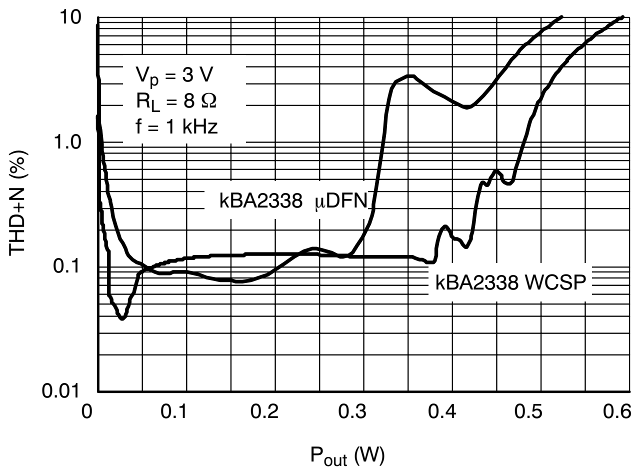


Figure 14. THD+N vs. P_{out}
V_p = 3 V, R_L = 8 Ω, f = 1 kHz

TYPICAL PERFORMANCE CHARACTERISTICS

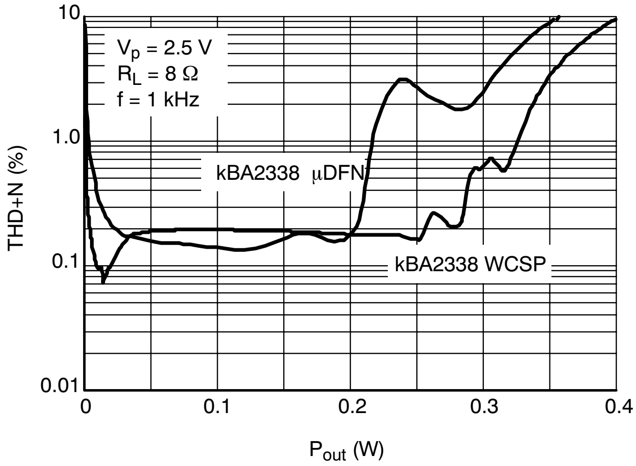


Figure 15. THD+N vs. Pout
V_p = 2.5 V, R_L = 8 Ω, f = 1 kHz

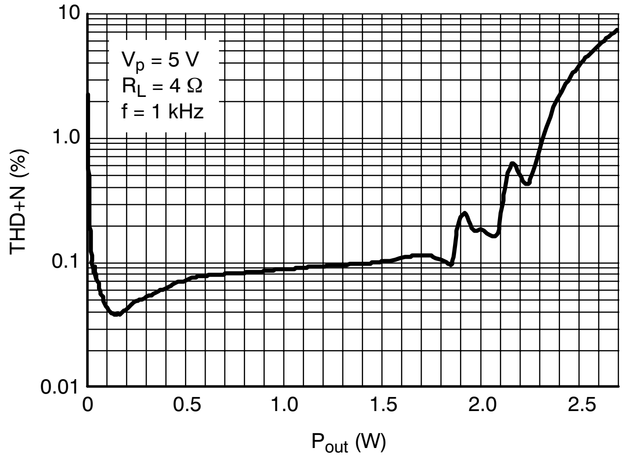


Figure 16. THD+N vs. Pout
V_p = 5 V, R_L = 4 Ω, f = 1 kHz

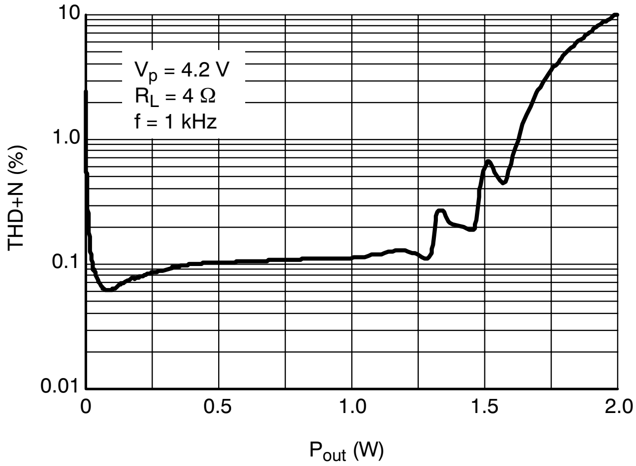


Figure 17. THD+N vs. Pout
V_p = 4.2 V, R_L = 4 Ω, f = 1 kHz

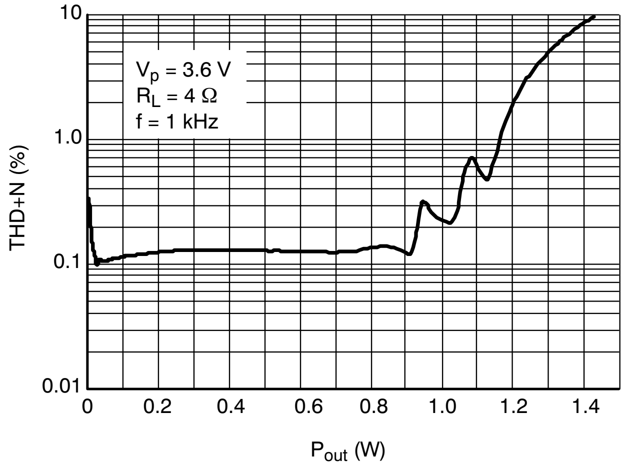


Figure 18. THD+N vs. Pout
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz

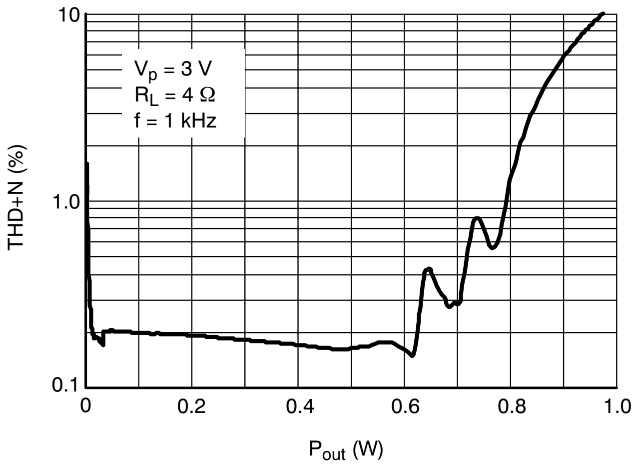


Figure 19. THD+N vs. Power Out
V_p = 3 V, R_L = 4 Ω, f = 1 kHz

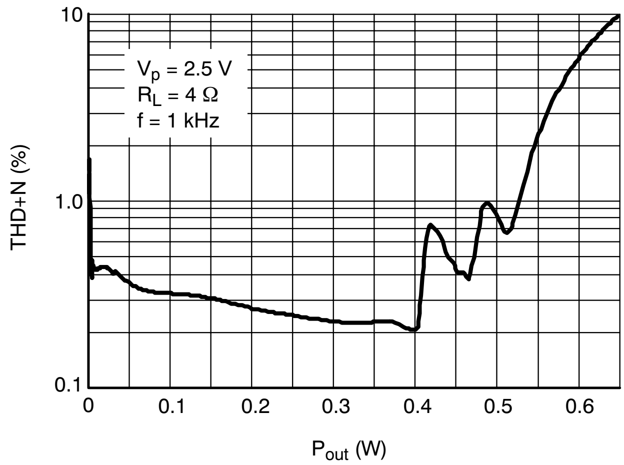


Figure 20. THD+N vs. Power Out
V_p = 2.5 V, R_L = 4 Ω, f = 1 kHz

TYPICAL PERFORMANCE CHARACTERISTICS

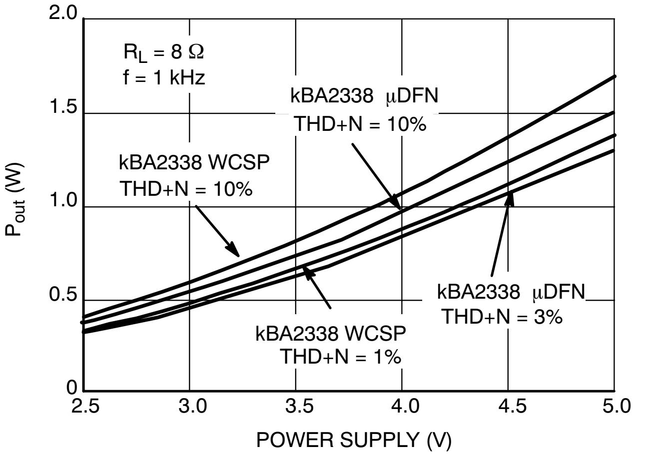


Figure 21. Output Power vs. Power Supply
R_L = 8 Ω @ f = 1 kHz

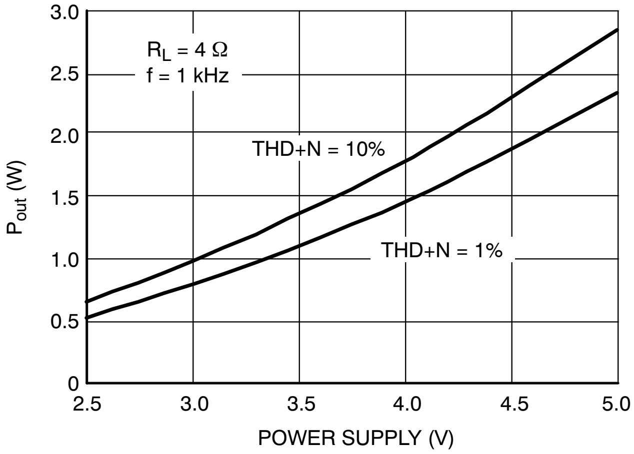


Figure 22. Output Power vs. Power Supply
R_L = 4 Ω @ f = 1 kHz

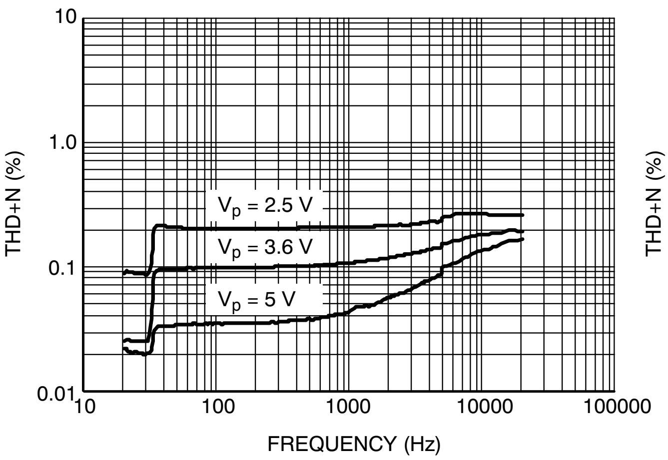


Figure 23. THD+N vs. Frequency
R_L = 8 Ω, P_{out} = 250 mW @ f = 1 kHz

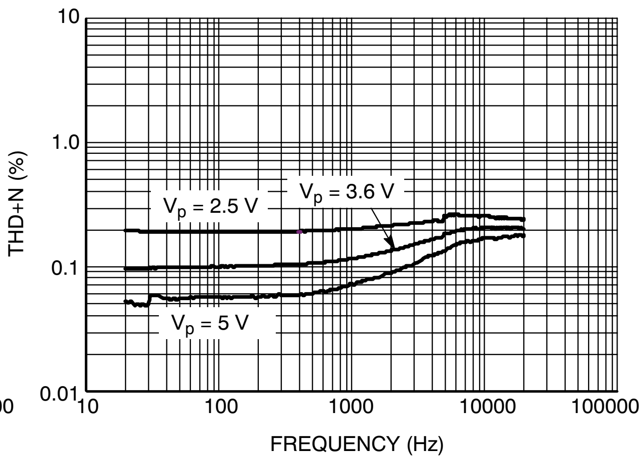


Figure 24. THD+N vs. Frequency
R_L = 4 Ω, P_{out} = 250 mW @ f = 1 kHz

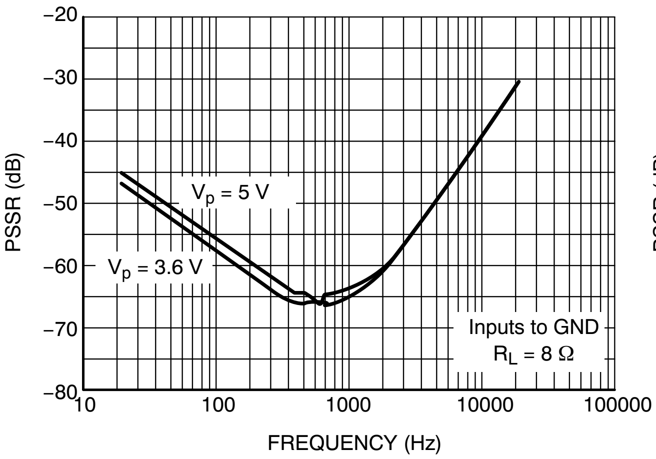


Figure 25. PSRR vs. Frequency
Inputs Grounded, R_L = 8 Ω, Vripple = 200 mvpkpk

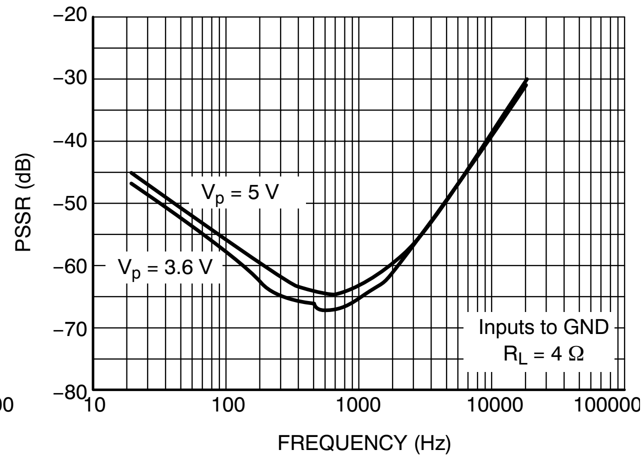


Figure 26. PSRR vs. Frequency
Inputs grounded, R_L = 4 Ω, Vripple = 200 mVpkpk

TYPICAL PERFORMANCE CHARACTERISTICS

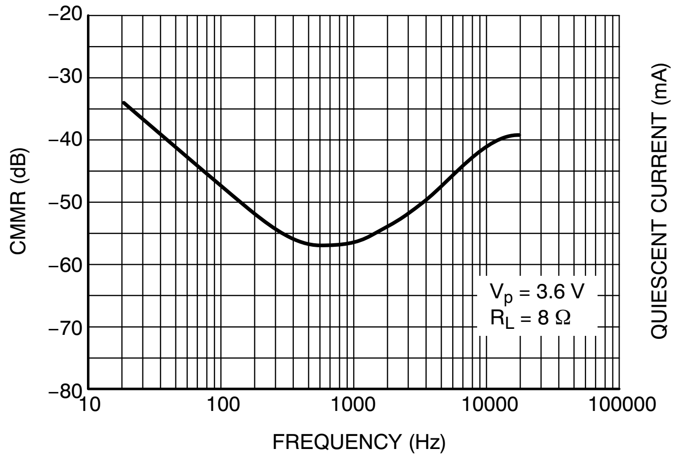


Figure 27. PSRR vs. Frequency
V_p = 3.6 V, R_L = 8 Ω, Vic = 200 mvpkpk

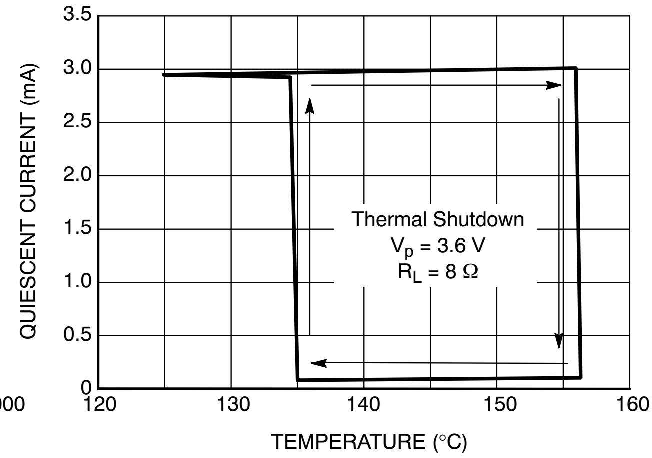


Figure 28. Thermal Shutdown vs. Temperature
V_p = 5 V, R_L = 8 Ω,

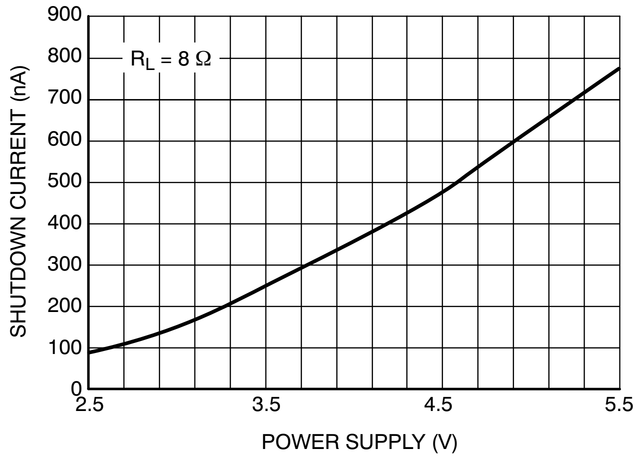


Figure 29. Shutdown Current vs. Power Supply
R_L = 8 Ω

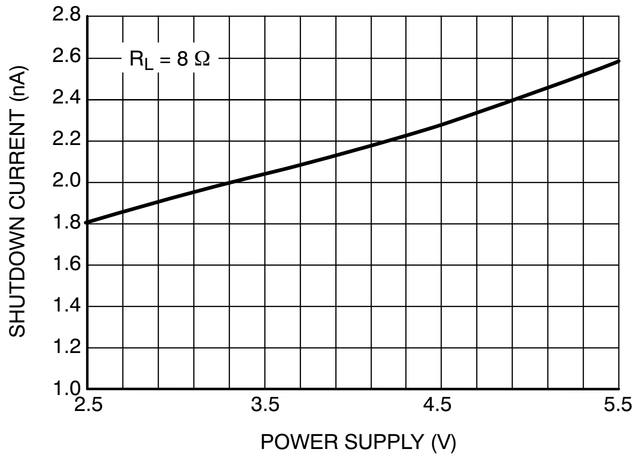


Figure 30. Quiescent Current vs. Power Supply
R_L = 8 Ω

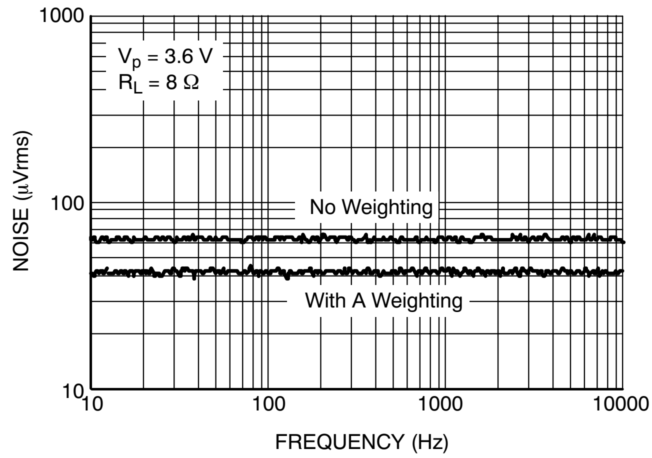


Figure 31. Noise Floor, Inputs AC Grounded
with 1 μF V_p = 3.6 V

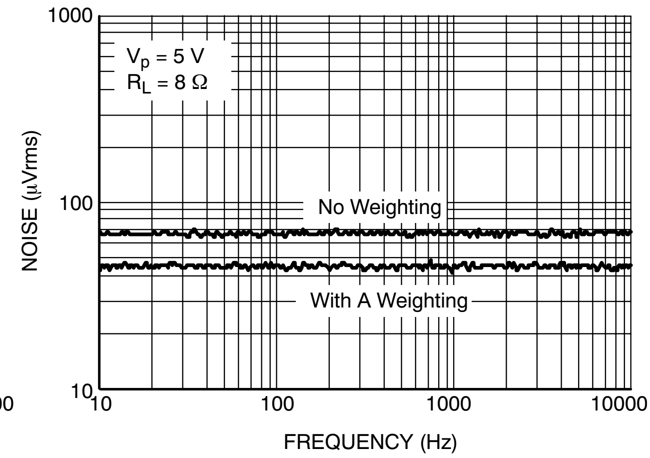


Figure 32. Noise Floor, Inputs AC Grounded
with 1 μF V_p = 5 V

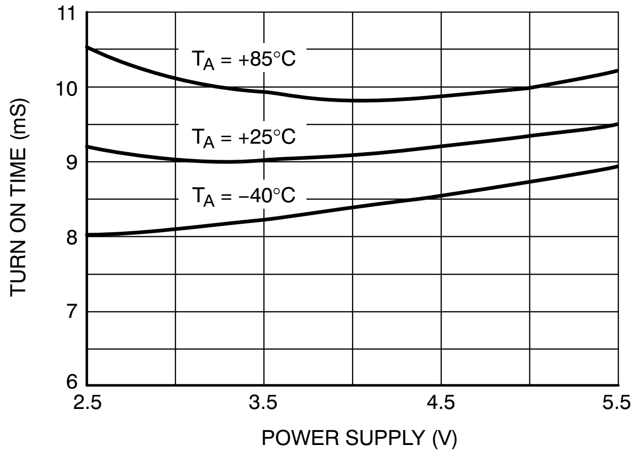


Figure 33. Turn on Time

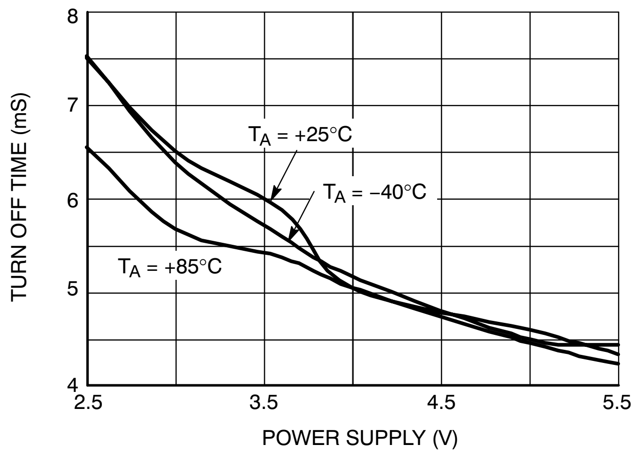


Figure 34. Turn off Time

Description Information

Detailed Description

The basic structure of the Kba2338 is composed of one analog pre−amplifier, a pulse width modulator and an H−bridge CMOS power stage. The first stage is externally configurable with gain−setting resistor R_i and the internal fixed feedback resistor R_f (the closed−loop gain is fixed by the ratios of these resistors) and the other stage is fixed. The load is driven differentially through two output stages.

The differential PWM output signal is a digital image of the analog audio input signal. The human ear is a band pass filter regarding acoustic waveforms, the typical values of which are 20 Hz and 20 kHz. Thus, the user will hear only the amplified audio input signal within the frequency range. The switching frequency and its harmonics are fully filtered. The inductive parasitic element of the loudspeaker helps to guarantee a superior distortion value.

Power Amplifier

The output PMOS and NMOS transistors of the amplifier have been designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors is typically 0.4 Ω.

Turn On and Turn Off Transitions in Case of 9 Pin Flip−Chip Package

In order to eliminate "pop and click" noises during transition, the output power in the load must not be established or cutoff suddenly. When a logic high is applied to the shutdown pin, the internal biasing voltage rises quickly and, 4 ms later, once the output DC level is around the common mode voltage, the gain is established slowly (5.0 ms). This method to turn on the device is optimized in terms of rejection of "pop and click" noises. Thus, the total turn on time to get full power to the load is 9 ms (typical).

The device has the same behavior when it is turned−off by a logic low on the shutdown pin. No power is delivered to the load 5 ms after a falling edge on the shutdown pin. Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

Turn On and Turn Off Transitions in Case of UDFN8

In case of UDFN8 package, the audio signal is established instantaneously after the rising edge on the shutdown pin. The audio is also suddenly cut once a low level is sent to the amplifier. This way to turn on and off the device in a very fast way also prevents from "pop & click" noise.

Shutdown Function

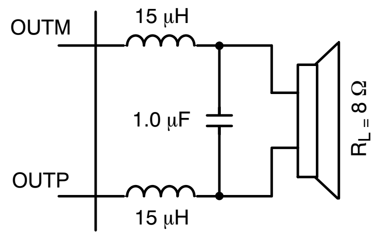
The device enters shutdown mode when the shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 1.5 μA.

Current Breaker Circuit

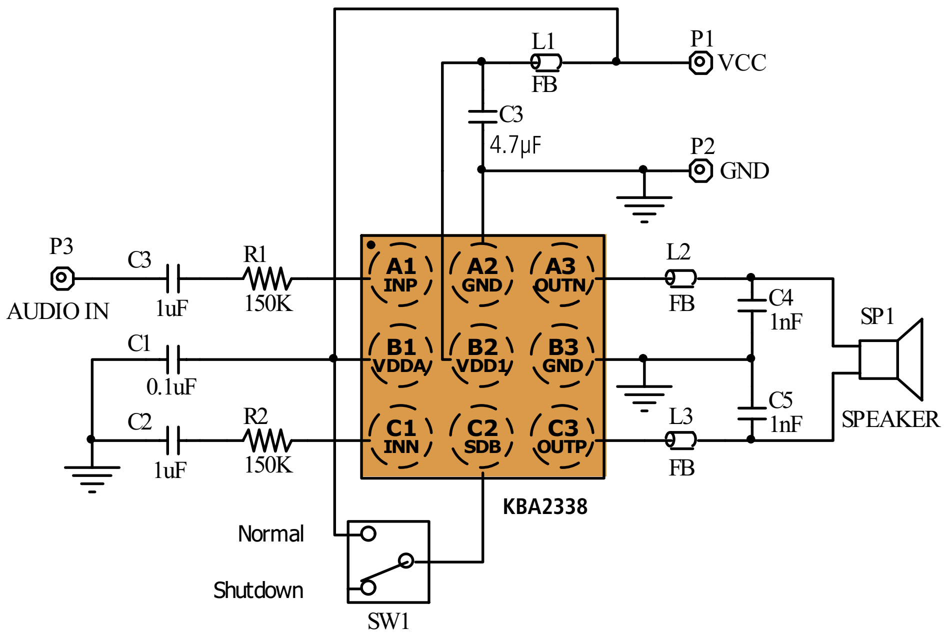
The maximum output power of the circuit corresponds to an average current in the load of 820 mA.

In order to limit the excessive power dissipation in the load if a short−circuit occurs, a current breaker cell shuts down the output stage. The current in the four output MOS transistors are real−time controlled, and if one current exceeds the threshold set to 1.5 A, the MOS transistor is opened and the current is reduced to zero. As soon as the short−circuit is removed, the circuit is able to deliver the expected output power.

This patented structure protects the Kba2338. Since it completely turns off the load, it minimizes the risk of the chip overheating which could occur if a soft current limiting circuit was used.



Optional Audio Output Filter

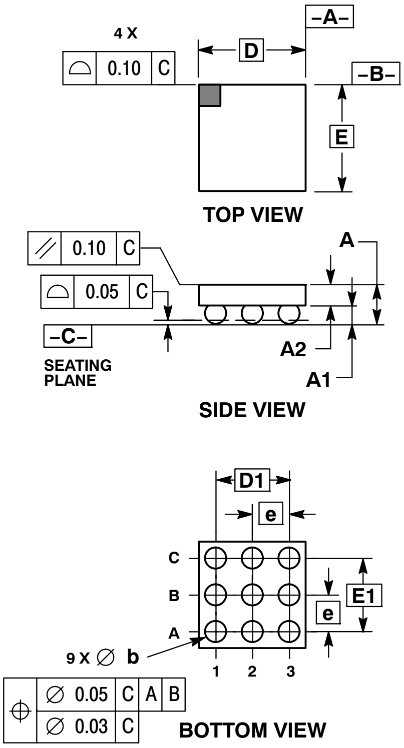


Ferrite Bead specification: Z=120 Ω @100MHz , Current rating=3A

kBA2338 WCSP Application Schematic

PACAGE DESCRIPTION

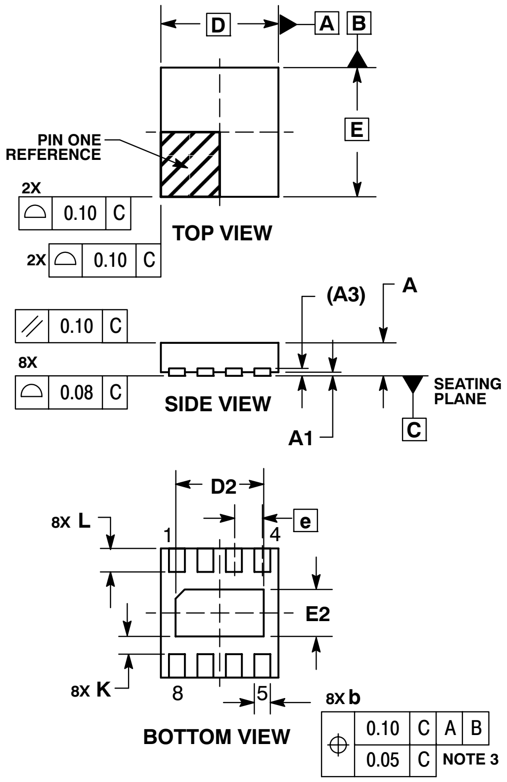
9 PIN WCSP



DIM	MILLIMETERS	
	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

PACAGE DESCRIPTION

8 PIN UDFN, 2x2.2, 0.5P



	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	2.00 BSC		
D2	1.40	1.50	1.60
E	2.20 BSC		
E2	0.70	0.80	0.90
e	0.50 BSC		
K	0.20	---	---
L	0.35	0.40	0.45

SOLDERING FOOTPRINT*