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Description

The VX-700 is a Voltage Controlled Crystal Oscillator that operates at the fundamental frequency of the internal HFF crystal. The HFF crystal is a high-Q quartz device that enables the circuit to achieve low phase jitter performance over a wide operating temperature range. The VX-700 is housed in an industry standard hermetically sealed LCC package and available in tape and reel.

Features

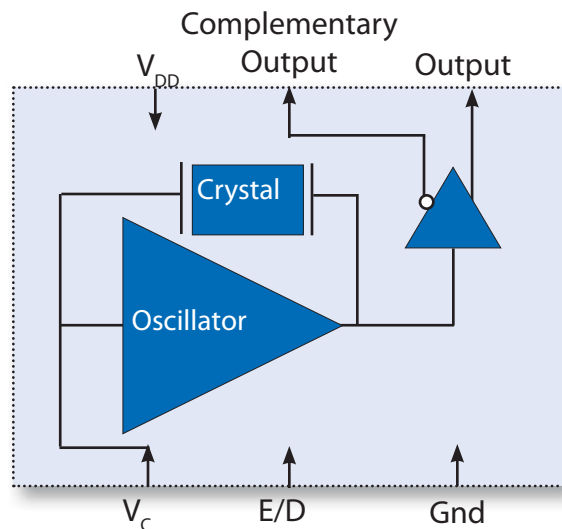
- Fundamental VCXO with no subharmonics or spurs
- Low Jitter, sub 1pS performance
- Output Frequencies from 77.76 MHz to 200 MHz
- 3.3 V Operation
- LVPECL Output
- Output Disable Feature
- Excellent ± 20 ppm temperature stability,
- 0/70°C or -40/85°C operating temperature
- Small Industry Standard Package, 5.0x7.5x1.8mm
- Product is free of lead and compliant to EC RoHS Directive



Applications

- Ideal for PLL circuits for clock smoothing and frequency translation
- SONET, SDH
 - Synchronous Ethernet
 - Fiber Channel
 - LAN / WAN
 - Test and Measurement

Block Diagram



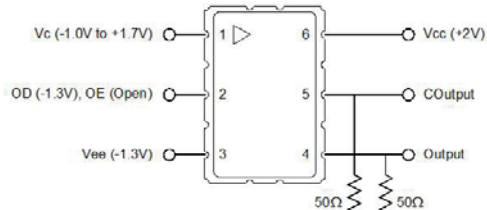
Performance Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	3.135	3.3	3.465	V
Current (No Load)	I_{DD}		50	90	mA
Frequency					
Nominal Frequency ²	f_N	77.7600		200	MHz
Absolute Pull Range ^{3,6}	APR	± 50			ppm
Linearity ³	Lin		5	10	%
Gain Transfer Positive ³ (See pg 5)	K_V		+65		ppm/V
Temperature Stability ³	f_{STAB}		± 20		ppm
Outputs					
Output Logic Levels ³ Output Logic High Output Logic Low	V_{OH} V_{OL}	$V_{DD}-1.025$ $V_{DD}-1.810$	$V_{DD}-0.950$ $V_{DD}-1.700$	$V_{DD}-0.880$ $V_{DD}-1.620$	V
Current	I_{OUT}			20	mA
Rise Time ⁴	t_R			1	ns
Fall Time	t_F			1	ns
Symmetry ³	SYM	45	50	55	%
Jitter (12 kHz - 20 MHz BW) ⁵	ϕ_J		0.3	0.5	ps
Jitter (50 kHz - 80 MHz BW) ⁵	ϕ_J		0.5	0.7	ps
Period Jitter, RMS (155.520 MHz) ⁷	ϕ_J		3.0		ps
Period Jitter, Peak - Peak (155.520MHz) ⁷	ϕ_J		20		ps
Spurious Suppression ²			-80		dBc
Control Voltage					
Control Voltage Range for APR	V_C	0.3		3.0	V
Control Voltage Input Impedance	Z_{IN}	10			M Ω
Control Voltage Modulation BW	BW	10	20		kHz
Enable/Disable					
Output Enabled, Option A ⁸ Output Disabled, Option A	V_{IH} V_{IL}	$0.7*V_{DD}$		$0.3*V_{DD}$	V
Output Enabled, Option C ⁸ Output Disabled, Option C	V_{IL} V_{IH}	$0.7*V_{DD}$		$0.2*V_{DD}$	V
Operating Temperature	T_{OP}	0/70 or -40/85			$^{\circ}C$
Package Size		5.0 x 7.5 x 1.8			mm

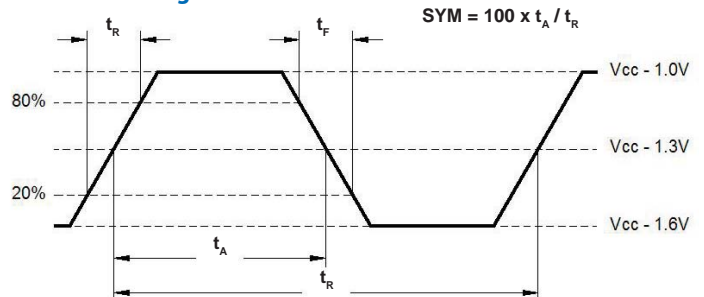
- 1] The VX-700 power supply should be filtered, eg, 0.1 and 0.01uF to ground
- 2] See Standard Frequencies and Ordering Information tables for more specific information
- 3] Parameters are tested with production test circuit below (Fig 1).
- 4] Measured from 20% to 80% of a full output swing (Fig 2).
- 5] Integrated across stated bandwidth.
- 6] Tested with $V_C = 0.3V$ to $3.0V$ unless otherwise stated in part description
- 7] Broadband Period Jitter measured using Lecroy Wavemaster 8600A 6 GHz Oscilloscope, 25K samples taken. See application note.
- 8] Output is Enabled if E/D is left floating

Fig 1: Test Circuit



Test Circuit Notes:
 1) To Permit 50 Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
 3) 50 Ω Terminations are Within Test Equipment.

Fig 2: LVPECL Waveform



Suggested Output Load Configurations

The VX-700 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 3. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 4, and a pull-up/pull-down scheme as shown in Figure 5. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

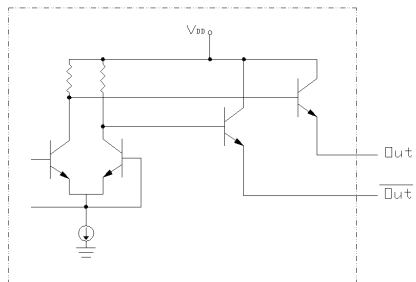


Figure 3 Standard PECL Output Configuration

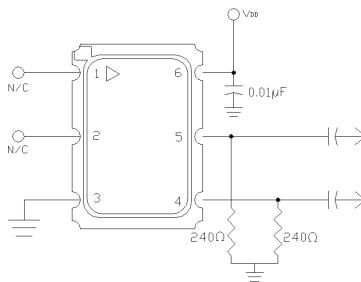


Figure 4 Single Resistor Termination Scheme
Resistor values are typically 120 to 240 ohms

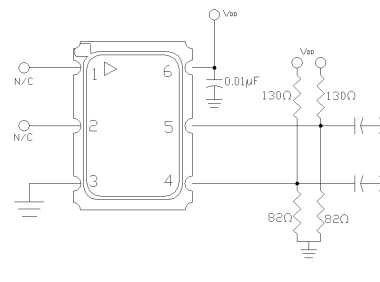


Figure 5 Pull-Up Pull-Down Termination

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VX-700 family is capable of meeting the following qualification tests:

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	0 to 6	V
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Storage Temperature	T_S	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 40	°C / sec

Although ESD protection circuitry has been designed into the VX-700 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 5. ESD Ratings

Model	Minimum	Conditions
Human Body Model	500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

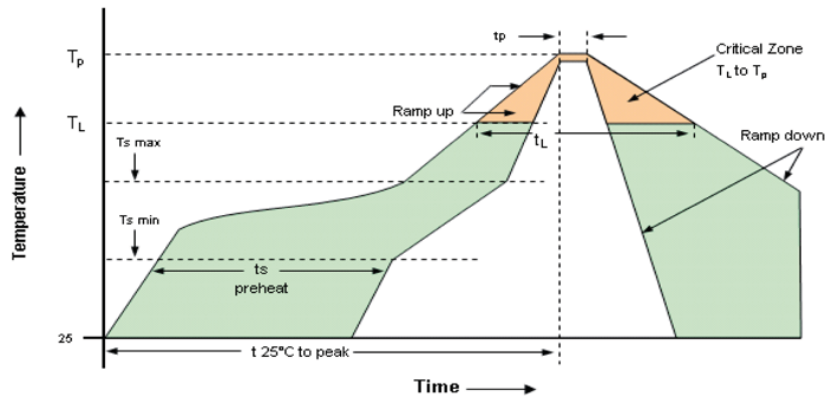
Table 6. Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	t_s	60 sec Min, 180 sec Max 150°C 200°C
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	$T_{25C \text{ to peak}}$	480 sec Max
Time at 260 °C	t_p	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VX-700 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating:
Electroless Gold Plate over Nickel Plate

Solderprofile:



Tape & Reel (EIA-481-2-A)

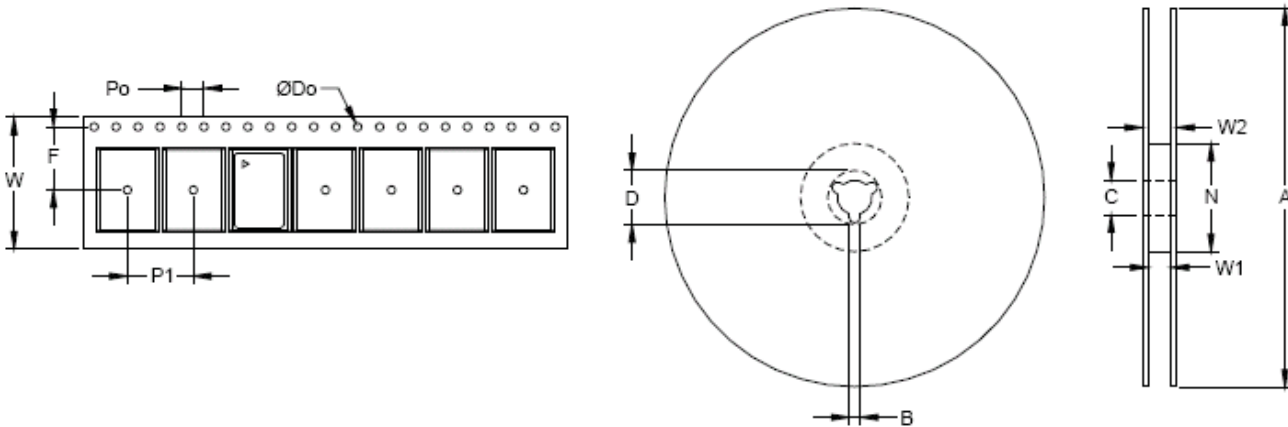


Table 7. Tape and Reel Information

Dimension	Tape Dimensions (mm)					Reel Dimensions (mm)							# Per Reel
	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VX-700	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Table 8. Standard Output Frequencies (MHz)

77.76000	80.00000	81.00000	88.47360	91.08000	92.16000	93.31200	96.00000
100.00000	101.99200	102.40000	106.25000	108.00000	110.00000	112.00000	112.64000
120.00000	122.80000	122.88000	124.41600	125.00000	128.00000	133.33000	134.21770
134.40000	135.00000	138.04860	139.23000	139.26400	139.50000	143.36000	144.00000
148.35160	148.50000	150.00000	153.60000	154.00000	155.52000	156.25000	157.50000
160.00000	161.13280	162.00000	166.62700	166.62860	167.33160	168.04067	175.00000
175.59375	180.00000	184.00000	184.32000	186.66600	187.50000	192.00000	192.45600
200.0000							

Ordering Information

VX-700- E C E - K X A N - xxxMxxxxxx

Product

VCXO, 5x7 Package

Voltage Options

E: +3.3 Vdc ±5%,

Output

C: LVPECL

Temp Range

T: 0/70°C

E: -40/85°C

Absolute Pull Range

K: ±50ppm

Frequency in MHz

Other (Future Use)

N: Standard

Enable/Disable

A: Enable High

C: Enable Low

Stability

X: Standard

E: ±20ppm Temperature Stability

**Note: not all combination of options are available.
Other specifications may be available upon request.*

Example: VX-700-ECE-KXAN-155M520000

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