SONY

CXD2453Q

Timing Generator for LCD Panels

Description

The CXD2453Q is a timing signal generator for driving the LCX017AL and LCX023AL LCD panels. This chip outputs timing signals which support XGA signals (1024 × 768 dots) and S-XGA signals (1280 × 1024 dots).

Features

- Supports various XGA signals (1024 × 768 dots) having horizontal scanning frequencies of 44-69kHz and vertical scanning frequencies of 55 to 85Hz.
- Supports S-XGA (1280 × 1024 dots) pulse eliminator (horizontal scanning frequency of 69kHz or less).
- Controls the sample-and-hold position of the CXA2112R sample-and-hold driver.
- Line inversion and field inversion signal generation
- AC drive of LCD panels during no signal.

Applications

LCD projectors, etc.

Structure

Silicon gate CMOS IC

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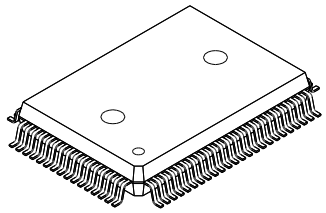
80 pin QFP (Plastic)



Absolute Maximum Ratings (V_{SS} = 0V)

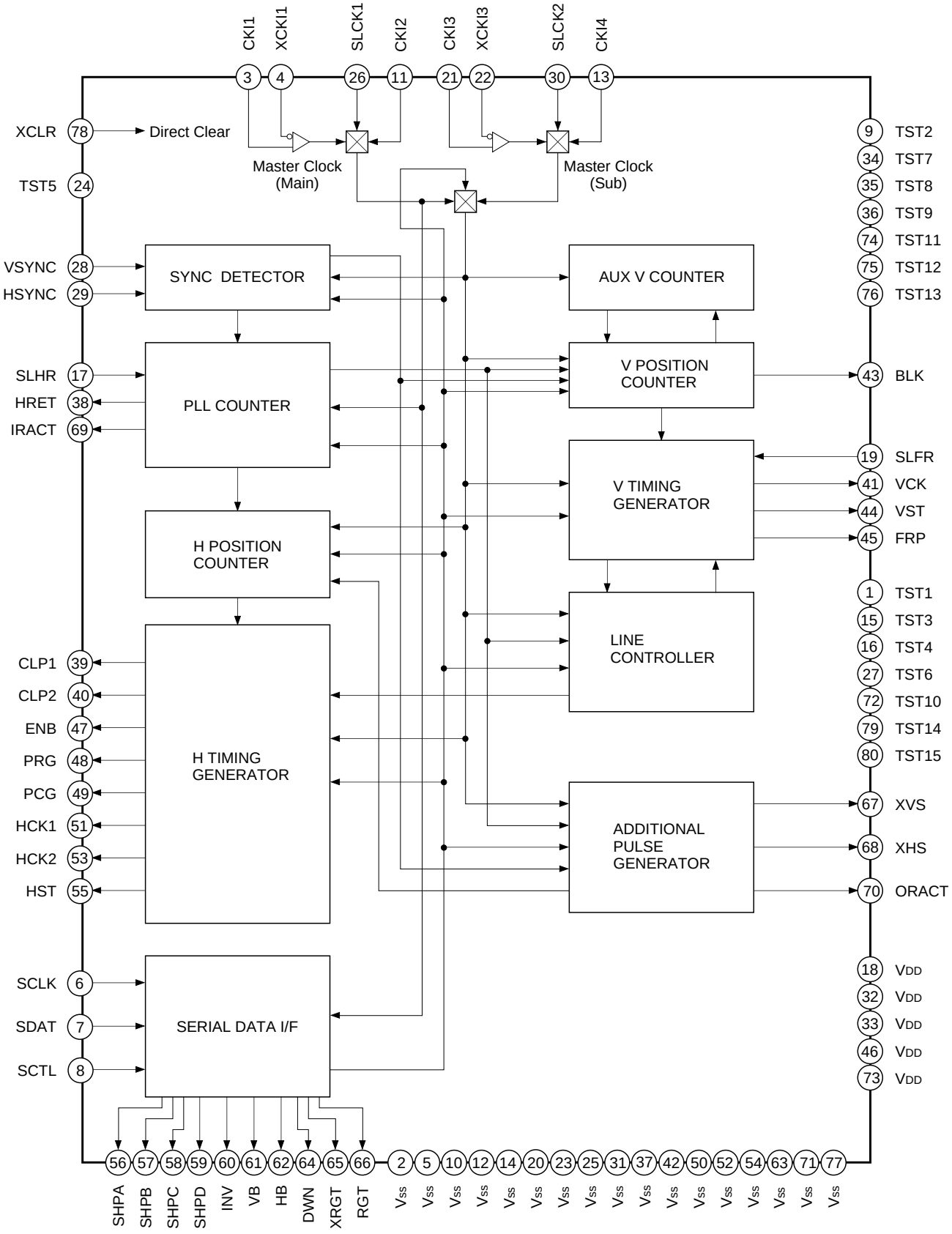
• Supply voltage	V_{DD}	V_{SS} – 0.5 to +4.0	V
• Input voltage	V_I		
(3.3V input pin)		V_{SS} – 0.5 to V_{DD} + 0.5	V
(5.0V input pin)		V_{SS} – 0.5 to V_{DD} + 2.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Storage temperature			
	Tstg	–55 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	+3.0 to +3.6	V
• Operating temperature			
	Topr	–20 to +75	°C

E97425B7Y-PS

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	TST1	—	Test pin (Not connected.)	—
2	V_{SS}	—	GND	—
3	CKI1	I	Master clock input 1 (differential)	—
4	XCKI1			
5	V_{SS}	—	GND	—
6	SCLK	I	Serial data clock input	—
7	SDAT	I	Serial data input	—
8	SCTL	I	Serial data control signal input	—
9	TST2	—	Test pin (connect to GND)	—
10	V_{SS}	—	GND	—
11	CKI2	I	Master clock input 2	—
12	V_{SS}	—	GND	—
13	CKI4	I	Master clock input 4	—
14	V_{SS}	—	GND	—
15	TST3	—	Test pin (Not connected.)	—
16	TST4	—	Test pin (Not connected.)	—
17	SLHR	I	Reset by HSYNC of PLL counter (High: Disabled, Low: Enabled)	H
18	V_{DD}	—	Power supply	—
19	SLFR	I	FRP polarity inversion cycle selection (High: Field inversion, Low: Line inversion)	L
20	V_{SS}	—	GND	—
21	CKI3	I	Master clock input 3 (differential)	—
22	XCKI3			
23	V_{SS}	—	GND	—
24	TST5	—	Test pin (Not connected.)	—
25	V_{SS}	—	GND	—
26	SLCK1	I	Clock input selection 1 (High: CKI2, Low: CKI1)	L
27	TST6	—	Test pin (Not connected.)	—
28	VSYNC	I	Vertical sync signal input	—
29	HSYNC	I	Horizontal sync signal input	—
30	SLCK2	I	Clock input selection 2 (High: CKI4, Low: CKI3)	L
31	V_{SS}	—	GND	—
32	V_{DD}	—	Power supply	—
33	V_{DD}	—	Power supply	—
34	TST7	—	Test pin (connect to V_{DD})	—
35	TST8	—	Test pin (connect to V_{DD})	—
36	TST9	—	Test pin (connect to V_{DD})	—

Pin No.	Symbol	I/O	Description	Input pin for open status
37	V_{SS}	—	GND	—
38	HRET	O	Phase comparison pulse output	—
39	CLP1	O	Pedestal clamp pulse 1 output	—
40	CLP2	O	Pedestal clamp pulse 2 output	—
41	VCK	O	V clock pulse output	—
42	V_{SS}	—	GND	—
43	BLK	O	BLK pulse output	—
44	VST	O	V start pulse output	—
45	FRP	O	AC drive inversion pulse output	—
46	V_{DD}	—	Power supply	—
47	ENB	O	ENB pulse output	—
48	PRG	O	PRG pulse output	—
49	PCG	O	PCG pulse output	—
50	V_{SS}	—	GND	—
51	HCK1	O	H clock 1 pulse output	—
52	V_{SS}	—	GND	—
53	HCK2	O	H clock 2 pulse output	—
54	V_{SS}	—	GND	—
55	HST	O	H start pulse output	—
56	SHPA	O	External sample-and-hold driver control signal output	—
57	SHPB	O	External sample-and-hold driver control signal output	—
58	SHPC	O	External sample-and-hold driver control signal output	—
59	SHPD	O	External sample-and-hold driver control signal output	—
60	INV	O	External sample-and-hold driver control signal output	—
61	VB	O	VB signal output	—
62	HB	O	HB signal output	—
63	V_{SS}	—	GND	—
64	DWN	O	Up/down inversion signal output	—
65	XRGT	O	Left/right inversion signal (reverse polarity) output	—
66	RGT	O	Left/right inversion signal output	—
67	XVS	O	Auxiliary pulse output	—
68	XHS	O	Auxiliary pulse output	—
69	IRACT	O	Auxiliary pulse output	—
70	ORACT	O	Auxiliary pulse output	—
71	V_{SS}	—	GND	—
72	TST10	—	Test pin (Not connected.)	—

Pin No.	Symbol	I/O	Description	Input pin for open status
73	V_{DD}	—	Power supply	—
74	TST11	—	Test pin (connect to V_{DD})	—
75	TST12	—	Test pin (connect to V_{DD})	—
76	TST13	—	Test pin (connect to V_{DD})	—
77	V_{SS}	—	GND	—
78	XCLR	I	System clear (Low: All clear)	H
79	TST14	—	Test pin (Not connected.)	—
80	TST15	—	Test pin (Not connected.)	—

* H: Pull-up, L: Pull-down

Electrical Characteristics

• DC characteristics (Topr = –20 to +75°C, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V_{DD}	—	3.0	3.3	3.6	V	—
Input voltage 1	$V_{IH}1$	3.3V CMOS input	0.65V_{DD}	—	V_{DD}		SLHR, SLFR, XCLR, SLCK1/2
	$V_{IL}1$		V_{SS}	—	0.25V_{DD}		
Input voltage 2	$V_{IH}2$	5.0V CMOS input	0.65V_{DD}	—	V_{DD} + 1.9		CKI2, CKI4
	$V_{IL}2$		V_{SS}	—	0.25V_{DD}		
Input voltage 3	$V_{IH}3$	5.0V CMOS Schmitt trigger input	0.8V_{DD}	—	V_{DD} + 1.9		SCLK, SDAT, SCTL, VSYNC, HSYNC
	$V_{IL}3$		V_{SS}	—	0.2V_{DD}		
Input voltage 4	V_C (center level)	Low amplitude differential input	(V_{DD} × 0.606) – 0.1	V_{DD} × 0.606	(V_{DD} × 0.606) + 0.1		CKI1/XCKI1, CKI3/XCKI3
	$V_{IH}4$*1		$V_{IL}4$ + 0.3	—	V_{DD}		
	$V_{IL}4$*1		V_{SS}	—	$V_{IH}4$ – 0.3		
Output voltage 1	V_{OH}	I_{OH} = –4mA	V_{DD} – 0.5	—	V_{DD}		*2
	V_{OL}	I_{OL} = 4mA	V_{SS}	—	0.4		
Output voltage 2	V_{OH}	I_{OH} = –8mA	V_{DD} – 0.5	—	V_{DD}		VCK, BLK, VST, ENB, PCG
	V_{OL}	I_{OL} = 8mA	V_{SS}	—	0.4		
Output voltage 3	V_{OH}	I_{OH} = –12mA	V_{DD} – 0.5	—	V_{DD}		HCK1, HCK2, HST
	V_{OL}	I_{OL} = 12mA	V_{SS}	—	0.4		
Input pull-up/pull-down resistance	R_P	Pull-up V_I = 0V	25	50	200	kΩ	SLHR, XCLR
		Pull-down V_I = V_{DD}					SLFR, SLCK1/2
Current consumption	I_{DD}	Master clock = 95MHz V_{DD} = 3.3V Output load = 30pF	—	—	40	mA	—

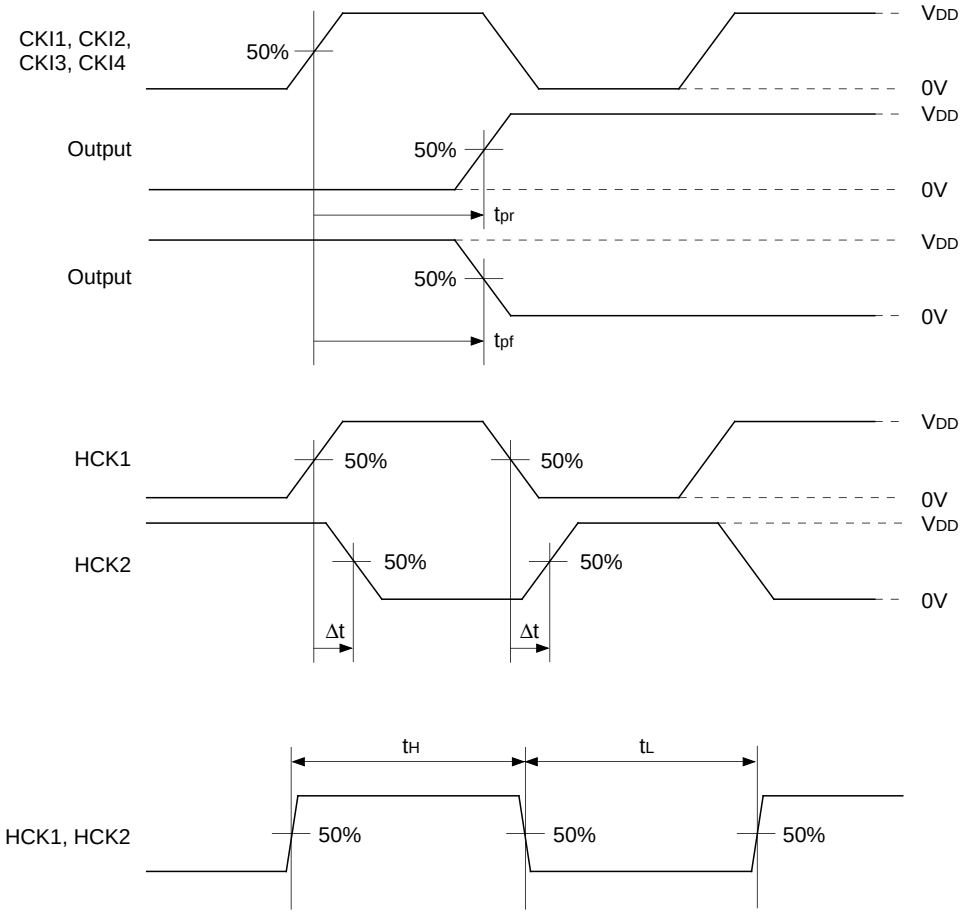
*1 $V_{IH}4$ > (max. value of V_C) and $V_{IL}4$ < (min. value of V_C)

*2 Output pins other than those indicated in items output voltage 2 and output voltage 3.

• **AC characteristics** (Topr = –20 to +75°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	—	CKI1/XCKI1, CKI3/XCKI3	—	10.5	—	—	ns
		CKI2, CKI4	—	10.5	—	—	
Output rise/fall delay time	tpr/tpf	HCK1, HCK2, HST	C_L = 90pF	—	—	25	
Output rise/fall delay time	tpr/tpf	VCK, BLK, VST, ENB, PCG	C_L = 50pF				
Output rise/fall delay time	tpr/tpf	Other output pins	C_L = 30pF				
Cross-point time difference	Δt	HCK1, HCK2	C_L = 90pF	–5	—	5	
Duty ratio	$t_H/(t_H + t_L)$	HCK1, HCK2	C_L = 90pF	48	50	52	%

Timing Definitions

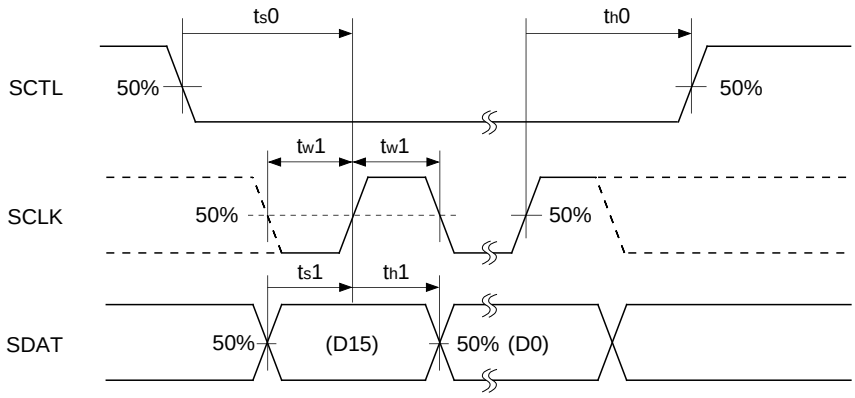


Serial Interface AC Characteristics (Topr = –20 to +75°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Item	Symbol	Min.	Typ.	Max.
SCTL setup time with respect to rise of SCLK	ts0	8T*3	—	—
SCTL hold time with respect to rise of SCLK	th0	8T	—	—
SDAT setup time with respect to rise of SCLK	ts1	4T	—	—
SDAT hold time with respect to rise of SCLK	th1	4T	—	—
SCLK pulse width	tw1	4T	—	—

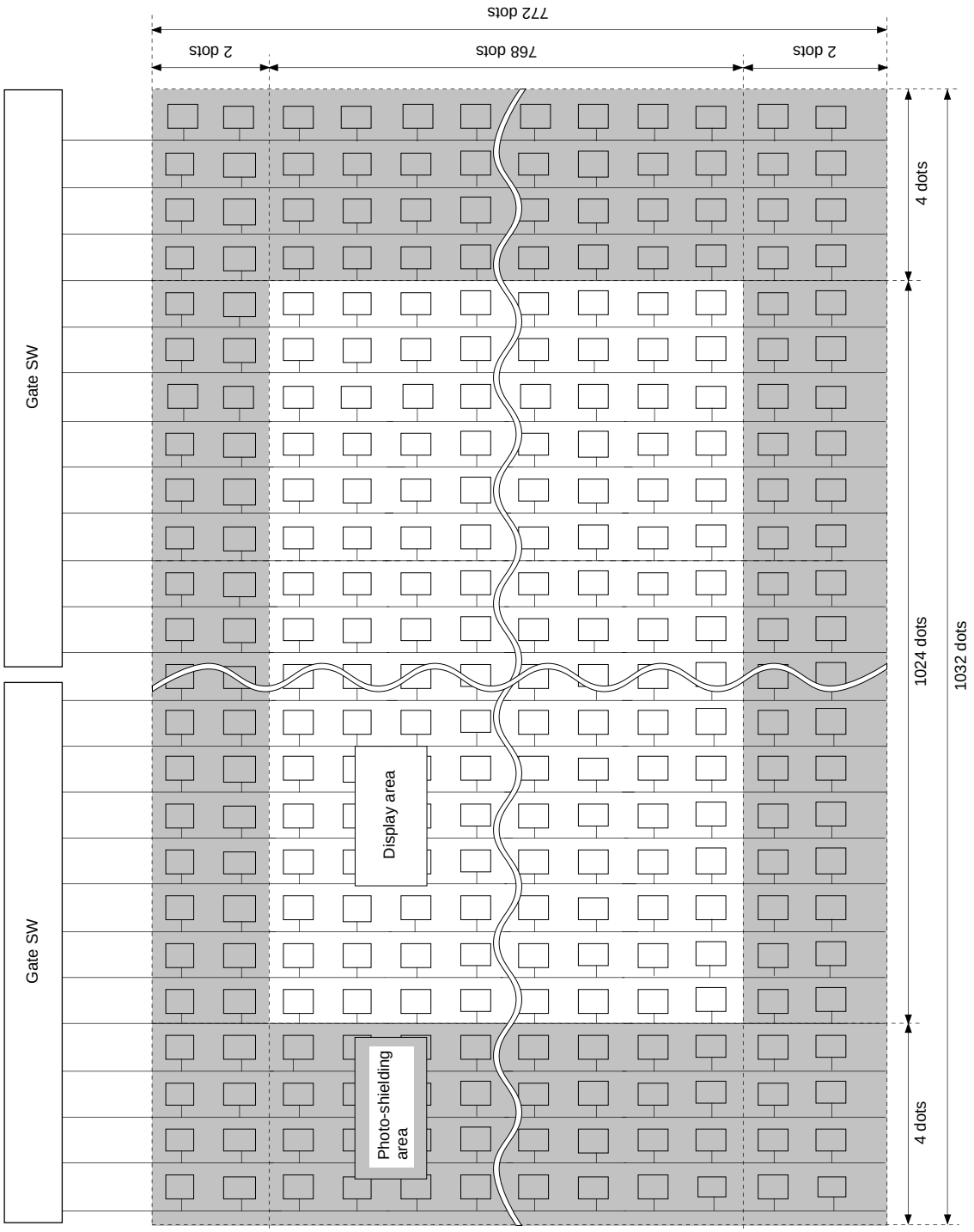
*3 T: Master clock cycle (ns)

Timing Definitions



LCD Panel Dot Arrangement

The dot arrangement of the LCD panel (LCX017AL) driven with this IC is shown below. The dot arrangement is a square arrangement. The shaded region in the diagram is not displayed.



Description of Operation

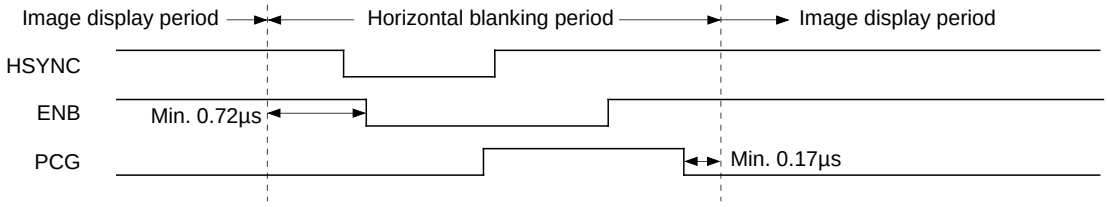
• Sync signal input pins (HSYNC, VSYNC)

Horizontal and vertical separate SYNC signals are input to the HSYNC (Pin 29) and VSYNC (Pin 28). The sync signals are compatible with both positive and negative polarity according to serial data settings. (Refer to the section on serial data interface for details regarding serial data.)

The CXD2453Q supports signals which are shown in the following table.

Effective dots	Horizontal scanning frequency	Vertical scanning frequency	Remarks
1024 × 768 (XGA)	44kHz to 69kHz	55Hz to 85Hz	
1280 × 1024 (S-XGA)	≤ 69kHz	Roughly ≤ 65Hz	Scanning line conversion from 1024 to 768 vertical lines

In the case of signals defined by special protocols that do not satisfy the conditions in the diagram below, it may not be possible to obtain a complete display even for the above signals when the image display position is properly set on the LCD panel. This IC does not support interlace signals.



• Master clock input pins (CKI1/XCKI1, CKI2, CKI3/XCKI3, CKI4) and Clock Selection Pins (SLCK1, SLCK2)

Since this IC does not contain a built-in phase comparator, phase comparison is performed externally and a divided clock is input. The 1/N (N is the clock number during 1 horizontal period) frequency divider output is output from the HRET (Pin 38) for the external phase comparator.

The clock input pin consists of two channels for small amplitude differential input (center level: 2.0V, amplitude: ±0.4V), and two channels for CMOS level input for a total of four channels. These are selected according to the SLCK1 (Pin 26), SLCK2 (Pin 30) and serial data.

(1) During normal operation (serial data SLLAP = 0)
All internal circuits of the IC operate with CKI1 or CKI2. CKI1/XCKI1 are selected when SLCK1 = L (Pins 3/4, small amplitude differential input), and CKI2 is selected when SLCK1 = H (Pin 11, CMOS level input).

(2) When using scan converter (serial data SLLAP = 1)
This is used when the input signal clock and output signal clock are different such as when performing dot conversion using a scan converter. Only the serial data interface and PLL counter of the IC internal circuits operate with CKI1 or CKI2 (clock synchronized with input signal). All other blocks operate with CKI3 or CKI4 (output signal clock). CKI3/XCKI13 are selected when SLCK2 = L (Pins 21/22, small amplitude differential input), and CKI4 is selected when SLCK2 = H (Pin 13, CMOS level input).

• Internal frequency divider reset selection pin (SLHR)

This selects whether reset of the PLL counter (loop counter) with HSYNC is to be enabled or disabled. In the case of performing phase comparison of the HSYNC and HRET pulses with an external phase comparator, the SLHR (Pin 17) is set to H (reset disabled). When phase comparison and frequency division are performed externally and HRET pulses for phase comparison are not used, the SLHR is set to L (reset enabled). At this time, the output of each pulse is delayed by approximately 8 clocks as compared with using HRET pulses for phase comparison.

• Signal inversion type selection pin (SLFR)

This selects the inversion cycle of the polarity inversion pulse (FRP pulse) for AC driving. Setting the SLFR (Pin 19) to H results in field inversion, while setting the SLFR to L results in line inversion.

• System clear pin (XCLR)

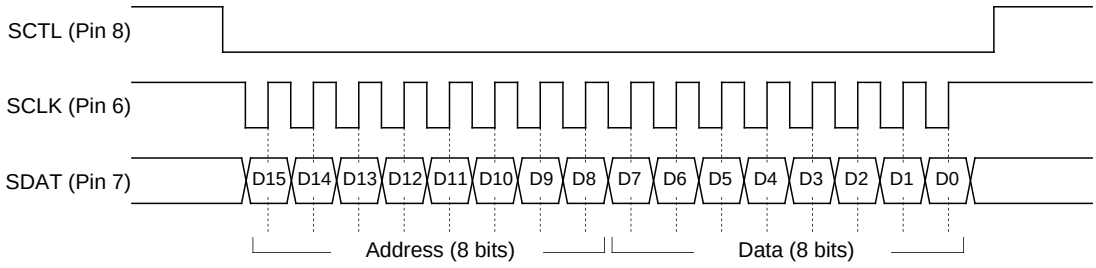
All internal circuits are initialized when the XCLR (Pin 78) is L. Always make sure to initialize all internal circuits when the power has been turned on.

• Serial data interface

Operating mode and other settings in this IC are performed by serial data. When the power is turned on, all data are set to the default values when the internal circuits are initialized. When the power supply is turned on, the value of SDAT is read with the rise of SCLK in groups of 16 bits consisting of 8 address bits and 8 data bits as shown in the Timing Chart below. The data that has been read is enabled by being transferred to the register corresponding to each address 10 clocks after the rise of SCLK of the 16th bit.

The Timing Chart and Data Format during transmission of serial data are as shown below.

Timing Chart



Data Format

Address	Data								Settings
D15 to D8	D7	D6	D5	D4	D3	D2	D1	D0	
F0	—	—	—	—	—	PLP10	PLP9	PLP8	PLL counter frequency division ratio
F1	PLP7	PLP6	PLP5	PLP4	PLP3	PLP2	PLP1	PLP0	
F2	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Screen horizontal position
F3	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Screen vertical position
F4	—	—	—	INV	SHP3	SHP2	SHP1	SHP0	CXA2112R S/H control
F5	—	—	VPOL	HPOL	VSCN	HSCN	SLXG	SLSX	Operating mode, etc.
F6	—	—	HB	VB	SLLAP	IRD10	IRD9	IRD8	Operating mode, etc./ IRACT fall position
F7	IRD7	IRD6	IRD5	IRD4	IRD3	IRD2	IRD1	IRD0	
F8	—	—	—	—	—	IRU10	IRU9	IRU8	IRACT rise position
F9	IRU7	IRU6	IRU5	IRU4	IRU3	IRU2	IRU1	IRU0	
FA	—	—	—	ORRS1	ORRS0	ORP10	ORP9	ORP8	ORACT reset cycle/ ORACT division frequency
FB	ORP7	ORP6	ORP5	ORP4	ORP3	ORP2	ORP1	ORP0	
FC	—	—	—	—	—	ORD10	ORD9	ORD8	ORACT fall position
FD	ORD7	ORD6	ORD5	ORD4	ORD3	ORD2	ORD1	ORD0	
FE	—	—	—	—	—	ORU10	ORU9	ORU8	ORACT rise position
FF	ORU7	ORU6	ORU5	ORU4	ORU3	ORU2	ORU1	ORU0	

Note) —: Don't care

The following provides a detailed description of each setting.

(a) Setting of PLL counter frequency division ratio

This is used to set the frequency division ratio of the 1/N frequency divider (PLL counter) for phase comparison. The value of (total number of dots of 1 horizontal period N) – 1 is set with PLP10 (MSB) through PLP0 (LSB). The frequency division ratio can be set up to 2048. Only even numbers can be set for the value of N. When it is necessary to set an odd number, use an external frequency divider. In this case, set the value of the frequency division ratio of the PLL counter to N-2.
The default value is 10100111111 (N = 1344).

(b) Setting of screen horizontal position

The horizontal display start position is set with HP7 (MSB) through HP0 (LSB). This setting enables the phase relationships of pulses HST, HCK1/2, ENB, PCG, PRG and CLP1/2 as well as the changing positions of VCK/FRP relative to HSYNC to change in an interlocked manner. Settings can be made in 1 dot units. Refer to the Timing Chart for the relationship between the set value and each pulse position.
The default value is 01000100.

(c) Setting of screen vertical position

The vertical display start position is set with VP7 (MSB) through VP0 (LSB). This setting enables the phase relationships of signals VST, VCK and FRP to change relative to VSYNC in an interlocked manner. Settings can be made in 1 line units. Refer to the Timing Chart for the relationship between the set value and each signal.
The default value is 00100011. 00000000 and 11111111 are not used.

(d) S/H control of CXA2112R

This is used to set the sample-and-hold position for the CXA2112R (sample-and-hold driver). INV setting data is output directly from the INV (Pin 60). Setting data of SHP3 (MSB) through SHP0 (LSB) is reflected as shown below in the SHPA through SHPD (Pins 56 to 59). Refer to the specifications of the CXA2112R for details.

Setting data	Output				Setting data	Output			
SHP3 to SHP0	SHPA	SHPB	SHPC	SHPD	SHP3 to SHP0	SHPA	SHPB	SHPC	SHPD
0000	L	L	L	L	1000	L	L	Z	L
0001	H	H	L	L	1001	H	H	Z	L
0010	Z	L	L	L	1010	Z	L	Z	L
0011	Z	H	L	L	1011	Z	H	Z	L
0100	L	L	H	H	1100	L	L	Z	H
0101	H	H	H	H	1101	H	H	Z	H
0110	Z	L	H	H	1110	Z	L	Z	H
0111	Z	H	H	H	1111	Z	H	Z	H

Note) Z: High impedance state

(e) Setting of operating mode, etc.

• VPOL, HPOL: These are used to set the polarity of VSYNC and HSYNC. A setting of "1" denotes positive polarity, while a setting of "0" denotes negative polarity.
The default values are VPOL = 0, HPOL = 0.

• VSCN, HSCN: These are used to set the vertical and horizontal scanning directions of the LCD panel. VSCN = 1 denotes downward scanning, while VSCN = 0 denotes upward scanning. HSCN = 1 denotes rightward scanning, while HSCN = 0 denotes leftward scanning. Setting data of VSCN is output from the DWN (Pin 64), while setting data of HSCN is output from the RGT (Pin 66).
The default values are VSCN = 0, HSCN = 1.

• SLXG, SLSX: These are used to set the input signals (operating mode). This IC has the following three operating modes.
The default values are SLXG = 0, SLSX = 0.

Operating mode	SLXG	SLSX
XGA-I	0	0
XGA-II	1	0
S-XGA	X	1

Note) X: Don't care

The XGA-I mode supports typical XGA signals. The XGA-II mode is for XGA signals in which there is a low number of dots during a portion of the horizontal blanking period (typically when HSYNC + back porch is 240 dots or less). Select the appropriate operating mode to satisfy the conditions in the diagram on page 6 corresponding to the input signal. In the S-XGA mode, 1024 vertical lines are displayed decimating to 768 lines corresponding to the S-XGA signal (1280 × 1024 dots).

• HB, VB: These are used to switch the number of display dots on the LCD panel. The display is set to 960 dots horizontally when HB = 0, and to 640 lines vertically when VB = 0. The data of each setting is output from the HB (Pin 62) and VB (Pin 61), respectively. Refer to the specifications of the LCX017AL for details.
The default values are HB = 1, VB = 1.

• SLLAP: This is used when the input signal clock and output signal clock differ such as when converting the number of dots using a scan converter. When SLLAP = 1, only the serial data interface and PLL counter of the IC internal circuits operate with CKI1 or CKI2 (clock synchronized with input signal), while other sections operated with CKI3 or CKI4 (output signal clock). When SLLAP = 0, all internal IC circuits operate with CKI1 or CKI2.
The default value is 0.

(f) Setting of IRACT fall/rise positions

• IRACT pulse

A pulse synchronized with HSYNC of the input signal can be output at any position and width. The fall position of the pulse is set with IRD10 (MSB) through IRD0 (LSB), while the rise position is set with IRU10 (MSB) through IRU0 (LSB). The values of IRD0 and IRU0 are ignored, and settings are made in 2-dot increments. The setting range is from "0" to (N – 2). The same value cannot be set for IRD and IRU. Refer to the Timing Chart for the relationship between setting values and pulse positions.

The default values are IRD10 through IRD0 = 00000000000, and IRU10 through IRU0 = 00010000000.

(g) Setting of ORACT reset cycle/ORACT frequency division ratio

• ORACT pulses

ORACT pulses are completely identical to IRACT pulses when serial data SLLAP = 0, when SLLAP = 1, they are generated by a dedicated counter (loop counter similar to the PLL counter) that operates according to an independent clock (CKI3 or CKI4) different from the clock synchronized with input signal HSYNC (CKI1 or CKI2). Since pulses for driving the LCD panel are also generated based on this counter at this time, the LCD panel can be driven based on a clock and cycle that are different from the input signal. ORACT pulses are synchronized with the cycle of the pulse for driving the LCD panel at this time, and can be output at any position and width.

The frequency division ratio of the above dedicated counter is set with ORP10 (MSB) through ORP0 (LSB). The value of (number of counter counts M) – 1 is the actual setting value. Only even numbers can be set for M, and settings are made in 2 dot increments. The maximum setting is 2048 counts. This counter is reset with VSYNC and HSYNC of a fixed cycle in order to synchronize it with the input signal, the interval of H at which it is to be reset with this HSYNC is set with ORRS1 and ORRS0.

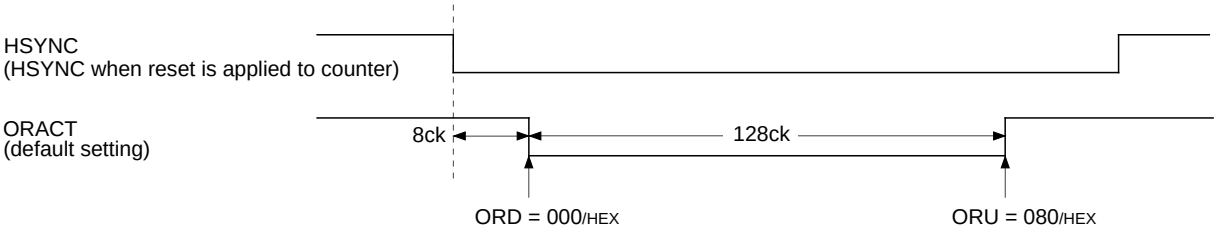
Setting data (ORRS1/ORRS0)	00	01	10	11
Reset cycle	Every 3H	Every 4H	Every 5H	Every 1H

The default values are ORRS1 = 1, ORRS0 = 1, and ORP10 through ORP0 = 10100111111.

(h) Setting of ORACT fall/rise positions

The fall position of the ORACT pulse is set with ORD10 (MSB) through ORD0 (LSB), while the rise position of the ORACT pulse is similarly set with ORU10 (MSB) through ORU0 (LSB). The values of ORD0 and ORU0 are ignored, and settings are made in 2-dot increments. The setting range is from "0" to (M – 2). The same value cannot be set for ORD and ORU. The relationship between setting values and pulse positions is as indicated below.

The default values are ORD10 through ORD0 = 00000000000, and ORU10 through ORU0 = 00010000000.



• XHS pulse and XVS pulse

The XHS pulse is output over a width of 32 clocks 34 clocks after the fall of the IRACT pulse when SLLAP = 0. The pulse has negative polarity. When SLLAP = 1, the pulse is similarly output over a width of 34 clocks after the fall of the ORACT pulse.

The XVS pulse is VSYNC latched with the XHS pulse. Its polarity is always negative regardless of the polarity of the input VSYNC.

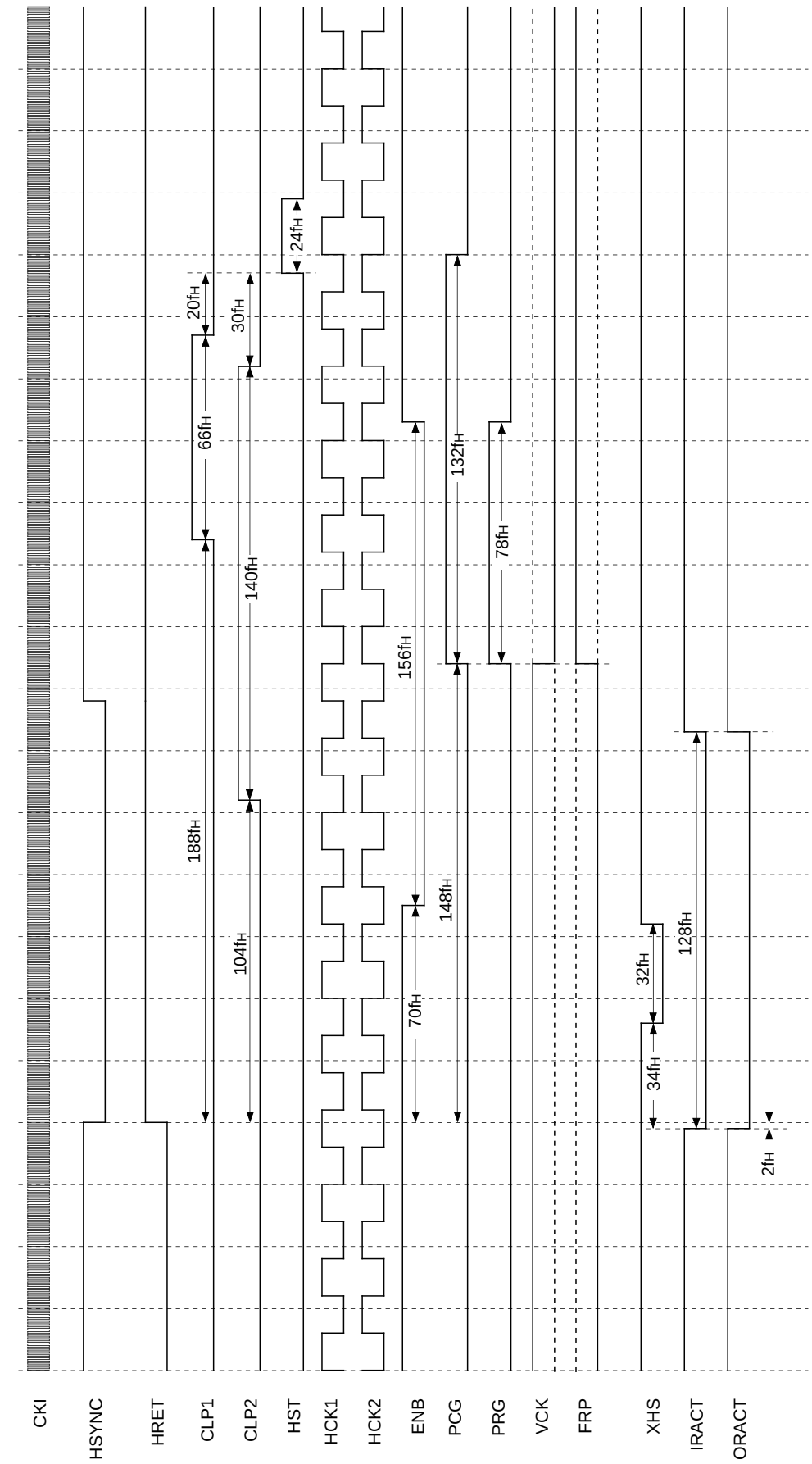
• AC driving of LCD panels for no signal

When VSYNC has not been input for a specified period, a judgment of "no signal" is made to allow AC driving of LCD panels even when there is no signal. A vertical start pulse and polarity inverted pulse (FRP) are output at a specified cycle. The timing by which a judgment of "no signal" is made and the free running cycle are as indicated below.

Operating mode	Free running detection timing (no signal period) and VST cycle during free running
All modes	1600H

Horizontal Direction Timing Chart (XGA-I (1024 × 768 dots))

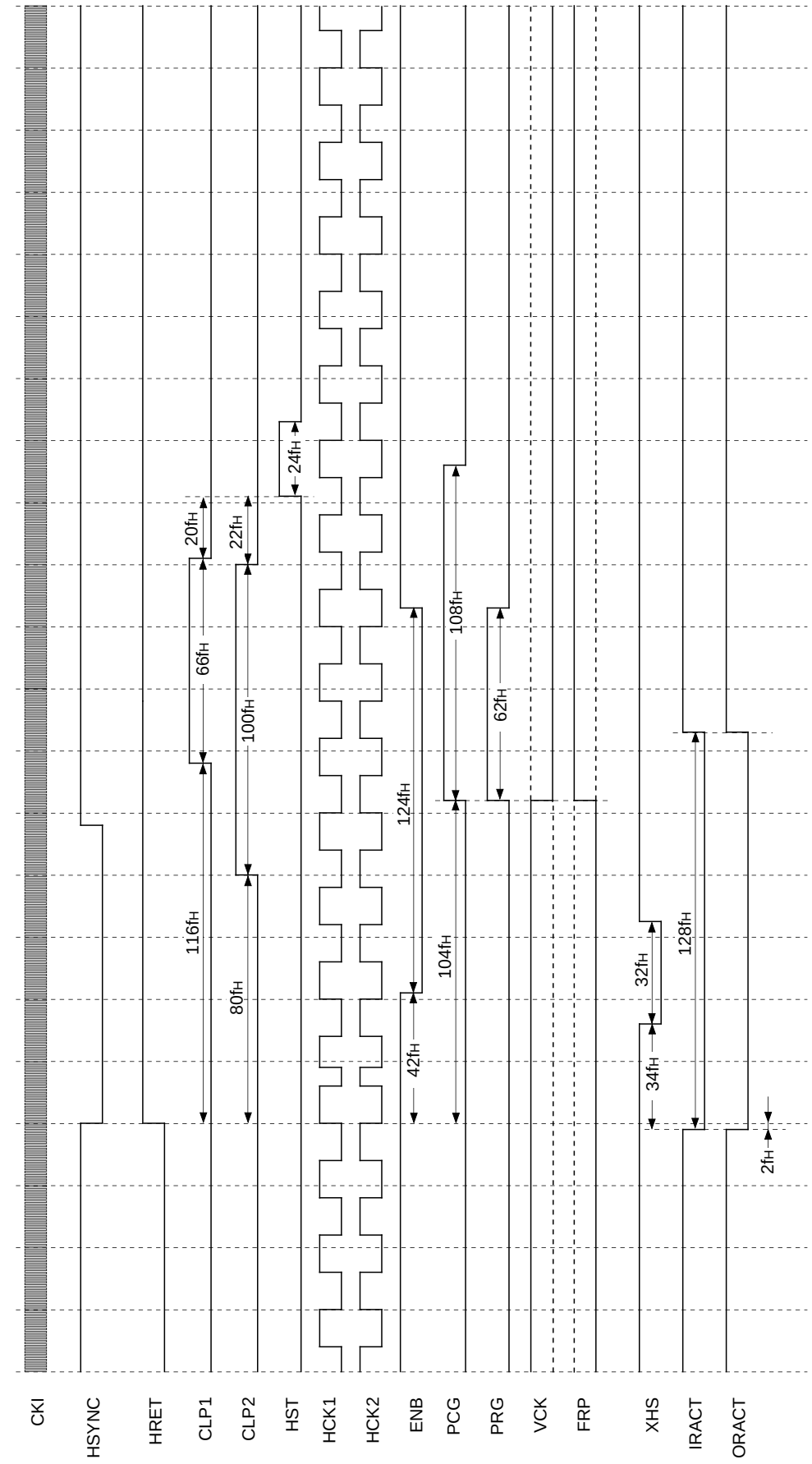
PLP = 53F/HEX, HP = 44/HEX, HPOL = 0, HSCN = 1,
SLXG = 0, SLSX = 0, IRD = 000/HEX, IRU = 080/HEX
SLHR: H, SLFR: L



Note) The phases of HCK1 and HCK2 are respectively reversed when HSCN = 0 (left/right inversion).
The polarity of 1H and 1V cycle of FRP is not defined.

Horizontal Direction Timing Chart (XGA-II (1024 × 768 dots))

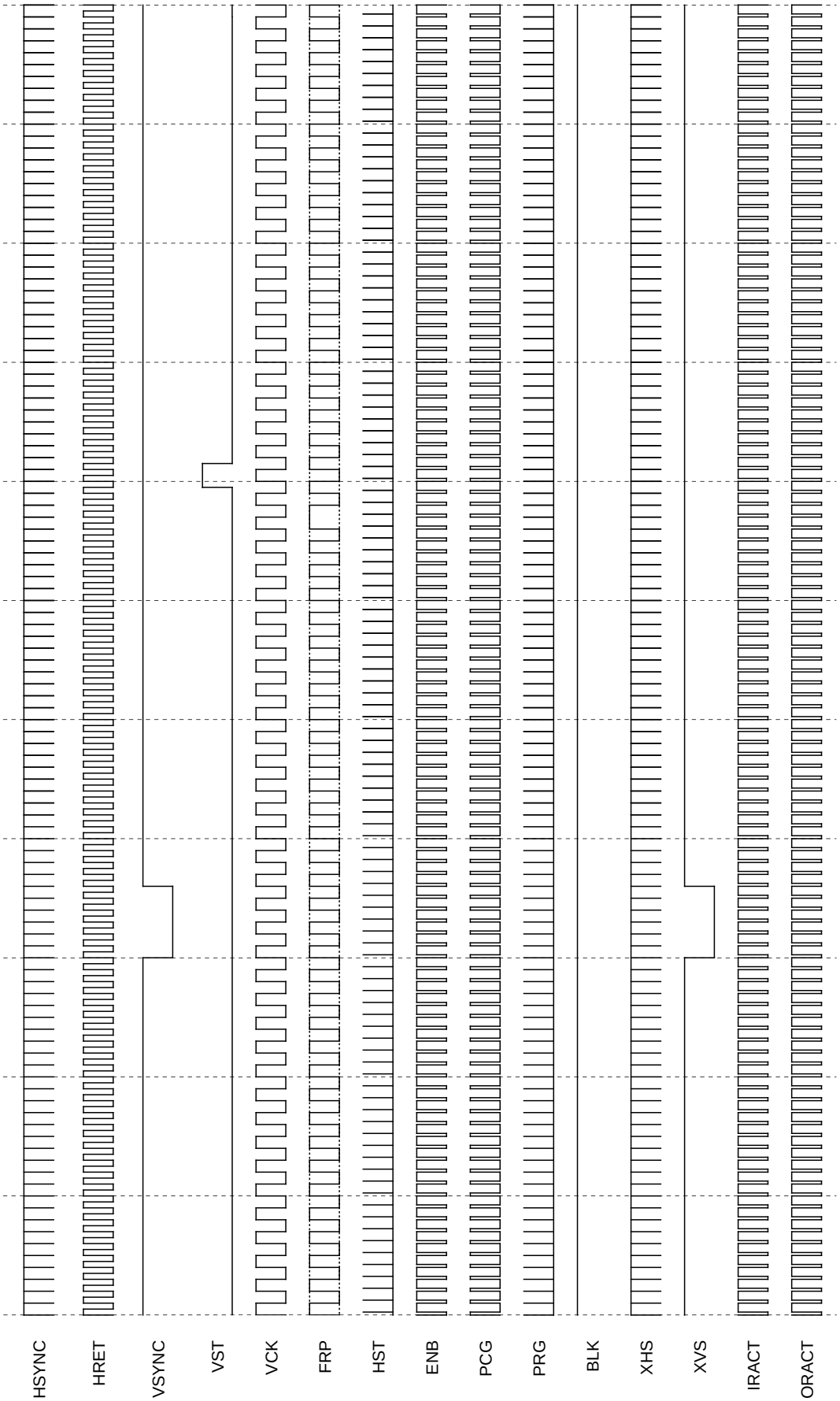
PLP = 51F/HEX, HP = 14/HEX, HPOL = 0, HSCN = 1,
SLXG = 1, SLSX = 0, IRD = 000/HEX, IRU = 080/HEX
SLHR: H, SLFR: L



Note) The phases of HCK1 and HCK2 are respectively reversed when HSCN = 0 (left/right inversion).
The polarity of 1H and 1V cycle of FRP is not defined.

Vertical Direction Timing Chart (XGA-I/II (1024 × 768 dots))

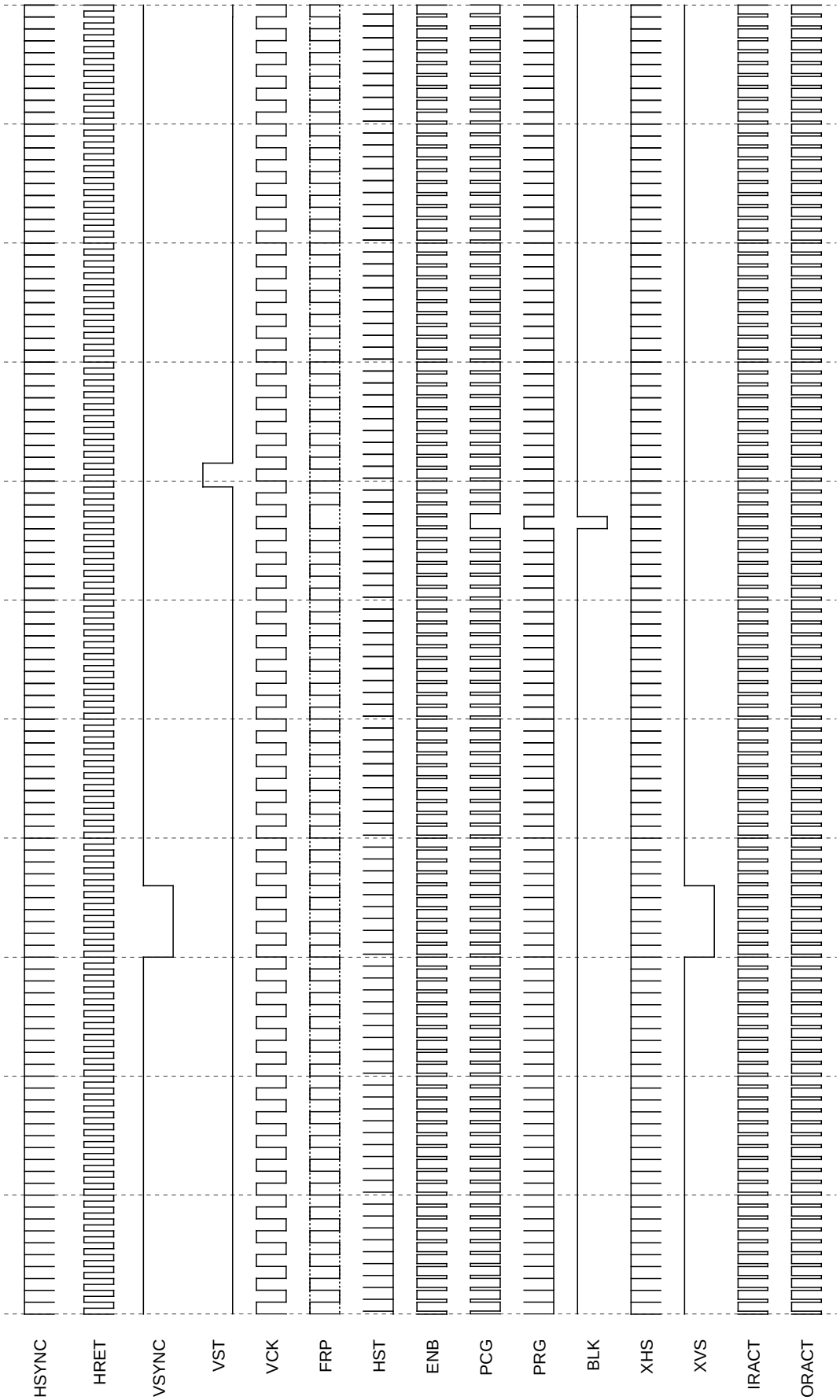
VP = 23HEX, VPOL = 0, SLSX = 0,
IRD = 000HEX, IRU = 080HEX, SLFR: L



Note) The polarity of 1H and 1V cycle of FRP is not defined.

Vertical Direction Timing Chart (XGA-I/II (during display of 640 vertical lines))

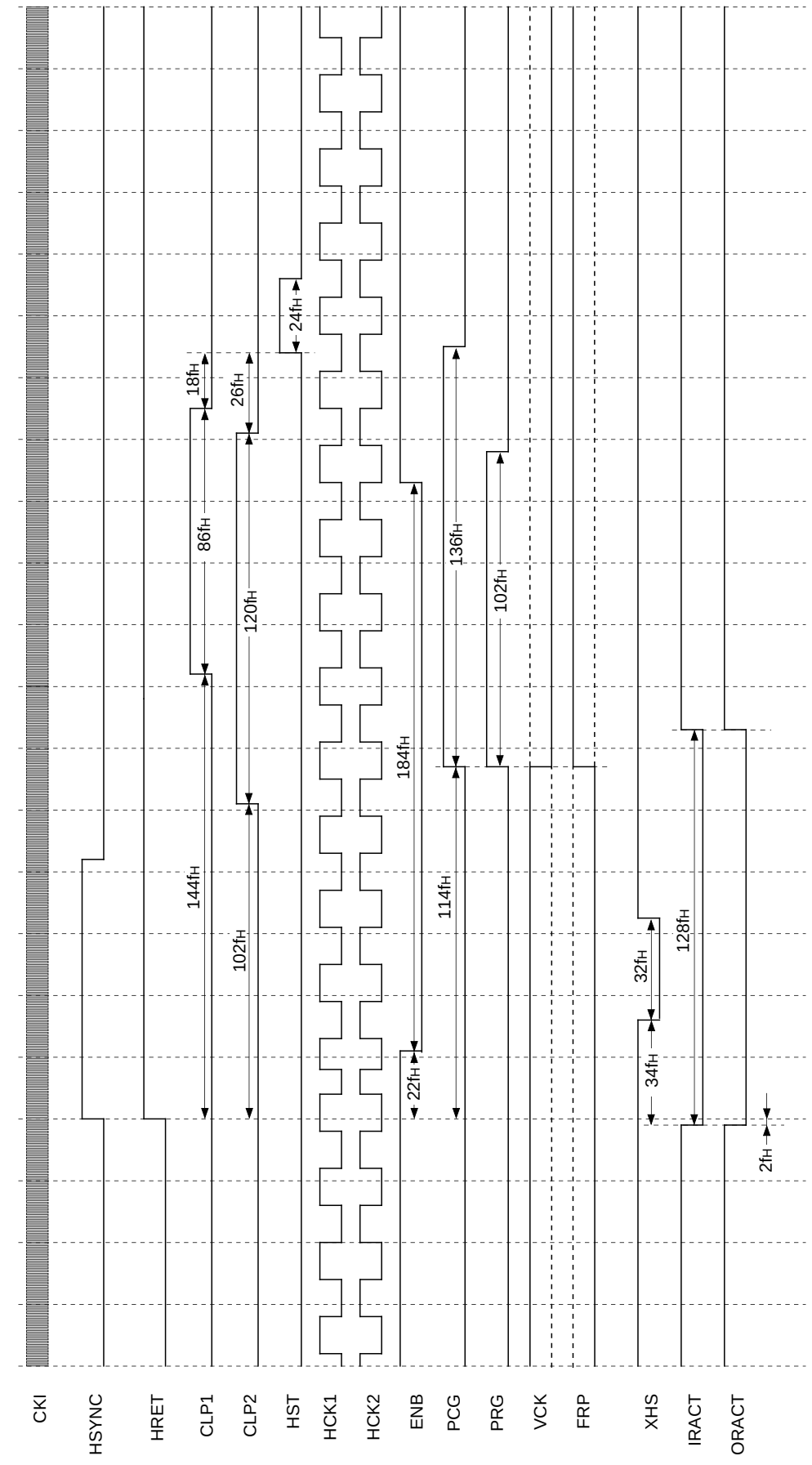
VP = 23HEX, VPOL = 0, SLSX = 0, VB = 0,
IRD = 000HEX, IRU = 080HEX, SLFR: L



Note) The polarity of 1H and 1V cycle of FRP is not defined.

Horizontal Direction Timing Chart (S-XGA (1280 × 1024 dots displayed on 960 × 768 dots))

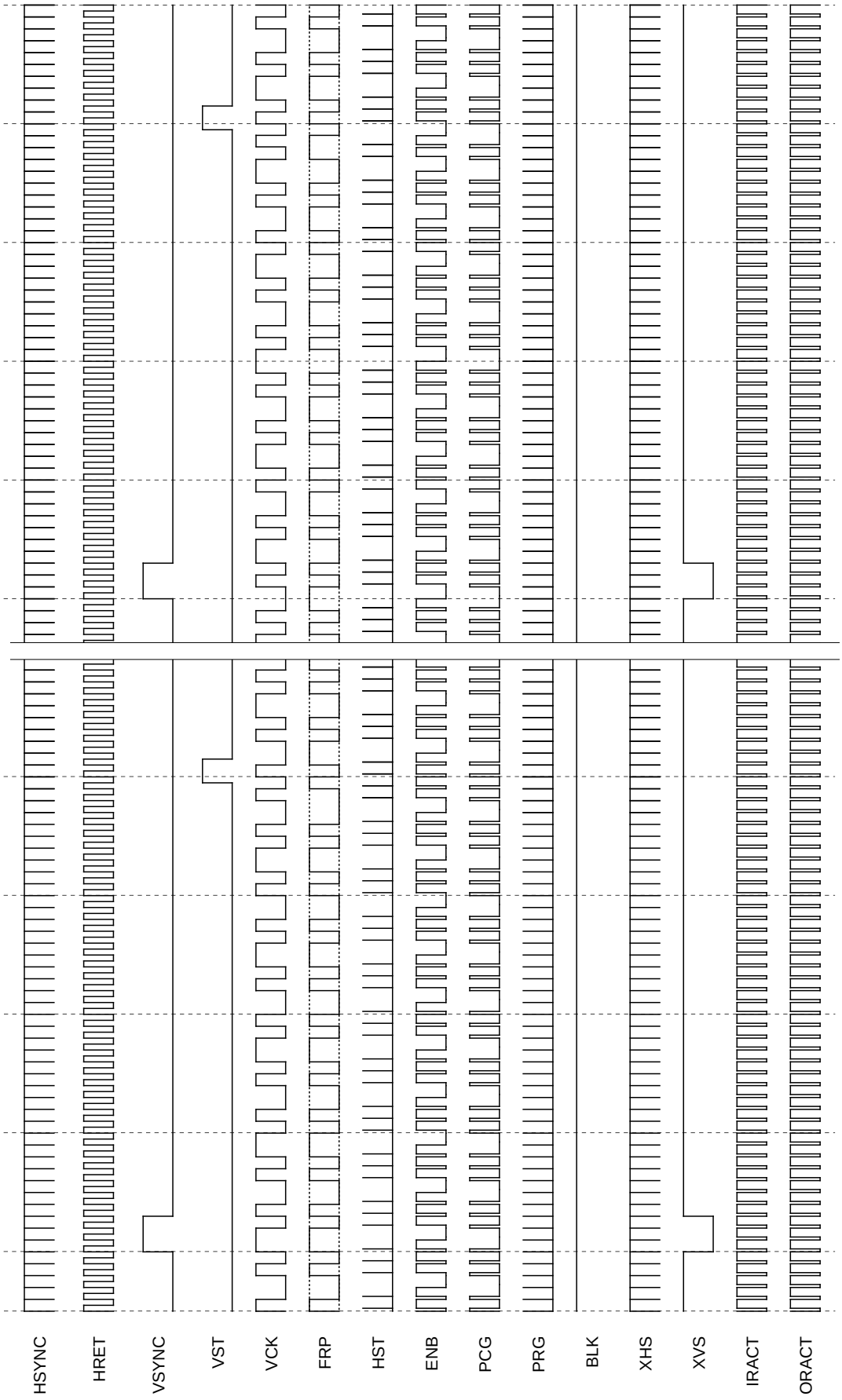
PLP = 4F1/HEX, HP = 12/HEX, HPOL = 1, HSCN = 1,
SLSX = 1, IRD = 000/HEX, IRU = 080/HEX
SLHR: H, SLFR: L



Note) The phases of HCK1 and HCK2 are respectively reversed when HSCN = 0 (left/right inversion).
The polarity of 1H and 1V cycle of FRP is not defined.

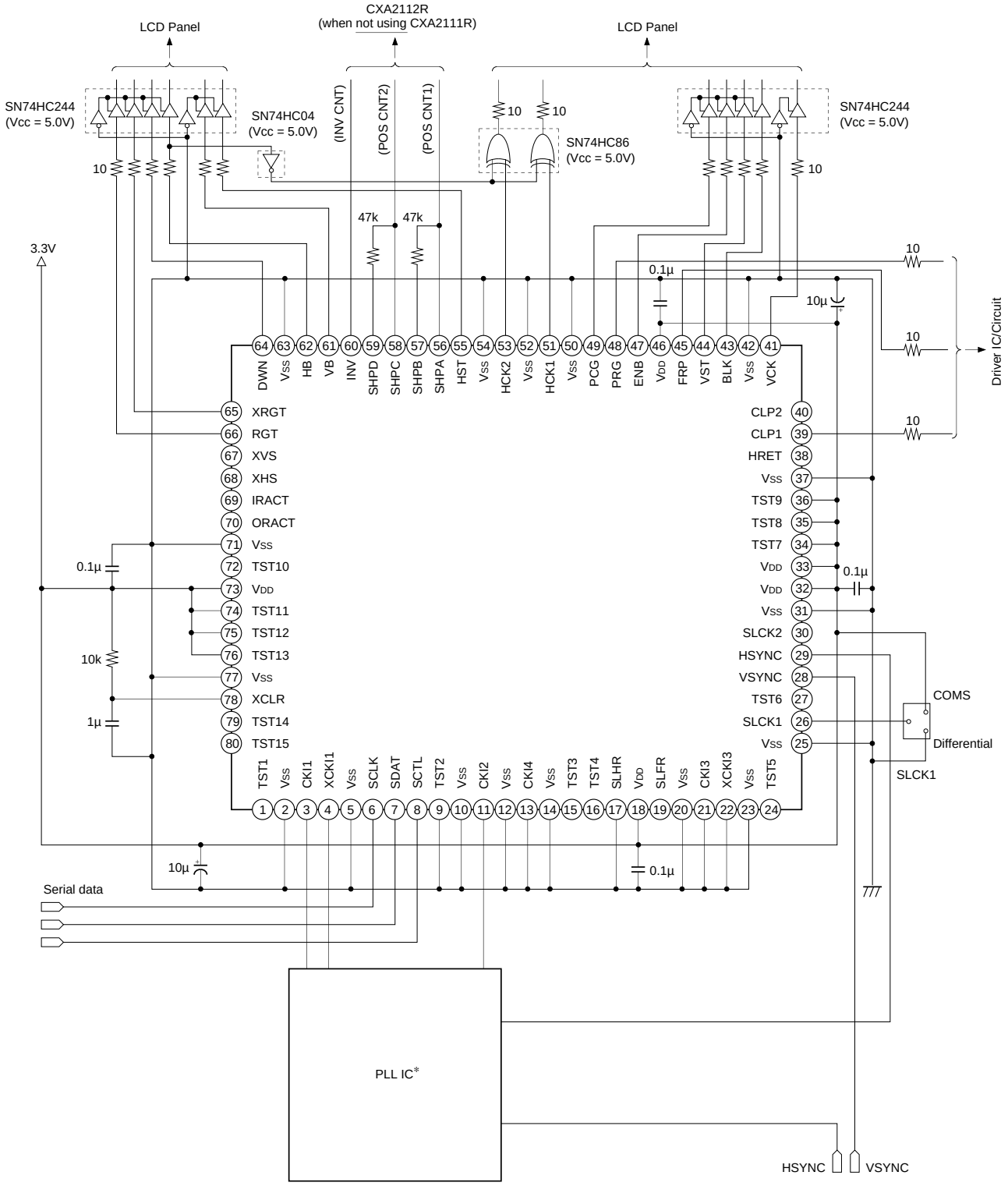
Vertical Direction Timing Chart (S-XGA (1280 × 1024 dots displayed on 960 × 768 dots))

VP = 24HEX, VPOL = 1, SLSX = 1, IRD = 000HEX,
IRU = 080HEX, SLFR: L



Note) The polarity of 1H and 1V cycle of FRP is not defined.

Application Circuit

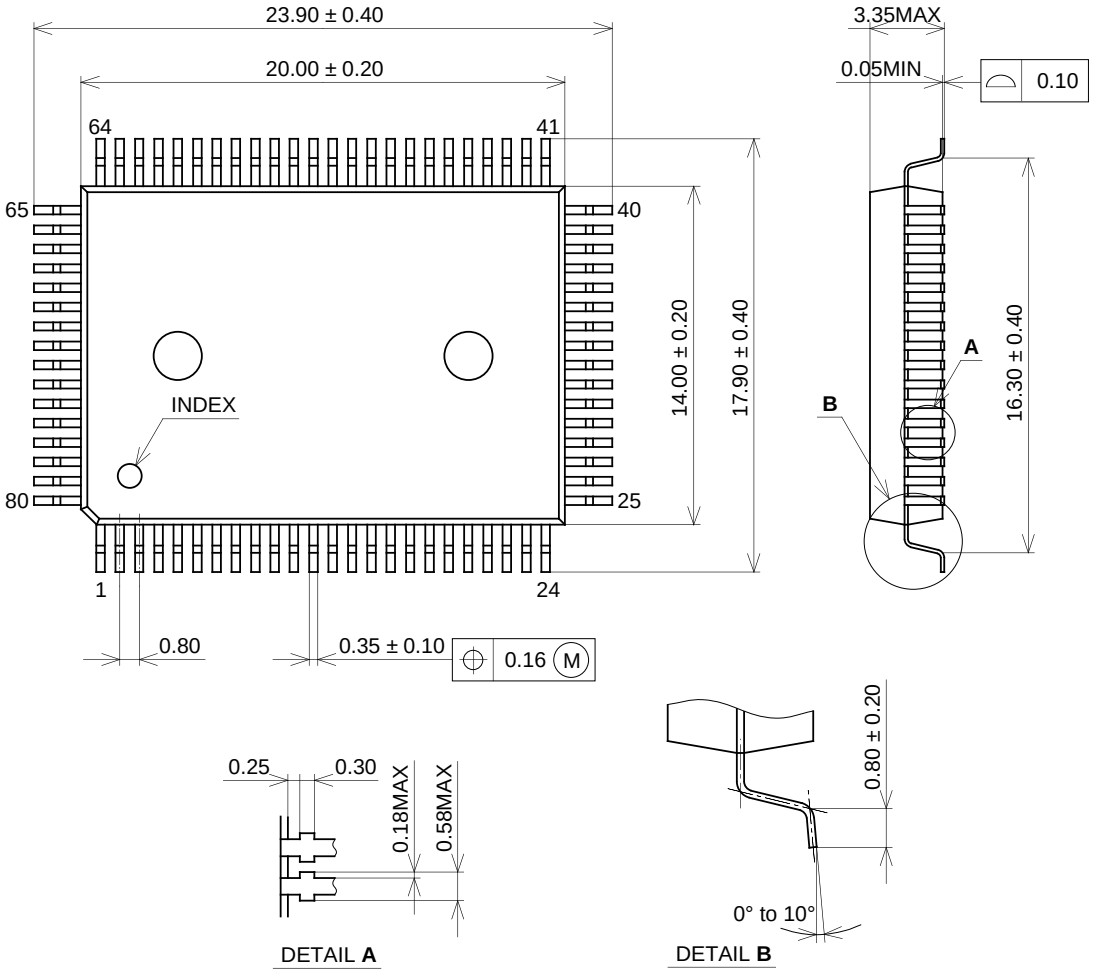


* PLL IC: Sony CXA3106Q (built-in phase comparator and frequency divider) is recommended.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN QFP(PLASTIC)



SONY CODE	QFP-80P-L022
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.7g