

## 64K (8K x 8) CMOS EEPROM

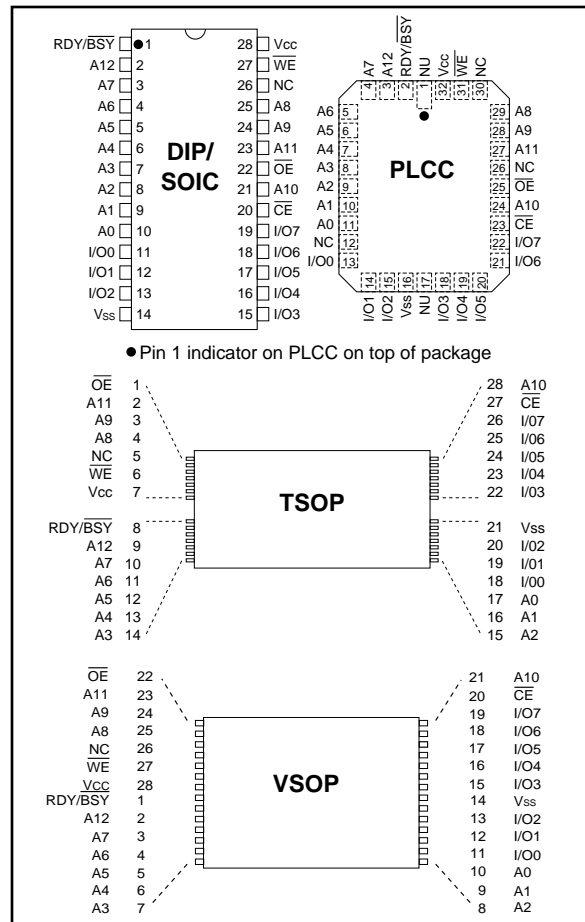
### FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100  $\mu$ A Standby
- Fast Byte Write Time—200  $\mu$ s or 1 ms
- Data Retention >200 years
- High Endurance - Minimum 100,000 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 8Kx8 JEDEC Standard Pinout
  - 28-pin Dual-In-Line Package
  - 32-pin PLCC Package
  - 28-pin Thin Small Outline Package (TSOP) 8x20mm
  - 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C

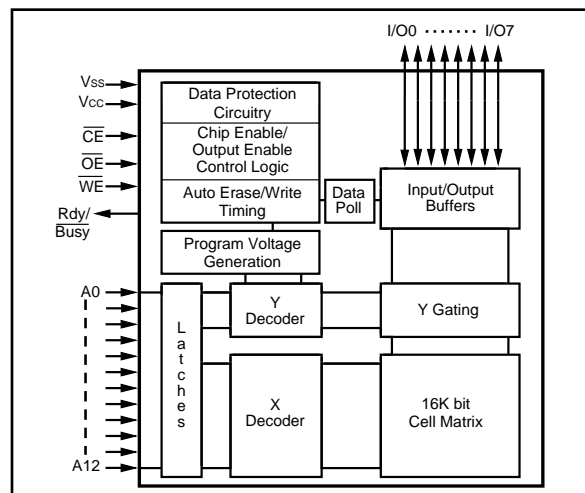
### DESCRIPTION

The Microchip Technology Inc. 28C64A is a CMOS 64K non-volatile electrically Erasable PROM. The 28C64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications

### PACKAGE TYPE



### BLOCK DIAGRAM



# 28C64A

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 MAXIMUM RATINGS\*

V<sub>CC</sub> and input voltages w.r.t. V<sub>SS</sub>..... -0.6V to + 6.25V  
 Voltage on  $\overline{OE}$  w.r.t. V<sub>SS</sub> ..... -0.6V to +13.5V  
 Voltage on A9 w.r.t. V<sub>SS</sub> ..... -0.6V to +13.5V  
 Output Voltage w.r.t. V<sub>SS</sub>.....-0.6V to V<sub>CC</sub>+0.6V  
 Storage temperature .....-65°C to +125°C  
 Ambient temp. with power applied .....-50°C to +95°C

**\*Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/ $\overline{Busy}$	Ready/ $\overline{Busy}$
V <sub>CC</sub>	+5V Power Supply
V <sub>SS</sub>	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTIC

V <sub>CC</sub> = +5V ±10% Commercial (C): T <sub>amb</sub> = 0°C to +70°C Industrial (I): T <sub>amb</sub> = -40°C to +85°C						
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic '1' Logic '0'	V <sub>IH</sub> V <sub>IL</sub>	2.0 -0.1	V <sub>CC</sub> +1 0.8	V V	
Input Leakage	—	I <sub>LI</sub>	-10	10	μA	V <sub>IN</sub> = -0.1V to V <sub>CC</sub> +1
Input Capacitance	—	C <sub>IN</sub>	—	10	pF	V <sub>IN</sub> = 0V; T <sub>amb</sub> = 25°C; f = 1 MHz (Note 2)
Output Voltages	Logic '1' Logic '0'	V <sub>OH</sub> V <sub>OL</sub>	2.4	0.45	V V	I <sub>OH</sub> = -400 μA I <sub>OL</sub> = 2.1 mA
Output Leakage	—	I <sub>LO</sub>	-10	10	μA	V <sub>OUT</sub> = -0.1V to V <sub>CC</sub> +0.1V
Output Capacitance	—	C <sub>OUT</sub>	—	12	pF	V <sub>IN</sub> = 0V; T <sub>amb</sub> = 25°C; f = 1 MHz (Note 2)
Power Supply Current, Active	TTL input	I <sub>CC</sub>	—	30	mA	f = 5 MHz (Note 1) V <sub>CC</sub> = 5.5V
Power Supply Current, Standby	TTL input TTL input CMOS input	I <sub>CC(S)TTL</sub> I <sub>CC(S)TTL</sub> I <sub>CC(S)CMOS</sub>	—	2 3 100	mA mA μA	$\overline{CE}$ = V <sub>IH</sub> (0°C to +70°C) $\overline{CE}$ = V <sub>IH</sub> (-40°C to +85°C) $\overline{CE}$ = V <sub>CC</sub> -0.3 to V <sub>CC</sub> +1

Note 1: AC power supply current above 5MHz: 2mA/MHz.

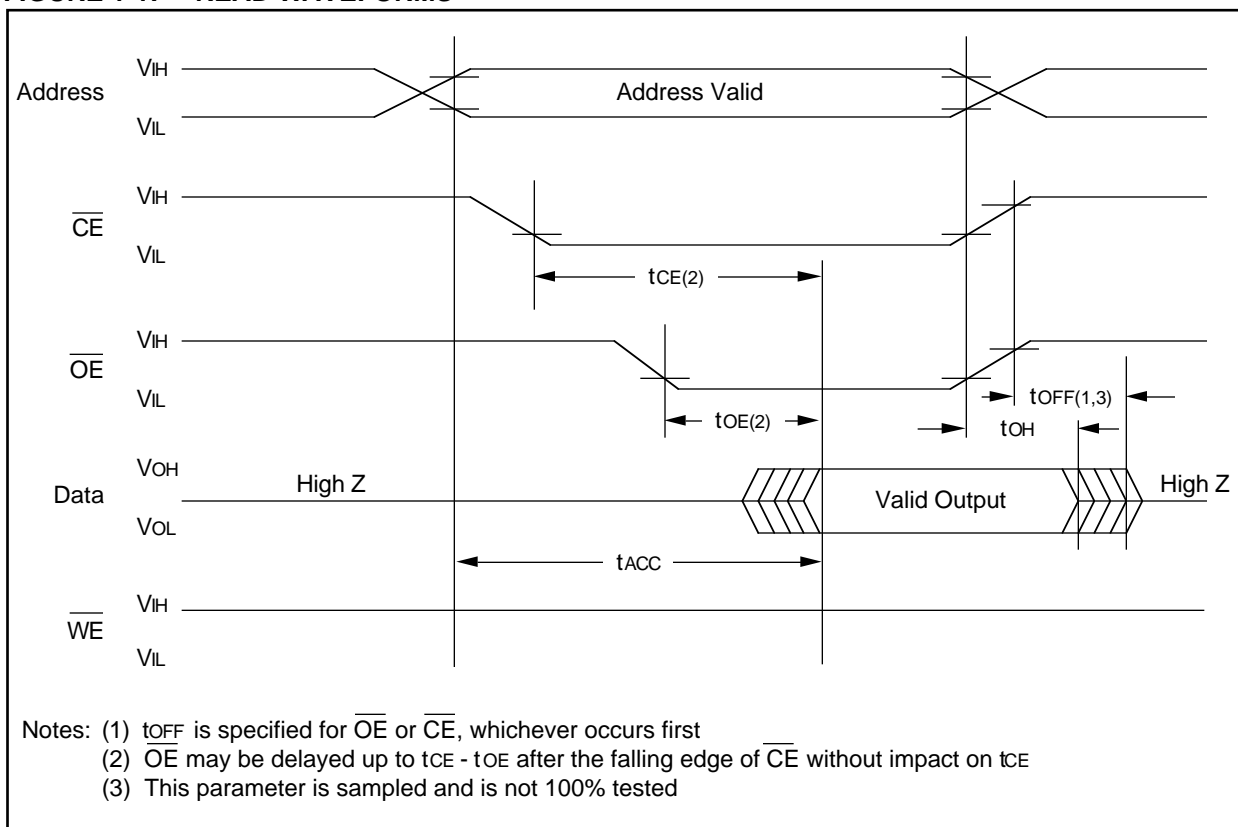
Note 2: Not 100% tested.

**TABLE 1-3: READ OPERATION AC CHARACTERISTICS**

Parameter	Symbol	28C64A-15		28C64A-20		28C64A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
		AC Testing Waveform: $V_{IH} = 2.4V$ ; $V_{IL} = 0.45V$ ; $V_{OH} = 2.0V$ ; $V_{OL} = 0.8V$ Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial (I): $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$							
Address to Output Delay	$t_{ACC}$	—	150	—	200	—	250	ns	$\overline{OE} = \overline{CE} = V_{IL}$
$\overline{CE}$ to Output Delay	$t_{CE}$	—	150	—	200	—	250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	$t_{OE}$	—	70	—	80	—	100	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ or $\overline{OE}$ High to Output Float	$t_{OFF}$	0	50	0	55	0	70	ns	Note 1
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ , whichever occurs first.	$t_{OH}$	0	—	0	—	0	—	ns	Note 1

Note 1: Not 100% tested.

**FIGURE 1-1: READ WAVEFORMS**



# 28C64A

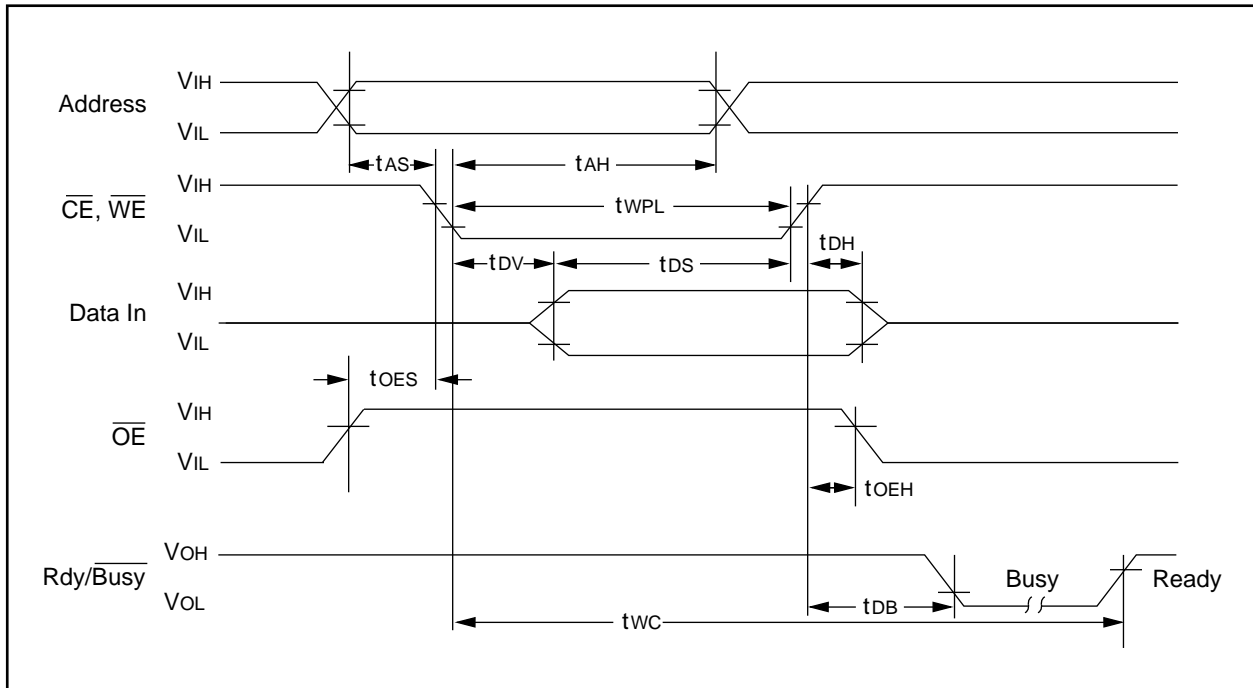
**TABLE 1-4: BYTE WRITE AC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Units	Remarks
AC Testing Waveform:		$V_{IH} = 2.4V$ ; $V_{IL} = 0.45V$ ; $V_{OH} = 2.0V$ ; $V_{OL} = 0.8V$ Output Load: 1 TTL Load + 100 pF Input Rise/Fall Times: 20 ns Ambient Temperature: Commercial (C): $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial (I): $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$			
Address Set-Up Time	tAS	10	—	ns	
Address Hold Time	tAH	50	—	ns	
Data Set-Up Time	tDS	50	—	ns	
Data Hold Time	tDH	10	—	ns	
Write Pulse Width	twPL	100	—	ns	Note 1
Write Pulse High Time	twPH	50	—	ns	
$\overline{OE}$ Hold Time	toEH	10	—	ns	
$\overline{OE}$ Set-Up Time	toES	10	—	ns	
Data Valid Time	tDV	—	1000	ns	Note 2
Time to Device Busy	tDB	2	50	ns	
Write Cycle Time (28C64A)	twC	—	1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	twC	—	200	$\mu s$	100 $\mu s$ typical

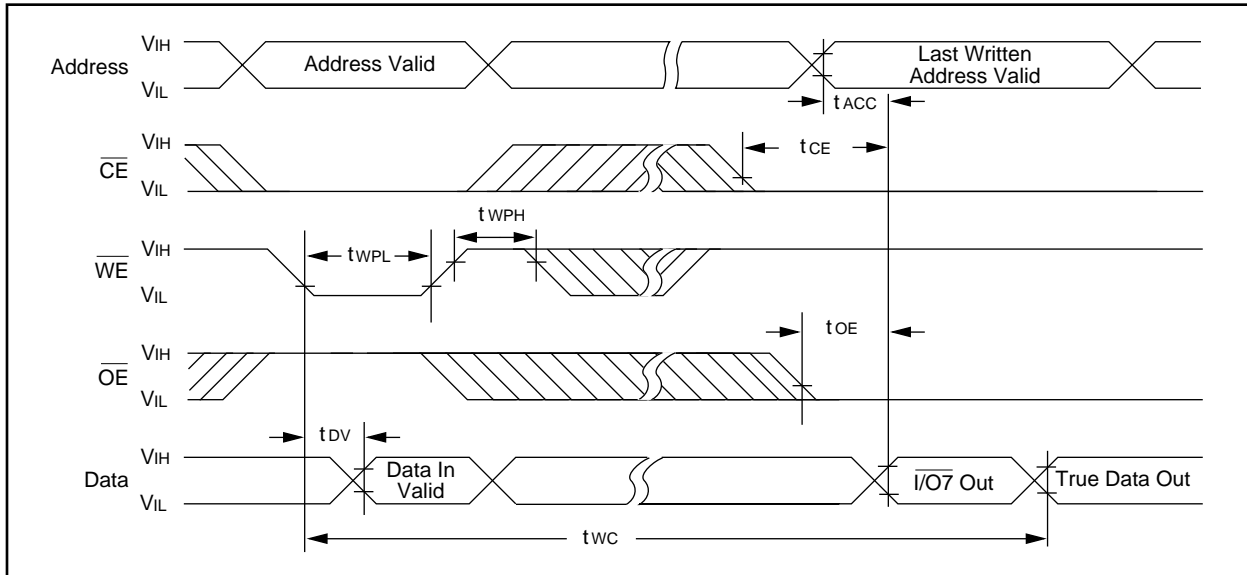
Note 1: A write cycle can be initiated by  $\overline{CE}$  or  $\overline{WE}$  going low, whichever occurs last. The data is latched on the positive edge of  $\overline{WE}$ , whichever occurs first.

Note 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until tDH after the positive edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs first.

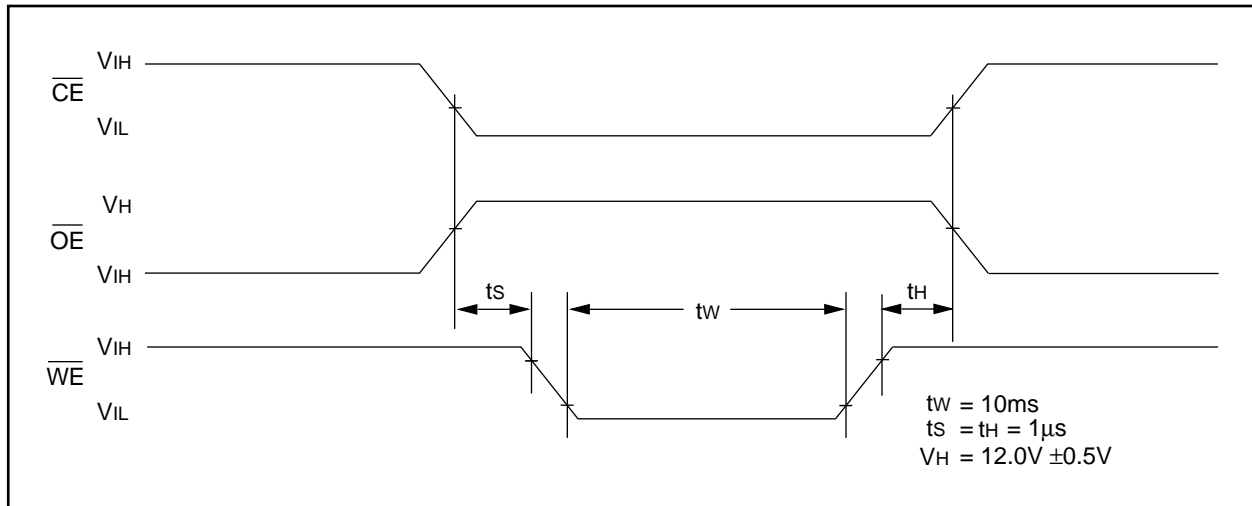
**FIGURE 1-2: PROGRAMMING WAVEFORMS**



**FIGURE 1-3: DATA POLLING WAVEFORMS**



**FIGURE 1-4: CHIP CLEAR WAVEFORMS**



**TABLE 1-5: SUPPLEMENTARY CONTROL**

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/O
Chip Clear	VIL	VIH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

**Note:**  $V_H = 12.0\text{V} \pm 0.5\text{V}$ . \*Pulsed per programming waveforms.

## 2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/Busy (1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note 1: Open drain output.

Note 2: X = Any TTL level.

### 2.1 Read Mode

The 28C64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the output  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been low and addresses have been stable for at least  $t_{ACC-t_{OE}}$ .

### 2.2 Standby Mode

The 28C64A is placed in the standby mode by applying a high signal to the  $\overline{CE}$  input. When in the standby mode, the outputs are in a high impedance state, independent of the  $\overline{OE}$  input.

### 2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a  $\overline{WE}$  filtering circuit that prevents  $\overline{WE}$  pulses of less than 10 ns duration from initiating a write cycle.

Third, holding  $\overline{WE}$  or  $\overline{CE}$  high or  $\overline{OE}$  low, inhibits a write cycle during power-on and power-off (VCC).

### 2.4 Write Mode

The 28C64A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the  $\overline{WE}$  pin. On the falling edge of  $\overline{WE}$ , the address information is latched. On rising edge, the data and the control pins ( $\overline{CE}$  and  $\overline{OE}$ ) are latched. The Ready/Busy pin goes to a logic low level indicating that the 28C64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/Busy goes back to a high, the 28C64A has completed writing and is ready to accept another cycle.

### 2.5 Data Polling

The 28C64A features  $\overline{Data}$  polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminate). After completion of the write cycle, true data is available.  $\overline{Data}$  polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

### 2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V  $\pm$ 0.5V and using address locations 1FEO to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

### 2.7 Chip Clear

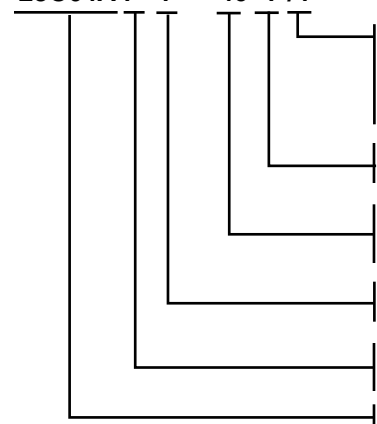
All data may be cleared to 1's in a chip clear cycle by raising  $\overline{OE}$  to 12 volts and bringing the  $\overline{WE}$  and  $\overline{CE}$  low. This procedure clears all data, except for the extra row.

NOTES

# 28C64A

## 28C64A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

<b>28C64A F T - 15 I / P</b>	
	
<b>Package:</b>	L = Plastic Leaded Chip Carrier (PLCC) P = Plastic DIP SO = Plastic Small Outline IC TS = Thin Small Outline Package (TSOP) 8x20mm VS = Very Small Outline Package (VSOP) 8x13.4mm
<b>Temperature Range:</b>	Blank = 0°C to +70°C I = -40°C to +85°C
<b>Access Time:</b>	15 150 ns 20 200 ns 25 250 ns
<b>Shipping:</b>	Blank Tube T Tape and Reel "L" and "SO"
<b>Option:</b>	- = twc = 1ms F = twc = 200 μs
<b>Device:</b>	28C64A 8K x 8 CMOS EEPROM

### AMERICAS

#### Corporate Office

Microchip Technology Inc.  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 602 786-7200 Fax: 602 786-7277  
Technical Support: 602 786-7627  
Web: <http://www.mchip.com/biz/mchip>

#### Atlanta

Microchip Technology Inc.  
500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770 640-0034 Fax: 770 640-0307

#### Boston

Microchip Technology Inc.  
5 Mount Royal Avenue  
Marlborough, MA 01752  
Tel: 508 480-9990 Fax: 508 480-8575

#### Chicago

Microchip Technology Inc.  
333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 708 285-0071 Fax: 708 285-0075

#### Dallas

Microchip Technology Inc.  
14651 Dallas Parkway, Suite 816  
Dallas, TX 75240-8809  
Tel: 214 991-7177 Fax: 214 991-8588

#### Dayton

Microchip Technology Inc.  
35 Rockridge Road  
Englewood, OH 45322  
Tel: 513 832-2543 Fax: 513 832-2841

#### Los Angeles

Microchip Technology Inc.  
18201 Von Karman, Suite 455  
Irvine, CA 92715  
Tel: 714 263-1888 Fax: 714 263-1338

#### New York

Microchip Technology Inc.  
150 Motor Parkway, Suite 416  
Hauppauge, NY 11788  
Tel: 516 273-5305 Fax: 516 273-5335

### AMERICAS (continued)

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408 436-7950 Fax: 408 436-7955

### ASIA/PACIFIC

#### Hong Kong

Microchip Technology  
Unit No. 3002-3004, Tower 1  
Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T. Hong Kong  
Tel: 852 2 401 1200 Fax: 852 2 401 3431

#### Korea

Microchip Technology  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku,  
Seoul, Korea  
Tel: 82 2 554 7200 Fax: 82 2 558 5934

#### Singapore

Microchip Technology  
200 Middle Road  
#10-03 Prime Centre  
Singapore 188980  
Tel: 65 334 8870 Fax: 65 334 8850

#### Taiwan

Microchip Technology  
10F-1C 207  
Tung Hua North Road  
Taipei, Taiwan, ROC  
Tel: 886 2 717 7175 Fax: 886 2 545 0139

### EUROPE

#### United Kingdom

Arizona Microchip Technology Ltd.  
Unit 6, The Courtyard  
Meadow Bank, Furlong Road  
Bourne End, Buckinghamshire SL8 5AJ  
Tel: 44 0 1628 851077 Fax: 44 0 1628 850259

#### France

Arizona Microchip Technology SARL  
2 Rue du Buisson aux Fraises  
91300 Massy - France  
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

#### Germany

Arizona Microchip Technology GmbH  
Gustav-Heinemann-Ring 125  
D-81739 Muenchen, Germany  
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

#### Italy

Arizona Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Pegaso Ingresso No. 2  
Via Paracelso 23, 20041  
Agrate Brianza (MI) Italy  
Tel: 39 039 689 9939 Fax: 39 039 689 9883

### JAPAN

Microchip Technology Intl. Inc.  
Benex S-1 6F  
3-18-20, Shin Yokohama  
Kohoku-Ku, Yokohama  
Kanagawa 222 Japan  
Tel: 81 45 471 6166 Fax: 81 45 471 6122

9/5/95



**MICROCHIP**

Printed in the USA, 9/95  
© 1995, Microchip Technology Incorporated

"Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights." The Microchip logo and name are registered trademarks of Microchip Technology Inc. All rights reserved. All other trademarks mentioned herein are the property of their respective companies.