FEATURES

- Supports DDS compatible subrate data multiplexing and DDS subrate data cross-connection.
- Processes up 128 DS0 channels where each DS0 channel may be individually and independently configured as a 2.4, 4.8, 9.6 or 56 kbit/s subrate DS0A (or 64 kbit/s clear channel) or a 2.4, 4.8, or 9.6 kbit/s subrate DS0B formatted channel.
- Supports any of the multiplexing or demultiplexing options provided by a standard subrate data multiplexor (SRDM) as outlined in TA-TSY-000189. For example, several byte-stuffed subrate DS0A channels can be multiplexed into a DS0B channel or a DS0B channel can be demultiplexed into several byte-stuffed DS0A channels.
- Supports any of the cross-connection options provided by a standard digital cross-connect (DCS) that supports the subrate data cross-connect (SRDC) feature as outlined in TA-TSY-000280. For example, constituent subrate channels within a DS0B channel can be cross-connected or constituent subrate channels in different DS0B channels can be cross-connected.
- Frames to incoming 2.4, 4.8, or 9.6 kbit/s subrate DS0B formatted channels and automatically inserts subrate mux-out-of-sync (SMOS) code upon loss of frame.
- Allows framing patterns to be inserted into outgoing 2.4, 4.8, or 9.6 kbits subrate DS0B formatted channels.
- Allows programmable idle code to be inserted into any outgoing subrate channel including unassigned-mux-channel (UMC) code.
- The PCM input interface can be configured as four 2.048 Mbit/s, 1.544 Mbit/s or 1.536 Mbit/s bit serial input busses or as one 1.024 Mbyte/s, 772 kbyte/s or 768 kbyte/s byte serial input bus.
- The PCM output interface can be configured as four 2.048 Mbit/s, 1.544 Mbit/s or 1.536 Mbit/s bit serial output busses or as one 1.024 Mbyte/s, 772 kbyte/s or 768 kbyte/s byte serial output bus.
- Utilizes two external 8K by 8, 100 ns static RAM devices.
- Supports an external 16.384 MHz, 12.352 MHz or 12.288 MHz crystal for timing generation.
- Provides a generic microprocessor interface for initial configuration, ongoing programming of channel formats and cross-connections, and status monitoring.

- Generates an interrupt upon detection of RAM parity errors and upon detection of loss or aquisition of DS0B frame alignment. Identification of interrupt sources, masking of interrupt sources, and acknowledgement of interrupts is provided via internal registers.

- Low power CMOS technology.

- 84-pin PLCC package.

REFERENCES

- Bell Communications Research, TA-TSY-000189 - "Generic Requirements For The Subrate Multiplexer", Issue 1, April 1986.

- Bell Communications Research, TA-TSY-000280 - "Digital Cross-Connect System (DCS) Requirements And Objectives For The Subrate Data Cross-Connect (SRDC) Feature", Issue 2, May 1986.

DESCRIPTION

The PM3321 SRDX Subrate Data Cross-Connect is a monolithic integrated circuit that supports DDS compatible subrate data multiplexing and subrate data cross-connection for up to 128 DS0 channels.

The DS0 channels that are processed by the SRDX can be input in bit serial or byte serial format and can be ouput in bit serial or byte serial format. A variety of clocking options provide compatibility with common backplane bus rates such as 2.048 Mbit/s, 1.544 Mbit/s, and 1.536 Mbit/s.

Each DS0 channel input by the SRDX can be configured as a subrate 2.4, 4.8, or 9.6 kbit/s DS0B formatted channel, or a subrate 2.4, 4.8, 9.6, or 56 kbit/s DS0A formatted channel, or as a clear 64 kbit/s channel. Each DS0 channel output by the SRDX can be configured as a subrate 2.4, 4.8, or 9.6 kbit/s DS0B formatted channel, or a subrate 2.4, 4.8, 9.6, or 56 kbit/s DS0A formatted channel, or as a clear 64 kbit/s channel. Any legal DDS multiplex, demultiplex, or cross-connect operation can be performed between appropriate sets of input and output channels.

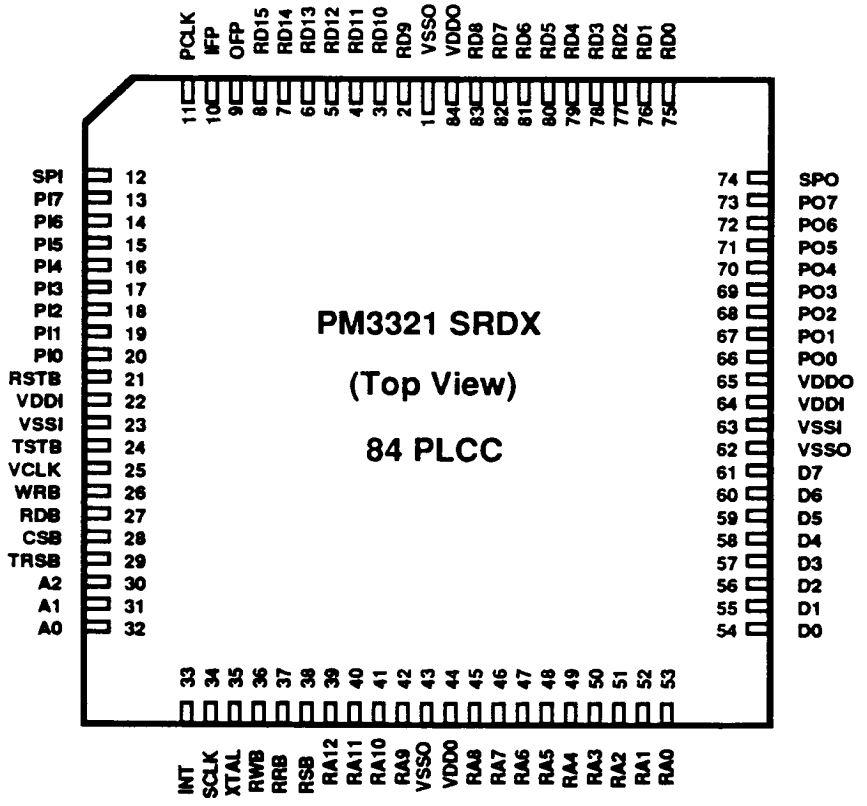
The SRDX frames to incoming subrate 2.4, 4.8, or 9.6 kbit/s DS0B channels and can be configured to generate interrupts when frame is found or when frame is lost for any given DS0B channel. The framing status can also be polled. When a loss of frame occurs for a DS0B channel, Subrate-Mux-Out-Of-Sync code is inserted in place of the incoming channel.

The SRDX inserts framing into outgoing subrate 2.4, 4.8, or 9.6 kbit/s DS0B channels and can be configured to force the framing bit high for outgoing DS0A channels. Unassigned-Mux-Channel code may be inserted into idle outgoing DS0A channels or into idle subrate channels within an outgoing DS0B channel.

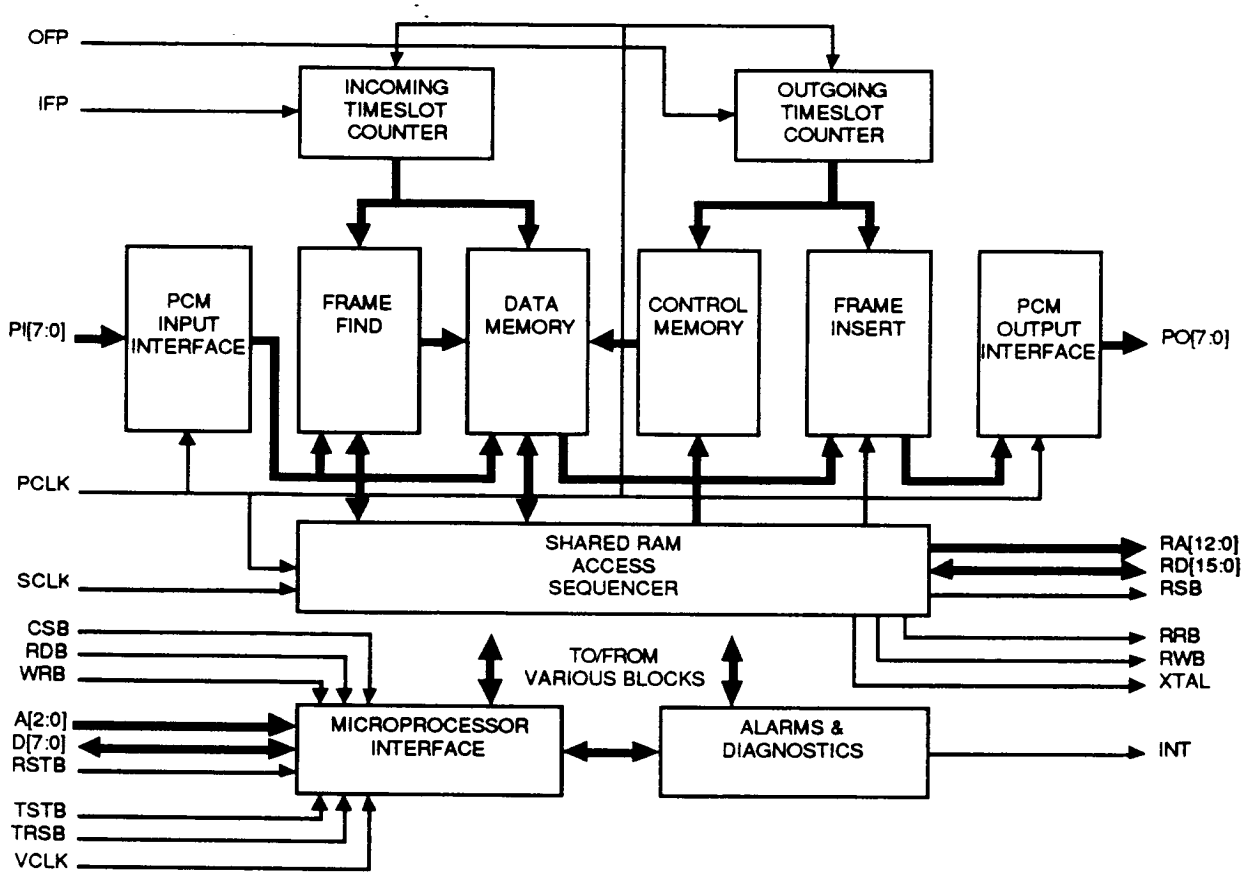
The SRDX operates in conjuction with two external 8K by 8 static RAMs. An external crystal may be used for high speed timing generation. The SRDX is configured, controlled, and monitored using registers that are accessed via a generic microprocessor interface. The SRDX is implemented with low power CMOS technology and is packaged in an 84-pin PLCC package.

PIN DIAGRAM

The SRDX is packaged in an 84-pin PLCC package.



BLOCK DIAGRAM



PIN DESCRIPTION

Connector Name	Type	Pin No.	Function
SCLK	Input	34	The system clock (SCLK) provides timing for SRDX internal operation. External RAM access timing is aligned to SCLK edges. SCLK is nominally a 16.384 MHz, 12.352 MHz, or 12.288 MHz, 50% duty cycle clock. SCLK may be driven externally or connected to an appropriate crystal. SCLK should be chosen to be nominally 8 times the frequency of PCLK and must be at least 7.5 times the frequency of PCLK.
XTAL	Output	35	The crystal output (XTAL) may be connected to a crystal in conjunction with SCLK to form a crystal oscillator. When not used, XTAL should be left unconnected.
PCLK	Input	11	The PCM clock (PCLK) provides timing for the incoming and outgoing PCM busses. PCLK is nominally a 2.048 MHz, 1.544 MHz, 1.536 MHz, 1.024 MHz, 772 kHz, or 768 kHz, 50% duty cycle clock depending upon whether the incoming and outgoing PCM busses are configured for bit serial or byte serial operation and upon the number of bits or bytes chosen to constitute a frame. Bit serial frames of 256 bits, 193 bits, or 192 bits are supported. Byte serial frames of 128 bytes or 96 bytes are supported. The inputs PI[7:0] (or SI[3:0]), IFP, and OFP are sampled on the rising edge of PCLK. The outputs PO[7:0] (or SO[3:0]) are updated on the falling edge of PCLK.
PI[0]/SI[0] PI[1]/SI[1] PI[2]/SI[2] PI[3]/SI[3] PI[4] PI[5] PI[6] PI[7]	Inputs	20 19 18 17 16 15 14 13	The parallel PCM inputs (PI[7:0]) carry DS0 channels in byte serial fashion when the SRDX is configured for byte serial input operation. PI[7:0] is sampled on the rising edge of PCLK. The serial PCM inputs (SI[3:0]) carry DS0 channels in bit serial fashion when the SRDX is configured for bit serial input operation. SI[3:0] is sampled on the rising edge of PCLK.

PO[0]/SO[0] PO[1]/SO[1] PO[2]/SO[2] PO[3]/SO[3] PO[4] PO[5] PO[6] PO[7]	Outputs	66 67 68 69 70 71 72 73	The parallel PCM outputs (PO[7:0]) carry DS0 channels in byte serial fashion when the SRDX is configured for byte serial output operation. PO[7:0] is updated on the falling edge of PCLK. The serial PCM outputs (SO[3:0]) carry DS0 channels in bit serial fashion when the SRDX is configured for bit serial output operation. SO[3:0] is updated on the falling edge of PCLK.
IFP	Input	10	The input frame pulse (IFP) marks the frame boundaries on the incoming PCM busses. IFP identifies the rising edge of PCLK that samples the first byte (or bit) of the frame on PI[7:0] (or SI[3:0]). IFP may go high for one or more consecutive PCLK rising edges; it is the first occurance of IFP being high that marks the begining of the incoming frame. It is not necessary to bring IFP high to mark the beginning of every frame; the SRDX will continue to operate when IFP is absent with incoming timing aligned to the last occurance of IFP. IFP is sampled on the rising edge of PCLK.
OFP	Input	9	The output frame pulse (OFP) marks the frame boundaries on the outgoing PCM busses. OFP identifies the rising edge of PCLK that may be used to sample the first byte (or bit) of the frame on PO[7:0] (or SO[3:0]). OFP may go high for one or more consecutive PCLK rising edges; it is the first occurance of OFP being high that marks the begining of the outgoing frame. It is not necessary to bring OFP high to mark the beginning of every frame; the SRDX will continue to operate when OFP is absent with outgoing timing aligned to the last occurance of OFP. The SRDX may be configured to align all subrate DS0B framing that it inserts to a subrate multiframe marked by OFP. In this configuration, OFP identifies the first byte (or bit) of the first frame of a twenty frame multiframe and OFP must only be brought high every twenty frames or a multiple thereof. OFP is sampled on the rising edge of PCLK.

RA[0]	Output	53	The RAM address bus (RA[12:0]) is used to access an external 8K by 16, static RAM (typically implemented using two 8K by 8 devices). RA[12:0] is updated with timing aligned to SCLK edges.
RA[1]		52	
RA[2]		51	
RA[3]		50	
RA[4]		49	
RA[5]		48	
RA[6]		47	
RA[7]		46	
RA[8]		45	
RA[9]		42	
RA[10]		41	
RA[11]		40	
RA[12]		39	
RD[0]	I/O	75	The RAM data bus (RD[15:0]) is used to access an external 8K by 16, static RAM (typically implemented using two 8K by 8 devices). RD[12:0] is updated and sampled with timing aligned to SCLK edges. RD[15:0] has integral pull up resistors.
RD[1]		76	
RD[2]		77	
RD[3]		78	
RD[4]		79	
RD[5]		80	
RD[6]		81	
RD[7]		82	
RD[8]		83	
RD[9]		2	
RD[10]		3	
RD[11]		4	
RD[12]		5	
RD[13]		6	
RD[14]		7	
RD[15]		8	

RSB	Output	38	The active low RAM select (RSB) signal is low during external RAM accesses. RSB is updated with timing aligned to SCLK edges. RSB is utilized to reduce external RAM power consumption when accesses are not underway.
RRB	Output	37	The active low RAM read enable (RRB) signal is low during external RAM read accesses. RRB is updated with timing aligned to SCLK edges.
RWB	Output	36	The active low RAM write strobe (RWB) signal is low during external RAM write accesses. RWB is updated with timing aligned to SCLK edges.
CSB	Input	28	The active low chip select (CSB) signal is low during SRDX register accesses.
RDB	Input	27	The active low read enable (RDB) signal is low during a SRDX register read access. The SRDX drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	26	The active low write strobe (WRB) signal is low during a SRDX register write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	54 55 56 57 58 59 60 61	The bidirectional data bus (D[7:0]) is used during SRDX register read and write accesses.
A[0] A[1] A[2]	Input	32 31 30	The address bus (A[2:0]) selects specific registers during SRDX register accesses.
INT	Output	33	The interrupt (INT) signal goes high when one of the various interrupting sources within the SRDX is active and enabled to generate interrupts. INT goes low when the interrupt is acknowledged by reading the Interrupt Status register or masked by writing to the Interrupt Enable register.

RSTB	Input	21	The active low reset (RSTB) signal provides an asynchronous SRDX reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
TSTB	Input	24	The active low test mode select (TSTB) signal is low during SRDX production testing. TSTB is high during normal operation. TSTB has an integral pull up resistor.
VCLK	Input	25	The test vector clock (VCLK) signal is used during SRDX production testing to verify internal functionality. VCLK has an integral pull up resistor.
TRSB	Input	29	The test register select (TRSB) signal discriminates between normal and test mode register accesses. TRSB is low during test mode register accesses, and is high during normal mode register accesses. TRSB has an integral pull up resistor.
SPI	Input	12	The spare input (SPI) is reserved for future applications. This input should be connected to GND.
SPO	Output	74	The spare output (SPO) is reserved for future applications. This output should be left unconnected.
VDDI[0] VDDI[1]	Power	22 64	The core power (VDDI[1:0]) pins should be connected to +5 VDC in common with VDDO[2:0].
VSSI[0] VSSI[1]	Ground	23 63	The core ground (VSSI[1:0]) pins should be connected to GND in common with VSSO[2:0].
VDDO[0] VDDO[1] VDDO[2]	Power	44 65 84	The pad ring power (VDDO[2:0]) pins should be connected to +5 VDC in common with VDDI[1:0].
VSSO[0] VSSO[1] VSSO[2]	Ground	43 62 1	The pad ring ground (VSSO[2:0]) pins should be connected to GND in common with VSSI[1:0].

Notes on Pin Description:

1. All SRDX inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels

2. All SRDX outputs and bidirectionals have 2 mA drive capability, except the INT output and the D[7:0] bidirectionals which have 4 mA drive capability.

FUNCTIONAL DESCRIPTION

PCM Input Interface

The PCM Input Interface may be configured to accept data in a variety of formats. Configuration options are programmed via internal registers.

Data may be input in bit serial format on the SI[3:0] inputs at 2.048 Mbit/s, 1.544 Mbit/s, or 1.536 Mbit/s where the bit serial input frames consist of 256, 193, or 192 bits per frame. When configured for 193 bits per frame, the first bit (corresponding to the DS-1 framing bit) is ignored. The serially input data is converted to parallel format and fed to the Frame Find and Data Memory blocks on a parallel bus having 128 or 96 bytes per frame.

Data may also be input in byte serial format on the PI[7:0] inputs at 1.024 Mbyte/s or 768 Mbyte/s, which corresponds to 128 or 96 bytes per frame.

When configured for byte serial format with 128 bytes per frame, either a 2.048 MHz PCLK or a 1.024 MHz PCLK may be used. When the higher PCLK rate is used, every second rising PCLK edge is used to sample PI[7:0], with IFP marking the PCLK rising edge that samples the first byte in each frame. The lower PCLK rate may only be used if both the PCM Input Interface and PCM Output Interface are configured for byte serial format.

When configured for byte serial format with 96 bytes per frame, two clocking options are supported (one corresponding to 193 bits per bit serial frame, and one corresponding to 192 bits per bit serial frame). In the first case, either a 1.544 MHz PCLK or a 772 kHz PCLK may be used. IFP marks a rising PCLK edge in each frame that is to be ignored. When the higher PCLK rate is used, the next rising PCLK edge and every second rising PCLK edge thereafter is used to sample PI[7:0]. The lower PCLK rate may only be used if both the PCM Input Interface and PCM Output Interface are configured for byte serial format.

In the second case, either a 1.536 MHz PCLK or a 768 kHz PCLK may be used. When the higher PCLK rate is used, every second rising PCLK edge is used to sample PI[7:0], with IFP marking the PCLK rising edge that samples the first byte in each frame. Again, the lower PCLK rate may only be used if both the PCM Input Interface and PCM Output Interface are configured for byte serial format.

PCM Output Interface

The PCM Output Interface may be configured to output data in a variety of formats. Configuration options are programmed via internal registers. The formats supported by the PCM Output Interface are the same as those supported by the PCM Input Interface

Incoming Timeslot Counter

The Incoming Timeslot Counter keeps track of the current incoming timeslot for the Frame Find and the Data Memory blocks. It cycles from 0 to 255 or from 0 to 95, as appropriate for the configuration of the SRDX. The incoming timeslot count identifies the current incoming DS0 channel being processed. The alignment of the Incoming Timeslot Counter is controlled by the IFP input.

Frame Find

The Frame Find block frames to incoming DS0B channels, generating an incoming subrate timeslot count that is then used by the Data Memory block. The Frame Find can frame to subrate 2.4 kbit/s, 4.8 kbit/s, or 9.6 kbit/s DS0B formatted channels. The incoming subrate timeslot count that is generated cycles from 0-4, 0-9, or 0-19, as appropriate, for each DS0B channel being processed This block indicates loss of frame and aquisition of frame, capturing indications of these events, and generating an interrupt, if enabled. Subrate-Mux-Out-Of-Sync (SMOS) code is inserted into incoming DS0B channels that are out of frame. The Frame Find can also be disabled so as to ignore subrate DS0A formatted channels or clear 64 kbit/s channels.

The per channel configuration of the Frame Find and the per channel status of the Frame Find is stored in the external RAM which the Frame Find accesses via the Shared RAM Access Sequencer block. The Frame Find configuration and status is also accessible via the Microprocessor Interface.

Outgoing Timeslot Counter

The Outgoing Timeslot Counter keeps track of the current outgoing timeslot and outgoing subrate timeslot for the Control Memory, the Data Memory, and the Frame Insert blocks. The timeslot portion cycles from 0 to 255 or from 0 to 95, as appropriate for the configuration of the SRDX. The subrate timeslot portion cycles from 0 to 19, corresponding to the twenty frame subrate multiframe. The outgoing timeslot count identifies the current outgoing DS0 channel being processed and the outgoing subrate timeslot count identifies the current outgoing subrate channel within outgoing DS0B channels. The alignment of the Outgoing Timeslot Counter is controlled by the OFP input.

Frame Insert

The Frame Insert block inserts framing into the outgoing DS0 channels. On a per channel basis it may be configured to insert patterns appropriate for subrate 2.4 kbit/s, 4.8 kbit/s, or 9.6 kbit/s DS0B channels, or force the framing bit high, as appropriate for subrate DS0A channels. Frame insertion can also be disabled, as appropriate for clear 64 kbit/s channels. The Frame Insert block may also be configured to insert Unassigned-Mux-Channel (UMC) code into idle DS0 channels.

The Frame Insert block utilizes timing provided by the Outgoing Timeslot Counter. The per channel configuration of the Frame Insert block is stored in the external RAM which the Frame Insert block accesses via the Shared RAM Access Sequencer block. The Frame Insert block configuration and status is also accessible via the Microprocessor Interface. The Frame Insert block provides an indication of outgoing DS0 channel format to the Control Memory block.

Control Memory

The Control Memory block provides information to the Data Memory block that determines the type of multiplexing, demultiplexing, or cross-connection, performed by the SRDX. For each outgoing timeslot and outgoing subrate timeslot identified by the Outgoing Timeslot Counter block, the Control Memory block provides a read pointer to the Data Memory block, as appropriate for the type of outgoing channel format identified by the Frame Insert block. The Control Memory may also be configured to substitute a programmable code into outgoing subrate timeslots. One application of this feature is the insertion of Unassigned-Mux-Channel (UMC) code into unused subrate timeslots within an outgoing DS0B channel.

The per channel and per subrate channel configuration of the Control Memory is stored in the external RAM which the Control Memory block accesses via the Shared RAM Access Sequencer Block. The Control Memory configuration is also accessible via the Microprocessor Interface.

Data Memory

The Data Memory block stores PCM data that is being multiplexed, demultiplexed, or cross-connected by the SRDX. Information is written into the Data Memory as specified by the Frame Find and Incoming Timeslot Counter. Information is read from the Data Memory as specified by the Control Memory and, indirectly, the.Outgoing Timeslot Counter and the Frame Insert block.

The information stored in the Data Memory is actually stored in the external RAM which the Data Memory block accesses via the Shared RAM Access Sequencer Block. This information is also accessible via the Microprocessor Interface, however, this capability is provided for test purposes only; it is not required during normal operation.

Shared RAM Access Sequencer

The Shared RAM Access Sequencer coordinates accesses to the external RAM by the Frame Find, Frame Insert, Control Memory, Data Memory, and Microprocessor Interface blocks. Each sequence of accesses is triggered by a PCLK edge that pushes through a byte of PCM data to be processed. RAM access timing is derived using the high speed SCLK signal, and a number of RAM accesses are performed in order to process each PCM byte. Optional RAM accesses also occur when

triggered via the Microprocessor Interface. The Shared RAM Access Sequencer generates the RA[12:0], RD[15:0], RSB, RRB, RWB, and XTAL outputs, and utilizes or samples the SCLK and RD[15:0] inputs.

Alarms & Diagnostics

The Alarms & Diagnostics block allows various alarms to be monitored and and various diagnostic features to be invoked. This block is configured and monitored via the Microprocessor Interface block. Alarms that may be monitored included parity on the RAM utilized by the Frame Find, Frame Insert, Control Memory, and Data Memory blocks, and loss of frame or frame aquisition by the Frame Find block. Alarms may activate the INT output if enabled. Alarms may be identified, and interrupts masked and acknowledged via internal registers. Diagnostic features that may be invoked include loopback from SRDX outputs to SRDX inputs and the ability to disable updates to the RAM utilized by the Data Memory, except by the Microprocessor Interface.

Microprocessor Interface

The Microprocessor Interface block provides the logic required to interface the normal mode and test mode registers within the SRDX to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the SRDX and the test mode registers are used to enhance the testability of the SRDX. The register set is accessed as follows:

A[2]	A[1]	A[0]	TRSB	Register
0	0	0	1	Configuration
0	0	1	1	Reserved
0	1	0	1	Interrupt Enable
0	1	1	1	Interrupt Status
1	0	0	1	Data Low
1	0	1	1	Data High
1	1	0	1	Address Low
1	1	1	1	Address High/Access Control
0	0	0	0	Test Register 0
0	0	1	0	Test Register 1 (Test Mode Select)
0	1	0	0	Test Register 2
0	1	1	0	Reserved
1	X	X	0	Reserved

For all register accesses, CSB must be low.

NOTES

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