

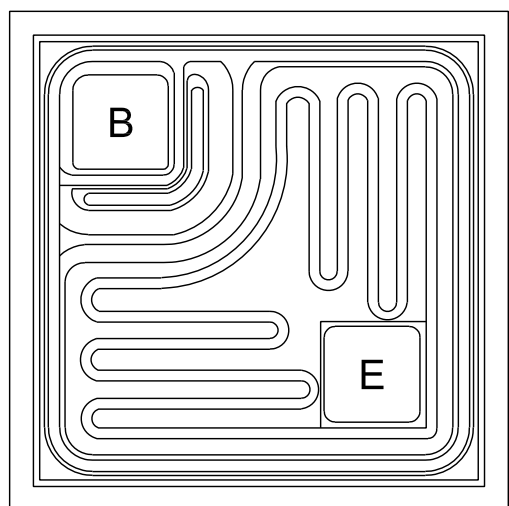
PROCESS CP327V
Small Signal Transistor
NPN - Silicon Darlington Transistor Chip



PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	23 x 23 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	4.7 x 4.7 MILS
Emitter Bonding Pad Area	4.7 x 4.7 MILS
Top Side Metalization	Al-Si - 30,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 5 INCH WAFER

33,085

PRINCIPAL DEVICE TYPES

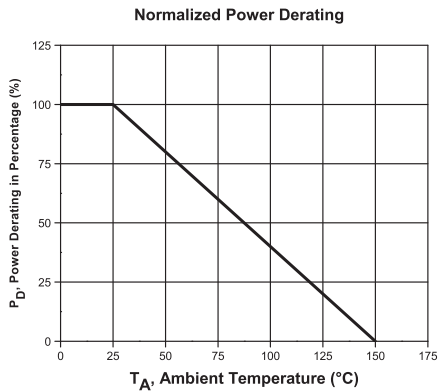
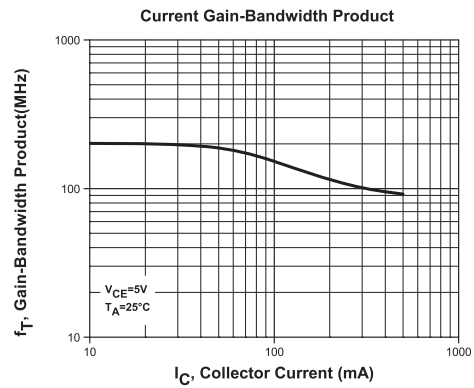
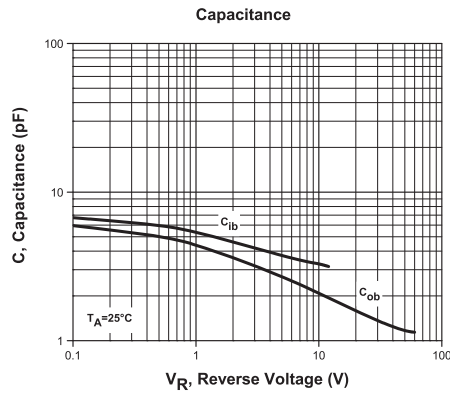
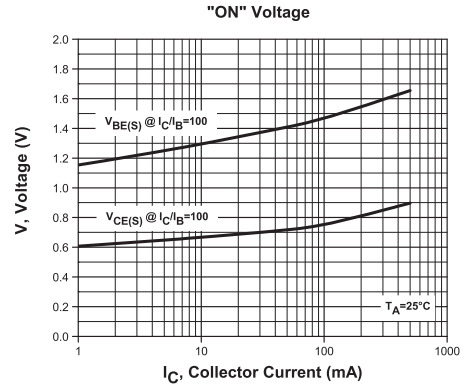
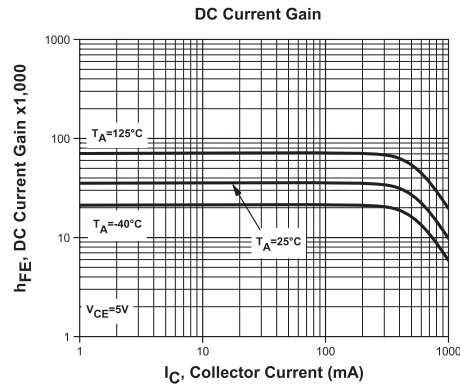
CMLT6427E

CMST6427E

R1 (9-September 2010)

PROCESS CP327V

Typical Electrical Characteristics



R1 (9-September 2010)