

## IC Arrays

### CMOS Array

Electrical Characteristics at  $T_A = 25^\circ\text{C}$

| Type              | Description                                              | Features                                                                                                                                                                                                                                       | Package Number of Pins* |
|-------------------|----------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|
| CD54/74<br>HC UO4 | QMOS Hex Inverter (Unbuffered) Linear Wideband Amplifier | $t_{PLH}, t_{PHL} = 6 \text{ ns}$ @ $V_{CC} = 5\text{V}$ , 2 - 6V operation<br>$T_A = -40$ to $+85^\circ\text{C}$<br>For application information, refer to RCA Application Note, ICAN7637 'Linear Application of the CD74HCUO4 QMOS Inverter.' | 14E, 14M                |

\*Pinouts included in this section. \* See interpretation guide and packaging section

### High-Speed CMOS Arrays

20-Lead (E), (F) and (M) Packages

| Type<br>$V_{CC} = 4.5\text{V}$ | $V_{IH}$<br>Min. V | $V_{IL}$<br>Max. V | $V_{OH}$<br>Min. V | $V_{OL}$<br>Max. V | $I_I$<br>Max. $\mu\text{A}$ | $I_{CC}$<br>Max. $\mu\text{A}$ | Switching Characteristics<br>$C_L = 50 \text{ pF}$ , $t_r, t_f = 6 \text{ ns}$ |                                 |                  |
|--------------------------------|--------------------|--------------------|--------------------|--------------------|-----------------------------|--------------------------------|--------------------------------------------------------------------------------|---------------------------------|------------------|
|                                |                    |                    |                    |                    |                             |                                | $t_{PLH}, t_{PHL}^*$<br>Max. ns                                                | $t_{TLH}, t_{THL}^*$<br>Max. ns | $C_1$<br>Max. pF |
| CD54/74<br>HC688               | 3.15               | 1.35               | 4.4/3.98*          | 0.1/0.26*          | $\pm 0.1 \uparrow$          | 8 $\uparrow$                   | 34/24 $\ddagger$                                                               | 15                              | 10               |
| CD54/74<br>HCT688              | 2                  | 0.8                | 4.4/3.98*          | 0.1/0.26*          | $\pm 0.1 \uparrow$          | 8 $\uparrow$                   | 34/24 $\ddagger$                                                               | 15                              | 10               |

\* CMOS/TTL loads

$\uparrow V_{CC} = 6\text{V}$

$\ddagger$  Rand B data to output/enable to output

Note: For information on Power Darlington Transistor/Arrays, see section on Bipolar Power Transistors