

CVE2 NTSC/PAL Encoder

CVE2 Product Brief

Zoran Corporation
3112 Scott Boulevard
Santa Clara, CA 95054-3317

Tel 408.919.4111
Fax 408.919.4122
www.zoran.com



Description

The Zoran NTSC/PAL encoder core continues a line of highly efficient, cost effective solutions for the digital video market. The CVE2 core encodes YCrCb video into all NTSC and PAL standards with full programmable timing parameters. The carrier frequency and phase provides maximum flexibility. The core also includes support for Macrovision 7.1.L1, the copy protection used by DVD and set-top boxes.

This synthesizable intellectual property core accepts YCrCb video as specified by the CCIR-601 standard or full range YCrCb. All timing signals are generated within the core, synchronized to an external 27 MHz clock. In master mode the core provides Hblank and Vblank to the video source. In slave mode Hblank and Vblank are inputs. In slave mode the core can also be configured to accept multiplexed YCrCb as specified by the CCIR-656 standard.

The outputs are 6 separate busses for Y, Composite, Chroma, and RGB. This allows for flexibility in connection and multiplexing to DACs.

Design Considerations

- Low silicon area: approximately 29,000 gates
- Fully synchronous design
- Technology independent; synthesizable to most CMOS libraries

Deliverables

- Compilable RTL source code
- Bit accurate C model
- Synopsis synthesis scripts
- Test input files
- IP core documentation

Features

- Encodes YCrCb into NTSC or PAL/SECAM
- Supports Macrovision 7.1.L1 copy protection
- Supports all variations of NTSC encoding
- Supports all variations of PAL encoding (I, B, G, D, N, M and combination N)
- RGB SCART output with (MV)
- Component YUV output with (MV)
- Controlled (smooth) edges on Sync and Burst
- Adheres to CCIR 601, 604 and 656 specs; also adheres to SMTPE 253 spec
- Programmable Notch Filter
- Upsampled design minimizes sinx/x distortion and complexity of external analog filter
- Nominal sample rate is 27 Msample/s
- Advanced Trick Play Features including Zoom, Smooth Scan
- Flexible input configuration: can be timing slave or master
- Outputs 10 bit data to DACs
- Generic register programming port
- Controlled entry and exit of active video line
- Fully programmable RGB setup and sync
- WSS & CGMS Data Line Encoding

Applications

- PC Video
- Digital camera process
- PC Graphic
- Any system requiring TV output

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Figure 1. Block Diagram of the CVE2 Intellectual Property Core

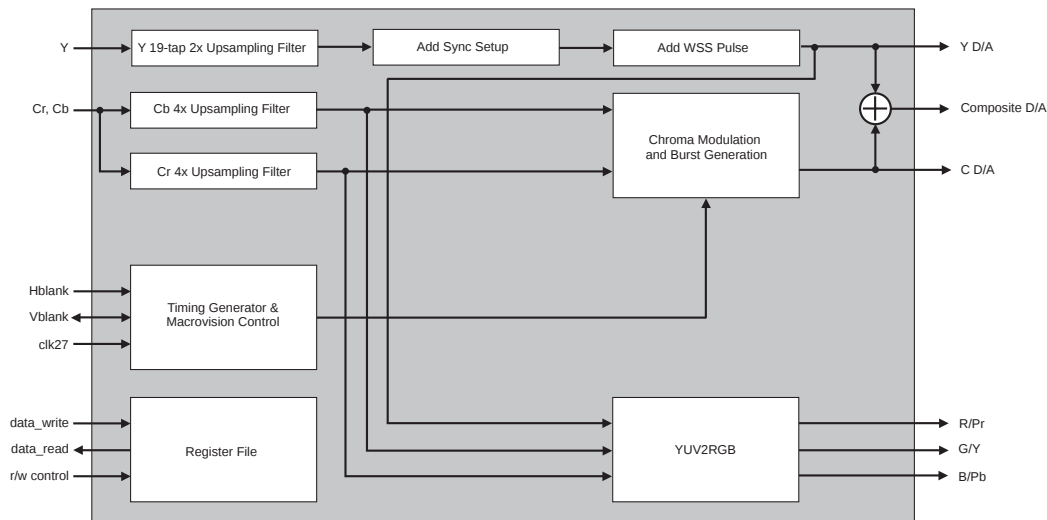
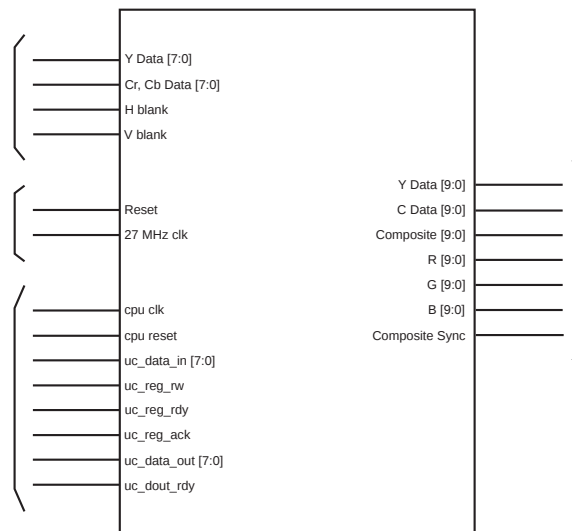


Figure 2. CVE2 Logical Pinout



For more information, contact Zoran's Santa Clara office or the office nearest you:

Canada	China	Hong Kong	Israel	Japan	Korea	Taiwan
Zoran Toronto Lab 2175 Queen St. East, Suite 302 Toronto, Ontario M4E 1E5 Canada Tel: (416) 690-3356 Fax: (416) 690-3363	Zoran China Office Suite 2507 Electronics Science & Tech Building 2070 Central Shennan Rd. Shenzhen, Guangdong, 518031 P.R. China Tel: +86-755-83780319 Fax: +86-755-83780852	Zoran Asia Pacific Ltd. Unit 504-505 New East Ocean Center No. 9 Science Museum Road Kowloon, Hong Kong Tel: +852-2-620-5838 Fax: +852-2-620-5238	Zoran Microelectronics Ltd. Advanced Technology Ctr. P.O. Box 2495 Haifa, 31024 Israel Tel: +972-4-8545-777 Fax: +972-4-8551-551	Zoran Japan Office 2-2-8 Roppongi, Minato-ku Tokyo 106-0032, Japan Tel: +81-03-5574-7081 Fax: +81-03-5574-7156	Zoran Korea Office 505, Dongbuk Building 45-20, Yoido-Dong, Youngdungpo-ku Seoul, Korea 150-891 Tel: +82-2-761-7471 Fax: +82-2-761-7472	Zoran Taiwan Office 4F-1, No. 5, Alley 22 Lane 513, Reikuang Rd. Taipei, Taiwan R.O.C. Tel: +886-2-2659-9797 Fax: +886-2-2659-9595