

## BIDIRECTIONAL I<sup>2</sup>C ISOLATORS WITH UNIDIRECTIONAL DIGITAL CHANNELS

### Features

- Independent, bidirectional SDA and SCL isolation channels
  - Open drain outputs with 35 mA sink current
  - Supports I<sup>2</sup>C clocks up to 1.7 MHz
- Unidirectional isolation channels support additional system signals (Si8405)
- Up to 2500 V<sub>RMS</sub> isolation
- Wide operating supply voltage: 3.0 to 5.5 V
- UL, CSA, VDE recognition
- Operating temperature range –40 to +125 °C max
- Transient immunity: 25 kV/μs
- Compact SO-8 and SO-16 narrow-body packages
- RoHS compliant

### Applications

- Isolated I<sup>2</sup>C buses
- Power over Ethernet
- Motor Control Systems
- Hot-swap applications
- Intelligent Power systems
- Isolated SMPS systems with PMBus interfaces

### Description

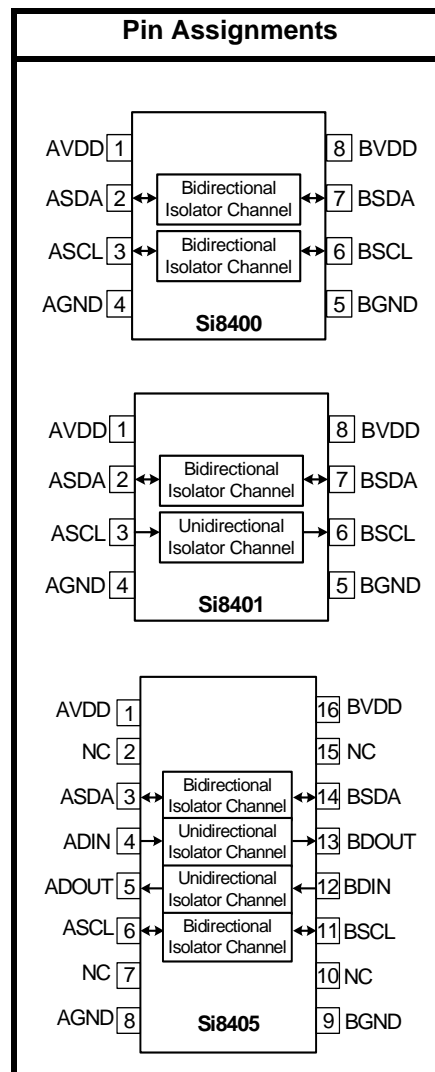
The Si840x series of isolators are single-package galvanic isolation solutions for I<sup>2</sup>C and SMBus serial port applications. These products are based on Silicon Labs proprietary RF isolation technology and offer shorter propagation delays, lower power consumption, smaller installed size, and more stable operation with temperature and age versus opto couplers or other digital isolators.

All devices in this family include hot-swap, bidirectional SDA and SCL isolation channels with open-drain, 35 mA sink capability that operate to a maximum frequency of 1.7 MHz. The 8-pin version (Si8400) supports bidirectional SDA and SCL isolation; the Si8401 supports bidirectional SDA and unidirectional SCL isolation, and the 16-pin version (Si8405) features two unidirectional isolation channels to support additional system signals, such as an interrupt or reset. All versions contain protection circuits to guard against data errors when an unpowered device is inserted into a powered system.

Small size, low installed cost, low power consumption, and short propagation delays make the Si840x family the optimum solution for isolating I<sup>2</sup>C and SMBus serial ports.

### Safety Regulatory Approval

- UL 1577 recognized
  - 2500 V<sub>RMS</sub> for 1 minute
- CSA component notice 5A approval
  - IEC 60950, 61010 approved
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)





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# Si840x

## 1. Electrical Specifications

**Table 1. Si840x Power Characteristics\***

3.0 V < VDD < 5.5 V. TA = -40 to +125 °C. Typical specs at 25 °C (See Figures 2 and 16 for test diagrams.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Si8400/01 Supply Current</b>						
AVDD current BVDD current	I <sub>dda</sub> I <sub>ddb</sub>	All channels = 0 dc	— —	4.2 3.9	6.3 5.9	mA mA
AVDD current BVDD current	I <sub>dda</sub> I <sub>ddb</sub>	All channels = 1 dc	— —	2.3 1.9	3.5 2.9	mA mA
AVDD current BVDD current	I <sub>dda</sub> I <sub>ddb</sub>	All channels = 1.7 MHz	— —	3.2 2.9	4.8 4.4	mA mA
<b>Si8405 Supply Current</b>						
AVDD current BVDD current	I <sub>dda</sub> I <sub>ddb</sub>	All non-I <sup>2</sup> C channels = 0 All I <sup>2</sup> C channels = 1	— —	3.2 2.9	4.8 4.4	mA mA
AVDD current BVDD current	I <sub>dda</sub> I <sub>ddb</sub>	All non-I <sup>2</sup> C channels = 1 All I <sup>2</sup> C channels = 0	— —	6.2 6.0	9.3 9.0	mA mA
AVDD current BVDD current	I <sub>dda</sub> I <sub>ddb</sub>	All non-I <sup>2</sup> C channels = 5 MHz All I <sup>2</sup> C channels = 1.7 MHz	— —	4.7 4.5	7.1 6.8	mA mA
<b>*Note:</b> All voltages are relative to respective ground.						

**Table 2. Si8400/01/05 Electrical Characteristics for Bidirectional I<sup>2</sup>C Channels<sup>1</sup>**

3.0 V &lt; VDD &lt; 5.5 V. TA = -40 to +125 °C. Typical specs at 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic Levels Side A						
Logic Input Threshold <sup>2</sup>	I <sup>2</sup> CV <sub>T</sub> (Side A)		450	—	780	mV
Logic Low Output Voltages <sup>3</sup>	I <sup>2</sup> CV <sub>OL</sub> (Side A)	ISDAA = ISCLA = 3.0 mA	650	—	910	mV
		ISDAA = ISCLA = 0.5 mA	550	—	825	mV
Input/Output Logic Low Level Difference <sup>4</sup>	I <sup>2</sup> CΔV (Side A)		50	—	—	mV
Logic Levels Side B						
Logic Low Input Voltage	I <sup>2</sup> CV <sub>IL</sub> (Side B)		—	—	0.8	V
Logic High Input Voltage	I <sup>2</sup> CV <sub>IH</sub> (Side B)		2.0	—	—	V
Logic Low Output Voltage	I <sup>2</sup> CV <sub>OL</sub> (Side B)	ISCLB = 35 mA	—	—	400	mV
SCL and SDA Logic High Leakage	Isdaa, Isdab Iscla, Isclb	SDAA, SCLA = VSSA SDAB, SCLB = VSSB	—	2.0	10	μA

**Notes:**

- All voltages are relative to respective ground.
- V<sub>IL</sub> < 0.450 V, V<sub>IH</sub> > 0.780 V.
- Logic low output voltages are 910 mV max from -10 to 125 °C at 3.0 mA.  
Logic low output voltages are 955 mV max from -40 to 125 °C at 3.0 mA.  
Logic low output voltages are 825 mV max from -10 to 125 °C at 0.5 mA.  
Logic low output voltages are 875 mV max from -40 to 125 °C at 0.5 mA.  
See "AN375: Design Considerations for Isolating an I<sup>2</sup>C Bus or SMBus" for additional information.
- I<sup>2</sup>CΔV (Side A) = I<sup>2</sup>CV<sub>OL</sub> (Side A) - I<sup>2</sup>CV<sub>T</sub> (Side A). To ensure no latch-up on a given bus, I<sup>2</sup>CΔV (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
- Side A measured at 0.6 V.

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**Table 2. Si8400/01/05 Electrical Characteristics for Bidirectional I<sup>2</sup>C Channels<sup>1</sup> (Continued)**

3.0 V < VDD < 5.5 V. TA = -40 to +125 °C. Typical specs at 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pin capacitance SDAA, SCLA, SDAB, SDBB	CA CB		— —	10 10	— —	pF pF
<b>Timing Specifications (Measured at 1.40 V Unless Otherwise Specified)</b>						
Maximum I <sup>2</sup> C bus Frequency	Fmax		—	—	1.7	MHz
Propagation Delay 5 V Operation						
Side A to side B rising <sup>5</sup>	Tphab	No bus capacitance, R1 = 1400, R2 = 499, See Figure 2	—	25	29	ns
Side A to side B falling <sup>5</sup>	Tplab		—	15	22	ns
Side B to side A rising	Tphba		—	20	30	ns
Side B to side A falling	Tplba		—	9.0	12	ns
3.3 V Operation						
Side A to side B rising <sup>5</sup>	Tphab	R1 = 806 R2 = 499	—	28	35	ns
Side A to side B falling <sup>5</sup>	Tplab		—	13	18	ns
Side B to side A rising	Tphba		—	20	40	ns
Side B to side A falling	Tplba		—	10	15	ns
Pulse width distortion 5 V						
Side A low to Side B low <sup>5</sup>	PWDAB	No bus capacitance, R1 = 1400, R2 = 499, See Figure 2	—	9.0	15	ns
Side B low to Side A low	PWDBA		—	11	20	ns
3.3 V						
Side A low to Side B low <sup>5</sup>	PWDAB	R1 = 806, R2 = 499	—	15	22	ns
Side B low to Side A low	PWDBA		—	11	30	ns
<b>Notes:</b>						
1. All voltages are relative to respective ground.						
2. V <sub>IL</sub> < 0.450 V, V <sub>IH</sub> > 0.780 V.						
3. Logic low output voltages are 910 mV max from -10 to 125 °C at 3.0 mA. Logic low output voltages are 955 mV max from -40 to 125 °C at 3.0 mA. Logic low output voltages are 825 mV max from -10 to 125 °C at 0.5 mA. Logic low output voltages are 875 mV max from -40 to 125 °C at 0.5 mA. See "AN375: Design Considerations for Isolating an I <sup>2</sup> C Bus or SMBus" for additional information.						
4. I <sup>2</sup> CΔV (Side A) = I <sup>2</sup> CV <sub>OL</sub> (Side A) - I <sup>2</sup> CV <sub>T</sub> (Side A). To ensure no latch-up on a given bus, I <sup>2</sup> CΔV (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.						
5. Side A measured at 0.6 V.						

**Table 3. Electrical Characteristics for Unidirectional Non-I<sup>2</sup>C Digital Channels (Si8405)**

3.0 V &lt; VDD &lt; 5.5 V. TA = -40 to +125 °C. Typical specs at 25 °C

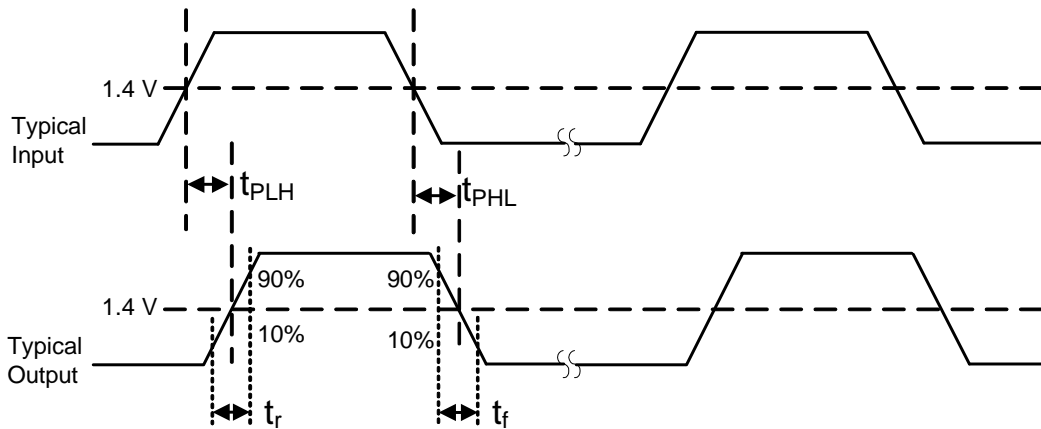
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V <sub>IH</sub>		2.0	—	—	V
Low Level Input Voltage	V <sub>IL</sub>		—	—	0.8	V
High Level Output Voltage	V <sub>OH</sub>	I <sub>oh</sub> = -4 mA	AVDD, BVDD -0.4	4.8	—	V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>ol</sub> = 4 mA	—	0.2	0.4	V
Input Leakage Current	I <sub>L</sub>		—	—	±10	μA
Output Impedance <sup>1</sup>	Z <sub>O</sub>		—	85	—	Ω
<b>Timing Characteristics</b>						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	40	ns
Propagation Delay	t <sub>PHL</sub> , t <sub>PLH</sub>	See Figure 1	—	—	20	ns
Pulse Width Distortion  t <sub>PLH</sub> - t <sub>PHL</sub>	PWD	See Figure 1	—	—	12	ns
Propagation Delay Skew <sup>2</sup>	t <sub>PSK(P-P)</sub>		—	—	20	ns
Channel-Channel Skew	t <sub>PSK</sub>		—	—	10	ns
Output Rise Time	t <sub>r</sub>	C <sub>3</sub> = 15 pF See Figure 1 and Figure 2	—	4.0	6.0	ns
Output Fall Time	t <sub>f</sub>	C <sub>3</sub> = 15 pF See Figure 1 and Figure 2	—	3.0	4.3	ns
<b>Notes:</b>						
<ol style="list-style-type: none"> <li>1. The nominal output impedance of a non-I<sup>2</sup>C isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.</li> <li>2. t<sub>PSK(P-P)</sub> is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.</li> </ol>						

**Table 4. Electrical Characteristics for All I<sup>2</sup>C and Non-I<sup>2</sup>C Channels**

3.0 V < VDD < 5.5 V. TA = -40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDD Undervoltage Threshold	VDDUV+	AVDD, BVDD rising	2.15	2.3	2.5	V
VDD Negative-going Lockout Hysteresis	VDDH-	AVDD, BVDD falling	45	75	95	mV
Common Mode Transient Immunity	CMTI	V <sub>I</sub> = V <sub>DD</sub> or 0 V	—	25	—	kV/μs
Shut Down Time from UVLO	t <sub>SD</sub>		—	3.0	—	μs
Start-up Time*	t <sub>START</sub>		—	15	40	μs

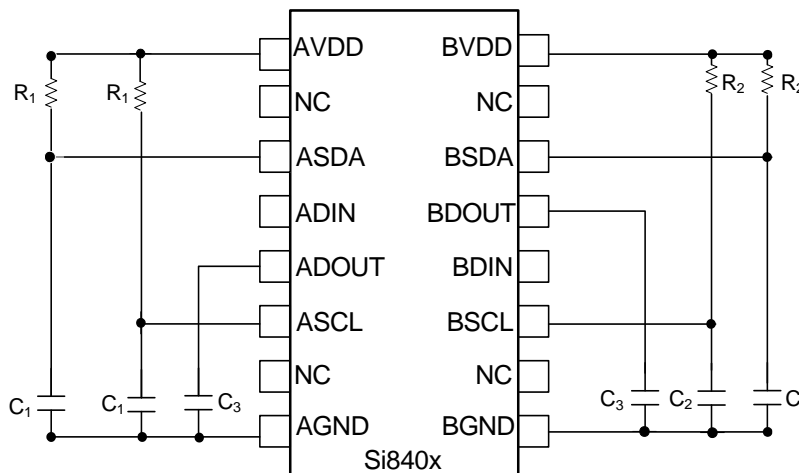
**\*Note:** Start-up time is the time period from the application of power to valid data at the output.



**Figure 1. Propagation Delay Timing (Non-I<sup>2</sup>C Channels)**

## 1.1. Test Circuits

Figure 2 depicts the timing test diagram.

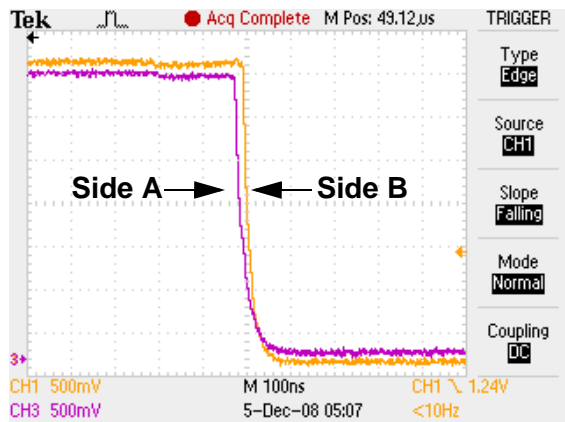


**Figure 2. Simplified Timing Test Diagram**

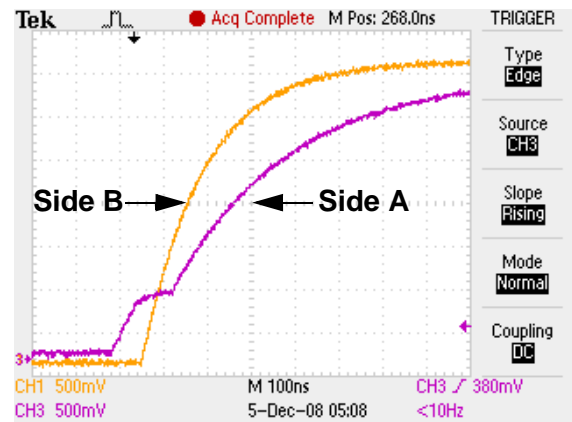


## 1.2. Typical Performance Characteristics

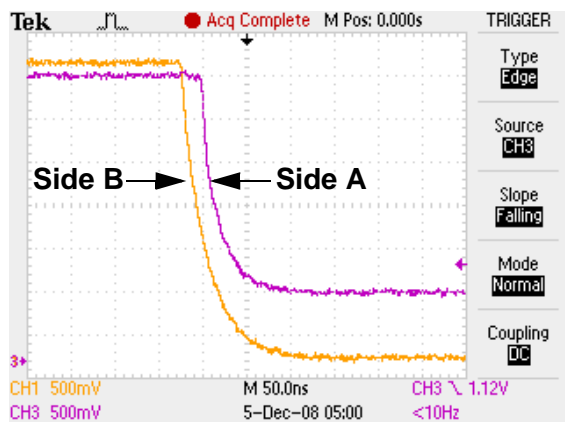
The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 1, 2, 3, and 4 for actual specification limits.



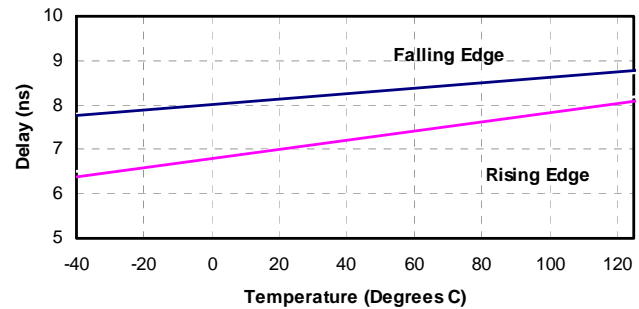
**Figure 3. I<sup>2</sup>C Side A Pulling Down (1100 Ω Pull-Up)**



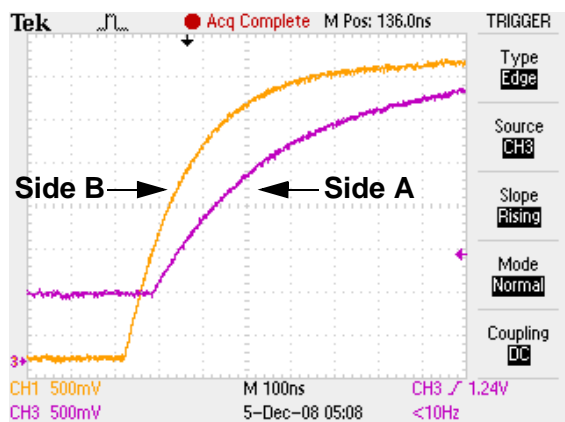
**Figure 6. I<sup>2</sup>C Side A Pulling Up, Side B Following**



**Figure 4. I<sup>2</sup>C Side B Pulling Down**



**Figure 7. Non I<sup>2</sup>C Channel Propagation Delay vs. Temperature**



**Figure 5. I<sup>2</sup>C Side B Pulling Up, Side A Following**

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**Table 5. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature <sup>2</sup>	$T_{STG}$	-65	—	150	°C
Ambient Temperature Under Bias	$T_A$	-40	—	125	°C
Supply Voltage (Revision A) <sup>3</sup>	$V_{DD}$	-0.5	—	5.75	V
Supply Voltage (Revision B) <sup>3</sup>	$V_{DD}$	-0.5	—	6.0	V
Input Voltage	$V_I$	-0.5	—	$V_{DD} + 0.5$	V
Output Voltage	$V_O$	-0.5	—	$V_{DD} + 0.5$	V
Output Current Drive (non-I <sup>2</sup> C channels)	$I_O$	—	—	±10	mA
Side A output current drive (I <sup>2</sup> C channels)	$I_O$	—	—	±15	mA
Side B output current drive (I <sup>2</sup> C channels)	$I_O$	—	—	±75	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s)		—	—	3600	$V_{RMS}$

**Notes:**

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from -40 to 150 °C.
3. See "8.Ordering Guide" on page 25 for more information.

**Table 6. Regulatory Information\***

<b>CSA</b>
The Si840x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
<b>VDE</b>
The Si840x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
<b>UL</b>
The Si840x is certified under UL1577 component recognition program. For more details, see File E257455.
<b>*Note:</b> Regulatory Certifications apply to 2.5 kV <sub>RMS</sub> rated devices which are production tested to 3.0 kV <sub>RMS</sub> for 1 sec. For more information, see "8.Ordering Guide" on page 25.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-8	NB SOIC-16	
Nominal Air Gap (Clearance) <sup>1</sup>	L(1O1)		4.9	4.9	mm
Nominal External Tracking (Creepage) <sup>1</sup>	L(1O2)		4.01	4.01	mm
Minimum Internal Gap (Internal Clearance)			0.008	0.008	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	>175	V
Resistance (Input-Output) <sup>2</sup>	R <sub>IO</sub>		10 <sup>12</sup>	10 <sup>12</sup>	Ω
Capacitance (Input-Output) <sup>2</sup>	C <sub>IO</sub>	f = 1 MHz	1.0	2.0	pF
Input Capacitance <sup>3</sup>	C <sub>I</sub>		4.0	4.0	pF

**Notes:**

- The values in this table correspond to the nominal creepage and clearance values as detailed in “9. Package Outline: 8-Pin Narrow Body SOIC” and “11. Package Outline: 16-Pin Narrow Body SOIC”. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-8 package and 4.7 mm minimum for the NB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 package and 3.9 mm minimum for the NB SOIC-16 package.
- To determine resistance and capacitance, the Si840x, SO-16, is converted into a 2-terminal device. Pins 1–8 (1-4, SO-8) are shorted together to form the first terminal and pins 9–16 (5–8, SO-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
- Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification
Basic Isolation Group	Material Group	IIIa
Installation Classification	Rated Mains Voltages ≤ 150 V <sub>RMS</sub>	I-IV
	Rated Mains Voltages ≤ 300 V <sub>RMS</sub>	I-III
	Rated Mains Voltages ≤ 400 V <sub>RMS</sub>	I-II

**Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB\***

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	$V_{IORM}$		560	V peak
Input to Output Test Voltage	$V_{PR}$	Method a After Environmental Tests Subgroup 1 ( $V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge < 5 pC)	896	V peak
		Method b1 ( $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, $t_m = 1$ sec, Partial Discharge < 5 pC)	1050	
		After Input and/or Safety Test Subgroup 2/3 ( $V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge < 5 pC)	672	
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 10$ sec)	$V_{TR}$		4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$		$>10^9$	$\Omega$
<p><b>*Note:</b> The Si840x is suitable for basic electrical isolation within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si840x provides a climate classification of 40/125/21.</p>				

**Table 10. IEC Safety Limiting Values<sup>1</sup>**

Parameter	Symbol	Test Condition	NB SOIC-8	NB SOIC-16	Unit
Case Temperature	$T_S$		150	150	$^{\circ}\text{C}$
Safety Input Current	$I_S$	$\theta_{JA} = 105$ $^{\circ}\text{C}/\text{W}$ (NB SOIC-16), $140$ $^{\circ}\text{C}/\text{W}$ (NB SOIC-8) AVDD, BVDD = 5.5 V, $T_J = 150$ $^{\circ}\text{C}$ , $T_A = 25$ $^{\circ}\text{C}$	160	210	mA
Device Power Dissipation <sup>2</sup>	$P_D$		220	275	W
<p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 8 and Figure 9.</li> <li>The Si840x is tested with AVDD, BVDD = 5.5 V; <math>T_J = 150</math> <math>^{\circ}\text{C}</math>; <math>C_1, C_2 = 0.1</math> <math>\mu\text{F}</math>; <math>C_3 = 15</math> pF; <math>R_1, R_2 = 3\text{k}\Omega</math>; input 1 MHz 50% duty cycle square wave.</li> </ol>					

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-8	NB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	$\theta_{JA}$		140	105	$^{\circ}\text{C}/\text{W}$

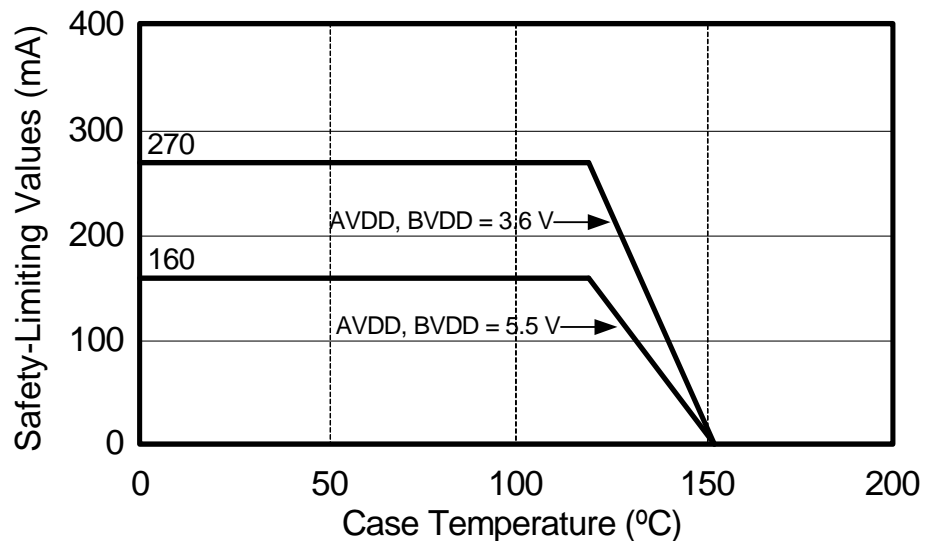


Figure 8. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

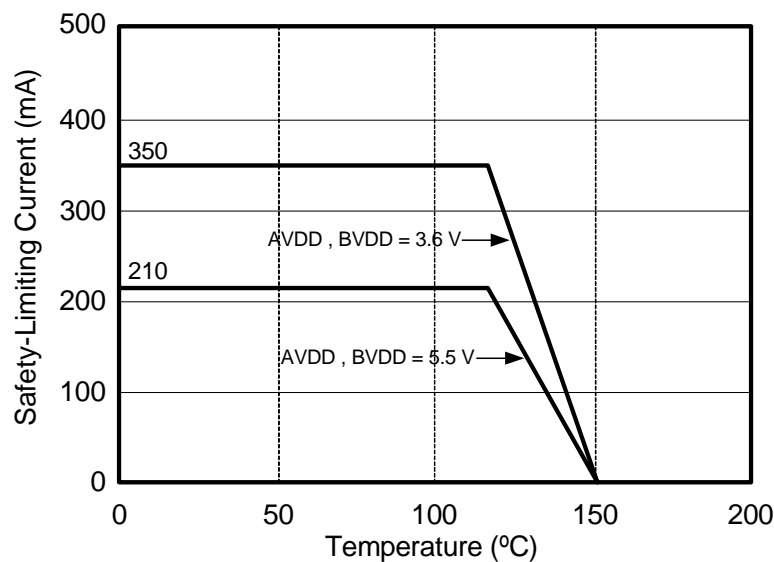
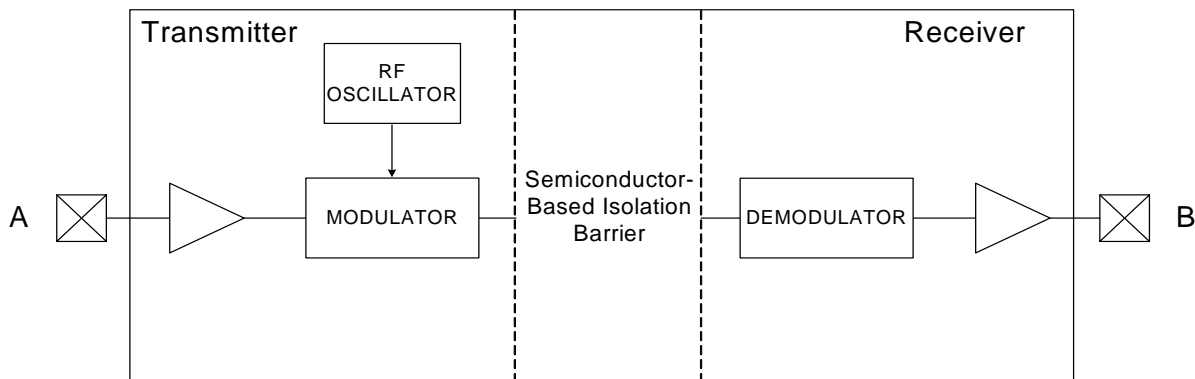


Figure 9. NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

## 2. Overview

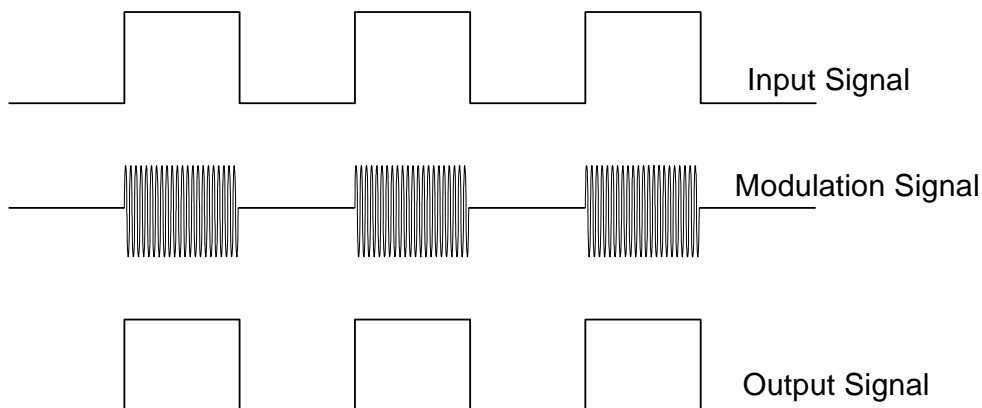
### 2.1. Theory of Operation

The operation of an Si84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single unidirectional Si84xx channel is shown in Figure 10.



**Figure 10. Simplified Channel Diagram**

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 11 for more details.



**Figure 11. Modulation Scheme**

### 3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 12, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 12 to determine outputs when power supply (VDD) is not present.

#### 3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period  $t_{START}$ . Following this, the outputs follow the states of inputs.

#### 3.2. Under Voltage Lockout

Under Voltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own under voltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when AVDD falls below  $AVDD_{UVLO-}$  and exits UVLO when AVDD rises above  $AVDD_{UVLO+}$ . Side B operates the same as Side A with respect to its BVDD supply.

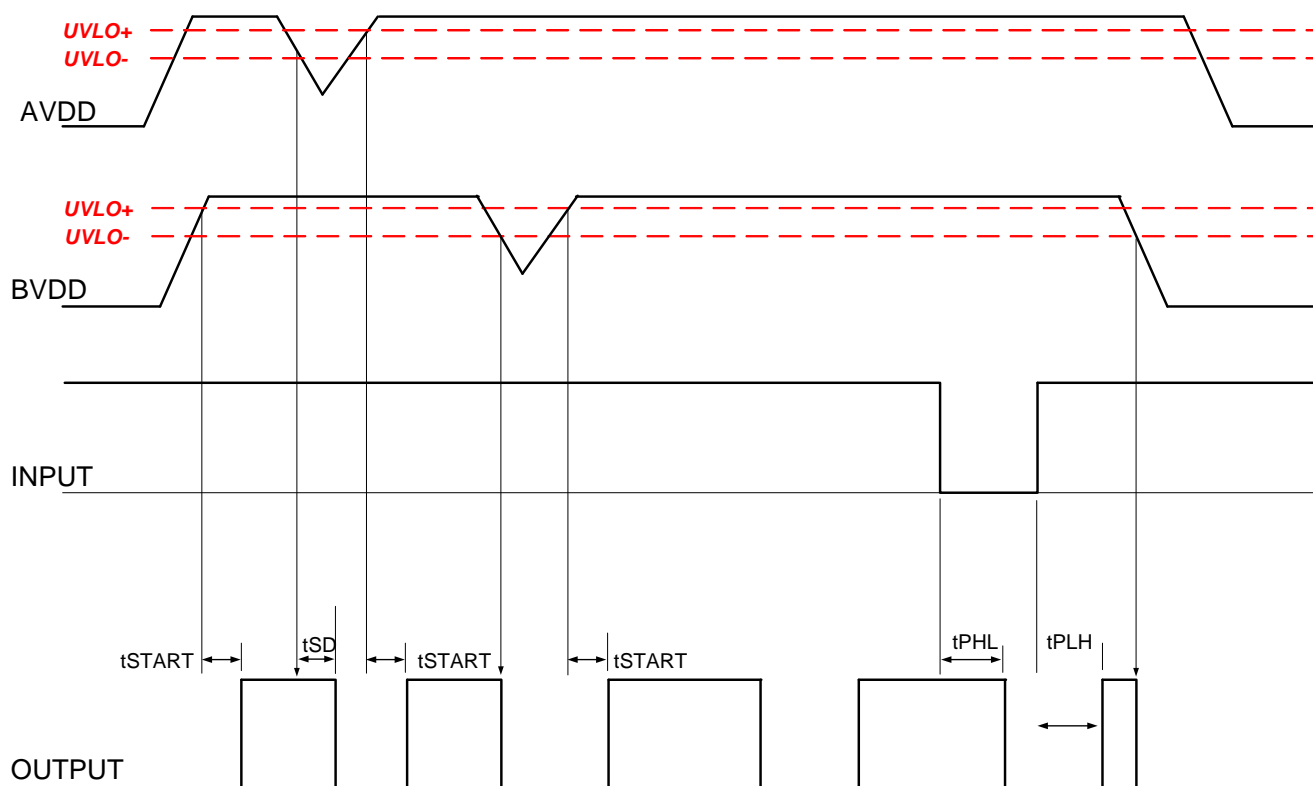


Figure 12. Device Behavior during Normal Operation

### 3.3. Input and Output Characteristics for Non-I<sup>2</sup>C Digital Channels

The Si84xx inputs and outputs are standard CMOS drivers/receivers. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. Table 12 details powered and unpowered operation of the Si84xx's non-I<sup>2</sup>C digital channels.

**Table 12. Si84xx Operation Table**

V <sub>I</sub> Input <sup>1,4</sup>	VDDI State <sup>1,2,3</sup>	VDDO State <sup>1,2,3</sup>	V <sub>O</sub> Output <sup>1,4</sup>	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	L	Upon transition of VDDI from unpowered to powered, V <sub>O</sub> returns to the same state as V <sub>I</sub> in less than 1 μs.
X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V <sub>O</sub> returns to the same state as V <sub>I</sub> within 1 μs.

**Notes:**

1. VDDI and VDDO are the input and output power supplies. V<sub>I</sub> and V<sub>O</sub> are the respective input and output terminals.
2. Powered (P) state is defined as 3.0 V < VDD < 5.5 V.
3. Unpowered (UP) state is defined as VDD = 0 V.
4. X = not applicable; H = Logic High; L = Logic Low.



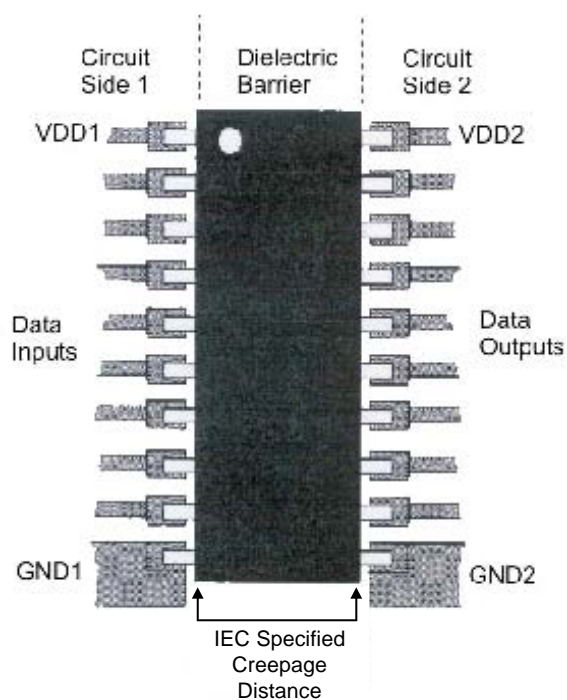
## 4. Layout Recommendations

Dielectric isolation is a set of specifications produced by safety regulatory agencies from around the world, which describes the physical construction of electrical equipment that derives power from high-voltage power systems, such as 100–240 V<sub>AC</sub> systems or industrial power. The dielectric test (or HIPOT test) given in the safety specifications places a very high voltage between the input power pins of a product and the user circuits and the user-touchable surfaces of the product. For the IEC relating to products deriving their power from the 100–240 V<sub>AC</sub> power grids, the minimum test voltage is 2500 V<sub>AC</sub> (or 3750 V<sub>DC</sub>, the peak equivalent voltage).

There are two terms described in the safety specifications:

- Creepage—the distance along the insulating surface an arc may travel.
- Clearance—the shortest distance through air that an arc may travel.

Figure 13 illustrates the accepted method of providing the proper creepage distance along the surface. For a 120 V<sub>AC</sub> application, this distance is 3.2 mm, and the narrow-body SOIC package can be used. For a 220–240 V<sub>AC</sub> application, this distance is 6.4 mm, and a wide-body SOIC package must be used. There must be no copper traces within this 3.2 or 6.4 mm exclusion area, and the surface should have a conformal coating, such as solder resist. The digital isolator chip must straddle this exclusion area.



**Figure 13. Creepage Distance**

### 4.1. Supply Bypass

The Si84xx families require a 1  $\mu$ F bypass capacitor between AVDD and AGND and BVDD and BGND. The capacitor should be placed as close as possible to the package. See "6. Errata and Design Migration Guidelines (Revision A Only)" on page 22 for more details.

## 4.2. RF Radiated Emissions

The Si84xx families use an RF carrier frequency of approximately 700 MHz. This results in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC but, rather, is due to a small amount of RF energy driving the isolated ground planes, which can act as a dipole antenna.

The unshielded Si84xx evaluation board passes FCC Class B (Part 15) requirements. Table 13 shows measured emissions compared to FCC requirements. Note that the data reflects worst-case conditions, where all inputs tied to logic 1 and the RF transmitters are fully active.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

**Table 13. Radiated Emissions**

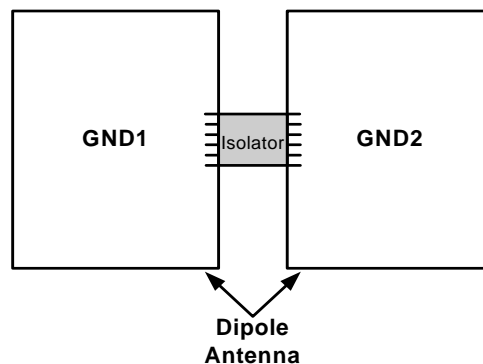
Frequency (MHz)	Measured (dB $\mu$ V/m)	FCC Spec (dB $\mu$ V/m)	Compared to Spec (dB)
712	29	37	-8
1424	39	54	-15
2136	42	54	-12
2848	43	54	-11
4272	44	54	-10
4984	44	54	-10
5696	44	54	-10

## 4.3. RF, Magnetic, and Common Mode Transient Immunity

The Si84xx families have very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures at 25 kV/ $\mu$ s (typical). During a high surge event, the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si84xx families pass the industrial requirements of CISPR24 for RF immunity of 10 V/m using an unshielded evaluation board. As shown in Figure 14, the isolated ground planes form a parasitic dipole antenna. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

The Si840x digital isolator can be used in close proximity to large motors and various other magnetic-field producing equipment. In theory, data transmission errors can occur if the magnetic field is too large and the field is too close to the isolator. However, in actual use, the Si84xx devices provide extremely high immunity to external magnetic fields and have been independently evaluated to withstand magnetic fields of at least 1000 A/m according to the IEC 61000-4-8 and IEC 61000-4-9 specifications.



**Figure 14. Dipole Antenna**

## 5. Typical Application Overview

### 5.1. I<sup>2</sup>C Background

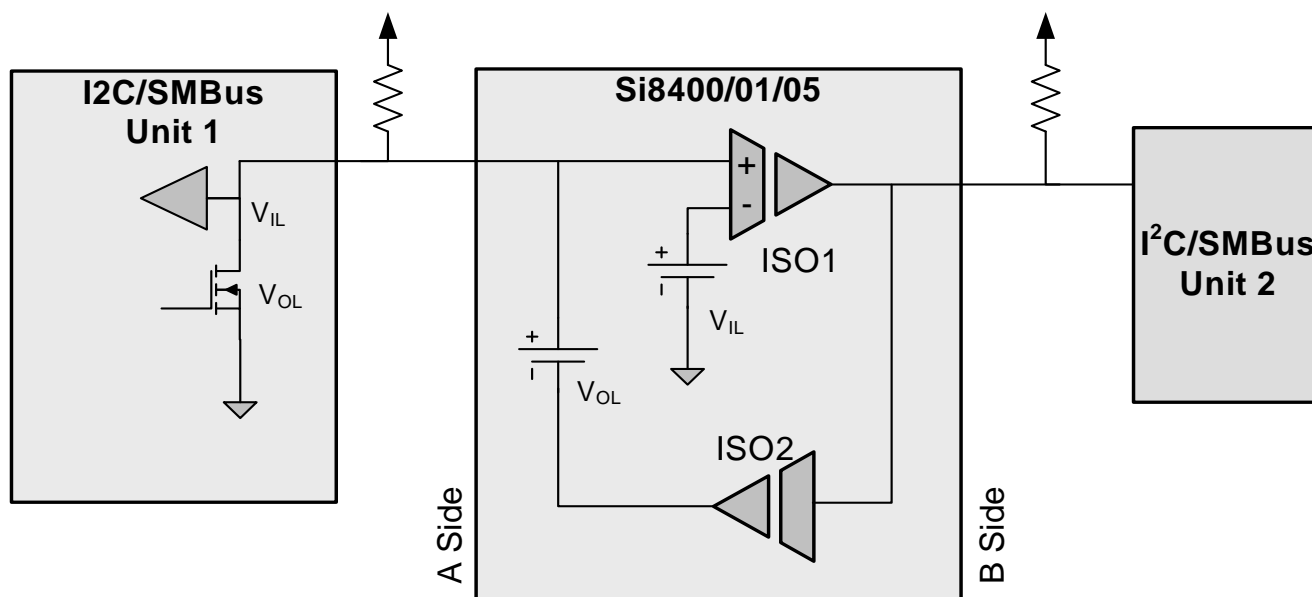
In many applications, I<sup>2</sup>C, SMBus, and PMBus interfaces require galvanic isolation for safety or ground loop elimination. For example, Power over Ethernet (PoE) applications typically use an I<sup>2</sup>C interface for communication between the PoE power sourcing device (PSE), and the earth ground referenced system controller. Galvanic isolation is required both by standard and also as a practical matter to prevent ground loops in Ethernet connected equipment.

The physical interface consists of two wires: serial data (SDA) and serial clock (SCL). These wires are connected to open collector drivers that serve as both inputs and outputs. At first glance, it appears that SDA and SCL can be isolated simply by placing two unidirectional isolators in parallel, and in opposite directions. However, this technique creates feedback that latches the bus line low when a logic low asserted by either master or slave. This problem can be remedied by adding anti-latch circuits, but results in a larger and more expensive solution. The Si840x products offer a single-chip, anti-latch solution to the problem of isolating I<sup>2</sup>C/SMBus applications and require no external components except the I<sup>2</sup>C/SMBus pull-up resistors. In addition, they provide isolation to a maximum of 2.5 kV<sub>RMS</sub>, support I<sup>2</sup>C clock stretching, and operate to a maximum I<sup>2</sup>C bus speed of 1.7 Mbps.

### 5.2. I<sup>2</sup>C Isolator Operation

Without anti-latch protection, bidirectional I<sup>2</sup>C isolators latch when an isolator output logic low propagates back through an adjacent isolator channel creating a stable latched low condition on both sides. Anti-latch protection is typically added to one side of the isolator to avoid this condition (the "A" side for the Si8400/01/05).

The following examples illustrate typical circuit configurations using the Si8400/01/05.



**Figure 15. Isolated Bus Overview**

The "A side" output low ( $V_{OL}$ ) and input low ( $V_{IL}$ ) levels are designed such that the isolator  $V_{OL}$  is greater than the isolator  $V_{IL}$  to prevent the latch condition.

## 5.3. I<sup>2</sup>C Isolator Design Constraints

Table 14 lists the design constraints.

**Table 14. Design Constraints**

Design Constraint	Data Sheet Values	Effect of Bus Pull-up Strength and Temperature
To prevent the latch condition, the isolator output low level must be greater than the isolator input low level.	Isolator $V_{OL}$ 0.8 V typical Isolator $V_{IL}$ 0.6 V typical  Input/Output Logic Low Level Difference $\Delta V_{SDA1}, \Delta V_{SCL1} = 50$ mV minimum	This is normally guaranteed by the isolator data sheet. However, if the pull up strength is too weak, the output low voltage will fall and can get too close to the input low logic level. These track over temperature.
The bus output low must be less than the isolator input low logic level.	Bus $V_{OL} = 0.4$ V maximum  Isolator $V_{IL} = 0.45$ V minimum	If the pull up strength is too large, the devices on the bus might not pull the voltage below the input low range. These have opposite temperature coefficients. Worst case is hot temperature.
The isolator output low must be less than the bus input low.	Bus $V_{IL} 0.3 \times V_{DD} = 1.0$ V minimum for $V_{DD} = 3.3$ V  Isolator $V_{OL} = 0.825$ V maximum, (0.5 mA pullup, $-10$ to $125$ °C)	If the pull up strength is too large, the isolator might not pull below the bus input low voltage. Si8400/01/05 Vol: $-1.8$ mV/C CMOS buffer: $-0.6$ mV/C This provides some temperature tracking, but worst case is cold temperature.

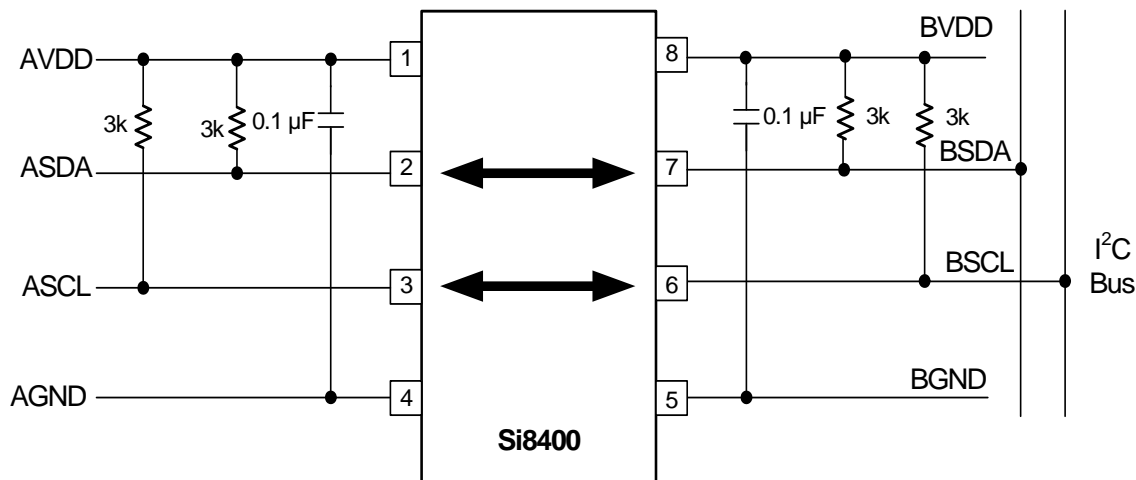
## 5.4. I<sup>2</sup>C Isolator Design Considerations

The first step in applying an I<sup>2</sup>C isolator is to choose which side of the bus will be connected to the isolator A side. Ideally, it should be the side which:

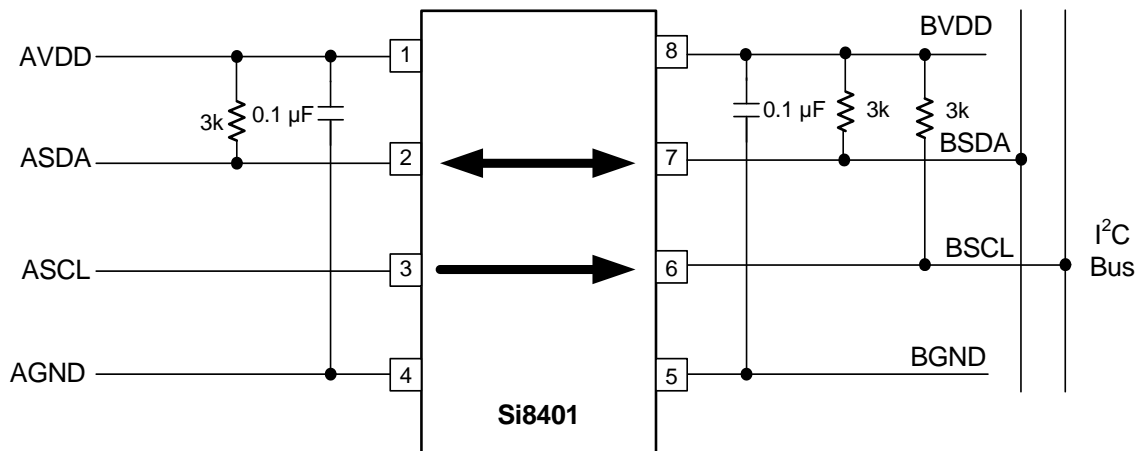
1. Is compatible with the range of bus pull up specified by the manufacturer. For example, the Si8400/01/05 isolators are normally used with a pull up of 0.5 mA to 3 mA.
2. Has the highest input low level for devices on the bus. Some devices may specify an input low of 0.9 V and other devices might require an input low of  $0.3 \times V_{DD}$ . Assuming a 3.3 V minimum power supply, the side with an input low of  $0.3 \times V_{DD}$  is the better side because this side has an input low level of 1.0 V.
3. Have devices on the bus that can pull down below the isolator input low level. For example, the Si840x input level is 0.45 V. As most CMOS devices can pull to within 0.4 V of GND this is generally not an issue.
4. Has the lowest noise. Due to the special logic levels, noise margins can be as low as 50 mV.

The Si840x isolators are not compatible with devices that have a logic low of 0.8 V. For this situation, a discrete circuit can be used. See “AN352: Low-Cost, High-Speed I<sup>2</sup>C Isolation with Digital Isolators” for additional information.

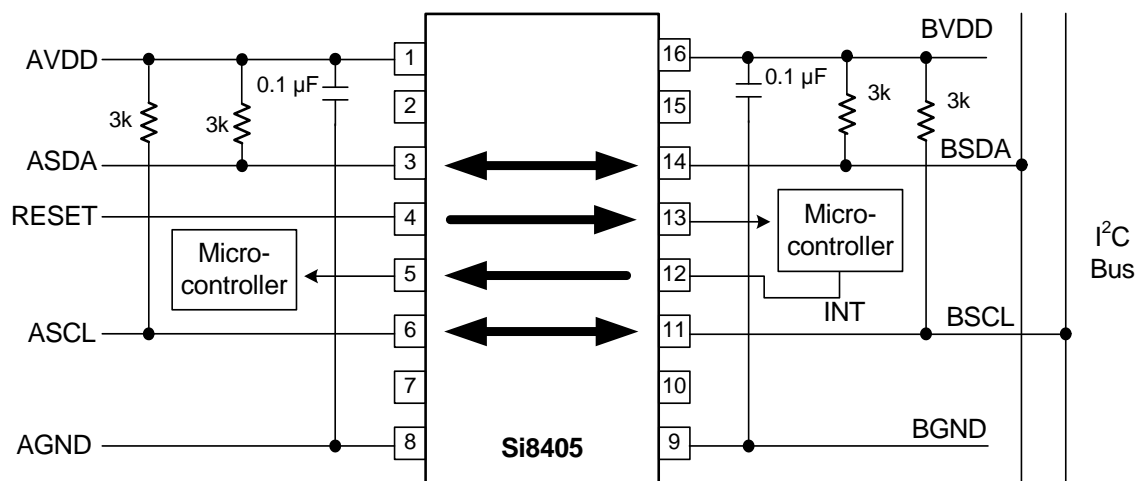
Figures 16, 17, and 18 illustrate typical circuit configurations using the Si8400, Si8401, and Si8405.



**Figure 16. Typical Si8400 Application Diagram**



**Figure 17. Typical Si8401 Application Diagram**



**Figure 18. Typical Si8405 Application Diagram**

## 6. Errata and Design Migration Guidelines (Revision A Only)

The following errata apply to Revision A devices only. See "8. Ordering Guide" on page 25 for more details. No errata exist for Revision B devices.

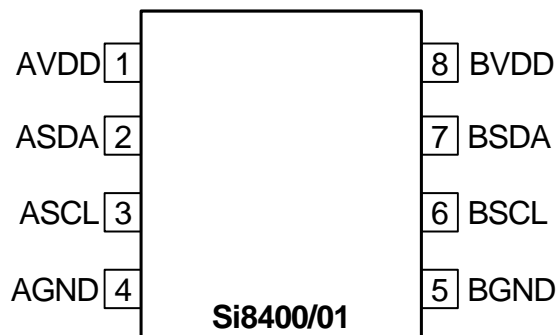
### 6.1. Power Supply Bypass Capacitors (Revision A Only)

When using the ISOpro isolators with power supplies  $\geq 4.5$  V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than  $0.5 \text{ V}/\mu\text{s}$  (which is  $> 9 \mu\text{s}$  for a  $\geq 4.5$  V supply). Although rise time is power supply dependent,  $\geq 1 \mu\text{F}$  capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

#### 6.1.1. Resolution

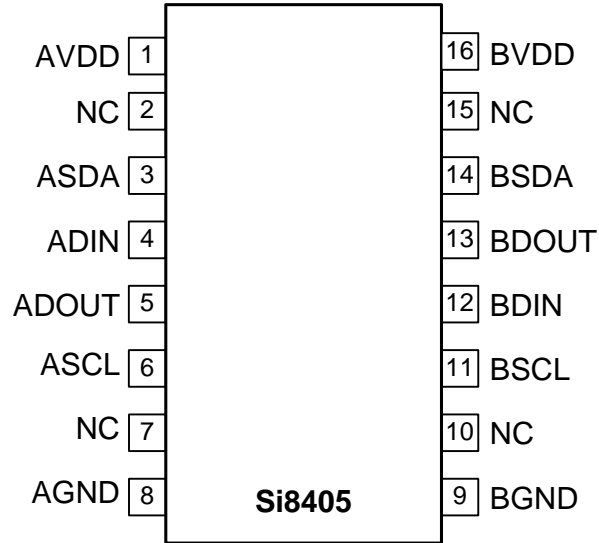
This issue has been corrected with Revision B of the device. Refer to "8. Ordering Guide" for current ordering information.

## 7. Pin Descriptions



**Table 15. Si8400/01 in SO-8 Package**

Pin	Name	Description
1	AVDD	Side A power supply terminal; connect to a source of 3.0 to 5.5 V.
2	ASDA	Side A data input or output.
3	ASCL	Side A clock input or output (Si8400); Side A clock input (Si8401).
4	AGND	Side A ground terminal.
5	BGND	Side B ground terminal.
6	BSCL	Side B clock input or output (Si8400); Side B clock output (Si8401).
7	BSDA	Side B data input or output.
8	BVDD	Side B power supply terminal; connect to a source of 3.0 to 5.5 V.



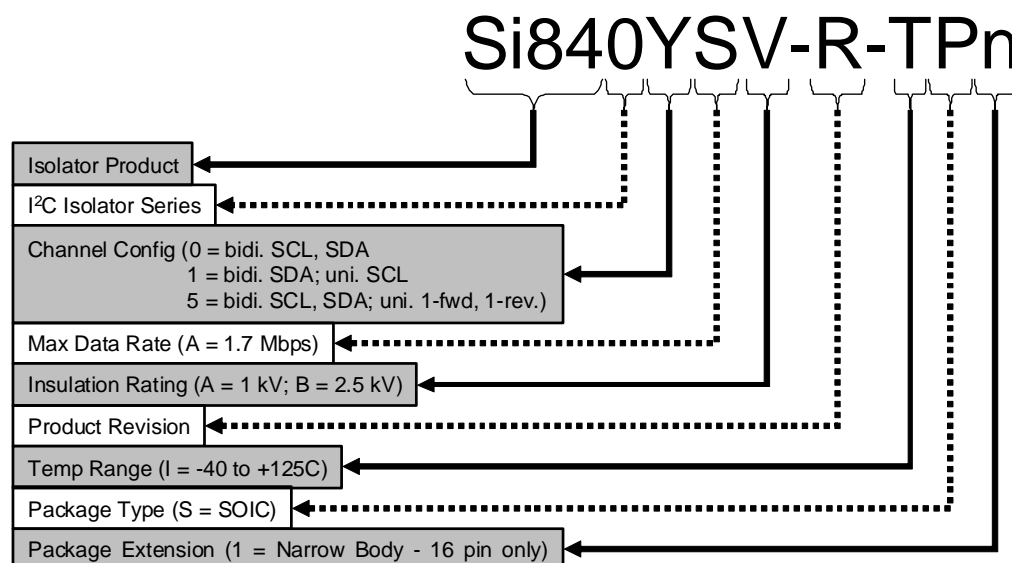
**Table 16. Si8405 in Narrow-Body SO-16 Package**

Pin	Name	Description
1	AVDD	Side A Power Supply Terminal. Connect to a source of 3.0 to 5.5 V.
2	NC	No connection.
3	ASDA	Side A Data Input or Output.
4	ADIN	Side A Digital Input (non I <sup>2</sup> C).
5	ADOUT	Side A Digital Output (non I <sup>2</sup> C).
6	ASCL	Side A Clock Input or Output.
7	NC	No connection.
8	AGND	Side A Ground Terminal.
9	BGND	Side B Ground Terminal.
10	NC	No connection.
11	BSCL	Side B Clock Input or Output.
12	BDIN	Side B Digital Input (non I <sup>2</sup> C).
13	BDOUT	Side B Digital Output (non I <sup>2</sup> C).
14	BSDA	Side B Data Input or Output.
15	NC	No connection.
16	BVDD	Side B Power Supply Terminal. Connect to a source of 3.0 to 5.5 V.



## 8. Ordering Guide

Revision B devices are recommended for all new designs.



**Figure 19. Naming Convention**

**Table 17. Ordering Guide<sup>1</sup>**

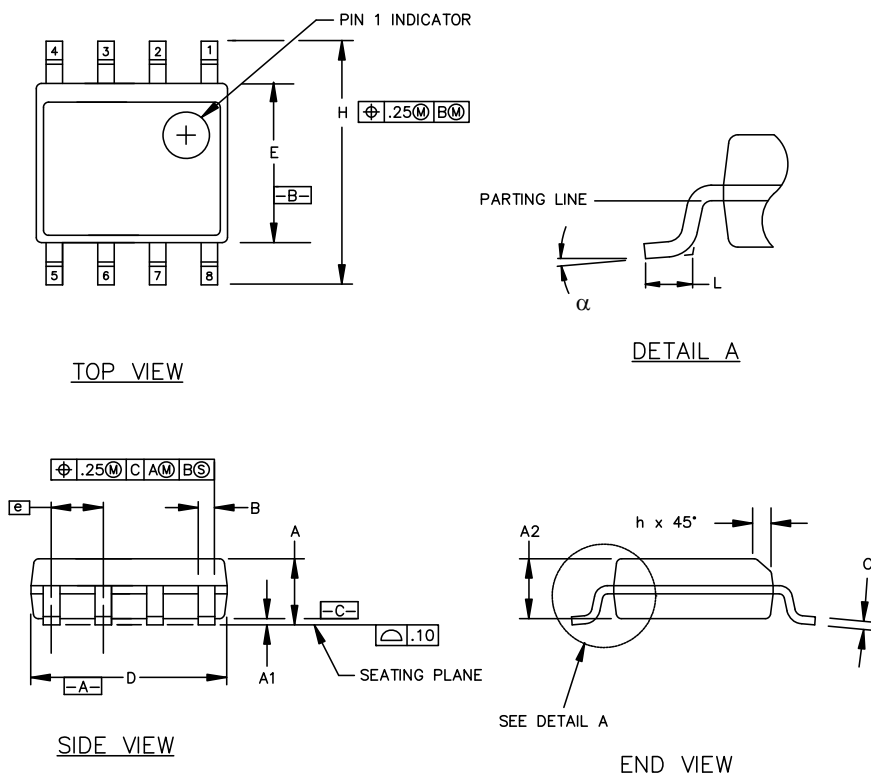
Ordering Part Number	Number of Bidirectional I <sup>2</sup> C Channels	Max I <sup>2</sup> C Bus Speed (MHz)	Number of Unidirectional Channels	Max Data Rate of Non-I <sup>2</sup> C Unidirectional Channels (Mbps)	Isolation Ratings	Temp Range (°C)	Package
Si8400AA-B-IS	2	1.7	0	—	1 kV <sub>RMS</sub>	–40 to 125	NB SOIC-8
Si8400AB-B-IS	2	1.7	0	—	2.5 kV <sub>RMS</sub>	–40 to 125	NB SOIC-8
Si8401AA-B-IS	1	1.7	1	—	1 kV <sub>RMS</sub>	–40 to 125	NB SOIC-8
Si8401AB-B-IS	1	1.7	1	—	2.5 kV <sub>RMS</sub>	–40 to 125	NB SOIC-8
Si8405AA-B-IS1	2	1.7	1 forward 1 reverse	10	1 kV <sub>RMS</sub>	–40 to 125	NB SOIC-16
Si8405AB-B-IS1	2	1.7	1 forward 1 reverse	10	2.5 kV <sub>RMS</sub>	–40 to 125	NB SOIC-16
<b>Revision A Devices<sup>2</sup></b>							
Si8400AA-A-IS <sup>2</sup>	2	1.7	0	—	1 kV <sub>RMS</sub>	–40 to 125	NB SOIC-8
Si8400AB-A-IS <sup>2</sup>	2	1.7	0	—	2.5 kV <sub>RMS</sub>	–40 to 125	NB SOIC-8
Si8405AA-A-IS1 <sup>2</sup>	2	1.7	1 forward 1 reverse	10	1 kV <sub>RMS</sub>	–40 to 125	NB SOIC-16
Si8405AB-A-IS1 <sup>2</sup>	2	1.7	1 forward 1 reverse	10	2.5 kV <sub>RMS</sub>	–40 to 125	NB SOIC-16

**Notes:**

- All packages are RoHS-compliant. Moisture sensitivity level is MSL2A with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.
- Revision A devices are supported for existing designs, but Revision B is recommended for all new designs.

## 9. Package Outline: 8-Pin Narrow Body SOIC

Figure 20 illustrates the package details for the Si840x in an 8-pin SOIC (SO-8). Table 18 lists the values for the dimensions shown in the illustration.



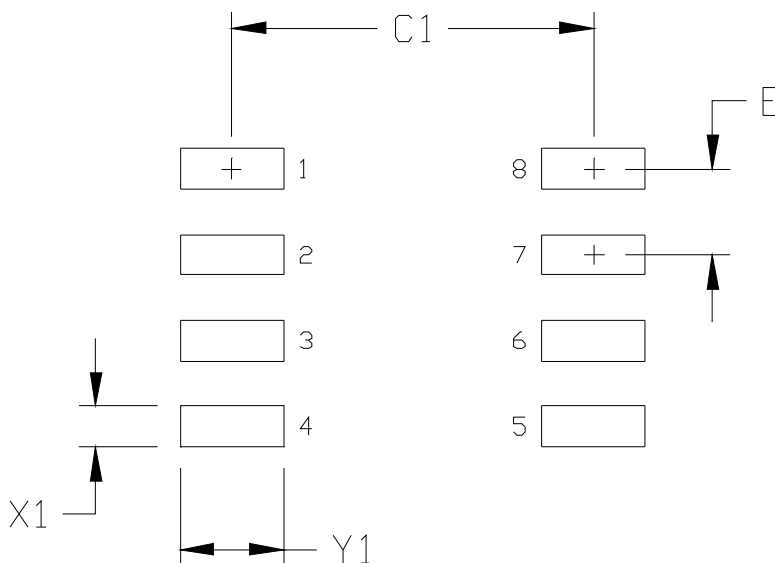
**Figure 20. 8-pin Small Outline Integrated Circuit (SOIC) Package**

**Table 18. Package Diagram Dimensions**

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

## 10. Landing Pattern: 8-Pin Narrow Body SOIC

Figure 21 illustrates the recommended landing pattern details for the Si840x in an 8-pin narrow-body SOIC. Table 19 lists the values for the dimensions shown in the illustration.



**Figure 21. PCB Landing Pattern: 8-Pin Narrow Body SOIC**

**Table 19. PCM Landing Pattern Dimensions (8-Pin Narrow Body SOIC)**

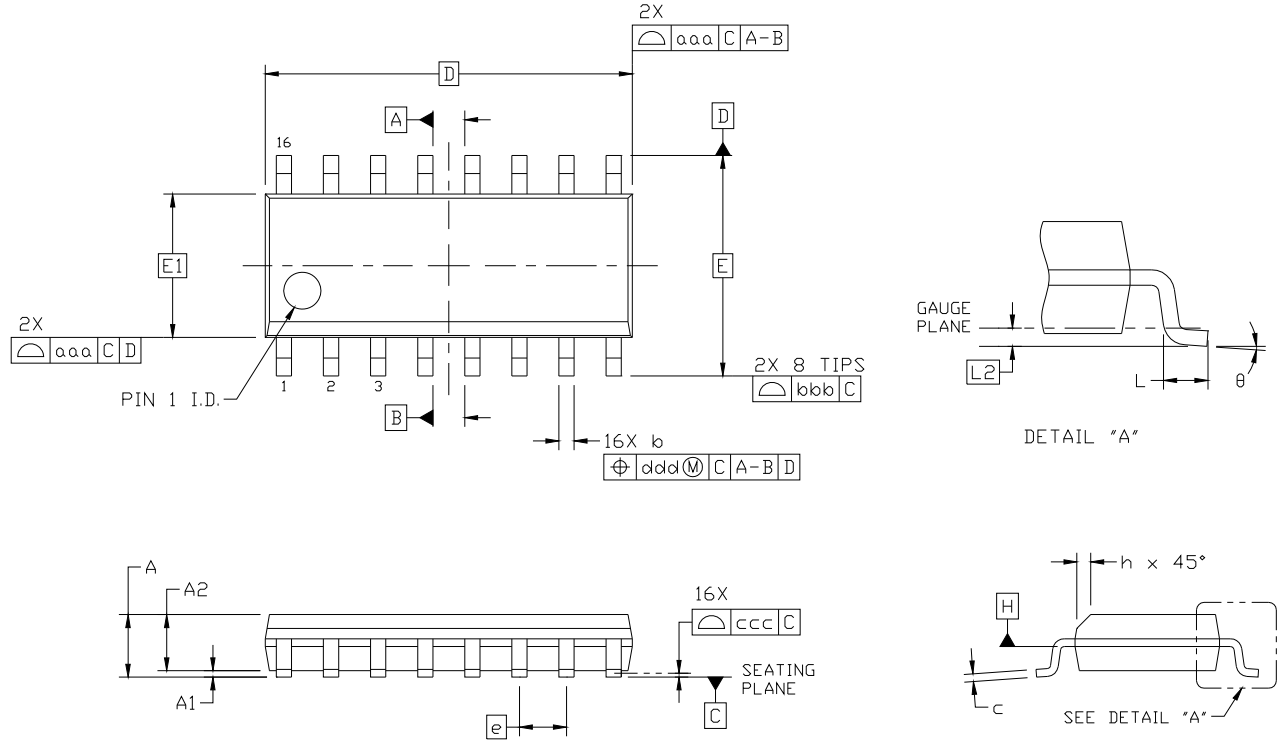
Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

**Notes:**

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 11. Package Outline: 16-Pin Narrow Body SOIC

Figure 22 illustrates the package details for the Si840x in a 16-pin narrow-body SOIC (SO-16). Table 20 lists the values for the dimensions shown in the illustration.



**Figure 22. 16-pin Small Outline Integrated Circuit (SOIC) Package**

**Table 20. Package Diagram Dimensions**

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Table 20. Package Diagram Dimensions (Continued)

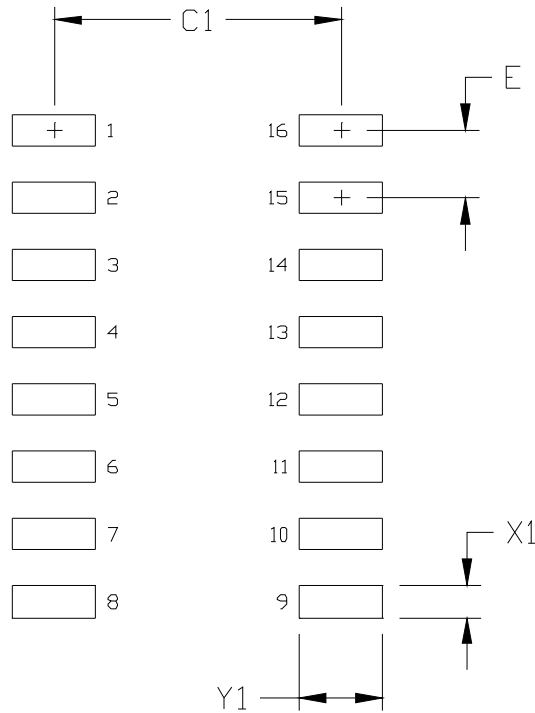
Dimension	Min	Max
h	0.25	0.50
$\theta$	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 12. Landing Pattern: 16-Pin Narrow Body SOIC

Figure 23 illustrates the recommended landing pattern details for the Si840x in a 16-pin narrow-body SOIC. Table 21 lists the values for the dimensions shown in the illustration.



**Figure 23. 16-Pin Narrow Body SOIC PCB Landing Pattern**

**Table 21. 16-Pin Narrow Body SOIC Landing Pattern Dimensions**

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

**Notes:**

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 13. Top Marking: 8-Pin Narrow Body SOIC

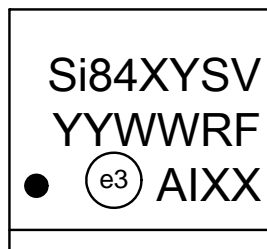


Figure 24. 8-Pin Narrow Body SOIC Top Marking

Table 22. 8-Pin Narrow Body SOIC Top Marking Table

<b>Line 1 Marking:</b>	Base Part Number Ordering Options  (See Ordering Guide for more information).	Si84 = Isolator I <sup>2</sup> C Product Series: <ul style="list-style-type: none"> <li>■ XY = Channel Configuration <ul style="list-style-type: none"> <li>● 00 = Bidirectional SCL and SDA channels</li> <li>● 01 = Bidirectional SDA channel; Unidirectional SCL channel</li> </ul> </li> <li>■ S = Speed Grade <ul style="list-style-type: none"> <li>● A = 1.7 Mbps</li> </ul> </li> <li>■ V = Isolation rating <ul style="list-style-type: none"> <li>● A = 1 kV; B = 2.5 kV</li> </ul> </li> </ul>
<b>Line 2 Marking:</b>	YY = Year WW = Work week	Assigned by assembly contractor. Corresponds to the year and work week of the mold date.
	R = Product Rev F = Wafer Fab	First two characters of the manufacturing code from Assembly.
<b>Line 3 Marking:</b>	Circle = 1.1 mm Diameter Left-Justified	"e3" Pb-Free Symbol
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last four characters of the manufacturing code from assembly.

## 14. Top Marking: 16-Pin Narrow Body SOIC

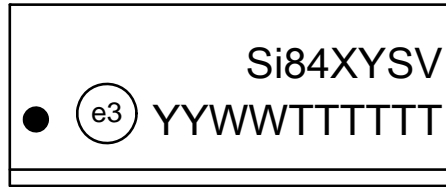


Figure 25. 16-Pin Narrow Body SOIC Top Marking

Table 23. 16-Pin Narrow Body SOIC Top Marking Table

<b>Line 1 Marking:</b>	Base Part Number Ordering Options	Si84 = Isolator product series <ul style="list-style-type: none"> <li>■ XY = Channel Configuration <ul style="list-style-type: none"> <li>• 05 = Bidirectional SCL, SDA; 1- forward and 1-reverse unidirectional channel</li> </ul> </li> <li>■ S = Speed Grade <ul style="list-style-type: none"> <li>• A = 1.7 Mbps</li> </ul> </li> <li>■ V = Isolation rating <ul style="list-style-type: none"> <li>• A = 1 kV; B = 2.5 kV</li> </ul> </li> </ul>	
	<b>Line 2 Marking:</b>	Circle = 1.2 mm Diameter	"e3" Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.	
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.	
	Circle = 1.2 mm diameter	"e3" Pb-Free Symbol.	



## DOCUMENT CHANGE LIST

### Revision 0.1 to Revision 1.0

- Updated document to reflect availability of Revision B silicon.
- Updated Tables 1, 2, 3, and 4.
  - Updated all supply currents and timing parameters.
  - Revised logic low output voltage specifications in Table 2.
- Updated Table 5.
  - Updated absolute maximum supply voltage.
- Updated Table 7.
  - Updated clearance and creepage dimensions.
- Updated "6.Errata and Design Migration Guidelines (Revision A Only)" on page 22.
- Updated "8.Ordering Guide" on page 25.

### Revision 1.0 to Revision 1.1

- Updated Table 3.
  - Updated Note 1 to reflect output impedance of 85  $\Omega$ .
  - Updated rise and fall time specifications.
- Updated Table 4.
  - Updated CMTI value.
- Updated "8. Ordering Guide".
- Added Si8401 device configuration throughout document.

### Revision 1.1 to Revision 1.2

- Updated document throughout to include MSL improvements to MSL2A.
- Updated "8.Ordering Guide" on page 25.
  - Updated Note 1 in ordering guide table to reflect improvement and compliance to MSL2A moisture sensitivity level.

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