Data Sheet
June 1995

AT&T Microelectronics

ATT20C567: 64-Bit Pixel Interface True-Color CMOS RAMDAC 3D Animation DAC

Features

- 170/135/110 MHz, 0.6 µm CMOS
- Software-configurable 64-bit, 32-bit, or 16-bit pixel port
- Full-scale DAC currents trimmed to ±3% (typical)
- Includes:
  - — Three 256 x 8 pixel look-up table RAMs
  - — Three 256 x 8 look-up table ROMs
  - — Three 4 x 8 overlay RAMs
  - — Three 8-bit *PrecisionDACs*
  - — Synchronous analog PLL Eliminates dead zone for $\overline{\text{LOAD}}$ clock
- Pixel formats supported:
  - — 8-8-8 true color with overlays
  - — 5-6-5 *XGA** with overlays
  - — 5-5-5 true color with overlays
  - — 4-4-4 true color with overlays
  - — 8-bit pseudocolor with overlays
- Supports:
  - — 2:1, 4:1, and 8:1 pixel formats
  - — Double-frame buffers for 4-4-4 true color and 8-bit pseudocolor
  - — On-the-fly color change for 8-8-8 true color, 5-5-5 true color 4-4-4 true color
  - — 3.3 V data I/O interface
  - — Powerdown mode
- Embedded visual control bits selects between:
  - — Color RAMs
  - — Gamma correction ROMs
  - — Bypass memory (direct to DACs)
  - — 8-bit pseudocolor pixel format
  - — Frame-buffer switching
- Register compatible with ATT20C458 and Bt467
- RS-343A and RS-170 compatible
- 132-pin JEDEC BQFP package

Applications

- Screen resolutions (interlaced)
  - — 1280 x 1024, 80 Hz, 16M colors
  - — 1600 x 1280, 60 Hz, 16M colors
- True-color workstations, PC/card
- *X-Windows*† terminals

Description

The ATT20C567 CMOS RAMDAC supports pixel-by-pixel selection of true color and pseudocolor by using embedded visual control bits. The visual control bits allow selection of double- or single-frame buffer operation.

The device can be programmed or hardware reset into a standard 467 RAMDAC workstation graphics architecture. The device is software compatible with a 467-type RAMDAC and allows an easy software upgrade path. In the 467 compatible mode, 8-bit pixels are 8:1 multiplexed.

The ATT20C567 inputs multiplexed pixels through a 64-bit wide port. Multiplexing ranges from eight 8-bit pixels to two 32-bit pixels. A 32-bit pixel consists of 24 bits of true color with up to 4 bits for visual control. An internal analog PLL synchronously multiplies the $\overline{\text{LOAD}}$ clock 2, 4, or 8 times to generate the internal pixel clock. In this mode, the ATT20C567 can operate with the $\overline{\text{LOAD}}$ clock only. A pixel clock is not required.

A unique feature of the ATT20C567 is the ability to embed pixel format control in the frame buffer which allows changing color formats on the fly. This enables an unlimited number of true-color windows in a pseudocolor background.

* *XGA* is a registered trademark of International Business Machines Corporation.
† *X-Windows* is a registered trademark of Massachusetts Institute of Technology.

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Description (continued)

A microprocessor port configures the internal registers and writes and reads the internal RAMs. The device includes three 256 x 8 pixel color look-up tables (CLUTs), three 4 x 8 overlay color RAMs, and three 256 x 8 gamma correction ROMs displaying 16.8M possible colors. The device has three 8-bit DACs. An on-chip voltage reference is used to trim the DAC currents (typical) to within ±3% (typical). Use of internal VREF will provide these specifications; external VREF may degrade the device specifications. The device is offered in an 132-pin JEDEC BQFP package with or without a heat spreader.

Overview

The ATT20C567 CMOS RAMDAC is a cost-effective solution for workstations, optimized for graphical user interface like *X-Windows*. It offers multiple multiplex modes and support for various visual classes on the fly includes an on-chip clock multiplier, three pixel and overlay RAMs, three ROMs, and three DACs. The backward register compatibility of the device with the ATT20C458 and Bt467 offers easy system software upgrade. A block diagram is shown in Figure 1.

The ATT20C567 is available in three speed grades: 110 MHz, 135 MHz, and 170 MHz. The device operation at 170 MHz results in a refresh rate of 80 Hz for 1280 x 1024 pixel size and 60 Hz for 1600 x 1280 pixel size.

The device can be used in high-end workstations supporting true-color schemes using 32-bit pixels with visual control on the fly for every pixel, and also in low-end workstations using 8-bit pixels in pseudocolor mode. It also supports 16-bit pixel mode with 5-5-5 or 5-6-5 bits for red, green, and blue colors.

The ATT20C567 pixel port is software configurable to be 64 bits, 32 bits, or 16 bits wide, and the overlay data port is programmable to be 16 bits, 8 bits, or 4 bits wide. This offers versatile frame buffer configuration.

The support for 2:1, 4:1, and 8:1 multiplex modes facilitates the frame buffer memory to operate at 1/8 to 1/2 the frequency of the RAMDAC. At the same time, this allows loading of up to eight pixels in one cycle resulting in enhanced performance at lower memory cost.

The ATT20C567 analog clock multiplier ensures easier board design for high-frequency operation and also eliminates the need for costly ECL crystal oscillators. The PLL logic on the device is capable of multiplying an external load clock by 2, 4, or 8, depending on the number of bits per pixel and pixel port size. For example, when a 64-bit pixel port is used, the multiplying factor is two with a 32-bit pixel, four with a 16-bit pixel, and eight with an 8-bit pixel.

The multiplication factor is automatically determined when the pixel port size and the bits per pixel are configured by initializing control registers. An optional clock output, SCLK, is available to generate the VRAM shift clock. The SCLK frequency depends on the multiplex factor. This clock is not required when PLL is used. This results in relaxed setup and hold times for pixel data relative to load clock which eases the system design.

The ATT20C567 includes three 256-byte color look-up tables (CLUTs), three 4-byte overlay CLUTs, three 256-byte ROMs, and three DACs, one each for red, blue, and green colors. The index mode allows a standard or private color cell allocation for an application. The mapping through ROM in gamma-correction mode facilitates linear true-color display. The ROMs and RAMs can be bypassed if a design has a mapping scheme in external logic. The user can select between the three options in real time by changing a register value or using the visual control bits in 16-bit and 32-bit pixel modes on a pixel-by-pixel basis.

The support for various color schemes by ATT20C567 allows the workstations to run different applications requiring different color capabilities by selecting various visual classes on a window-by-window basis. It may be possible for a workstation screen to have a desktop publishing application requiring a monochrome color scheme in one window, an 8-bit pixel diagram application in the other window, and yet another window running a CAD/CAM application with 24-bit pixel true color.

The ATT20C567 supports any combination of six basic visual classes—pseudocolor, direct color, gray scale, static color, true color, and static gray, all available in *X-Windows*, on the same screen.

The ATT20C567 supports two banks of VRAM. The information from either bank can be displayed in 32-bit pixel mode on the fly. This feature expedites frame buffer switching. It is also helpful in CAD/CAM applications using 3-D modeling and rotation.

A separate power input pin is provided for the output buffers. For low-voltage applications, this input can be connected to a 3.3 V power source. The ATT20C567 also supports sleep mode in which the pixel clock can be disabled to reduce power dissipation. The RAMs retain data and can be accessed for read or write operations by the MPU.

Overview (continued)

A block diagram of a system using the ATT20C567 is depicted in Figure 2 (the design requires minimal external logic). The SCLK and $\overline{\text{LOAD}}$ frequencies should be 67.5 MHz for 2:1 multiplex mode, 33.75 MHz for 4:1 multiplex mode, and 16.875 for 8:1 multiplex mode when 135 MHz ATT20C567 is used. For true-color operation, the system requires separate memories for red, blue, and green colors.

The visual bits may be implemented in memory or hardwired, depending on the application. The frame buffer can consist of a single bank for 64-bit interface with the video controller. Double-bank configuration is required for 128-bit interface. The 128-bit frame buffer also requires an external 2:1 multiplexer to generate 64-bit pixel input for the ATT20C567. Refer to the Application Information section for various application examples.

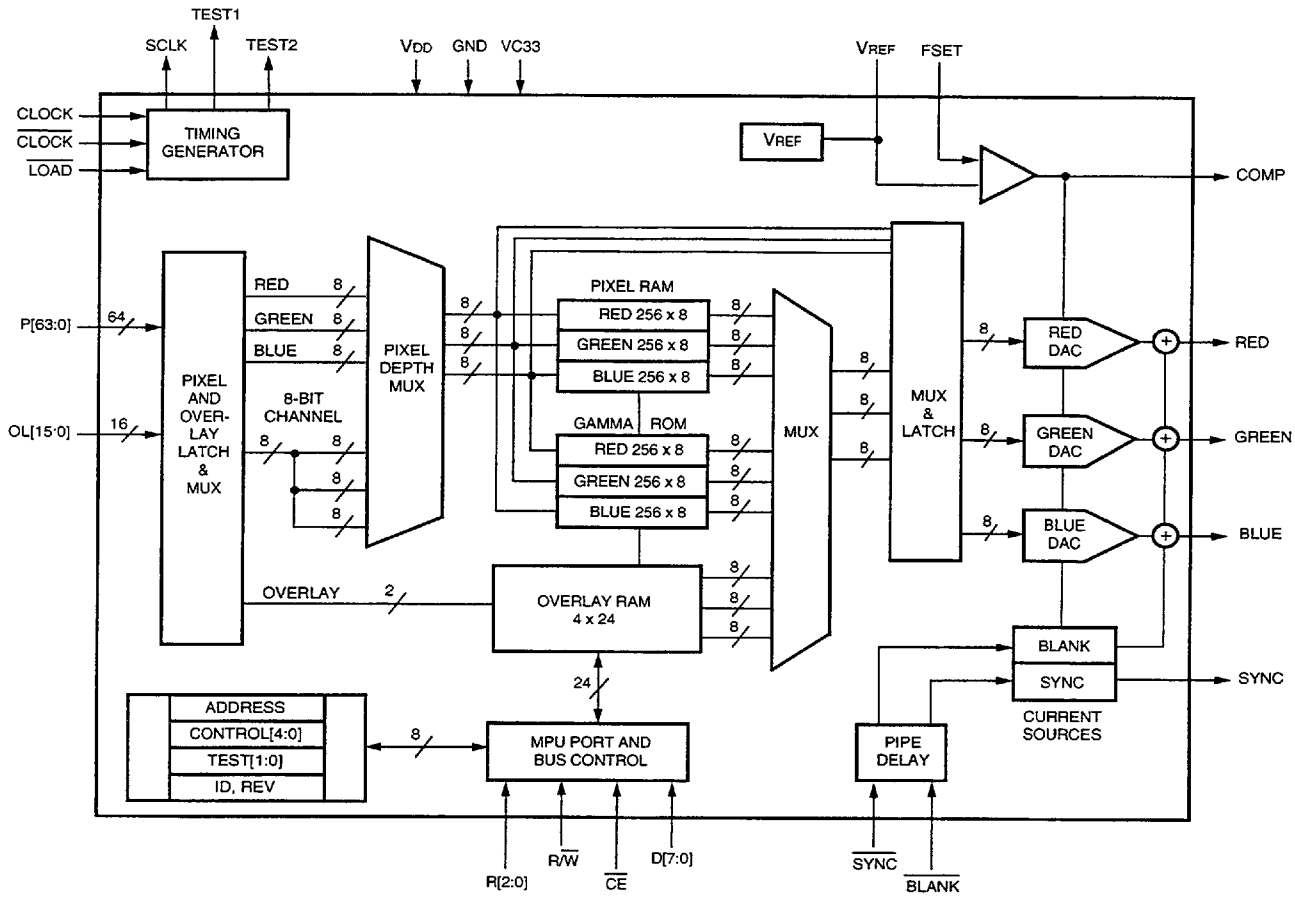
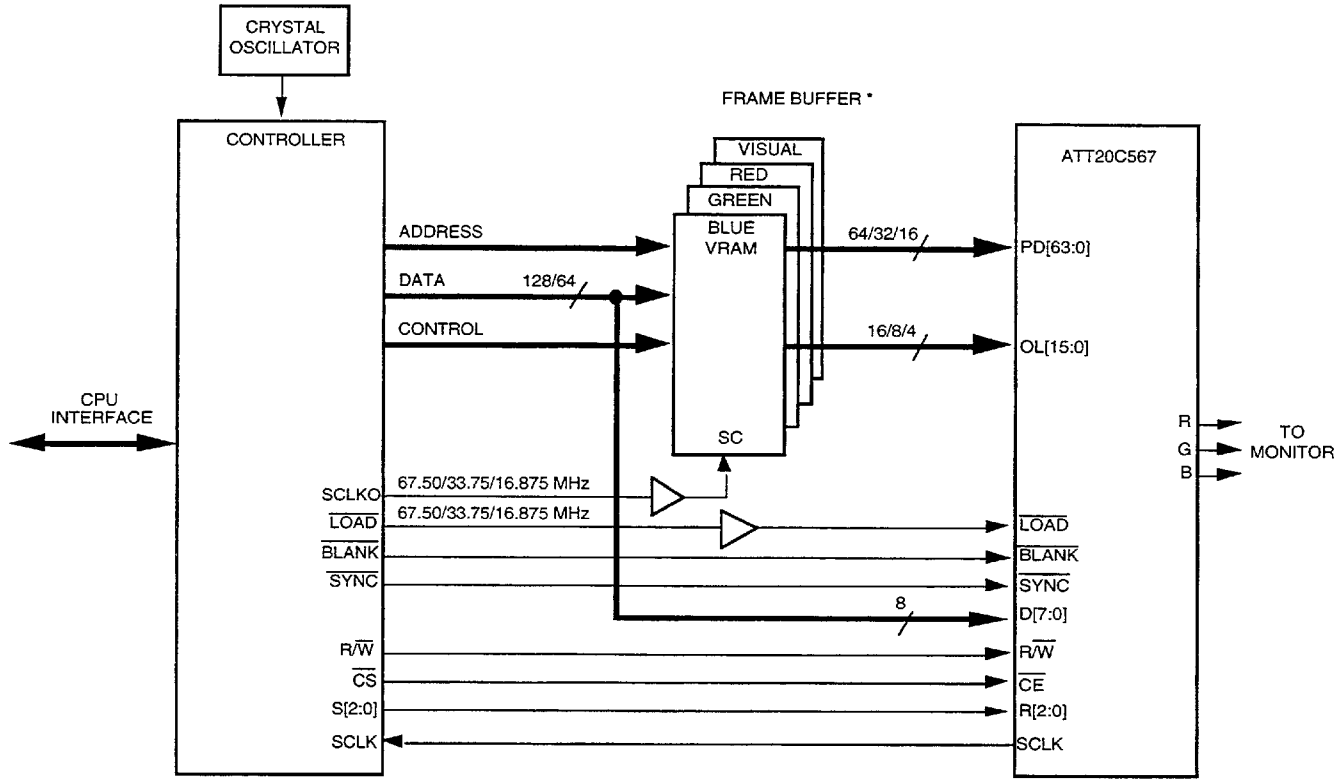


Figure 1. Block Diagram

Overview (continued)



* Single bank for 64-bit input data, double bank for 128-bit input data requires external MUX.

Figure 2. System Diagram

Pin Information

Table 1. Distribution of Pins

Pins	Quantity
Pixel	64
Overlay	16
MPU	13
Pixel Control Inputs: CLOCK, $\overline{\text{CLOCK}}$, $\overline{\text{LOAD}}$, $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, RESET, SCLK, TEST1, and TEST2	9
Video Output: V_{REF}, COMP, FSET, and SYOUT	4
DACs	3
V_{CC}	9
GND	10
VC33	2
NC	2
Total	132

Pin Information (continued)

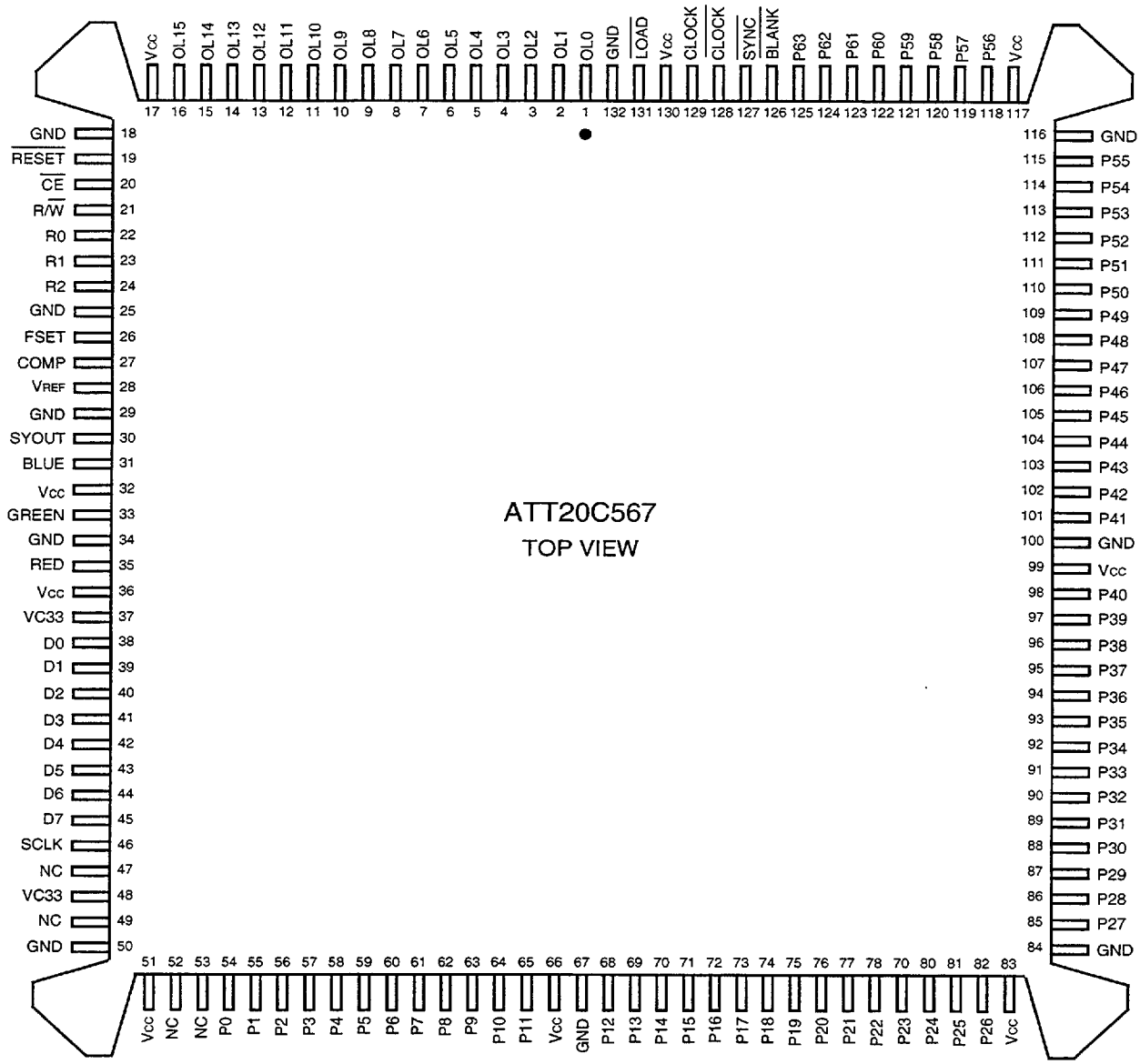


Figure 3. 132-Pin PQFP Diagram

Pin Information (continued)

Table 2. Pin Descriptions

Pin #	Symbol	Type	Name/Function
16—1	OL[15:0]	I	**Overlays.** TTL compatible. Two, four, or eight consecutive overlay values are input through this port on the rising edge of $\overline{LOAD}$. The overlay values, together with the control register bits, determine whether pixel or overlay information is displayed. When the overlays are selected, the pixel inputs are ignored. Unused inputs should be tied to ground.
17, 32, 36, 51, 66, 83, 99, 117, 130	Vcc	—	**Power (+5 V).**
18, 25, 29, 34, 50, 67, 84, 100, 116, 132	GND	—	**Ground.**
19	$\overline{RESET}$	I	**Reset (Active-Low).** TTL compatible. This pin resets the control register bits and places the device in a 467-type RAMDAC mode.
20	$\overline{CE}$	I	**Chip Enable (Active-Low).** TTL compatible. This input must be low to enable reading or writing to the MPU port. During write operations, D[7:0] is latched on the rising edge of $\overline{CE}$. Avoid glitches on this edge-triggered input.
21	R/$\overline{W}$	I	**Read/Write Control (Active-Low).** TTL compatible. R/$\overline{W}$ is latched on the falling edge of $\overline{CE}$. The R[2:0] inputs, together with the internal address register, control the read/write operation of the pixel color RAM, overlay color RAM, and control registers. A logic 0 on R/$\overline{W}$ corresponds to a write operation.
24—22	R[2:0]	I	**Control.** TTL compatible. These inputs are latched on the falling edge of $\overline{CE}$ to determine which one of the internal registers is to be accessed.
26	FSET	I	**Full-Scale Set Connection.** An external resistor (RSET) is connected between the FSET pin and GND to control the magnitude of the full-scale current.
27	COMP	—	**Compensation Pin.** Bypass this pin with an external 0.1 µF capacitor to Vcc.
28	VREF	I	**Voltage Reference.** If an external voltage is used, it must supply this input with a 1.235 V reference. To use the internal voltage reference, bypass this pin to GND with 0.1 µF.
30	SYOUT	O	**Synchronize.** This pin provides analog output delay information to a clock generator chip. This information is used when more than one ATT20C567 is used in parallel. By sampling the time difference of the SYOUT signals, the clock chip may then skew the individual clock signals between the RAMDACs to line up the red, green, and blue DAC outputs. In addition, this output can be tied to any one of the R, G, B outputs to generate composite sync.
31 33 35	BLUE GREEN RED	O	**Color Signals.** These pins are analog outputs. High-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable. The SYOUT pin may be tied to any one of the R, G, B outputs to provide composite sync.
37, 48	VC33	I	**Power (+3.3 V).** This pin provides 3.3 V Vcc power to the D[7:0] I/O pins and the SCLK output pin. In a +5 V design, tie VC33 pins to the +5 V power plane. In a design using 3.3 V Vcc and I/O logic levels, tie VC33 pins to the 3.3 V supply.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

Pin #	Symbol	Type	Name/Function
45—38	D[7:0]	I/O	**Data Bus.** TTL compatible. Internal register addresses and data are transferred over this port under control of the R[2:0], $\overline{CE}$, and R/$\overline{W}$ signals. In an MPU write operation, D[7:0] is latched on the rising edge of $\overline{CE}$. To read data D[7:0] from the device, R/$\overline{W}$ must be in an active-high state. The rising edge of the $\overline{CE}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. D0 is the LSB. For 3.3 V designs, the D[7:0] pins support 3.3 V logic levels when the VC33 power pins are connected to 3.3 V.
46	SCLK	O	**Shift Clock.** TTL compatible. Shift clock is meant to clock the video RAMs in the frame buffer. The output frequency is the pixel clock frequency divided by the multiplex ratio (SCLK = clock/MUX ratio). SCLK supports 3.3 V logic levels when the VC33 power pins are connected to 3.3 V.
47, 49, 52, 53	NC	—	**No Connect.** Connect on PCB accordingly.
65—54, 82—68, 98—85, 115—101, 125—118	P[11:0] P[26:12] P[40:27] P[55:41] P[63:56]	I	**Pixels.** TTL compatible. These pins are latched on the rising edge of $\overline{LOAD}$. Pixels can be presented to the DACs as color data (bypass modes) or used as addresses to look up color data in the color RAM or gamma ROM. The overlay inputs must be logic 0 for the pixel inputs to accept data unless the overlay inputs are disabled (CR0[1:0] = 00). Pixels may be multiplexed at 2:1, 4:1, or 8:1. Unused inputs should be connected to GND.
126	$\overline{BLANK}$	I	**Blank (Active-Low).** TTL compatible. $\overline{BLANK}$ is latched on the rising edge of $\overline{LOAD}$. When $\overline{BLANK}$ is low, the 1.44 mA current source on the analog outputs will be turned off. The DACs ignore digital inputs and are driven to the blank level. $\overline{BLANK}$ has a two-, four-, or eight-pixel resolution. The pixel and overlay color RAMs can be updated during blanking.
127	$\overline{SYNC}$	I	**Sync (Active-Low).** TTL compatible. $\overline{SYNC}$ is latched on the rising edge of $\overline{LOAD}$. When active, sync can be configured to remove a 7.62 mA (RS-343A) current source from the PLL output. For systems having a sync signal separate from the RAMDAC, $\overline{SYNC}$ should be tied low to turn off the sync current source. Sync has a two-, four-, or eight-pixel resolution.
128 129	$\overline{CLOCK}$, CLOCK	I	**Pixel Clock.** +5 V ECL compatible. These pins provide the high-speed pixel clock. The duty cycle of the clock should be between 40% and 60%. If using the internal $\overline{LOAD}$ clock multiplier to provide the internal pixel clock in the 2:1, 4:1, or 8:1 multiplex modes, CLOCK should be held at a logic 1, and $\overline{CLOCK}$ should be held at a logic 0.
131	$\overline{LOAD}$	I	**$\overline{LOAD}$ (Active-Low).** TTL compatible. The rising edge of $\overline{LOAD}$ latches P[63:0], OL[15:0], $\overline{BLANK}$, and $\overline{SYNC}$. $\overline{LOAD}$ equals the selected pixel clock divided by the programmed multiplexing rate (2 for 2:1, 4 for 4:1, 8 for 8:1). The $\overline{LOAD}$ clock is multiplied by 2, 4, or 8 to provide the internal pixel clock in 2:1, 4:1, or 8:1 multiplex modes.

Internal Registers

The internal registers consist of an address register, system control registers, mask registers, and test registers.

The address register holds the address value of the register or RAM (pixel or overlay) to be accessed for read or write.

There are four system control registers that are used for selecting various operational functions. Two mask registers, blink mask and read mask, control the blinking and display of pixel data.

The register map is depicted in Table 3.

Address Register

The address register, AD, holds an 8-bit address used for addressing the pixel color RAM, overlay color RAM, and internal registers. The address register auto-increments from $FF to $00. The address register is read or written to by setting R[2:0] = X00 and executing a read or write operation. The address register is operational upon powerup and is not initialized. $\overline{\text{RESET}}$ does not affect this register.

Identification and Revision Registers

The identification (ID), revision (REV), and version (VER) registers uniquely identify the RAMDAC and its revision. The ID and REV registers are addressed by setting R[2:0] = X10 and AD[7:0] = $00 and $01 respectively. The VER register is accessed when R[2:0] = 110 and AD[7:0] = $14. These registers are read only. The ID value read is $54. The VER value is $01. When the device is in the '567 mode (CR3[7] = 1), the REV value is $67 for ATT20C567. When the RAMDAC is emulating Bt467 (CR3[7] = 0), the REV value read is $46. The ID and VER values remain the same.

Pixel Read Mask Register

The read mask register operates in all modes. The register is initialized to $FF during initialization for transparent operation. Writing $00 to the 8-bit pixel read mask register masks the address for all three (red, green, and blue) RAMs, ROMs, and bypass paths. The read mask register is bit-wise logically ANDed with the pixel addresses. A logic 1 stored in a data bit of the read mask register leaves the corresponding bit in the pixel unchanged. A logic 0 in the read mask register sets the pixel bit to zero.

Bit D0 of the pixel read mask register corresponds to the LSB of the pixel. The read mask register is addressed by setting R[2:0] = X10 and AD[7:0] = $04.

Blink Mask Register (BMR)

The blink mask register operates in all CLUT modes. The register is initialized to $00 during initialization for nonblinking operation. Writing $FF to the 8-bit blink mask register blinks the address for all three (red, green, and blue) RAMs or gamma ROMs in true-color modes. A logic 0 stored in a data bit of the blink mask register leaves the corresponding bit in the pixel or pixel address unchanged. A logic 1 in the blink mask register blinks the pixel bit plane at the blink rate specified by the control register. Bit D0 of the blink mask register corresponds to the LSB of the pixel. The blink mask register is addressed by setting R[2:0] = X10 and AD[7:0] = $05.

Signature Analysis Registers

The signature analysis registers (SARs) have two modes, a signature analysis mode and data strobe mode. The signature analysis mode is set by bit CR2[0] = 0 in the control register 2.

The three signature analysis registers, RSAR, GSAR, and BSAR, are linear feedback shift registers (LFSRs). The SARs accumulate a pixel during every clock cycle. Because the SARs are accumulating the bytes fed to the DACs, they also accumulate and test overlay values. Initially, the registers are written with a seed value. The seed value provides a starting value for the SARs to use in their accumulation. The seed values need only be written once. After the $\overline{\text{BLANK}}$ signal rises, the SARs will calculate a signature and store the result back in the SAR for every pixel.

The SARs are active and cannot be accessed during the time when $\overline{\text{BLANK}}$ is high. The SARs may be read or written to while $\overline{\text{BLANK}}$ is a logic 0. This is done with a direct access to the registers. The SARs are valuable for testing the devices on a board and are useful for detecting cold solder joints, as well as RAMDACs injured during the manufacturing process. A good RAMDAC with good connections will always generate the same signature for the same seed value and pixel input.

The SARs can also be configured to reflect the DAC inputs in the data strobe mode. CR2[0] = 1 configures the RAMDAC for this mode.

Internal Registers (continued)

Signature Analysis Registers (continued)

Table 3. Register Map

AD[7:0]	R[2:0]	Register Name	Addressed by MPU	Reset Value
$XX	X00	AD	Address register.	$XX
$00—$FF	X01	—	Pixel color RAM.	$XX
$00—$03	X11	—	Overlay color RAM.	$XX
$00	X10	ID	ID register.	$54
$01	X10	REV	Revision register.	$67* $46†
$02	X10	—	Reserved.	—
$03	X10	—	Reserved.	—
$04	X10	RMR	Read mask register.	$00
$05	X10	BMR	Blink mask register.	$00
$06	X10	CR0	Control register 0.	$60
$07	X10	TR0	Test Register 0.	$X0
$08	110	—	Reserved.	—
$09	110	CR2	Control register 2.	$00
$0A	110	—	Reserved.	—
$0B	110	TR1	Test Register 1.	$00
$0C	110	RSAR	Red signature analysis register.	$XX
$0D	110	GSAR	Green signature analysis register.	$XX
$0E	110	BSAR	Blue signature analysis register.	$XX
$0F	110	—	Reserved.	—
$10	110	CR3	Control register 3.	$00
$11	110	CR4	Control register 4.	$00
$14	110	VER	Version register.	$02

* ATT20C567 mode.
† ATT20C458 or Bt467 mode.

Internal Registers (continued)

Control Register 0

This register is operational on powerup. It can be read or written to by the MPU at any time. This register can be read or written to by using AD[7:0] = $06, R[2:0] = X10. The register bits are set to logic $60 upon reset.

Table 4. Control Register 0

CR0	D7	D6	D5	D4	D3	D2	D1	D0
	—	RAMSEL	BLRATE[1:0]		OBEN1	OBEN0	ODEN1	ODEN0
Reset	0	1	1	0	0	0	0	0

Bit	Name	Description
CR0[7]	—	**Reserved.** This bit may be written and read, but has no internal connection to control logic. It will retain the values written until modified.
CR0[6]	RAMSEL	**RAM/Overlay Select.** Logic 0: Overlay RAM enabled. Logic 1: Pixel color RAM enabled (reset value). This bit selects between pixel RAM and overlay RAM. If overlay RAM is enabled, then all pixel inputs will be disabled and only overlay inputs will be displayed. If the pixel color RAM is enabled, then pixel data will be displayed when the overlay inputs are all logic 0.
CR0[5:4]	BLRATE[1:0]	**Blink Rate.** Logic 00: 16 frames on, 48 frames off. Logic 01: 16 frames on, 16 frames off. Logic 10: 32 frames on, 32 frames off (reset value). Log ic 11: 64 frames on, 64 frames off. These 2 bits control the blink rate by determining how many frames the blink plane will be on and off. All blink rates are of 50% duty cycle except for logic 00 which is 25% on to 75% off. Pixels blink to pixel color 0 (or black for bypass). When overlays blink off, pixel data passes through. If pixels are blinked off at the same time overlays are blinked off, pixel RAM location 0 will be displayed (black for bypass).
CR0[3]	OBEN1	**OL1 Blink Enable.** Logic 0: Disable blinking (reset value). Logic 1: Enable blinking. This bit enables the odd overlay inputs to blink between a logic 0 and the value on the odd overlay inputs. This feature applies to all color modes. Blinking off will result in the pixels being displayed when CR0[6] = 1 and overlay color 0 being displayed when CR0[6] = 0. Note that pixels can be blinked with the blink mask register at the same time overlays are blinked.
CR0[2]	OBEN0	**OL0 Blink Enable.** Logic 0: Disable blinking (reset value). Logic 1: Enable blinking. This bit enables the even overlay inputs to blink between a logic 0 and the value on the even overlay inputs. This feature applies to all color modes. Blinking off will result in the pixels being displayed when CR0[6] = 1 and overlay color 0 being displayed when CR0[6] = 0. Note that pixels can be blinked with the blink mask register at the same time overlays are blinked.

Internal Registers (continued)

Control Register 0 (continued)

Table 4. Control Register 0 (continued)

Bit	Name	Description
CR0[1]	ODEN1	**OL1 Display Enable.** Logic 0: Disable (reset value). Logic 1: Enable. A logic 1 enables the odd overlay inputs, and a logic 0 forces the odd overlays to zero before proceeding to the overlay pipeline.
CR0[0]	ODEN0	**OL0 Display Enable.** Logic 0: Disable (reset value). Logic 1: Enable. A logic 1 enables the even overlay inputs, and a logic 0 forces the even overlays to zero before proceeding to the overlay pipeline.

Internal Registers (continued)

Control Register 2

This register is operational on powerup. It can be read or written to by the MPU at any time. This register is be accessed by AD[7:0] = $09 and R[2:0] = 110. All bits are set to logic 0 upon reset.

Table 5. Control Register 2

CR2	D7	D6	D5	D4	D3	D2	D1	D0
	—	PEDEN	—	—	SYOUT	SYEN	SYSEL	TEST
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
CR2[7]	—	**Reserved.** This bit may be written and read, but has no internal connection to control logic. It will retain the values written until modified.
CR2[6]	PEDEN	**Blank Pedestal Enable.** Logic 0: Blank pedestal disabled (reset value). Logic 1: Blank pedestal enabled. This bit determines whether there will be a blanking pedestal on the video outputs. When the blank pedestal is disabled, the black level is equal to the blank level. When enabled, there is a 7.5% blank pedestal where 100% is the white to blank level.
CR2[5:4]	—	**Reserved.** This bit may be written and read, but has no internal connection to control logic. It will retain the values written until modified.
CR2[3]	SYOUT	**SYOUT Source.** Logic 0: SYNC (reset value). Logic 1: BLANK. This bit determines whether the SYOUT output is generated from the SYNC or BLANK signals.
CR2[2]	SYEN	**SYOUT Enable.** Logic 0: Disabled (reset value). Log ic 1: Enabled. This bit enables SYOUT when set to a logic 1 and is disabled when set to a zero.
CR2[1]	SYSEL	**SYOUT/SYNC Select.** Logic 0: Output SYOUT (reset value). Logic 1: Output SYNC. If this bit is a logic 0, the SYOUT signal is output on the SYOUT pin. The SYOUT signal is determined by using the SYOUT source bit above (CR23). If this bit is a logic 1, then the SYNC signal is output on the SYOUT pin.
CR2[0]	TEST	**Test Type Select.** Logic 0: Signature analysis (reset value). Logic 1: Data strobe test. These bits select the type of test to be run on the RAMDAC. The signature analysis registers hold the results of either test.

Internal Registers (continued)

Control Register 3

All bits are set to logic 0 upon asserting $\overline{\text{RESET}}$. Control register 3 is not in the standard set of Bt467 registers. This register is operational on powerup. It can be read or written to by the MPU at any time and is accessed by setting AD[7:0] = $10, R[2:0] = 110.

Table 6. Control Register 3

CR3	D7	D6	D5	D4	D3	D2	D1	D0
	MODE	SCLK	PIXINT	SLEEP	OVRD	B	I	G
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
CR3[7]	MODE	**Mode Enable.** Logic 0: Bt467 compatible mode (clock modes 2 and 3) (reset value). Logic 1: Enhanced visuals enabled (clock mode 1). When a logic 0, the RAMDAC emulates an 8:1 multiplexed device. CR3 is interpreted as all bits set to zero, and CR4 is interpreted as CR4 = $02. When a logic 1, the enhanced true-color visuals and pixel control bits are enabled. During a reset, a zero is written to this bit.
CR3[6]	SCLK	**SCLK Polarity.** Logic 0: No inversion of SCLK (reset value). Logic 1: Inverted SCLK.
CR3[5]	PIXINT	**Pixel Interface Timing.** Logic 0: Bt 467 compatible $\overline{\text{LOAD}}$ synchronization (clock mode 3) (reset). Logic 1: ATT20C567 $\overline{\text{LOAD}}$ synchronization (clock modes 1 and 2). If this bit is a logic 0, the device loading is the same as the ATT20C458 and Bt467-type devices. If this bit is a logic 1, the shift clock (SCLK) output is enabled. SCLK output rising edge indicates when pixels are copied from the input latch clocked with $\overline{\text{LOAD}}$ into the pixel serializer. SCLK is always divided down from the CLOCK and $\overline{\text{CLOCK}}$ input pins or the pixel clock synthesizer output based on the multiplex ratio. It can be used to clock the serial port of VRAM. $\overline{\text{LOAD}}$ has a setup and hold specification to SCLK in this mode. See timing parameter number 10 in the ac characteristics tables in the Electrical Characteristics section. **Note:** ATT20C567 compatible loading must be used for 2:1 multiplexed operation.
CR3[4]	SLEEP	**Sleep Enable.** Logic 0: Normal operation. Logic 1: Sleep mode. If this bit is logic 0, the device will be in normal operation. If this bit is logic 1, the DAC is turned off and the palette RAM is powered down while the RAM retains data. After programming the device for normal operation, valid data will appear at the DAC outputs in about one second. Access to the control registers during sleep is supported, while access to the color RAMs is not supported during sleep. The PLL is powered down separately by setting CR4[7] = 0.
CR3[3]	OVRD	**Override Pixel.** Logic 0: Pixel control of visuals by decoding embedded visual bits V[3:0]. Logic 1: Control register controls B, I, G (CR3[2:0]). This bit allows the control register to override the pixel control bits and use the values of B, I, and G in the control register to set the visual type. **Note:** Pixels without visual bits will be interpreted as being in the default visual mode. Override disables double-buffering by ignoring the visual control bits.

Internal Registers (continued)

Control Register 3 (continued)

Table 6. Control Register 3 (continued)

Bit	Name	Description
CR3[2]	B	**Bypass (B).** Logic 0: Select color RAM or gamma ROM. Logic 1: Bypass color RAM and gamma ROM. When logic 1 and CR3[3] = 1, this bit causes the pixel data to bypass the color RAM and gamma ROM and be input to the DACs directly.
CR3[1]	I	**Index (I) (Pseudo- or True-Color Select).** Logic 0: Address R, G, and B color RAMs, gamma ROMs, or DACs separately. Logic 1: Index pseudocolor or gray scale. A logic 1 and CR3[3] = 1 enables the red, green, and blue look-up tables or ROMs to be addressed with the same address value. A logic 0 enables the red, green, and blue look-up tables or ROMs to be addressed separately.
CR3[0]	G	**Gamma (G).** Logic 0: Select color RAM output. Logic 1: Select gamma ROM output. If this bit is a logic 0 and CR3[3] = 1, the output of the color RAM is directed to the bypass multiplexer. If this bit is a logic 1, the output of the gamma ROM is directed to the bypass multiplexer.

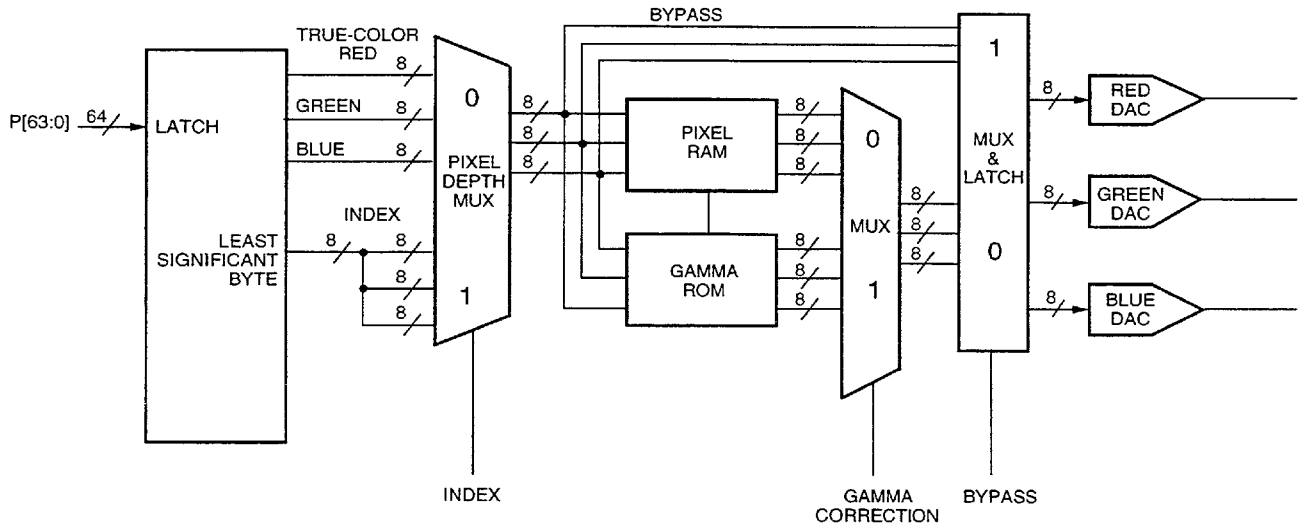


Figure 4. Operation of B, I, and G Control Bits in Control Register 3

Internal Registers (continued)

Control Register 4

All bits are set to logic $00 upon asserting $\overline{\text{RESET}}$. Control register 4 is not in the standard set of Bt467 registers. This register is operational on powerup. It can be read or written to by the MPU at any time. Control register 4 is accessed by setting AD[7:0] = $11, R[2:0] = 110.

Table 7. Control Register 4

CR4	D7	D6	D5	D4	D3	D2	D1	D0
	PLLEN	—	BPP[1:0]		—	—	PINEN[1:0]	
Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
CR4[7]	PLLEN	**PLL Enable.** Logic 0: Disable PLL $\overline{\text{LOAD}}$ clock multiplier (clock modes 2 and 3) (reset value). Logic 1: Enable PLL $\overline{\text{LOAD}}$ clock multiplier (clock mode 1). When this bit is a one, an internal PLL $\overline{\text{LOAD}}$ clock doubler will generate the pixel clock from the $\overline{\text{LOAD}}$ clock. CLOCK and $\overline{\text{CLOCK}}$ are used only to generate SCLK. The pixel interface timing must be in 567 mode (CR3[5] = 1). There is no ac requirement between $\overline{\text{LOAD}}$ and SCLK in PLL enable mode.
CR4[6]	—	**Reserved.** This bit may be written and read, but has no internal connection to control logic. It will retain the values written until modified.
CR4[5:4]	BPP[1:0]	**Bits-per-Pixel Select.** Logic 00: 8 bits per pixel (index). Logic 01: 16 bits per pixel (5-5-5 or 4-4-4 with visual control). Logic 10: 16 bits per pixel (5-6-5, no visual control, nonlinear true-color). Logic 11: 32 bits per pixel (8-8-8 with visual control). These bits control the operation of the enhanced color modes. The format table for each pixel depth describes the details of how these bits interact with the pixel visual control bits embedded in the pixels in the frame buffer. The 8-8-8 format uses extra bits in the final byte (32 total bits) for control of visual type. These bits, together with the number of active pixels, CR4[1:0] determine the multiplexing rate. For example, 16 bits per pixel with 32 active pixel pins will set the device into a 2:1 multiplexing ratio.
CR4[3:2]	—	**Reserved.** This bit may be written and read, but has no internal connection to control logic. It will retain the values written until modified.
CR4[1:0]	PINEN[1:0]	**Number of Active Pixel Pins.** Logic 00: Pixel pins P[15:0] are used for latching pixel data. Logic 01: Pixel pins P[31:0] are used for latching pixel data. Logic 10: Pixel pins P[63:0] are used for latching pixel data. Logic 11: Reserved, correct operation not guaranteed. These bits control the number of active pixel pins. These pins, together with the number of bits per pixel, determine the multiplex ratio.

Internal Registers (continued)

Test Register 0

Test Register 0 is in the standard set of Bt467 registers. This register is operational upon powerup. It can be read or written to by the MPU at any time and is not initialized. Test Register 0 is accessed by setting AD[7:0] = $07 and R[2:0] = X10. The upper 4 bits are unknown while the lower 4 bits are 1001 upon asserting $\overline{\text{RESET}}$.

Test Register 0 allows the DAC inputs to be read directly. The DAC inputs are read one nibble at a time. The 4 bits TR0[3:0] select which nibble is to be read; the DAC input nibble can be read out of TR0[7:4]. Set only one of the red, green, or blue select bits at a time (TR0[2:0]). This portion of test capability does not operate at pixel speed. Therefore, the same pixel information should be presented to the pixel inputs while reading a particular nibble, or the pixel clock should be slowed down to the MPU port speed. Table 9 outlines an example of the Test Register 0 functions.

Table 8. Test Register 0

TR0	D7	D6	D5	D4	D3	D2	D1	D0
	DACIN[3:0]				NIBSEL	BDAC	GDAC	RDAC
Reset	X	X	X	X	1	0	0	1

Bit	Name	Description
TR0[7:4]	DACIN[3:0]	**DAC Input Nibble.** These bits show the upper or lower nibble input to the red, green, or blue DAC. The selection of upper or lower of red, green, or blue DACs is controlled by TR0[3:0]. TR0[7] is the MSB of the nibble, and TR0[4] is the LSB of the nibble.
TR0[3]	NIBSEL	**Nibble Select.** TR0[3] = 1: Low nibble will be loaded into TR0[7:4]. TR0[3] = 0: High nibble will be loaded into TR0[7:4]. This bit selects whether the low or high nibble will be loaded into TR0[7:4].
TR0[2]	BDAC	**Blue DAC Select.** TR0[2] = 1: Select blue DAC inputs. TR0[2] = 0: Deselect blue DAC inputs. Either the high or low nibble will be written to TR0[7:4] depending on which nibble is selected by TR0[3].
TR0[1]	GDAC	**Green DAC Select.** TR0[1] = 1: Select green DAC inputs. TR0[1] = 0: Deselect green DAC inputs. Either the high or low nibble will be written to TR0[7:4] depending on which nibble is selected by TR0[3].
TR0[0]	RDAC	**Red Select.** TR0[0] = 1: Select red DAC inputs. TR0[0] = 0: Deselect red DAC inputs. Either the high or low nibble will be written to TR0[7:4] depending on which nibble is selected by TR0[3].

Internal Registers (continued)

Test Register 0 (continued)

Table 9. Test Register 0 Operation

Bit	WR	RD	WR	RD	WR	RD	WR	RD	WR	RD	WR	RD
TR0[7]	X	B7	X	B3	X	G7	X	G3	X	R7	X	R3
TR0[6]	X	B6	X	B2	X	G6	X	G2	X	R6	X	R2
TR0[5]	X	B5	X	B1	X	G5	X	G1	X	R5	X	R1
TR0[4]	X	B4	X	B0	X	G4	X	G0	X	R4	X	R0
TR0[3]	0	0	1	1	0	0	1	1	0	0	1	1
TR0[2]	1	1	1	1	0	0	0	0	0	0	0	0
TR0[1]	0	0	0	0	1	1	1	1	0	0	0	0
TR0[0]	0	0	0	0	0	0	0	0	1	1	1	1

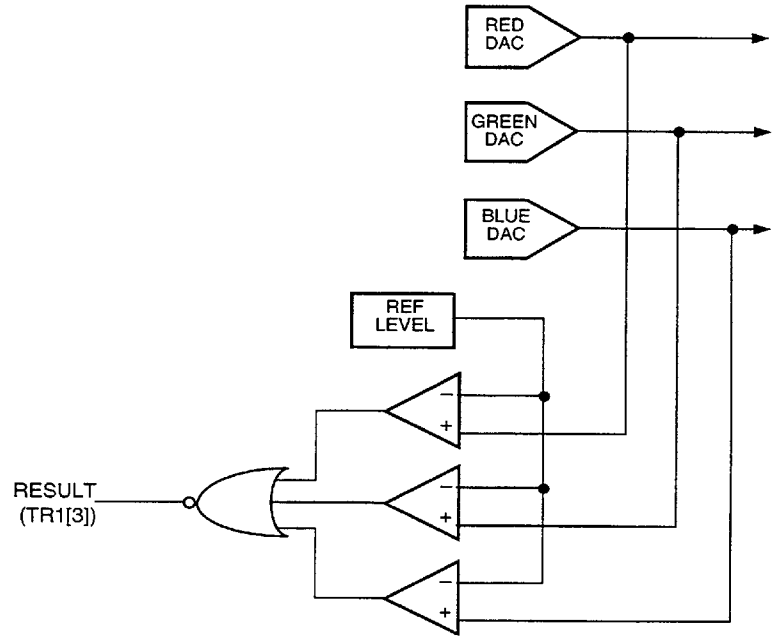


Figure 5. Block Diagram of DAC Compare Circuitry

Internal Registers (continued)

Test Register 1

Test Register 1 is read only and is in the standard set of Bt467 registers. This register is operational upon powerup. It can be read by the MPU at any time. Test Register 1 is accessed by setting AD[7:0] = $08 and R[2:0] = 110. All reserved bits are set to logic 0 upon asserting $\overline{\text{RESET}}$.

Table 10. Test Register 1

TR1	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved				DACRES	Reserved		
Reset	0	0	0	0	X	0	0	0

Bit	Name	Description
TR1[7:4]	—	**Reserved.** When read, these bits will return the value written. The value will not affect the operation of the device.
TR1[3]	DACRES	**DAC Output Compare Result.** TR1[3] = 1: The DAC outputs are less than the internal reference level. TR1[3] = 0: The DAC outputs are greater than the internal reference level. This bit indicates whether one or more of the R, G, and B outputs are greater than the internal voltage reference level of 340 mV (see dc characteristics tables under Electrical Characteristics section for tolerance specs). This is used to determine the presence of an external monitor. Before reading this bit, make sure the DAC outputs are stable for 5 microseconds. Refer to Figure 5.
TR1[2:0]	—	**Reserved (Formerly Pixel Select for Signature Analysis).** Write zeros to these bits. These bits will return the value written when read and will not affect the operation of the device.

Functional Description

The ATT20C567 is register compatible with the ATT20C458 and Bt467. The ATT20C567 contains two additional control registers to enable its new features. This device allows pixel-by-pixel selection between 16-bit and 8-bit pixel formats or 32-bit and 8-bit formats. Multiplexers are provided and can be switched on a pixel-by-pixel basis, which can select between the output of the color look-up table (color RAM), a gamma correction ROM, or a bypass path leading directly to the DAC inputs. These multiplexers, plus the pixel format control bits, enable simultaneous display of direct color, linear true color, nonlinear true color, and index color. The pixel format control bits, V[3:0], support alternating between double-frame buffers. Since this information is encoded in the pixel data, an unlimited number of different application windows can be simultaneously supported.

Color Mode Definitions

Index — Pseudocolor where all pixel bits address the RGB color RAM in the same way.

Direct Color — Individual RGB fields in the pixel address the appropriate color RAM.

Linear True Color — Individual RGB fields in the pixel address the appropriate gamma ROM.

Nonlinear True Color — Individual RGB fields in the pixel go directly to the appropriate DACs.

Linear Gray Scale — Index mode through the gamma ROM.

Nonlinear Gray Scale — Index mode which bypasses the gamma ROM and color RAM.

Note that, in all modes, overlays index the overlay color RAM.

Pixel Loading and Multiplexing

Pixels are clocked into the ATT20C567 by using the rising edge of the $\overline{\text{LOAD}}$ signal. The user must configure the ATT20C567 for 16, 32, or 64 active pixel pins, and 8-, 16-, or 32-bit pixels. Based on this configuration, the multiplex rate will be set. The RAMDAC buffers from 16 to 64 pixel data bits prior to serialization. For 16 active pixel pins, the graphics controller inputs data on P[15:0]. For 32 active pixel pins, the graphics controller inputs data on P[31:0]. For 16 active pixel pins, choosing 32-bit pixels will result in invalid operation. There are two unsupported modes: 1:1 MUX at 16 and 32 bits per pixel (see Table 11).

These pixels are serialized starting with the pixel that occupies the least significant byte of the internal pixel field and the two least significant bits of the internal overlay field. The pixels are shifted into the RAMDAC pipeline, one at a time, until the entire group of pixels is exhausted.

All pixel and overlay pins map directly. When the number of active pixel pins is 16, P[15:0] are active with P15 as the MSB. When the number of active pixel pins is 32, P[31:0] are active with P31 as the MSB. When the number of active pixel pins is 64, P[63:0] are active with P63 as the MSB. For the pixel formatting for each pixel depth, refer to Tables 15, 17, and 18.

Table 11. Available Modes Listed by Order of Active Pixel Pins

Number of Active Pixel Pins	Pixel Size	Multiplex Mode	PLL $\overline{\text{LOAD}}$ Multiplex Factor
16	8	2:1	2X
16	16	not supported	not supported
16	32	invalid	NA
32	8	4:1	4X
32	16	2:1	2X
32	32	not supported	not supported
64	8	8:1	8X
64	16	4:1	4X
64	32	2:1	2X

Overlays

Overlays are 2-bit index visual only. Overlays do not support any true-color visuals. Control register 0 determines the operation of the overlays.

The overlays can be displayed on a pixel-by-pixel basis by setting CR0[6] = 1. When the overlay inputs are zero, the pixel data is selected and fed into the pipeline. When CR0[6] = 0, only overlay data is fed into the pixel pipeline. In this case, overlay color zero is displayed when the overlay inputs are zero.

The overlays can be disabled by CR0[1:0]. When enabled, the overlays may be blinked at the blink rate specified by CR0[5:4]. The overlays blink to overlay color zero when enabled. Otherwise, the overlays blink to the pixel value. If pixels and overlays blink at the same time, they blink to pixel location 0.

Functional Description (continued)

Overlays (continued)

When both overlay bits are disabled or blinked to zero, the overlay will become transparent if CR0[6] = 1, and the overlay will display overlay color 0 if CR0[6] = 0.

The interaction of blink mask register, read mask register, control register 0 bits, blink counter output and value of overlay data is depicted in Table 12.

Table 12. Display Data Selection

RAMSEL CR0[6]	Blink Mask Reg. Bit	Blink Counter	Read Mask Reg. Bit	ODEN1/0 CR0[1/0]	OBEN1/0 CR0[3/2]	Overlay Data	Display Data Selected
0	X	X	X	0	X	X	Overlay RAM 0
0	X	X	X	1	0	X	Overlay Index
0	X	OFF	X	1	1	X	Overlay RAM 0
0	X	ON	X	1	1	X	Overlay Index
1	0	X	1	X	X	Zero	Pixel Index
1	1	OFF	1	X	X	Zero	Pixel RAM 0
1	1	ON	1	X	X	Zero	Pixel Index
1	X	X	0	X	X	Zero	Pixel RAM 0
1	X	X	X	0	X	Nonzero	Overlay RAM 0
1	X	X	X	1	0	Nonzero	Overlay Index
1	X	OFF	X	1	1	Nonzero	Overlay RAM 0
1	X	ON	X	1	1	Nonzero	Overlay Index

Extended True-Color Functions

The chip supports twenty visuals in 32-bit mode, four visuals in 16-bit mode, and one visual in 8-bit mode as specified in Tables 15, 16, and 18, respectively. The tables show the formatting of all pixels.

The pixels may be multiplexed and loaded in various ways as specified in control register 3 and control register 4. The multiplexing is illustrated in Table 11. Tables 15 and 16 show how the various visuals are encoded in a given pixel. Table 18 indicates the pseudocolor mapping.

32-Bit Pixel Mode

Pixels must be 2:1 multiplexed when 32-bit pixels are used. There are 20 visuals for 32-bit pixels including support for double-buffering. Table 14 shows the frame buffer formatting for 32-bit pixels. The bits per pixel and number of active pixels must be set in control register 4. The bits per pixel and number of active pixels will determine the multiplex ratio. This must be set to 64 active pixel pins and 32-bit pixels. An unlimited number of windows can be displayed by using the different visuals.

The values of B, I, and G in the control register bits CR3[2:0] will have no effect on pixels unless the override bit (CR3[3]) is set to 1. In the case of override = 1, all pixels will be interpreted according to CR3[2:0] (B, I, G). This mode requires synchronous timing of pixel clock and load clock signals (for ATT20C567 loading, see CR3[5]) since it is 2:1 multiplexed.

16-Bit Pixel Mode

Pixels must be either 2:1 or 4:1 multiplexed in this mode. 1:1 multiplexing is not supported. There are four visuals in this mode. Table 17 shows frame buffer formatting for control of 16-bit visuals. The bits per pixel and number of active pixels must be set in control register 4.

The bits per pixel and number of active pixels will determine the multiplex ratio. The values of X, V[1:0] can be embedded in the frame buffer to yield the pixel formats in Table 16. This switching of formats can be done on the fly for support of an unlimited number of windows of different visuals. The second half of Table 16 shows the 5-6-5 *XGA* compatible visual. There are no embedded visual control bits in this pixel format.

Functional Description (continued)

Extended True-Color Functions (continued)

The values of B, I, and G in the control register (CR3[2:0]) may be programmed to select bypass, index, or gamma operation. Override (CR3[3]) must be programmed with a one for B, I, and G control register bits to be active. When the override bit CR3[3] = 0, the default 5-6-5 visual mode is nonlinear true color.

8-Bit Pixel Mode

Pixels must be either 2:1, 4:1, or 8:1 multiplexed in this mode (1:1 multiplexing is not supported). There is one visual in this mode. Table 18 shows pixel formatting for the 8-bit indexed visual.

The following table shows the format of the pixel values. The 8-bit indexed visual may be multiplexed at two, four, or eight pixels per load clock. The bits per pixel and number of active pixels must be set in control register 4. There are no embedded visual control bits in the pixels. The value of I in the control register 3 bit CR3[1] will have no effect because this mode is pseudocolor only. This is a nonwindow visual, and the entire screen will be in one format. The default visual is index color when override bit CR3[3] = 0.

Table 13. Definitions and Descriptions of the 32-Bit Visual Control Bits

V1	V0	Visual
0	0	Index or 8-bit pseudocolor (through pixel color RAM).
0	1	Direct color (through pixel color RAM).
1	0	Linear true color (through gamma ROM).
1	1	Nonlinear true color (bypass pixel color RAM and ROM).
V2 — Nibble Mask. When equal to a logic 1, this bit will mask the lower 4 bits of the red, green, and blue fields to zero before forwarding into the pixel pipeline.		
V3 — Double-Buffer Swap. This bit is operable for all visual modes above. For index mode, the 8 bits of the green field are used as an address instead of the red field. In direct or true-color modes when V3 = 1, the lower nibble in each byte is copied into the upper nibble. If V2 = 1, the mask operation is executed after the swap.		

Table 14. 32-Bit Pixel Formats

Visual	P[31:28]	P27	P26	P25	P24	P[23:16]	P[15:8]	P[7:0]
8-8-8 color	Reserved	V3 = 0	V2 = 0	V1	V0	B[7:0] = P[23:16]	G[7:0] = P[15:8]	R[7:0] = P[7:0]
Nibble swap	Reserved	V3 = 1	V2 = 0	V1	V0	B[7:4] = B[3:0] = P[19:16]	G[7:4] = G[3:0] = P[11:8]	R[7:4] = R[8:0] = P[3:0]
4-bit mask	Reserved	V3 = 0	V2 = 1	V1	V0	B[7:4] = P[23:20], B[3:0] = 0000	G[7:4] = P[15:12], G[3:0] = 0000	R[7:4] = P[7:4], R[3:0] = 0000
Swap and mask	Reserved	V3 = 1	V2 = 1	V1	V0	B[7:4] = P[19:16], B[3:0] = 0000	G[7:4] = P[11:8], G[3:0] = 0000	R[7:4] = P[3:0], R[3:0] = 0000
8-bit pseudo	Reserved	V3 = 0	V2 = 0	V1 = 0	V0 = 0	—	—	P[7:0]
Use green field	Reserved	V3 = 1	V2 = 0	V1 = 0	V0 = 0	—	P[7:0]	—
4-bit pseudo	Reserved	V3 = 0	V2 = 1	V1 = 0	V0 = 0	—	—	P[7:4], 0000
Use green field	Reserved	V3 = 1	V2 = 1	V1 = 0	V0 = 0	—	P[7:4], 0000	—

Functional Description (continued)

Extended True-Color Functions (continued)

Table 15. Visual Modes for 32-Bit Pixels

The following table shows the V[3:0] control bits embedded in the pixel bits for visual control. **This mode requires synchronous timing of pixel clock and load clock signals.**

V3	V2	V1	V0	Visual
0	0	0	0	8-bit index color using the red field to address pixel color RAM.
1	0	0	0	8-bit index color using the green field to address pixel color RAM.
0	1	0	0	8-bit index color using the red field to address pixel color RAM. Mask lower 4 bits of address to zero.
1	1	0	0	8-bit index color using the green field to address pixel color RAM. Mask lower 4 bits of address to zero.
0	0	0	1	8-8-8 direct color (through pixel color RAM).
1	0	0	1	8-8-8 direct color (through pixel color RAM), lower nibble copied to upper nibble within each color field.
0	1	0	1	4-4-4 direct color. Mask lower 4 address bits of each pixel color RAM to zero.
1	1	0	1	4-4-4 direct color. Lower nibble copied to upper nibble within each color field prior to masking the lower 4 address bits of each pixel color RAM to zero.
0	0	1	0	8-8-8 linear true color (through gamma ROM).
1	0	1	0	8-8-8 linear true color (through gamma ROM). Lower nibble copied to upper nibble within each color field.
0	1	1	0	4-4-4 linear true color. Mask the lower 4 address bits of each gamma ROM to zero.
1	1	1	0	4-4-4 linear true color. Lower nibble copied to upper nibble within each color field prior to masking the lower 4 address bits of each pixel color ROM to zero.
0	0	1	1	8-8-8 nonlinear true color (bypass pixel color RAM and ROM).
1	0	1	1	8-8-8 nonlinear true color (bypass pixel color RAM and ROM). Lower nibble copied to upper nibble within each color field.
0	1	1	1	4-4-4 nonlinear true color (bypass pixel color RAM). Mask lower 4 bits of each red, green, and blue DAC to zero.
1	1	1	1	4-4-4 nonlinear true color (bypass pixel color RAM). Lower nibble to upper nibble within each color field prior to masking the lower 4 bits of each red, green, and blue DAC to zero.

Table 16. Visual Modes for 16-Bit Pixels

The following table shows the options for embedded visual control in the pixel bits. Note that the X pixel control bit is used in the 16-bit per pixel mode. The default is 5-5-5 nonlinear true color for X = 0.

X	V1	V0	Visual
0	X	X	5-5-5 nonlinear true color (bypass).
1	0	X	8-bit pseudocolor (through pixel color RAM).
1	1	0	4-4-4 direct color (through pixel color RAM).
1	1	1	4-4-4 linear true color (through gamma ROM).

Functional Description (continued)

Extended True-Color Functions (continued)

Table 17. Frame Buffer Formatting for Control of 16-Bit Visuals

16-Bit Pixel, 5-5-5 Nonlinear True Color, 4-4-4 Direct and Linear True Color, 8-Bit Index Color																			
Input Pins	Pixel 1	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	OL1	OL0
	Pixel 2	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	OL3	OL2
	Pixel 3	P47	P46	P45	P44	P43	P42	P41	P40	P39	P38	P37	P36	P35	P34	P33	P32	OL5	OL4
	Pixel 4	P63	P62	P61	P60	P59	P58	P57	P56	P55	P54	P53	P52	P51	P50	P49	P48	OL7	OL6
Visuals and Pixel Bits	5-5-5	X = 0	B7	B6	B5	B4	B3	G7	G6	G5	G4	G3	R7	R6	R5	R4	R3	OL1	OL0
	4-4-4	X = 1	B7	B6	B5	B4	V1	G7	G6	G5	G4	V0	R7	R6	R5	R4	—	OL1	OL0
	Pseudo	X = 1	—	—	—	—	V	—	—	P7	P6	P5	P4	P3	P2	P1	P0	OL1	OL0

16-Bit Pixel, 5-6-5 Nonlinear True Color																			
Input Pins	Pixel 1	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0	OL1	OL0
	Pixel 2	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	OL3	OL2
	Pixel 3	P47	P46	P45	P44	P43	P42	P41	P40	P39	P38	P37	P36	P35	P34	P33	P32	OL5	OL4
	Pixel 4	P63	P62	P61	P60	P59	P58	P57	P56	P55	P54	P53	P52	P51	P50	P49	P48	OL7	OL6
Visuals and Pixel Bits	5-6-5	B7	B6	B5	B4	B3	G7	G6	G5	G4	G3	G2	R7	R6	R5	R4	R3	OL1	OL0

Table 18. Pixel Formatting for 8-Bit Indexed Visual

8-Bit Pixel, Index Color											
Input Pins	Pixel 1	P7	P6	P5	P4	P3	P2	P1	P0	OL1	OL0
	Pixel 2	P15	P14	P13	P12	P11	P10	P9	P8	OL3	OL2
	Pixel 3	P23	P22	P21	P20	P19	P18	P17	P16	OL5	OL4
	Pixel 4	P31	P30	P29	P28	P27	P26	P25	P24	OL7	OL6
	Pixel 5	P39	P38	P37	P36	P35	P34	P33	P32	OL9	OL0
	Pixel 6	P47	P46	P45	P44	P43	P42	P41	P40	OL11	OL2
	Pixel 7	P55	P54	P53	P54	P53	P52	P51	P50	OL13	OL4
	Pixel 8	P63	P62	P61	P60	P59	P58	P57	P56	OL15	OL6
Visuals and Pixel Bits	Pseudo	P7	P6	P5	P4	P3	P2	P1	P0	OL1	OL0

Functional Description (continued)

Override

When the override bit is set to one (CR3[3] = 1), the B, I, and G bits control the visual. Double-buffering is not supported when override is active. The control bits V[3:0] embedded in the pixels are ignored. Bits CR4[5:4] and CR4[1:0] set the bits per pixel, the number of active pixel pins, and the multiplex ratio.

For example, switching to OVRD = 1 and I = 1 will cause the device to interpret all pixels as index or gray scale (see Figure 4). In this case, the least significant 8 bits of the pixel will be used as a common index to the three palettes, the three gamma ROMs, and the three bypass paths. B and G could then be used to select index, nonlinear gray scale, or linear gray scale visuals. Also, OVRD will not affect the hardware interpretation of the X-bit in the 5-5-5 16-bit pixel. If X = 1, OVRD = 1, and I = 0, the pixel will be fed forward in the pipeline as 4-4-4. If X = 0, OVRD = 1, and I = 0, the pixel will be fed forward in the pipeline as 5-5-5.

V[3:2] in the 32-bit pixel controls double-buffering and masking and will always be set to logic 0 when OVRD = 1.

The final multiplexers which drive data forward from the ROM or color RAM or bypass path have the following order of precedence:

1. Microprocessor color RAM read. RAM is selected.
2. Active overlays as a result of nonzero overlay data. RAM is selected.
3. OVRD = 1 and B = 1. Bypass is selected.
4. OVRD = 1, B = 0, and G = 1. ROM is selected.
5. OVRD = 1, B = 0, and G = 0. Color RAM is selected.
6. V0 or V1 bits embedded in pixel. See pixel format in Tables 15 or 16.
7. Default pixel mode.

   For 8-bit pixels, select color RAM.
   For 5-5-5 16-bit pixel (X = 0), select bypass.
   For 5-6-5 16-bit pixel, select bypass.

Double-Buffering (V3)

The V3 bit in 32-bit pixels supports double-buffering. Double-buffer support allows switching between two frame buffers on a pixel-by-pixel basis. Double buffering is supported in index color mode and 4-4-4 true color. In index mode, when V3 = 0, the 8-bit address is input on the red field, P[7:0] and P[39:32]. In index mode, when V3 = 1, the 8-bit address is input on the green field, P[15:8] and P[47:40].

In 4-4-4 true color, two 12-bit pixels may be input from each buffer (see Figure 15). The V3 bit selects which buffer will be displayed. Only one frame buffer needs to contain the V3 bit, and that frame buffer is the controlling frame buffer. When V3 = 1, the lower nibble of each byte is latched into the pipeline. When V3 = 0, the upper nibble of each byte is latched into the pipeline.

Nibble Masking (V2)

The lower nibble of the 4-4-4 true-color pixels can be masked after being copied to the upper nibble. The V2 embedded visual control bit controls this operation. When V2 = 0, the pixel data is unmodified. When V2 = 1, the lower nibble is copied to the upper nibble and the lower nibble is masked to zeros before being sent to the serializer.

Functional Description (continued)

Nibble Masking (V2) (continued)

Table 19. Truth Table Showing Logical Values for Setting Each Visual (8-bit and 16-bit)

Note: The same visual can be sent by different logic values.

Visual	CR4 [5]	CR4 [4]	X	V3	V2	V1	V0	OV RD CR3 [3]	B CR3 [2]	I CR3 [1]	G CR3 [0]	Pixel Type (bits)	Default
8 Bits Per Pixel (Index)													
8-bit index	0	0	NA	NA	NA	NA	NA	0	X	X	X	8	index
8-bit index	0	0	NA	NA	NA	NA	NA	1	0	X	0	8	index
8-bit linear gray scale	0	0	NA	NA	NA	NA	NA	1	0	X	1	8	index
8-bit nonlinear gray scale	0	0	NA	NA	NA	NA	NA	1	1	X	X	8	index
16 Bits Per Pixel, 5-6-5													
5-6-5 nonlinear true color	1	0	NA	NA	NA	NA	NA	0	X	X	X	16-565	NLTC
5-6-5 direct color	1	0	NA	NA	NA	NA	NA	1	0	0	0	16-565	NLTC
5-6-5 linear true color	1	0	NA	NA	NA	NA	NA	1	0	0	1	16-565	NLTC
8-bit index	1	0	NA	NA	NA	NA	NA	1	0	1	0	16-565	NLTC
8-bit linear gray scale	1	0	NA	NA	NA	NA	NA	1	0	1	1	16-565	NLTC
5-6-5 nonlinear true color	1	0	NA	NA	NA	NA	NA	1	1	0	X	16-565	NLTC
8-bit nonlinear gray	1	0	NA	NA	NA	NA	NA	1	1	1	X	16-565	NLTC
16 Bits Per Pixel, 5-5-5													
5-5-5 nonlinear true color	0	1	0	NA	NA	NA	NA	0	X	X	X	16-555	NA
8-bit index	0	1	1	NA	NA	0	X	0	X	X	X	16-555	NA
4-4-4 direct color	0	1	1	NA	NA	1	0	0	X	X	X	16-555	NA
4-4-4 linear true color	0	1	1	NA	NA	1	1	0	X	X	X	16-555	NA
5-5-5 direct color	0	1	0	NA	NA	X	X	1	0	0	0	16-555	NA
5-5-5 linear true color	0	1	0	NA	NA	X	X	1	0	0	1	16-555	NA
8-bit index	0	1	X	NA	NA	X	X	1	0	1	0	16-555	NA
8-bit linear gray scale	0	1	X	NA	NA	X	X	1	0	1	1	16-555	NA
5-5-5 nonlinear true color	0	1	0	NA	NA	X	X	1	1	0	X	16-555	NA
8-bit linear gray scale	0	1	X	NA	NA	X	X	1	1	1	X	16-555	NA
4-4-4 direct color	0	1	1	NA	NA	X	X	1	0	0	0	16-555	NA
4-4-4 linear true color	0	1	1	NA	NA	X	X	1	0	0	1	16-555	NA
4-4-4 nonlinear true color	0	1	1	NA	NA	X	X	1	1	0	X	16-555	NA

Note: NLTC = nonlinear true color.

Functional Description (continued)

Nibble Masking (V2) (continued)

Table 20. Truth Table Showing Logical Values for Setting Each Visual (32-bit)

Note: The same visual can be sent by different logic values.

Visual	CR4 [5]	CR4 [4]	X	V3	V2	V1	V0	OV RD CR3 [3]	B CR3 [2]	I CR3 [1]	G CR3 [0]	Pixel Type (bits)	Default
32 Bits Per Pixel													
8-bit index (red)	1	1	NA	0	0	0	0	0	X	X	X	32	NA
8-8-8 direct	1	1	NA	0	0	0	1	0	X	X	X	32	NA
8-8-8 linear true color	1	1	NA	0	0	1	0	0	X	X	X	32	NA
8-8-8 nonlinear true color	1	1	NA	0	0	1	1	0	X	X	X	32	NA
4-bit index	1	1	NA	0	1	0	0	0	X	X	X	32	NA
4-4-4 direct color (MSBs)	1	1	NA	0	1	0	1	0	X	X	X	32	NA
4-4-4 linear true color (MSBs)	1	1	NA	0	1	1	0	0	X	X	X	32	NA
4-4-4 nonlinear true color (MSBs)	1	1	NA	0	1	1	1	0	X	X	X	32	NA
8-bit index (green)	1	1	NA	1	0	0	0	0	X	X	X	32	NA
8-8-8 direct color (low nibbles replicated)	1	1	NA	1	0	0	1	0	X	X	X	32	NA
8-8-8 linear true color (low nibbles replicated)	1	1	NA	1	0	1	0	0	X	X	X	32	NA
8-8-8 nonlinear true color (low nibbles replicated)	1	1	NA	1	0	1	1	0	X	X	X	32	NA
4-bit index (LSBs)	1	1	NA	1	1	0	0	0	X	X	X	32	NA
4-4-4 direct color (LSBs)	1	1	NA	1	1	0	1	0	X	X	X	32	NA
4-4-4 linear true color (LSBs)	1	1	NA	1	1	1	0	0	X	X	X	32	NA
4-4-4 nonlinear true color (LSBs)	1	1	NA	1	1	1	1	0	X	X	X	32	NA
8-8-8 direct color	1	1	NA	X	X	X	X	1	0	0	0	32	NA
8-8-8 linear true color	1	1	NA	X	X	X	X	1	0	1	0	32	NA
8-bit index	1	1	NA	X	X	X	X	1	0	1	1	32	NA
8 bit linear gray scale	1	1	NA	X	X	X	X	1	0	1	1	32	NA
8-8-8 nonlinear true color	1	1	NA	X	X	X	X	1	1	0	X	32	NA
8 bit nonlinear gray scale	1	1	NA	X	X	X	X	1	1	1	X	32	NA

Functional Description (continued)

Clocking

The ATT20C567 supports three modes of pixel interface timing. In one mode, an external clock provides the TTL $\overline{\text{LOAD}}$ clock. The $\overline{\text{LOAD}}$ clock is multiplied to the required pixel rate inside the RAMDAC. In the two remaining modes, an external clock drives the clock inputs. The three clocking modes are described below.

ATT50C567 PLL Clock Mode
(CR3[7] = CR3[5] = CR4[7] = 1)
(Set MUX ratio with CR4[5:4] and CR4[1:0])

In the first clocking mode, the TTL $\overline{\text{LOAD}}$ clock is the only signal clocking the RAMDAC. The RAMDAC provides its own internal pixel clock by multiplying the TTL $\overline{\text{LOAD}}$ clock. The multiplication factor is adjusted depending on the multiplex ratio. The internal clock multiplier can multiply the $\overline{\text{LOAD}}$ clock by 2, 4, or 8 times. The multiplex ratio is set by CR4[5:4] and CR4[1:0]. No CLOCK or $\overline{\text{CLOCK}}$ signal is needed in this mode unless an output on SCLK is desired (see Figure 6). If CLOCK and $\overline{\text{CLOCK}}$ are not toggled, CLOCK should be logic high and $\overline{\text{CLOCK}}$ should be logic low. If CLOCK and $\overline{\text{CLOCK}}$ are toggled, SCLK can be output after being divided by the multiplex ratio. In this clocking mode, the system designer does not need to satisfy timing requirements between SCLK and $\overline{\text{LOAD}}$. This eliminates the requirement for external synchronization of the clocking and loading signals.

When changing multiplexing rates in this clocking mode, the internal pixel clock will not be valid for 1 second. The SCLK output is not affected because it is driven by the external CLOCK and $\overline{\text{CLOCK}}$ pins.

Copy the color RAMs to system memory before changing multiplex ratios. The data can be copied back to the color RAMs after 1 second. Copying the RAM data to system memory provides maximum security for pixel and overlay color RAM data when switching multiplex ratios in this clocking mode.

ATT20C567 NonPLL Clock Mode
(CR3[7] = CR3[5] = 1, CR4[7] = 0)

In the ATT20C567 nonPLL clock mode, CLOCK and $\overline{\text{CLOCK}}$ are driven with an external positive ECL clock source. The clock signal is divided and output on the SCLK output. The SCLK output can be used to clock the shift clock of VRAMs. The system can use SCLK to generate the $\overline{\text{LOAD}}$ signal for loading pixels into the RAMDAC (see Figure 7). See ac characteristics under Electrical Characteristics for the timing relationship between SCLK and $\overline{\text{LOAD}}$. This mode of clocking is valid for all multiplex ratios.

ATT20C458 Clock Mode
(CR3[7] = CR3[5] = CR4[7] = 0)

The ATT20C567 can be clocked like the ATT20C458 RAMDAC (see Figure 8). The CLOCK and $\overline{\text{CLOCK}}$ pins are driven with an external positive ECL clock source. An external $\overline{\text{LOAD}}$ signal loads pixels into an input latch. In this mode, there is an internal load signal, ILOAD, which loads the latched data into the internal pixel pipeline. ILOAD will automatically synchronize itself to $\overline{\text{LOAD}}$. ILOAD may also be reset externally. The 458 clocking mode is valid for 4:1 and 8:1 multiplexing only. See Resetting the Pipeline Delay for information indicating how to set the pipeline delay in the ATT20C458 clock mode.

Table 21. Clocking Mode Control Bits

Clocking Mode	Enhanced Visuals CR3[7]	ATT20C567 $\overline{\text{LOAD}}$ CR3[5]	PLL $\overline{\text{LOAD}}$ CLOCK Multiplier CR4[7]	Comment
1	1	1	1	Set MUX ratio and CLOCK multiplication factor CR4[5:4] and CR4[1:0] (ATT20C567 PLL clock mode).
2	1	1	0	CLOCK multiplier not used (ATT20C567 nonPLL clock mode).
3	0	0	0	CLOCK multiplier not used (ATT20C458 clock mode).

Functional Description (continued)

Clocking (continued)

The following diagram shows 4:1 MUX, 135 MHz operation. $\overline{\text{LOAD}}$ and SCLK do not need to be synchronized.

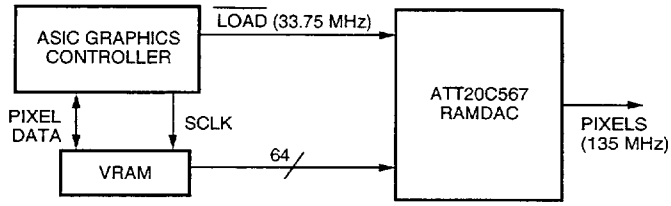


Figure 6. Clocking in ATT20C567 Clock Mode

$\overline{\text{LOAD}}$ rising edge timing requirement must meet SCLK rising edge.

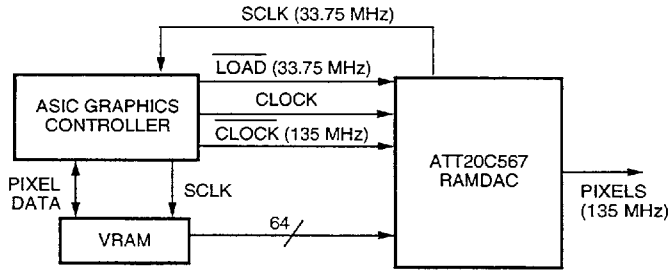


Figure 7. Clocking in ATT20C567 NonPLL Clock Mode

ATT20C458 compatible loading and clocking.

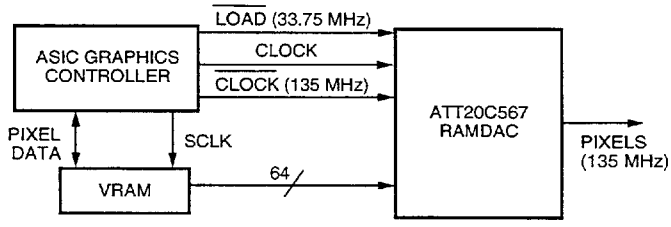


Figure 8. Clocking in ATT20C458 Clock Mode

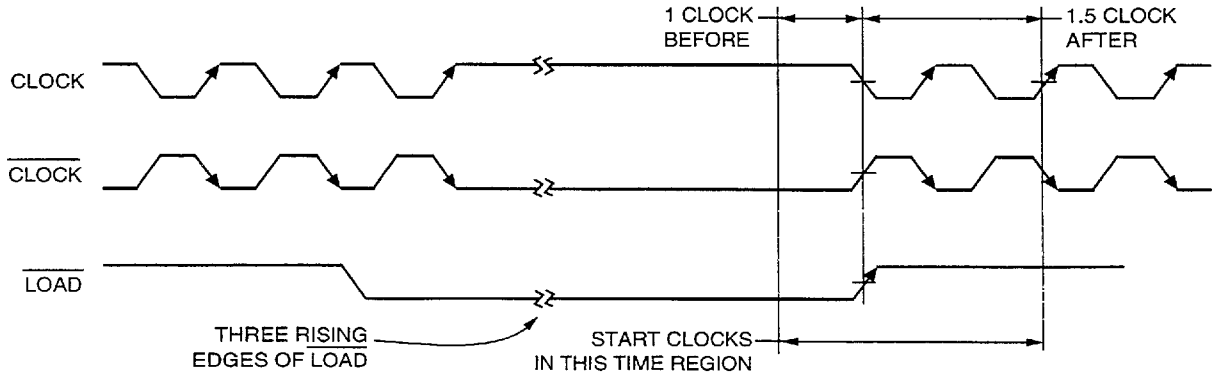


Figure 9. Resetting and Resynchronizing $\overline{\text{LOAD}}$ and ILOAD Externally (ATT20C458 Clock Mode)

Functional Description (continued)

Resetting the Pipeline Delay

After resetting, the CLOCK, $\overline{\text{CLOCK}}$, and $\overline{\text{LOAD}}$ edges do not have to be in a fixed phase relationship. The phase between CLOCK, $\overline{\text{CLOCK}}$, and $\overline{\text{LOAD}}$ can change up to ±180° after the internal load signal ILOAD has been synchronized to the external load signal $\overline{\text{LOAD}}$.

To synchronize the load signals and set the pipeline delay, the chip must be powered up with CLOCK, $\overline{\text{CLOCK}}$, and $\overline{\text{LOAD}}$ running. Stop the clock signal with CLOCK high and $\overline{\text{CLOCK}}$ low for at least three rising edges of $\overline{\text{LOAD}}$. Restart CLOCK and $\overline{\text{CLOCK}}$ as close to the rising edge of $\overline{\text{LOAD}}$ as possible. CLOCK and $\overline{\text{CLOCK}}$ must start switching no more than one clock cycle before the rising edge of $\overline{\text{LOAD}}$ and not more than one and a half clock cycles after the rising edge of $\overline{\text{LOAD}}$ (see Figure 9).

3.3 V I/O Support

The D[7:0] MPU pins and the SCLK output pin support 3.3 V I/O operation. When using 3.3 V I/O, connect the VC33 pins to 3.3 V. If 3.3 V I/O is not required on the MPU data pins and SCLK pin, connect the VC33 pins to 5 V.

SYOUT and $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ Current

The ATT20C567 can output either the $\overline{\text{SYNC}}$ or the $\overline{\text{BLANK}}$ waveform on the SYOUT pin or this output may be disabled. SYOUT is controlled with CR2[3:1]. The SYOUT pin may be used as a signal (current source) to indicate the analog output delay. This is useful when generating a $\overline{\text{SYNC}}$ signal or when using multiple ATT20C567 devices. When using SYOUT as a $\overline{\text{SYNC}}$ current source, tie the SYOUT output to one of the DAC outputs. The output with SYOUT tied to it will have a composite $\overline{\text{SYNC}}$ signal on that output. When using multiple devices, this output can be fed back to a clock skewing device. The clock skewing device will skew the clocks to the devices causing all output pixels to line up.

Sleep Mode

The ATT20C567 can be powered down by setting CR3[4] = 1. When asleep, the RAMDAC will consume minimum power and retain the contents of the color and overlay RAMs. The color and overlay RAMs cannot be written or read while the device is asleep, while the internal registers can be written or read.

MPU Interface

The ATT20C567 supports a standard MPU interface, allowing the MPU to access the RAMDAC registers or RAMs. The R[2:0] inputs select which RAM or register will be accessed. An 8-bit address register indirectly addresses the RAMDAC RAMs. The address registers' bit 0 (AD[0]) corresponds to D0 of the MPU port and is the least significant bit.

Operation of the MPU interface occurs asynchronously to the pixel clock. The internal color look-up tables are single-ported memories, and internal logic synchronizes the MPU data to the pixel stream.

To monitor the red, green, and blue read/write cycles, the address register has an internal modulo three counter, as shown in the table below. They are reset to 0 when the MPU writes to the address register, and are not reset to 0 when the MPU reads the address register. The MPU can read the address register at any time without modifying its contents. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAMs.

Table 22. Modulo Counter Operation

MOD[1:0]	Addressed by MPU
00	Red value
01	Green value
10	Blue value

Functional Description (continued)

Writing the RAMDAC Color RAMs

The MPU writes the address register, AD, (see Table 3) with the address of the RAM location to be modified. To write pixel or overlay colors, the MPU completes three continuous write cycles (8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written. Following a blue write cycle to pixel color RAMs at location $FF, the address register resets to $00.

Reading the RAMDAC Color RAMs

The MPU writes the address register, AD, (see Table 3) with the address of the RAM location to be read. The contents of the pixel or overlay color RAM at the address specified by the address register are copied into an internal RGB register. The MPU completes three continuous read cycles (8 bits each of red, green, and blue), and the address register advances to the next address. The first address must be written to the address register to ensure the RGB register has the data desired. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Following a blue read or write cycle to pixel color RAMs at location $FF, the address register resets to $00.

Monitor Sense

The sense bit, TR1[3], is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level (340 mV). This output is used to determine the presence of a CRT monitor, and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a ±70 mV tolerance. Note that $\overline{SYNC}$ should be a logic 0 for TR1[3] to be stable.

Setting DAC Output Current

The equation to set the devices full-scale DAC output current is shown below. V_{REF} is the voltage reference in volts, and RSET is the resistor connected between the FSET pin and ground.

For RS-343A output voltage levels, RSET should be 523 Ω for an output with $\overline{SYNC}$ or $\overline{BLANK}$ current and 495 Ω for an output with no $\overline{BLANK}$ current. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below:

I_{OUT} (mA) = [V_{REF} (V) · 8,067]/RSET (Ω)

With $\overline{SYNC}$ tied to an output, use the following formula for the composite output.

Composite I_{OUT} (mA) = [V_{REF} (V) · 11,294]/RSET (Ω)

In this case, a voltage reference of 1.235 V with RSET = 523 Ω or 495 Ω results in an output of 19.05 mA for the equations above without $\overline{SYNC}$ current and 26.67 mA with $\overline{SYNC}$ current. For RS-343A voltage levels, convert this current to voltage with a doubly terminated 75 Ω system.

Functional Description (continued)

Gamma ROM

Table 23. Gamma ROM Values

The ROM reads are performed in similar fashion as the RAM reads.

Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
0	0	44	116	88	158	132	190	176	216	220	239
1	21	45	117	89	159	133	190	177	216	221	239
2	29	46	118	90	160	134	191	178	217	222	240
3	34	47	119	91	160	135	191	179	217	223	240
4	39	48	120	92	161	136	192	180	218	224	241
5	43	49	121	93	162	137	193	181	219	225	241
6	47	50	122	94	163	138	193	182	219	226	242
7	50	51	124	95	163	139	194	183	220	227	242
8	54	52	125	96	164	140	195	184	220	228	242
9	57	53	126	97	165	141	195	185	221	229	243
10	59	54	127	98	166	142	196	186	221	230	243
11	62	55	128	99	167	143	197	187	222	231	244
12	64	56	129	100	167	144	197	188	222	232	244
13	67	57	130	101	168	145	198	189	223	233	245
14	69	58	131	102	169	146	198	190	223	234	245
15	71	59	132	103	170	147	199	191	224	235	246
16	73	60	133	104	170	148	200	192	224	236	246
17	75	61	134	105	171	149	200	193	225	237	247
18	77	62	135	106	172	150	201	194	225	238	247
19	79	63	136	107	172	151	201	195	226	239	248
20	81	64	137	108	173	152	202	196	226	240	248
21	83	65	138	109	174	153	203	197	227	241	249
22	85	66	139	110	175	154	203	198	228	242	249
23	86	67	140	111	175	155	204	199	228	243	250
24	88	68	141	112	176	156	204	200	229	244	250
25	90	69	142	113	177	157	205	201	229	245	250
26	91	70	142	114	177	158	206	202	230	246	251
27	93	71	143	115	178	159	206	203	230	247	251
28	94	72	144	116	179	160	207	204	231	248	252
29	96	73	145	117	180	161	207	205	231	249	252
30	97	74	146	118	180	162	208	206	232	250	253
31	99	75	147	119	181	163	208	207	232	251	253
32	100	76	148	120	182	164	209	208	233	252	254
33	102	77	149	121	182	165	210	209	233	253	254
34	103	78	150	122	183	166	210	210	234	254	255
35	104	79	150	123	184	167	211	211	234	255	255
36	106	80	151	124	184	168	211	121	235		
37	107	81	152	125	185	169	212	213	235		
38	108	82	153	126	186	170	212	214	236		
39	109	83	154	127	186	171	213	215	236		
40	111	84	155	128	187	172	214	216	237		
41	112	85	155	129	188	173	214	217	237		
42	113	86	156	130	188	174	215	218	238		
43	114	87	157	131	189	175	215	219	238		

Functional Description (continued)

Gamma ROM (continued)

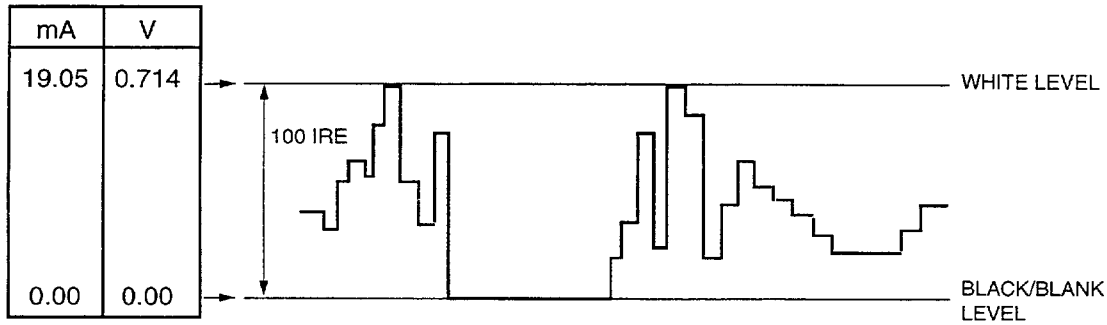


Figure 10. RS-343A Video Output Waveforms (No Sync or Blank)

Table 24. RS-343A Video Output Levels

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	IOUT (mA)
$FF	0	1	White	19.05
data	0	1	DATA	data
$00	0	1	BLACK	0
$XX	0	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load; SETUP = 0 IRE. VREF = 1.235 V, RSET = 495 Ω.

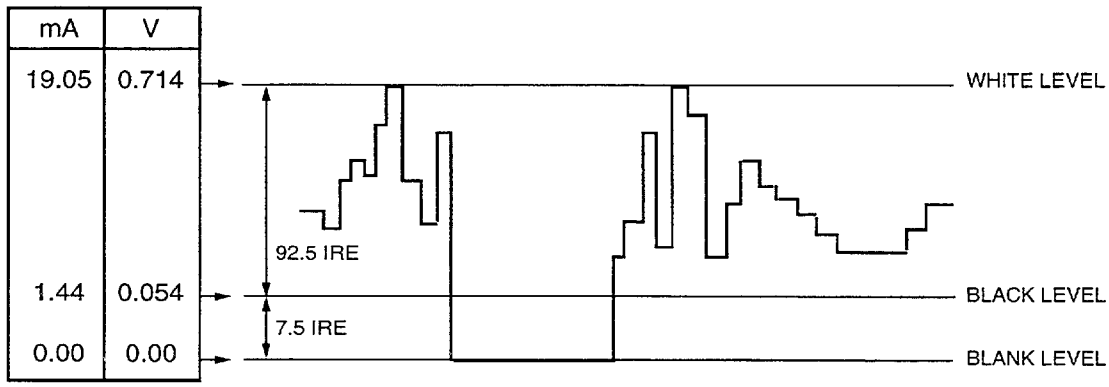


Figure 11. RS-343A Video Output Waveforms (No Sync)

Table 25. RS-343A Video Output Levels

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	IOUT (mA)
$FF	0	1	White	19.05
data	0	1	DATA	data + 1.44
$00	0	1	BLACK	1.44
$XX	0	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load; SETUP = 0 IRE. VREF = 1.235 V, RSET = 523 Ω.

Functional Description (continued)

Gamma ROM (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

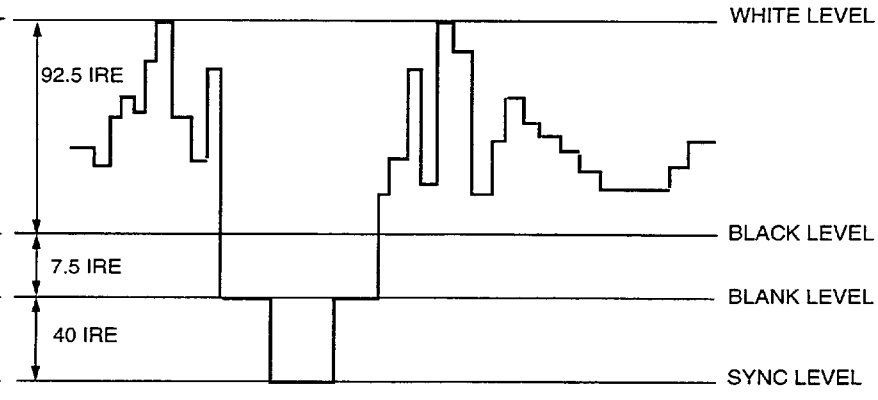


Figure 12. RS-343A Video Output Waveforms (PLL Output Tied to Green Output)

Table 26. RS-343A Video Output Levels

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	IOUT (mA) $\overline{\text{SYNC}}$ Disabled	IOUT (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	White	19.05	26.67
data	1	1	DATA	data + 1.44	data + 9.05
data	0	1	DATA-$\overline{\text{SYNC}}$	data + 1.44	data + 1.44
$00	1	1	BLACK	1.44	9.05
$00	0	1	BLACK-$\overline{\text{SYNC}}$	1.44	1.44
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load; blank pedestal on. VREF = 1.235 V, RSET = 523 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This also helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A four-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies, as well as less spectral content in emitted frequency bands. Using a solid ground plane, the board should have signal layers 1 and 4 (outside layers) and supply layers 2 and 3 (inside layers).

The ATT20C567 should be placed close to the video output connector and between the video output connector and the edge card connector (see Figure 13). This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

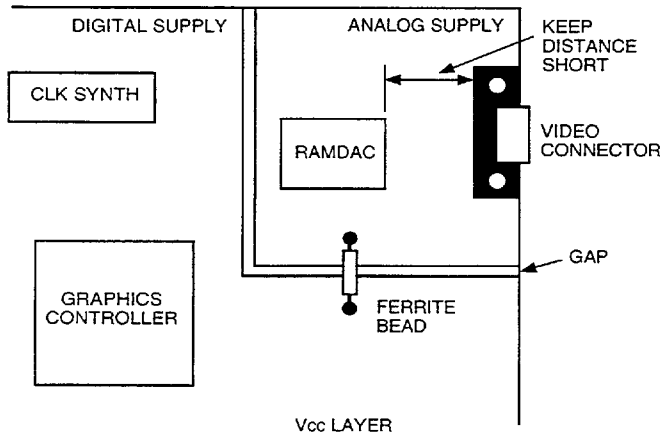


Figure 13. Digital and Analog Supply Plane Split

Power Distribution

Separate the power plane into digital and analog areas as illustrated in Figures 13 and 22. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, mixed-signal chips, and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the board, but lower than the second harmonic (2x) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz: Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690.

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT20C567, decouple Vcc pin groupings to ground with a 0.1 µF capacitor. For higher-frequency pixel clocks (>120 MHz), use a 0.01 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher-frequency noise to ground. Power supply noise should be less than 200 mV for a good design. Supply noise greater than 400 mV should be avoided. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figure 22, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Application Information (continued)

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the V[7:0] and P[A:D] [7:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges since they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Avoiding high slew rate pixel inputs is especially important with the ATT20C567 because the RAMDAC has 40 digital pixel inputs. The increased number of pixel inputs increases the noise that may be coupled to the DAC outputs through capacitive coupling into the substrate. Wherever possible, use slower edge rate (3 ns—5 ns) logic such as 74S or 74ALS devices. If this is not possible, edges can be slowed down by using series termination (75 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled-impedance striplines and parallel termination. The 2x clock doubler in the ATT20C567 will help to reduce signal quality problems and EMI radiations by reducing the frequency of the clock signal to the device.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination, which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector. Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the ground of the edge card connector (see Figure 14).

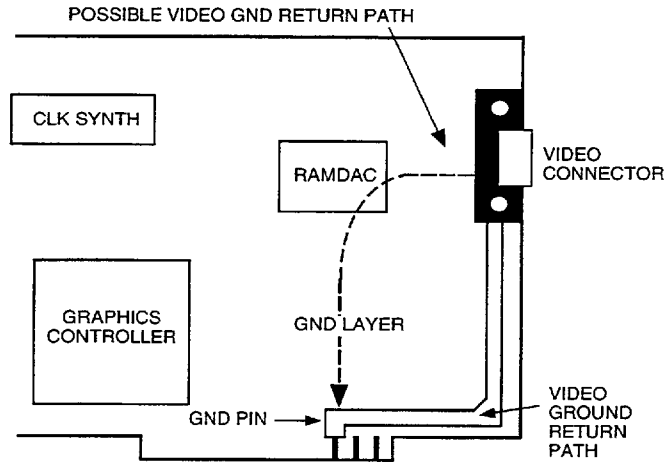


Figure 14. Video Ground Return Current Path

DAC Outputs

The ATT20C567 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figure 15 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

Application Information (continued)

Application Examples

This section details several examples of using the ATT20C567 in various applications in different operating modes.

Generation of SCLK

The shift clock, SCLK, for VRAMs can be generated by either the controller or by the ATT20C567.

The cost-effective solution is to have the controller generate SCLK as well as LOAD. This eliminates the clock synthesizer for the CLOCK and $\overline{\text{CLOCK}}$ inputs on the ATT20C567. The SCLK pin of the RAMDAC is then left unconnected. The SCLK output from the controller is connected to the VRAM banks, and the LOAD output is directly connected to the $\overline{\text{LOAD}}$ input (see Figure 15).

The RAMDAC generates SCLK only in the ATT20C567 mode of operation. It requires a clock input on CLOCK and $\overline{\text{CLOCK}}$ pins. The input clock is divided by the multiplex factor and is output on SCLK. An external $\overline{\text{LOAD}}$ is generated from SCLK by delaying it (see Figure 16). The PLL logic of the ATT20C567 generates the internal pixel clock from the load clock by multiplying it by 2, 4, or 8 depending on the multiplex mode. The generation of the internal pixel clock from $\overline{\text{LOAD}}$ instead of CLOCK and $\overline{\text{CLOCK}}$ eliminates the $\overline{\text{LOAD}}$ to SCLK ac specifications of the ATT20C567 (i.e., no dead zone).

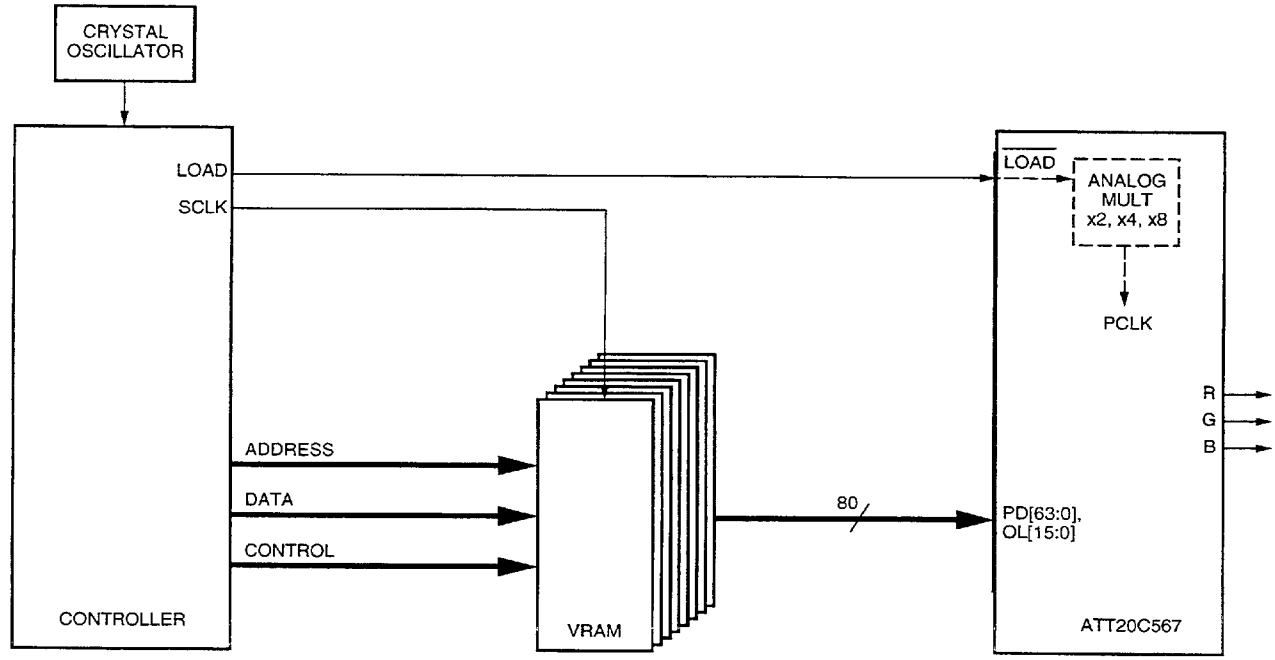


Figure 15. SCLK Generated by Controller

Application Information (continued)

Application Examples (continued)

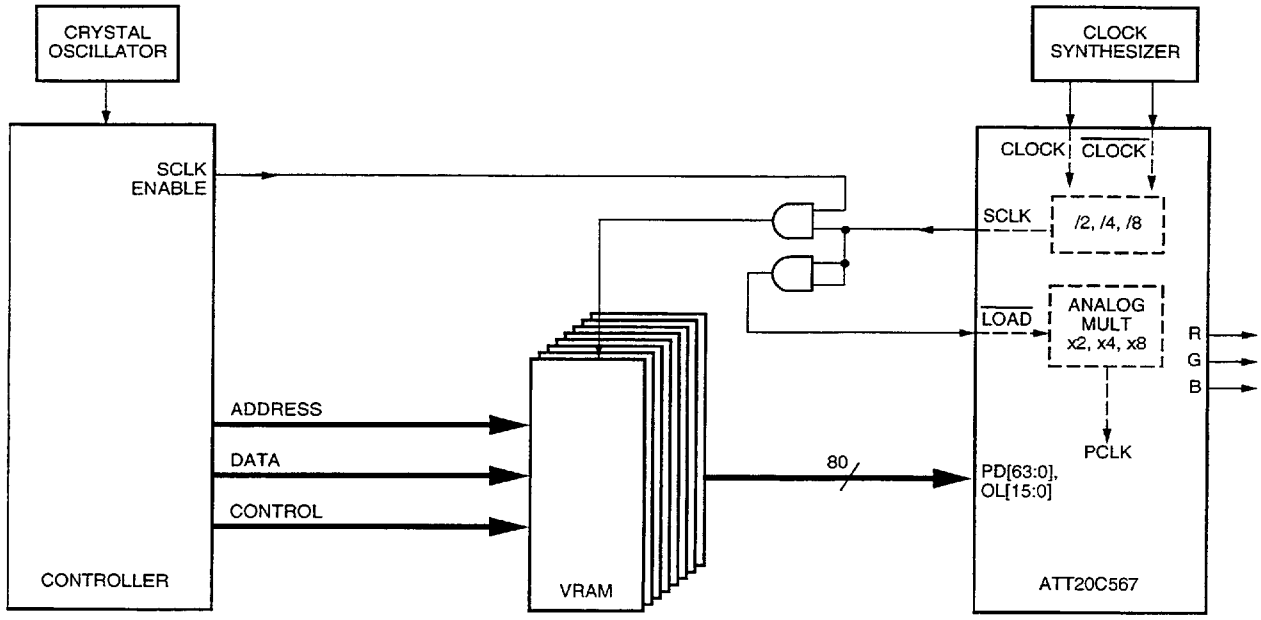


Figure 16. Generation of SCLK by ATT20C567

Single-Frame Buffer, 64-Bit Interface

The single-bank, single-frame buffer design is for low-cost workstations. The data bus connecting the controller and the VRAM frame buffer is limited to a maximum of 64 bits. An example for 4:1 MUX mode is shown in Figure 17, and 2:1 MUX mode is shown in Figure 18. Note that the pixel port can be enabled for input in the ATT20C567 to 16, 32, or 64 pins.

Application Information (continued)

Application Examples (continued)

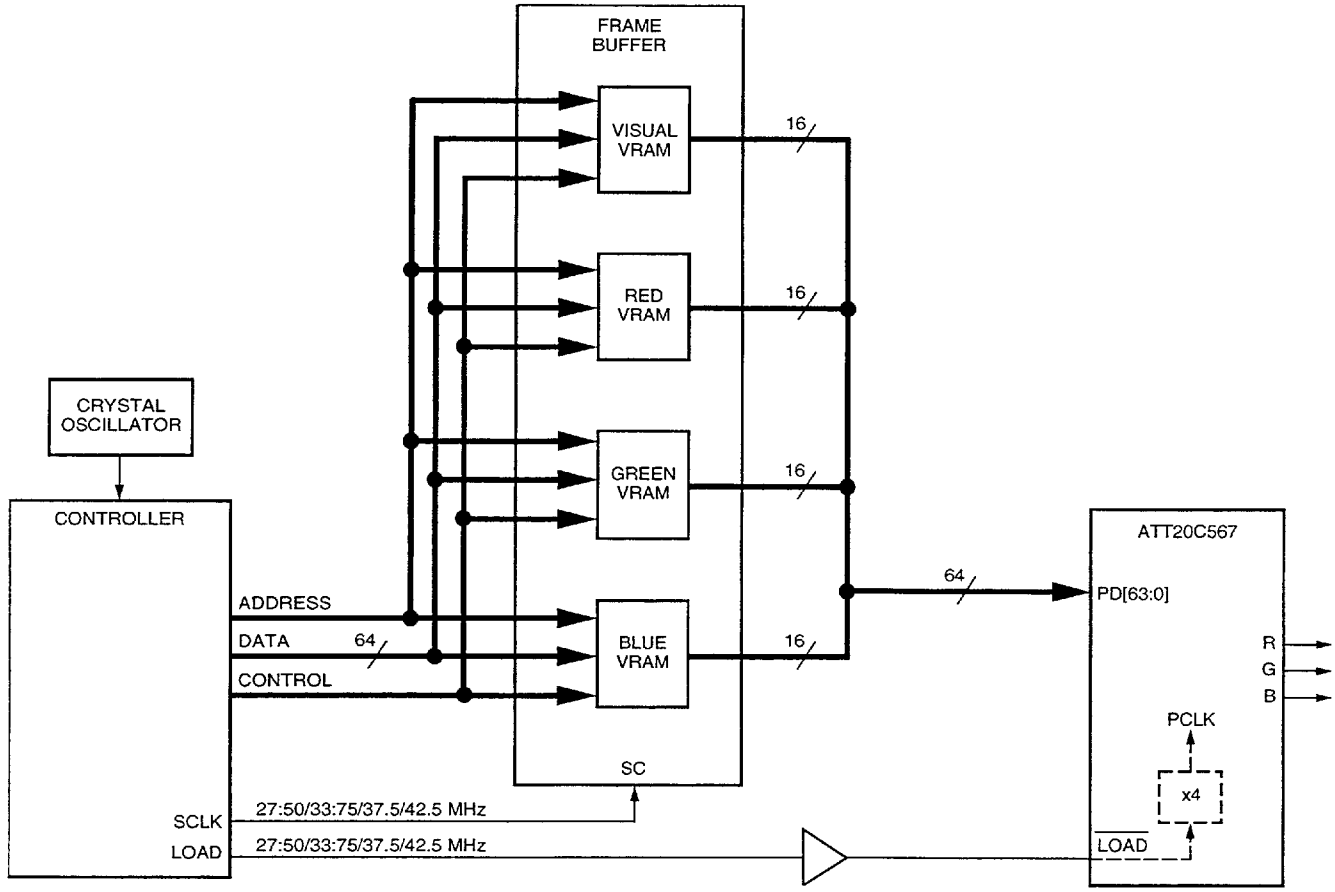


Figure 17. Single-Frame Buffer, 64-Bit Interface for 16-Bit Pixel, 4:1 MUX Mode

Application Information (continued)

Application Examples (continued)

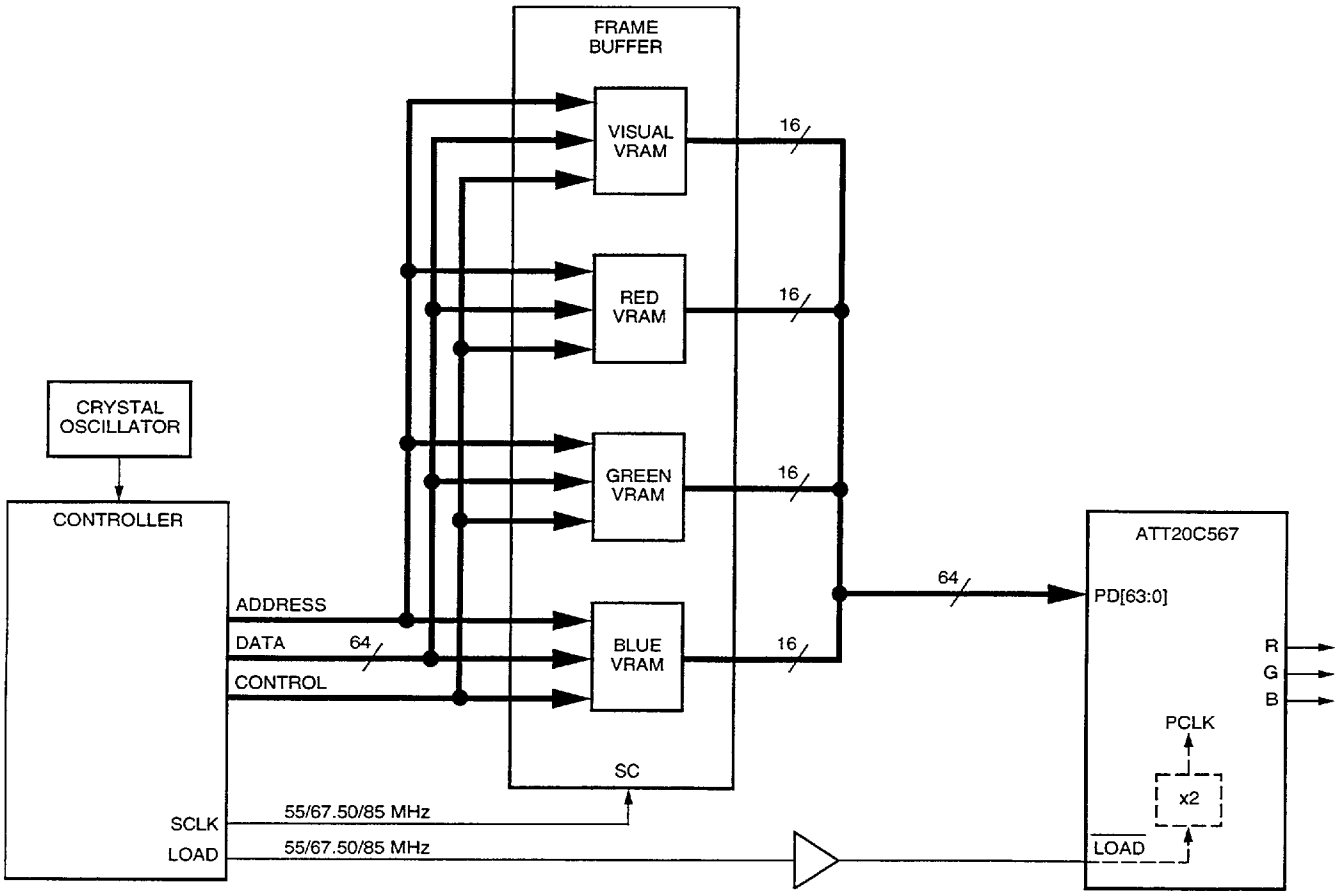


Figure 18. Single-Frame Buffer, 64-Bit Interface for 32-Bit Pixel, 2:1 MUX Mode

Application Information (continued)

Application Examples (continued)

Single-Frame Buffer, 128-Bit Interface

The newer controllers are capable of bursting data into the VRAM. Normally, four dwords (32-bit data) burst in one cycle. The graphics performance can be improved if all four dwords are transferred into the RAMDAC in only one load cycle. This can be achieved with the ATT20C567 by using an external 2-to-1 multiplexer as shown in Figure 19.

The controller is connected to two 64-bit VRAM banks used for storing pixel data and two 16-bit banks used for overlay data.

The consecutive pixels are loaded into alternate banks. Both banks are connected to the same SCLK. However, only one bank is enabled for output at a time. The data output from the bank is fed into the 2-to-1 multiplexer.

The load clock is divided by two and used as data select input for the multiplexer. The 64-bit pixel data and 16-bit overlay data is fed into the RAMDAC from the multiplexer.

The load clock is delayed to meet the pixel data to $\overline{\text{LOAD}}$ setup before it is fed into the RAMDAC.

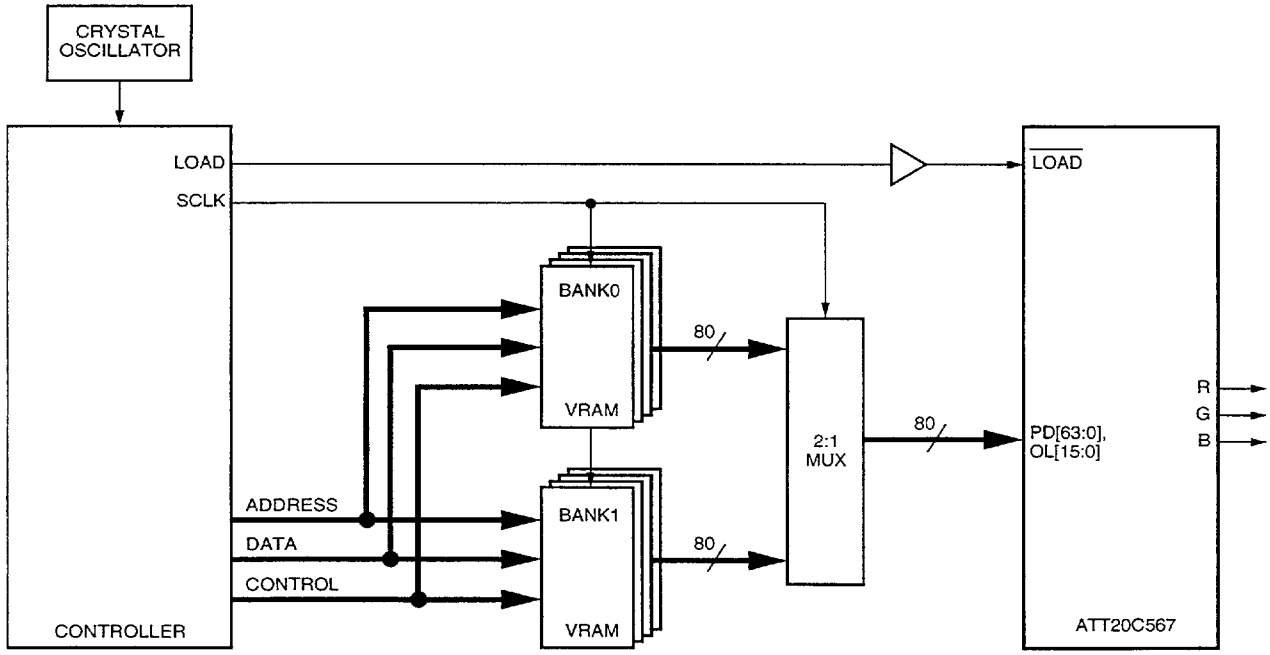


Figure 19. Single-Frame Buffer, 128-Bit Interface

Application Information (continued)

Application Examples (continued)

Double-Frame Buffer Interface

The ATT20C567 supports double-buffering in 32-bit pixel 4-4-4 true-color or pseudocolor modes. When two frame buffers are used, the pixel to be displayed is selected from either bank depending on the state of the visual bit V3. While the data from one buffer is being displayed, the controller can modify the data in the other buffer without affecting the visual quality of the display.

An example for 32-bit pseudomode double-buffering is shown in Figure 20. Each frame buffer contains two 8-bit pixels. Pixel 0 of frame buffer 0 is connected to PD[7:0], while pixel 0 of buffer 1 is transferred to the RAMDAC on PD[15:8].

Similarly, pixel 1 of buffer 0 is presented on PD[39:32] and that of buffer 1 on PD[47:40]. The visual bit V3 is passed on data bit PD[27] for pixel 0 and PD[59] for pixel 1. When V3 is low, PD[7:0] is selected as input for pixel 0 and PD[39:32] for pixel 1. A logic high on V3 selects PD[15:8] and PD[47:40] from buffer 1.

Figure 21 depicts a system connection diagram for double-buffering using 32-bit pixel 4-4-4 true-color mode. For each color, lower and upper nibbles are connected to separate frame buffers. The lower nibble, for example, in Figure 21, is connected to frame buffer 0 while the upper one is connected to frame buffer 1. Depending on the status of the visual bit V3, either of the nibbles is selected.

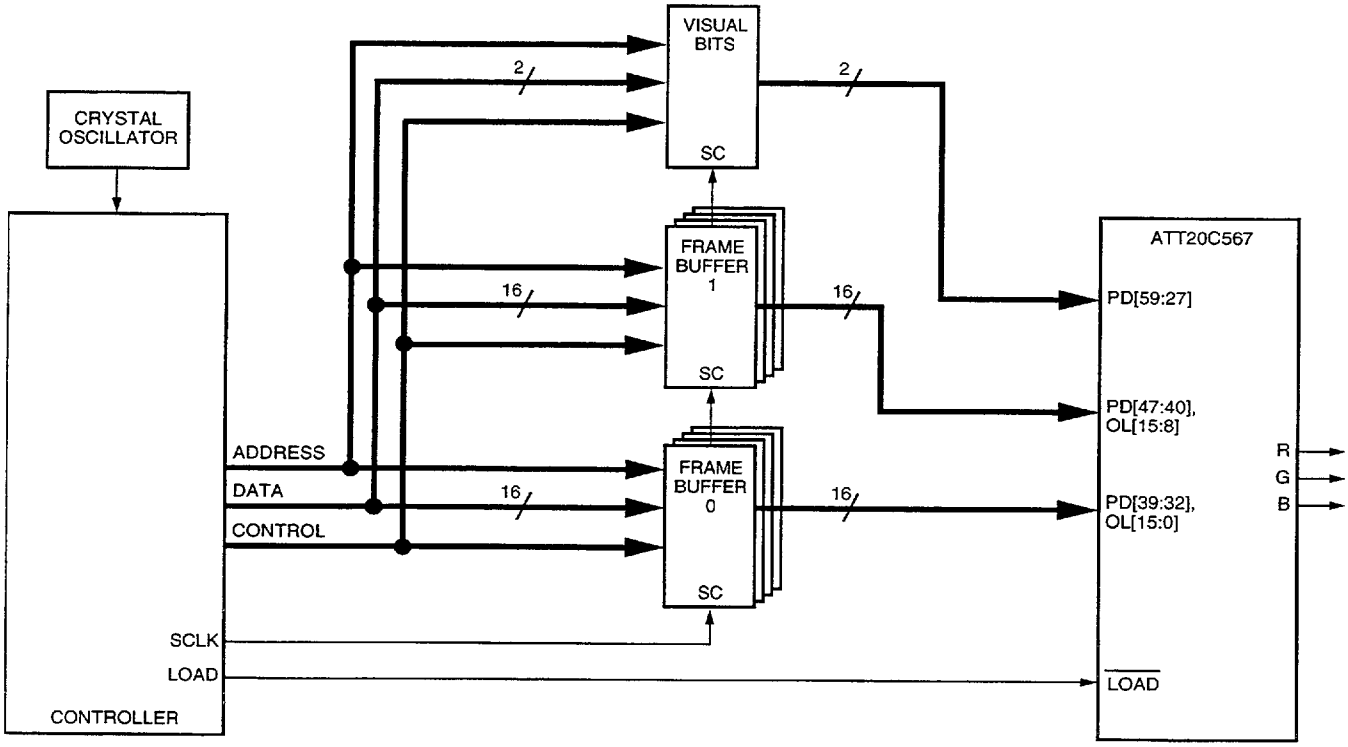


Figure 20. Double-Frame Buffer, 32-Bit Pseudocolor Mode

Application Information (continued)

Application Examples (continued)

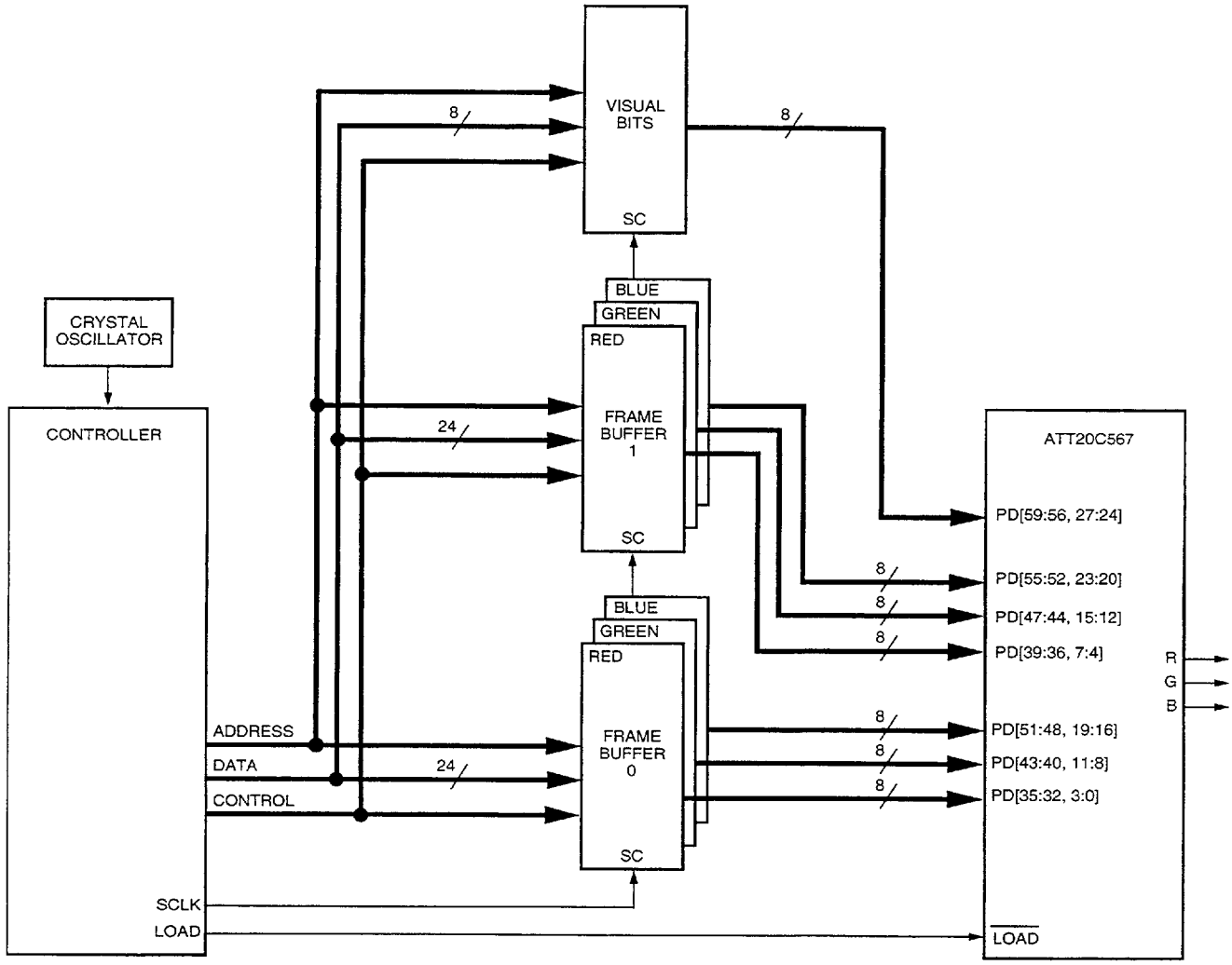


Figure 21. Double-Frame Buffer, 32-Bit 4-4-4 True-Color Mode

Application Information (continued)

Application Examples (continued)

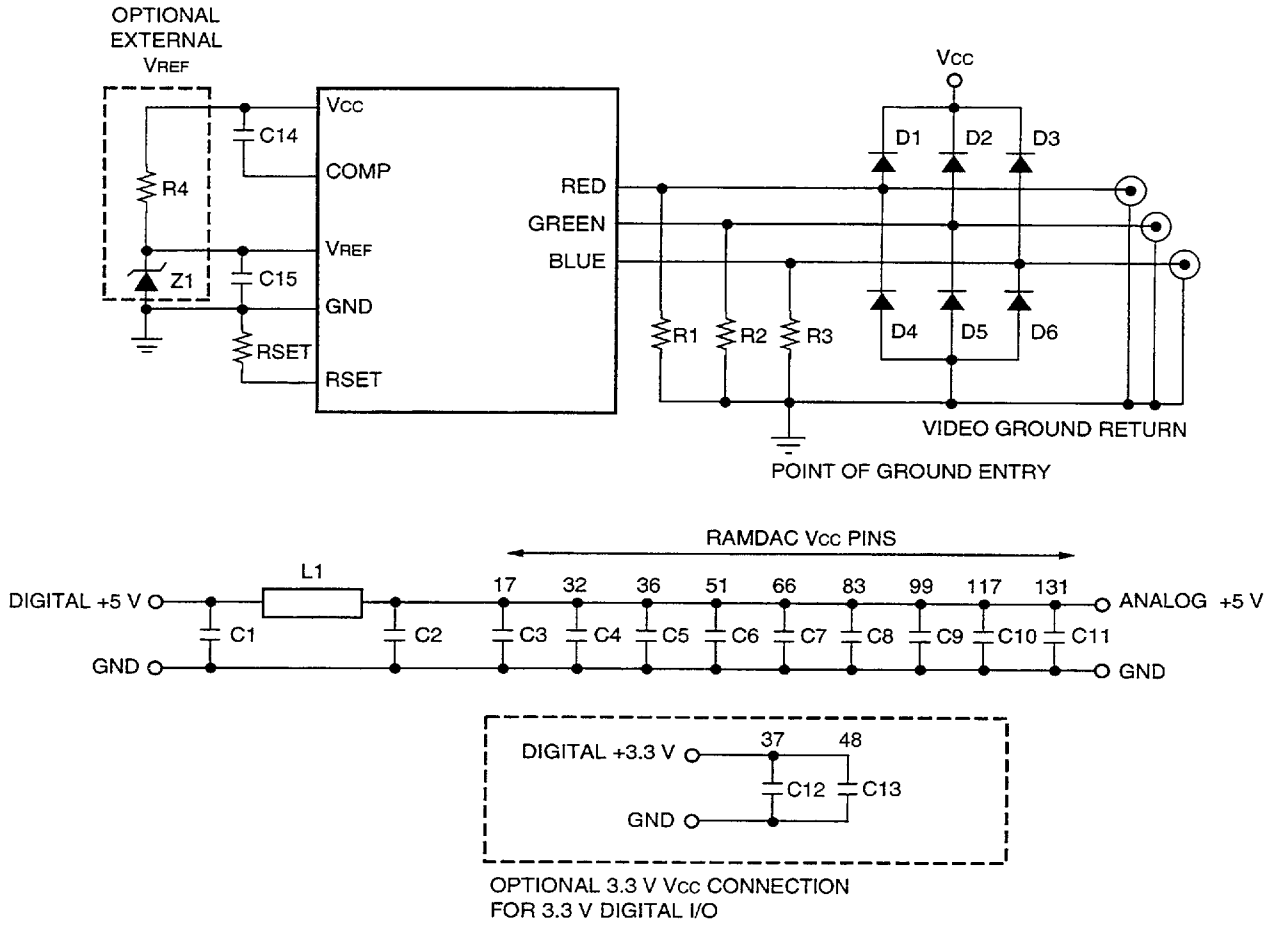


Figure 22. External and Internal Voltage Reference Typical Connection Diagram

Table 27. External and Internal Voltage Reference Parts List

Location	Description	Vendor Part Number
C1, C3—C16	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C
D1—D6	Fast-switching diodes	National 1N4148/49
Z1*	1.2 voltage reference	National Semiconductor LM385BZ-1.2
R4*	1 kΩ, 5% resistor	—

* Optional for external VREF.

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C567.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Vcc (measured to GND)	—	—	—	7.0	V
Voltage on Any Digital Pin	—	GND – 0.5	—	Vcc + 0.5	V
Analog Output Short Circuit: Duration to Any Power Supply or Common	ISC	—	indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	T_{stg}	–65	—	150	°C
Junction Temperature	TJ	—	—	150	°C
Vapor Phase Soldering (60 s)	TV_{SOL}	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	Vcc VC33	4.75 3.14	5.00 3.3	5.25 3.47	V V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	RL	—	37.5	—	Ω
White Level Adjust Resistor	FSET	—	523	—	Ω

Electrical Characteristics

Table 28. dc Characteristics 1

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 523 Ω, internal V_{REF}, SETUP = 7.5 IRE. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	Cin	—	—	7	pF
Digital Outputs (including SCLK):					
Output Voltage:					
Low (I_{OL} = 4 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –4 mA)	V_{OH}	2.4	—	—	V
3-State Current	I_{OZ}	—	—	50	µA
Capacitance	C_{DOUT}	—	—	7	pF
Differential Clock Operation:					
Input Voltage:	Del VCLK	0.6	—	6	V
Low (I_{IN} = –1 µA)	V_{IL}	GND – 0.5	—	V_{CC} – 1.5	V
High (I_{IN} = 1 µA)	V_{IH}	V_{CC} – 1.1	—	V_{CC} – 0.8	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{ILC}	—	—	–1	µA
High (V_{IN} = 4.0 V)	I_{IHC}	—	—	1	µA
Single-ended Clock Operation: (110 MHz max):					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.4	V
High	V_{IH}	2.8	—	V_{CC} + 0.5	V
V_{BB} (for $\overline{CLOCK}$)	V_{BB}	—	1.6	—	V
Capacitance (f = 1 MHz, V_{IN} = 4.0 V)	Cin	—	4	4	pF

Electrical Characteristics (continued)

Table 29. dc Characteristics 2

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 523 Ω, internal V_{REF}, SETUP = 7.5 IRE. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC):	—	8	8	8	bits
Accuracy (each DAC):					
Integral Linearity Error	IL	—	—	±1	LSB
Differential Linearity Error	DL	—	—	±1	LSB
Gain Error	—	—	±3	±5	%
Monotonicity	—	—	Guaranteed	—	Scale
Coding	—	—	—	—	Binary
Analog Outputs:					
Gray Scale Current Range	Igray	—	—	20	mA
Output Current:					
White Level Relative to Black	Iwb	16.74	17.62	18.50	mA
Black Level Relative to Blank:	Ibb				
With Pedestal	—	0.95	1.44	1.90	mA
Without Pedestal	—	0	5	50	µA
Blank Level	Iblank	6.29	7.62	8.96	mA
Sync Level	Isync	0	5	50	µA
LSB Size	Ilsb	—	69.9	—	
DAC to DAC Matching	—	—	2	5	%
Output Compliance	V_{OC}	–0.5	—	1.5	V
Output Impedance	RA_{OUT}	—	10	—	kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}	—	—	30	pF
Internal Reference Output @1 mA	V_{REF}	—	1.235	—	V
SENSE Trip Level	V_{SEN}	270	340	410	mV
Power Supply Rejection Ratio	PSRR	—	—	0.5	%/% ΔV_{CC}
COMP = 0.1 F, f = 1 kHz	—	—	—	–6	dB

Electrical Characteristics (continued)

Table 30. ac Characteristics—Clocks

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is RSET = 523 Ω, internal V_{REF}. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. SCLK output loading ≤15 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		170 MHz Devices		135 MHz Devices		110 MHz Devices		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
CLOCK, $\overline{CLOCK}$ Rate:								
Differential Inputs	fmax	—	170	—	135	—	110	MHz
Single-ended Inputs	fmax	—	110	—	110	—	110	MHz
$\overline{LOAD}$ and SCLK Rates:								
2:1	—	—	85.00	—	67.5	—	55	MHz
4:1	—	—	42.50	—	33.5	—	27.5	MHz
8:1	—	—	21.25	—	16.9	—	13.75	MHz
CLOCK, $\overline{CLOCK}$ Cycle Time	1	5.88	—	7.4	—	9.09	—	ns
CLOCK, $\overline{CLOCK}$ Width High or Low	2	2.94	—	3.2	—	4	—	ns
$\overline{LOAD}$ and SCLK Cycle Time:								
2:1	3	11.76	—	14.81	—	18.18	—	ns
4:1	3	23.52	—	29.58	—	36.36	—	ns
8:1	3	47.04	—	59.17	—	72.72	—	ns
$\overline{LOAD}$ and SCLK Widths High or Low:								
2:1	4	4.70	—	6	—	7.25	—	ns
4:1	4	9.41	—	12	—	14.5	—	ns
8:1	4	18.82	—	24	—	29	—	ns

Table 31. ac Characteristics—Supply Current

		170 MHz Devices		135 MHz Devices		110 MHz Devices		
Parameter	**Symbol**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Vcc Supply Current	Icc	270	360	276	315	206	275	mA
Powerdown Current	Islp	10	—	10	—	10	—	mA

Electrical Characteristics (continued)

Table 32. ac Characteristics—DAC Performance and Pipeline Delay

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is RSET = 523 Ω, internal V_{REF}. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. SCLK output loading ≤15 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
DAC Performance:					
Analog Output Delay	5	—	—	30	ns
Analog Output Rise/Fall Time	6	—	2	—	ns
Analog Output Setting Time	—	—	11	—	ns
Clock and Data Feedthrough	—	—	–30	—	dB
Glitch Energy	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	dB
Analog Output Skew	—	—	—	2	ns
Pipeline Delay:					
2:1 Multiplex, All Clock Modes	—	9	—	9	clks
4:1 Multiplex, All Clock Modes	—	9	—	9	clks
8:1 Multiplex, All Clock Modes	—	9	—	9	clks

Table 33. ac Characteristics—Pixel Timing and MPU Port

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is RSET = 523 Ω, internal V_{REF}. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. SCLK output loading ≤15 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		170 MHz Devices			135 MHz Devices			110 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Pixel Timing:											
P[63:0], OL[15:0], $\overline{BLANK}$, $\overline{SYNC}$, Setup to $\overline{LOAD}$	7	1	—	—	1	—	—	1	—	—	ns
P[63:0], OL[15:0], $\overline{BLANK}$, $\overline{SYNC}$, Hold from $\overline{LOAD}$	8	3	—	—	3	—	—	3	—	—	ns
$\overline{LOAD}$ Rising Edge Setup from SCLK Rising Edge	9	8	—	—	8	—	—	8	—	—	ns
$\overline{LOAD}$ Rising Edge Hold to SCLK Rising Edge	10	0	—	—	0	—	—	0	—	—	ns
Microprocessor Port:											
$\overline{R/W}$, R[2:0] Setup Time	11	10	—	—	10	—	—	10	—	—	ns
$\overline{R/W}$, R[2:0] Hold Time	12	10	—	—	10	—	—	10	—	—	ns
$\overline{CE}$ Pulse Width Low	13	50	—	—	50	—	—	50	—	—	ns
$\overline{CE}$ Pulse Width High	14	6	—	—	6	—	—	6	—	—	ns
$\overline{CE}$ Asserted to D[7:0] Driven	15	5	—	—	5	—	—	5	—	—	pclk
$\overline{CE}$ Asserted to D[7:0] Valid	16	—	—	40	—	—	40	—	—	—	ns
$\overline{CE}$ Asserted to D[7:0] 3-Stated	17	—	—	20	—	—	20	—	—	—	ns
Write D[7:0] Setup Time	18	10	—	—	10	—	—	10	—	—	ns
Write D[7:0] Hold Time	19	10	—	—	10	—	—	10	—	—	ns

Timing Characteristics

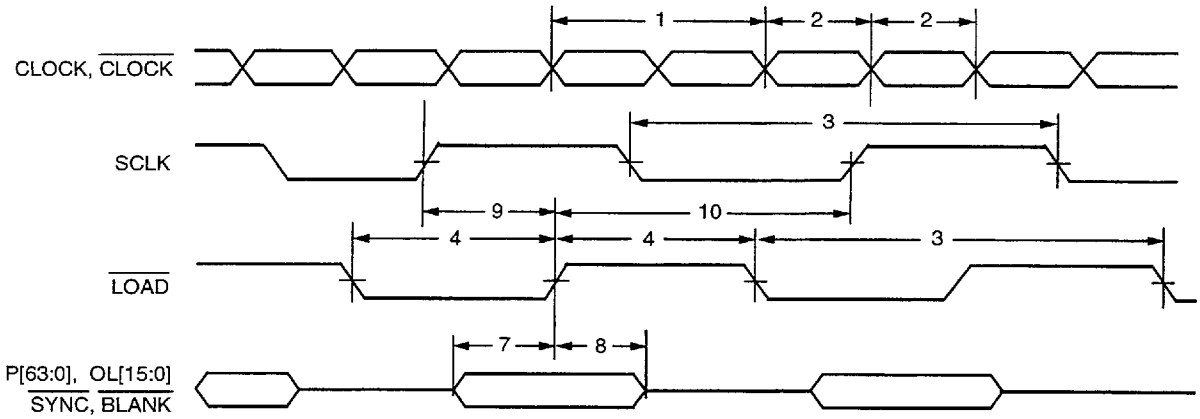


Figure 23. Video Input Timing for 2:1 MUX, 567-Type $\overline{\text{LOAD}}$

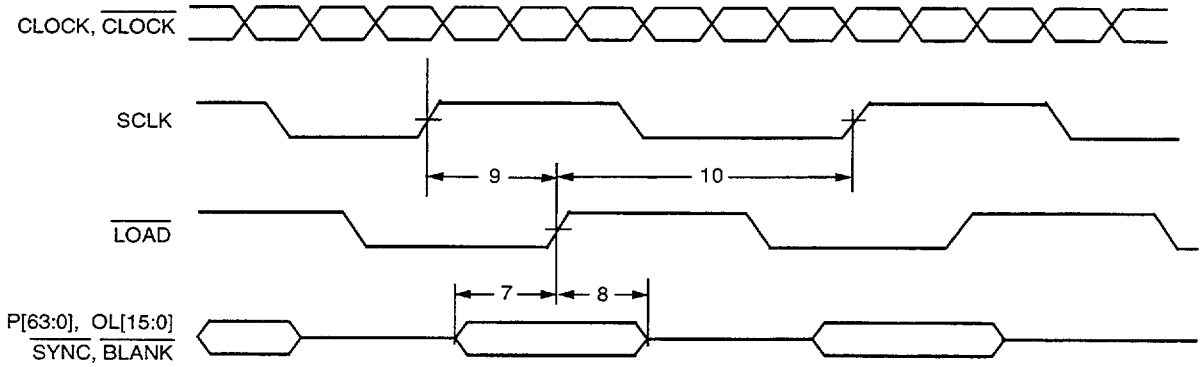


Figure 24. Video Input Timing for 4:1 MUX, 567-Type $\overline{\text{LOAD}}$

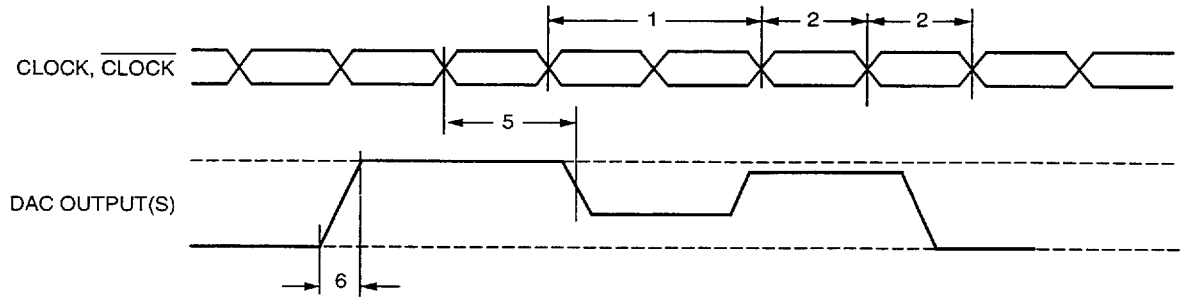


Figure 25. Video Output Timing

Timing Characteristics (continued)

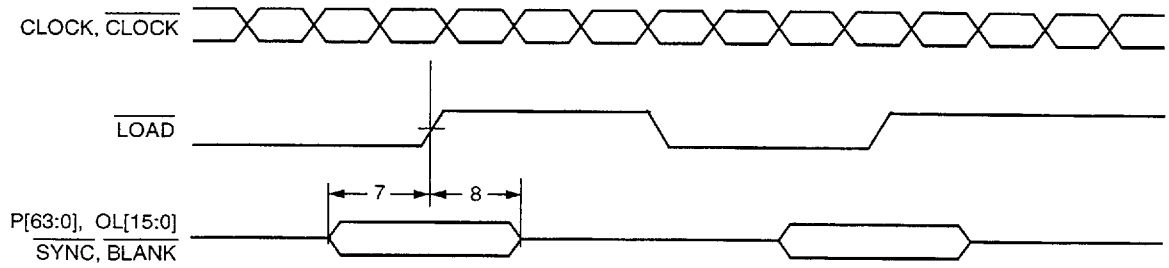


Figure 26. Video Input Timing for 4:1 MUX, 458-Type LOAD

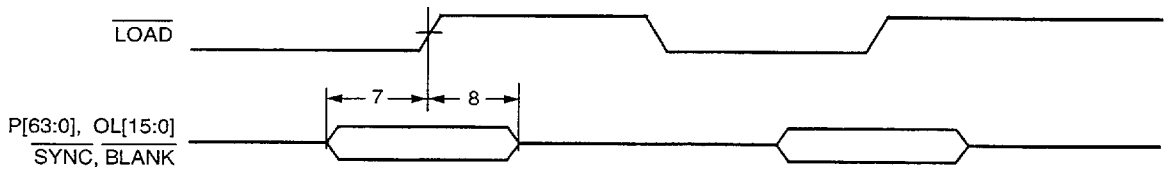


Figure 27. Video Input Timing Using LOAD Only in Clock Mode 3

Timing Characteristics (continued)

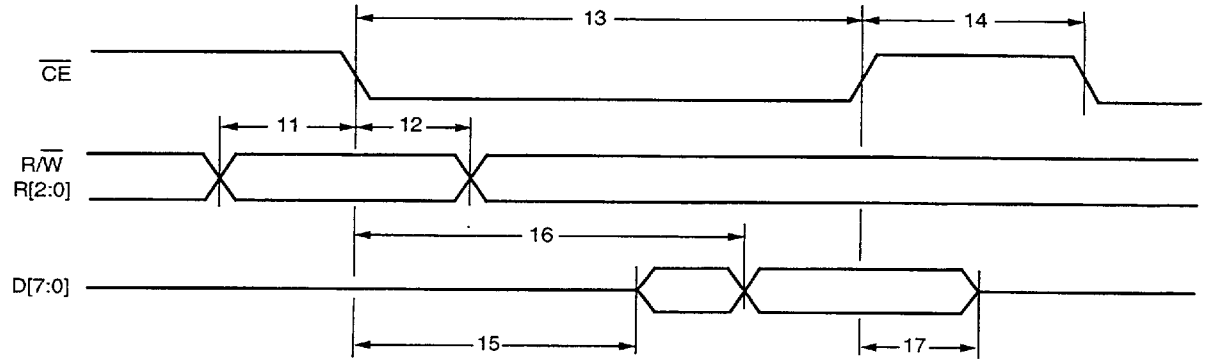


Figure 28. Read-Cycle Timing Diagram

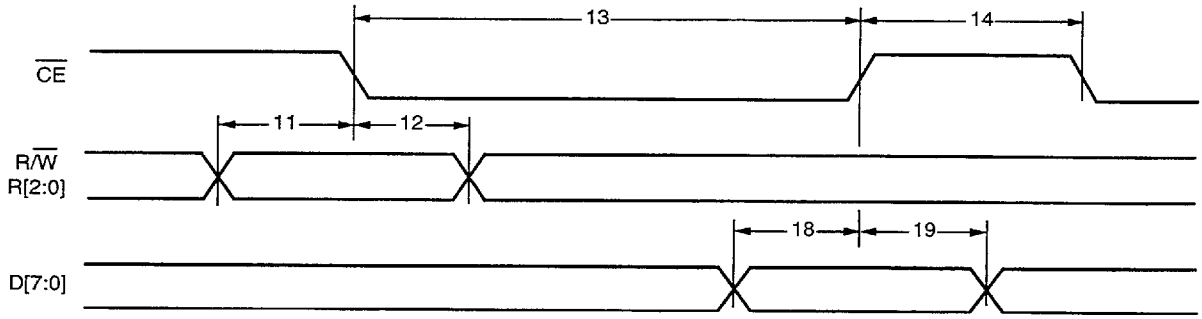
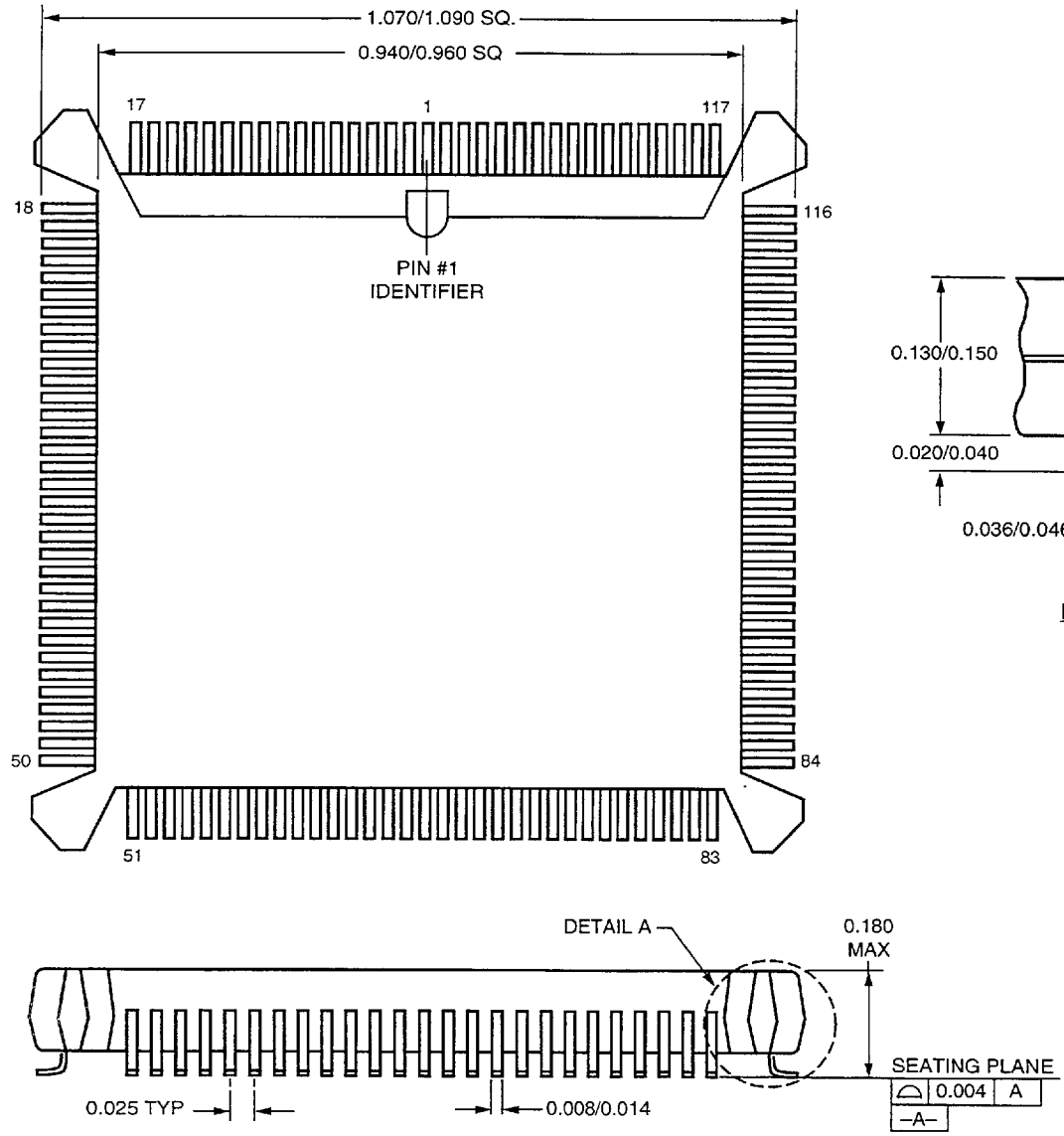


Figure 29. Write-Cycle Timing Diagram

Outline Diagram

132-Pin BQFP Package

Dimensions are in inches.



Ordering Information

Device	Speed	Temperature
ATT20C56717HF132	170 MHz	0 °C—70 °C
ATT20C56713F132	135 MHz	0 °C—70 °C
ATT20C56711F132	110 MHz	0 °C—70 °C