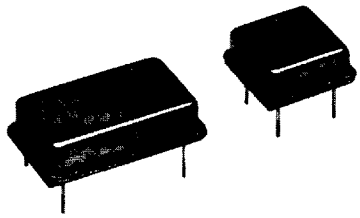
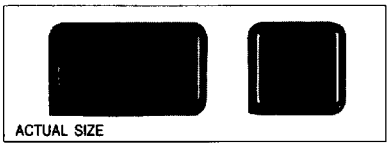
Crystal Clock Oscillator

HCMOS/ACMOS, High Drive

Technical Data

STA Series





Description

A crystal controlled, low-current oscillator providing precise rise and fall times to drive HCMOS/ACMOS and 50 Ohm loads. The tri-state function enables the output to go high impedance. Available in either a 14 or an 8 pin DIP compatible, resistance welded, all metal case. Pin 7 (or Pin 4) is grounded to case to reduce EMI.

Applications & Features

- Suited for use with new HCMOS/ ACMOS MPU's
- Very broad frequency range 250 kHz to 135 MHz
- High Drive ACMOS and HCMOS capability
- Tri-State output
- Optional reverse tri-state logic input
- Reduced EMI circuitry
- Short circuit protected output
- Available in Surface Mount Packages:
  metal: with formed "gull" wing leads (Dimensions not shown - consult factory)
  plastic: See SaRonix STT/STA Series, Type F

Frequency Range:	250 kHz to 135 MHz
Frequency Stability:	±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.
Temperature Range:	
Operating:	0°C to +70°C
Storage:	-55°C to +125°C
Supply Voltage:	
Operating:	+5 VDC ±10%
Absolute Maximum:	+7 VDC
Supply Current:	
up to 60 MHz:	20mA typical, 30mA max @ 25°C 35mA max over operating temperature range
60+ MHz to 80 MHz:	35mA typical, 40mA amx @ 25°C 50mA max over operating temperature range
Above 80 MHz	55mA typical, 65mA max @ 25°C 75mA max over temperature range
Output Drive:	
ACMOS	
Symmetry:	50% ±10% or 5% at 50% V_{DD}
Rise & Fall Times:	20% to 80% V_{DD}, see Part Numbering Guide
Logic 0:	10% V_{DD} max
Logic 1:	90% V_{DD} min
Output Load:	50Ω; or 50pF up to 80 MHz; or 50mA sink and source
Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-883, Method 211, Conditions A and C
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Meethod 210, Condition B
Environmental:	
Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2 $<5 \times 10^{-8}$ ATM cc/sec
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

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SaRonix

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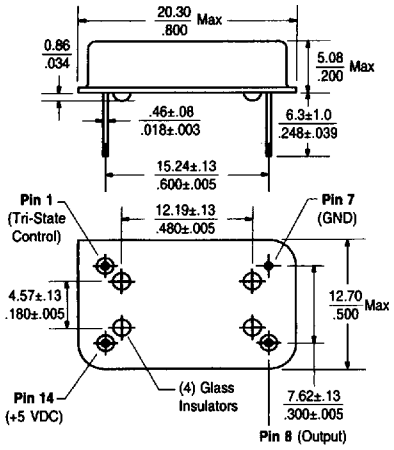
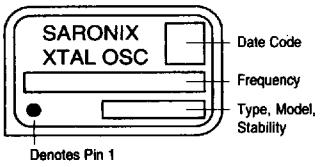
Technical Data — STA Series

Package Details

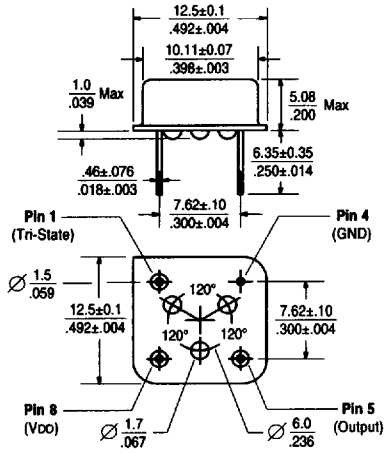
FULL SIZE PACKAGE



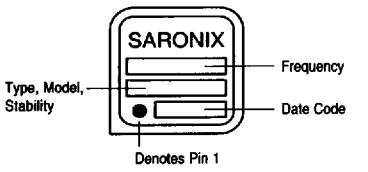
Standard Marking Format



HALF SIZE PACKAGE



Standard Marking Format



Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

STA 0 7 0 C - 40.0000

Series

Symmetry
0 = Symmetry 50% ±10%
A = Symmetry 50% ±5%

Rise/Fall Times
7 = 4.0 nsec r/f, 5.0 nsec max (Std to 44.9 MHz)*
8 = 2.5 nsec r/f, 4.0 nsec max (Std 45 to 84.9 MHz)*
9 = 1.8 nsec r/f, 3.0 nsec max (Std 85 to 135 MHz)*

Package Style
0 = Full Size (14 Pin DIP compatible)
9 = Half Size (8 Pin DIP compatible)

Stability Tolerance
A = ±25 ppm (0.0025%)
B = ±50 ppm (0.005%)
C = ±100 ppm (0.01%)

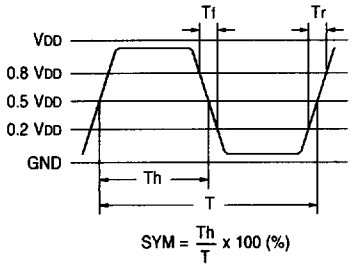
Logic
R = Reverse Logic Tri-State Address Option

Frequency

* Non-standard r/f times available on some models. Consult factory.

Example PN: STA090C - 100.0000

Output Waveform



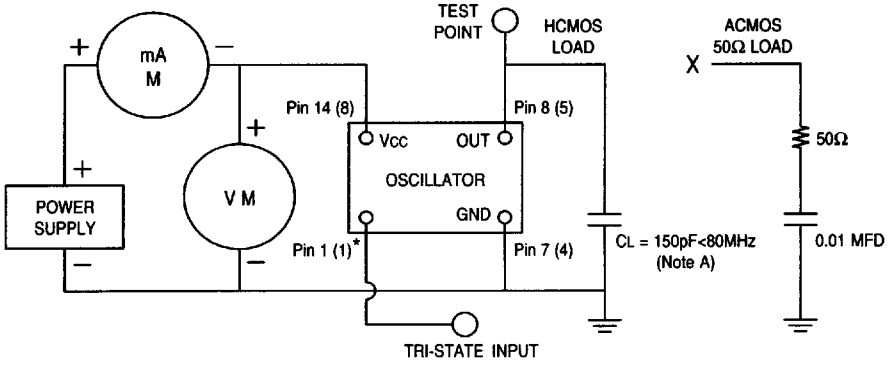
$SYM = \frac{Th}{T} \times 100\ (\%)$

Tri-State Logic Table

Pin 1 Input	Output Standard Logic	Output Reverse Logic
Logic "1" or NC	Oscillation	High Impedance
Logic "0" or GND	High Impedance	Oscillation

Required Input Levels on Pin 1:
Logic "1" = 2.0V min
Logic "0" = 0.8V max

Test Circuit



NOTE A: CL includes probe and fixture capacitance
*( ) Indicates pin numbers for half-size package

TEST CIRCUIT

49374 N

All specifications are subject to change without notice.

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