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DSP56651/D
Rev 0, 6/98

Advance Information

DSP56651

INTEGRATED CELLULAR BASEBAND PROCESSOR DEVELOPMENT IC

Motorola designed the RAM-based DSP56651 emulation device to support the rigorous demands of developing applications for the cellular subscriber market. The high level of on-chip integration in the DSP56651 and its volume production companion device DSP56652 minimizes application system design complexity and component count, resulting in very compact implementations. This integration also yields very low-power consumption and cost-effective system performance. The DSP56651 chip combines the power of Motorola's 32-bit M•CORE ™ MicroRISC Engine (MCU) and the DSP56600 digital signal processor (DSP) core with on-chip memory, protocol timer, and custom peripherals to provide a single-chip cellular base-band processor. **Figure 1** shows the basic block diagram of the DSP56651.

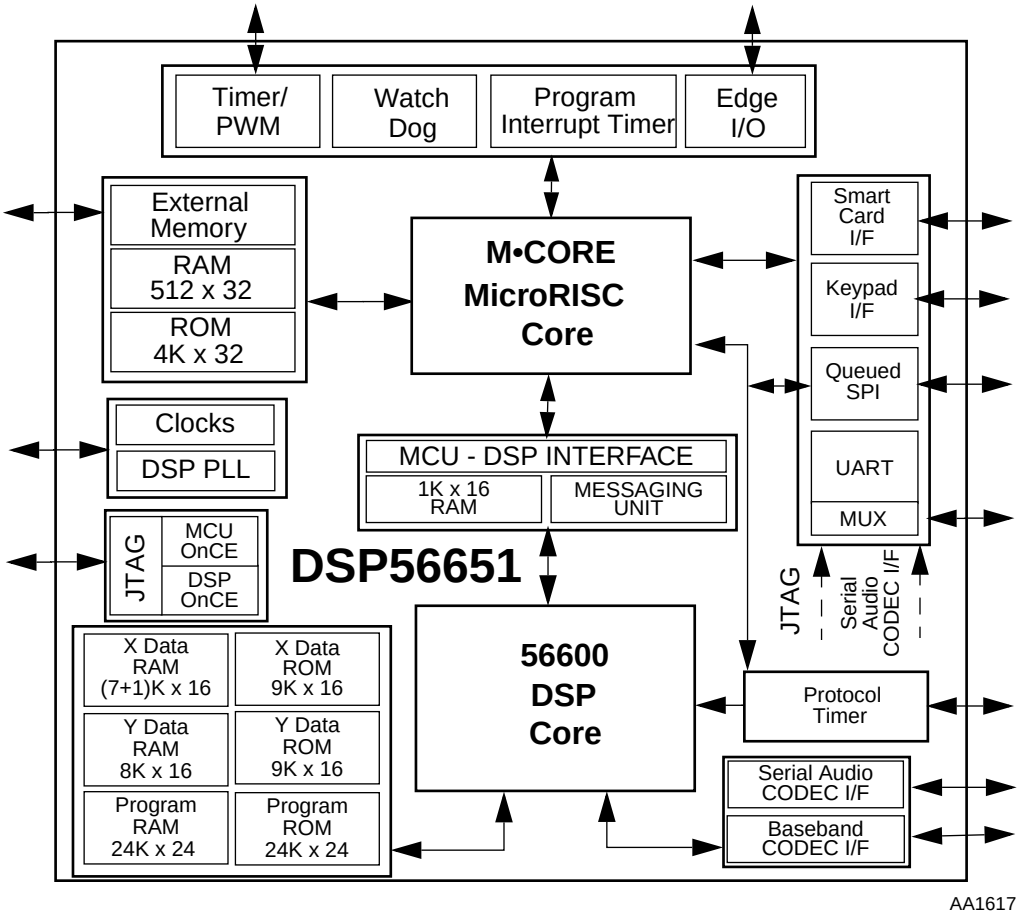

Figure 1-1 DSP56651 System Block Diagram

Development Part Only—Not intended for production.
Requires a higher voltage than the production part

Preliminary

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FOR TECHNICAL ASSISTANCE:

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Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low; for example, the $\overline{\text{RESET}}$ pin is active when low
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

RISC M•CORE MCU

- 32-bit load / store RISC architecture
- Fixed 16-bit instruction length
- 16-entry 32-bit general-purpose register file
- 32-bit internal address and data buses
- Efficient four-stage, fully interlocked execution pipeline
- Single-cycle execution for most instructions, two cycles for branches and memory accesses
- Special branch, byte, and bit manipulation instructions
- Support for byte, half-word, and word memory accesses
- Fast interrupt support via vectoring / auto-vectoring and a 16-entry dedicated alternate register file

High Performance DSP56600 Core

- 1 × engine (e.g., 70 MHz = 70 MIPS)
- Fully pipelined 16 × 16-bit parallel multiplier-accumulator (MAC)
- Two 40-bit accumulators including extension bits
- 40-bit parallel barrel shifter
- Highly parallel instruction set with unique DSP addressing modes
- Position-independent code support
- Nested hardware DO loops
- Fast auto-return interrupts
- On-chip support for software patching and enhancements
- Realtime trace capability via address bus visibility mode

On-chip Memories

- 4K × 32-bit MCU ROM
- 512 × 32-bit MCU RAM
- 24K × 24-bit DSP program ROM
- 24K × 24-bit DSP program RAM
- 18K × 16-bit DSP data ROM, split into 9K × 16-bit X and 9K x 16 Y data ROM spaces
- 16K × 16-bit DSP data RAM, split into (7+1)K × 16-bit X and 8K x 16-bit Y data RAM spaces

On-chip Peripherals

- Fully programmable phase-locked loop (PLL) for DSP clock generation
- External interface module (EIM) for glueless system integration
- External 22-bit address and 16-bit data MCU buses
- Thirty-two source MCU interrupt controller
- Intelligent MCU / DSP interface (MDI) dual 1K x 16-bit RAM (shares 1K DSP X data RAM) with messaging status and control
- Serial audio codec port
- Serial baseband codec port
- Protocol timer frees the MCU from radio channel timing events
- Queued serial peripheral interface (SPI)
- Keypad port capable of scanning up to an 8 × 8 matrix keypad
- General-purpose MCU and DSP timers
- Pulse width modulation output
- Universal asynchronous receiver / transmitter (UART) with FIFO
- IEEE 1149.1-compliant boundary scan JTAG test access port (TAP)
- Integrated DSP / M•CORE On-Chip Emulation (OnCE™) module
- DSP address bus visibility mode for system development
- ISO 7816-compatible Smart Card port

Operating Features:

- Comprehensive static and dynamic power management
- M•CORE operating frequency: dc to 16.8 MHz at 2.4 V
- DSP operating frequency: dc to 58.8 MHz at 2.4 V
- Operating temperature: –40˚ to 85˚C ambient
- Package option: 17 × 17 mm, 196-lead PBGA

TARGET APPLICATIONS

The DSP56651 is intended for the development of cellular subscriber applications and other applications needing both DSP and control processing.

PRODUCT DOCUMENTATION

The four manuals listed in **Table 1** are required for a complete description of the DSP56651 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

Table 1 DSP56651 Documentation

Document Name	Description of Contents	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family core processor architecture and instruction set	DSP56600FM/AD
M•CORE Reference Manual	Detailed description of the M•CORE MCU and instruction set	MCORERM/AD
DSP56652 User's Manual	Detailed description of DSP56652 memory, peripherals, and interfaces, much of which are common to the DSP56651	DSP56652UM/AD
DSP56651 Technical Data	DSP56651 pin and package descriptions; electrical and timing specifications	DSP56651/D

SECTION 1

PIN AND SIGNAL DESCRIPTIONS

INTRODUCTION

The pins and signals of the DSP56651 are described in the following sections. **Figure 1-1** and **Figure 1-2** on page 1-3 are top and bottom views of the package, respectively, showing the pin-outs. Subsequent tables list the pins by number and signal name. **Figure 1-3** on page 1-11 is a representational pin-out of the chip grouping the signals by their function. Subsequent tables identify the signals of each group.

DSP56651 PIN DESCRIPTION

The following section provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals of the DSP56651 are allocated for the 196-pin plastic ball grid array (PBGA) package. Top and bottom views of the PBGA package are shown in **Figure 1-1** and **Figure 1-2** on page 1-3 with their pin-outs.

PBGA Package Description

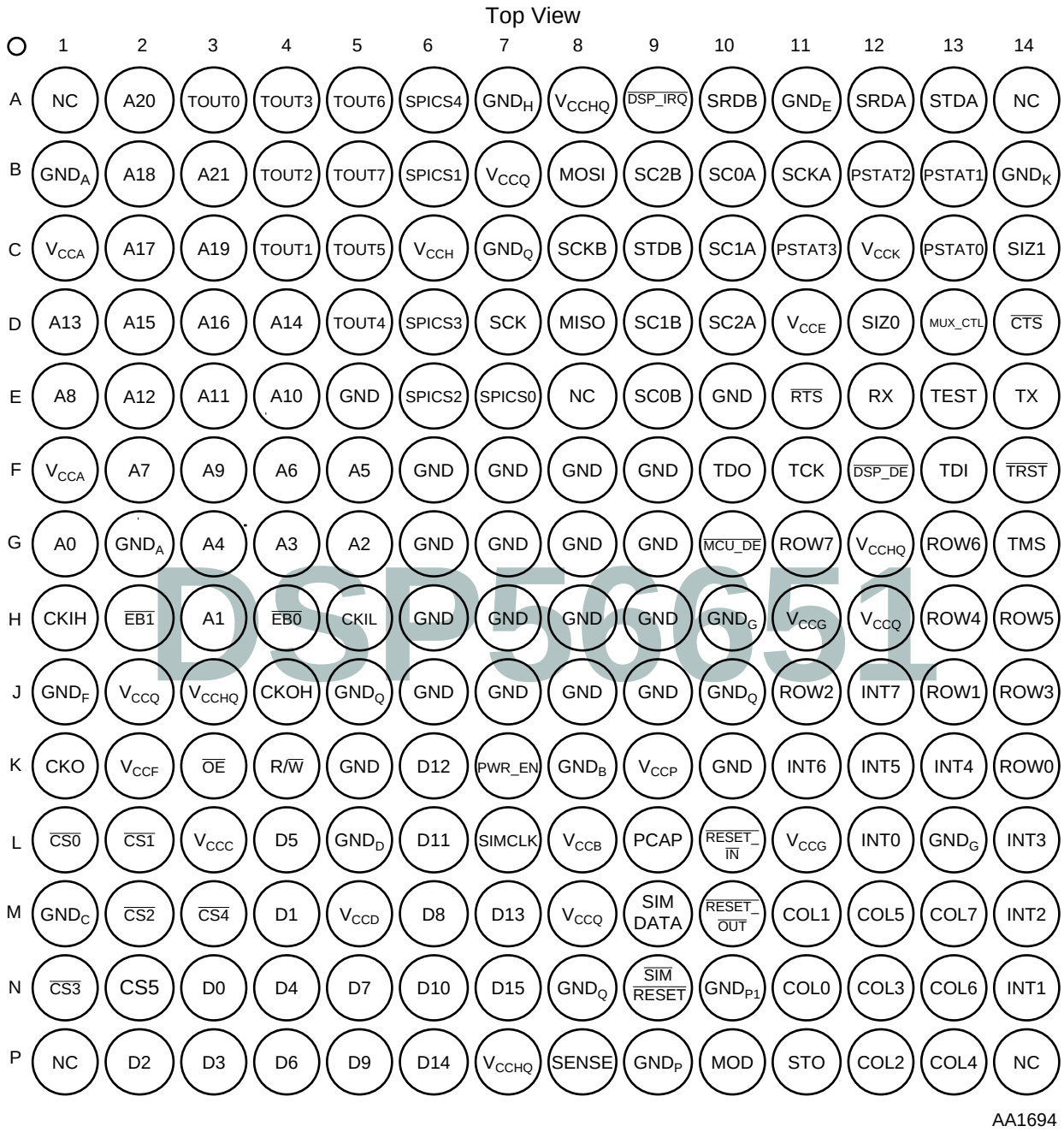


Figure 1-1 DSP56651 Plastic Ball Grid Array (PBGA), Top View

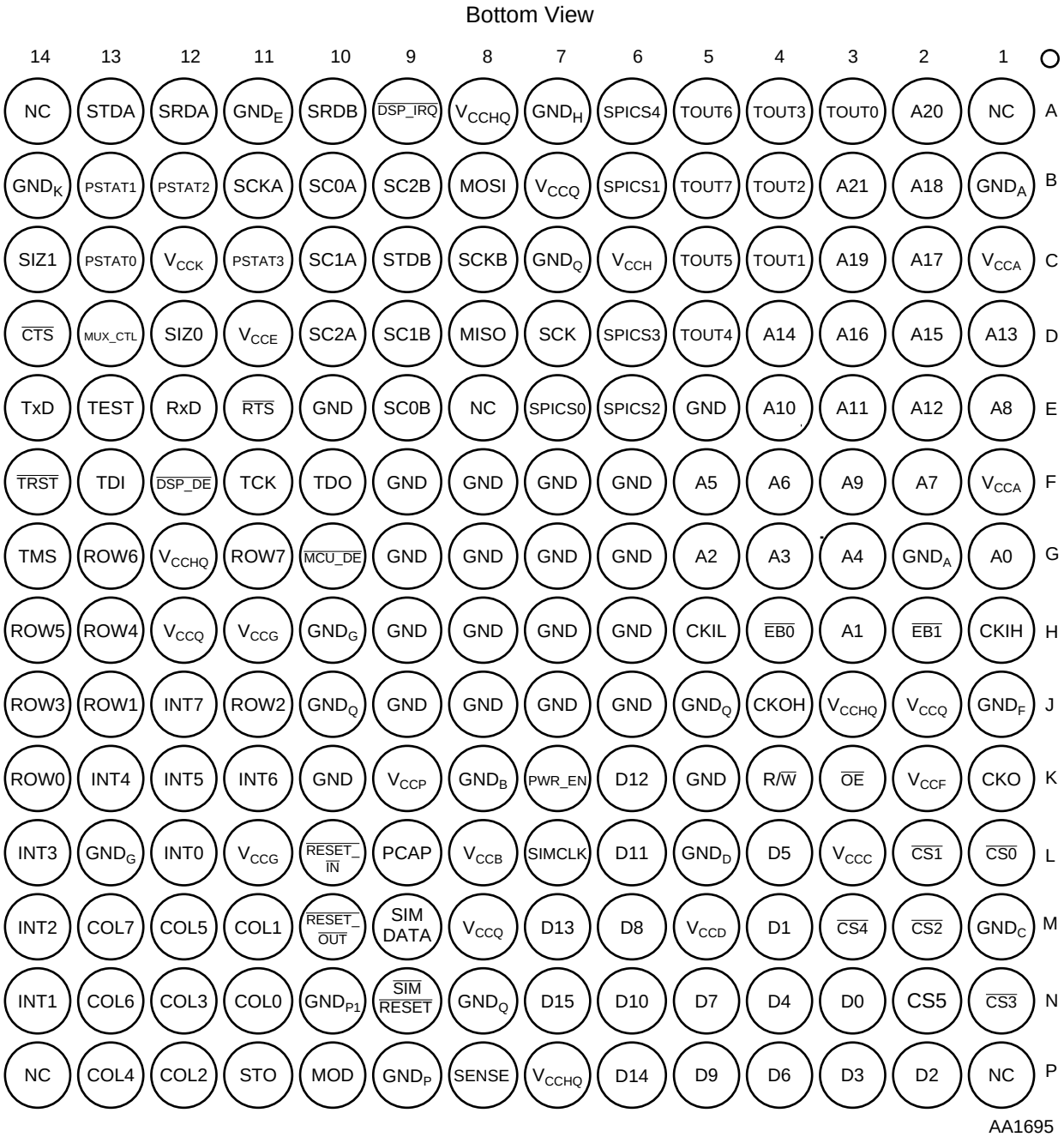


Figure 1-2 DSP56651 Plastic Ball Grid Array (PBGA), Bottom View

Table 1-1 DSP56651 PBGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	Not Connected (NC), reserved	B12	PSTAT2	D9	SC1B
A2	A20	B13	PSTAT1	D10	SC2A
A3	TOUT0	B14	GND_K	D11	V_{CCE}
A4	TOUT3	C1	V_{CCA}	D12	SIZ0
A5	TOUT6	C2	A17	D13	MUX_CTL
A6	SPICS4	C3	A19	D14	$\overline{CTS}$
A7	GND_H	C4	TOUT1	E1	A8
A8	V_{CCHQ}	C5	TOUT5	E2	A12
A9	$\overline{DSP\_IRQ}$	C6	V_{CCH}	E3	A11
A10	SRDB	C7	GND_Q	E4	A10
A11	GND_E	C8	SCKB	E5	GND
A12	SRDA	C9	STDB	E6	SPICS2
A13	STDA	C10	SC1A	E7	SPICS0
A14	NC	C11	PSTAT3	E8	NC
B1	GND_A	C12	V_{CCK}	E9	SC0B
B2	A18	C13	PSTAT0	E10	GND
B3	A21	C14	SIZ1	E11	$\overline{RTS}$
B4	TOUT2	D1	A13	E12	RxD
B5	TOUT7	D2	A15	E13	TEST
B6	SPICS1	D3	A16	E14	TxD
B7	V_{CCQ}	D4	A14	F1	V_{CCA}
B8	MOSI	D5	TOUT4	F2	A7
B9	SC2B	D6	SPICS3	F3	A9
B10	SC0A	D7	SCK	F4	A6
B11	SCKA	D8	MISO	F5	A5

Table 1-1 DSP56651 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
F6	GND	H3	A1	J14	ROW3
F7	GND	H4	$\overline{EB0}$	K1	CKO
F8	GND	H5	CKIL	K2	V_{CCF}
F9	GND	H6	GND	K3	$\overline{OE}$
F10	TDO	H7	GND	K4	R/$\overline{W}$
F11	TCK	H8	GND	K5	GND
F12	$\overline{DSP\_DE}$	H9	GND	K6	D12
F13	TDI	H10	GND_G	K7	PWR_EN
F14	$\overline{TRST}$	H11	V_{CCG}	K8	GND_B
G1	A0	H12	V_{CCQ}	K9	V_{CCP}
G2	GND_A	H13	ROW4	K10	GND
G3	A4	H14	ROW5	K11	INT6
G4	A3	J1	GND_F	K12	INT5
G5	A2	J2	V_{CCQ}	K13	INT4
G6	GND	J3	V_{CCHQ}	K14	ROW0
G7	GND	J4	CKOH	L1	$\overline{CS0}$
G8	GND	J5	GND_Q	L2	$\overline{CS1}$
G9	GND	J6	GND	L3	V_{CCC}
G10	$\overline{MCU\_DE}$	J7	GND	L4	D5
G11	ROW7	J8	GND	L5	GND_D
G12	V_{CCHQ}	J9	GND	L6	D11
G13	ROW6	J10	GND_Q	L7	SIMCLK
G14	TMS	J11	ROW2	L8	V_{CCB}
H1	CKIH	J12	INT7	L9	PCAP
H2	$\overline{EB1}$	J13	ROW1	L10	$\overline{RESET\_IN}$

Table 1-1 DSP56651 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
L11	V_{CCG}	M13	COL7	P1	NC
L12	INT0	M14	INT2	P2	D2
L13	GND_G	N1	$\overline{CS3}$	P3	D3
L14	INT3	N2	CS5	P4	D6
M1	GND_C	N3	D0	P5	D9
M2	$\overline{CS2}$	N4	D4	P6	D14
M3	$\overline{CS4}$	N5	D7	P7	V_{CCHQ}
M4	D1	N6	D10	P8	SENSE
M5	V_{CCD}	N7	D15	P9	GND_P
M6	D8	N8	GND_Q	P10	MOD
M7	D13	N9	$\overline{SIMRESET}$	P11	STO
M8	V_{CCQ}	N10	GND_{P1}	P12	COL2
M9	SIMDATA	N11	COL0	P13	COL4
M10	$\overline{RESET\_OUT}$	N12	COL3	P14	NC
M11	COL1	N13	COL6		
M12	COL5	N14	INT1		

Table 1-2 DSP56651 PBGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	G1	CKOH	J4	D9	P5
A1	H3	COL0	N11	D10	N6
A2	G5	COL1	M11	D11	L6
A3	G4	COL2	P12	D12	K6
A4	G3	COL3	N12	D13	M7
A5	F5	COL4	P13	D14	P6
A6	F4	COL5	M12	D15	N7
A7	F2	COL6	N13	$\overline{\text{DSP\_DE}}$	F12
A8	E1	COL7	M13	$\overline{\text{DSP\_IRQ}}$	A9
A9	F3	$\overline{\text{CS0}}$	L1	$\overline{\text{EB0}}$	H4
A10	E4	$\overline{\text{CS1}}$	L2	$\overline{\text{EB1}}$	H2
A11	E3	$\overline{\text{CS2}}$	M2	GND	E10
A12	E2	$\overline{\text{CS3}}$	N1	GND	E5
A13	D1	$\overline{\text{CS4}}$	M3	GND	F6
A14	D4	CS5	N2	GND	F7
A15	D2	$\overline{\text{CTS}}$	D14	GND	F8
A16	D3	D0	N3	GND	F9
A17	C2	D1	M4	GND	G6
A18	B2	D2	P2	GND	G7
A19	C3	D3	P3	GND	G8
A20	A2	D4	N4	GND	G9
A21	B3	D5	L4	GND	H6
CKIH	H1	D6	P4	GND	H7
CKIL	H5	D7	N5	GND	H8
CKO	K1	D8	M6	GND	H9

Table 1-2 DSP56651 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	J6	INT2	M14	$\overline{\text{RESET\_OUT}}$	M10
GND	J7	INT3	L14	ROW0	K14
GND	J8	INT4	K13	ROW1	J13
GND	J9	INT5	K12	ROW2	J11
GND	K10	INT6	K11	ROW3	J14
GND	K5	INT7	J12	ROW4	H13
GND_A	B1	$\overline{\text{MCU\_DE}}$	G10	ROW5	H14
GND_A	G2	MISO	D8	ROW6	G13
GND_B	K8	MOD	P10	ROW7	G11
GND_C	M1	MOSI	B8	$\overline{\text{RTS}}$	E11
GND_D	L5	MUX_CTL	D13	RxD	E12
GND_E	A11	NC	A1	SC0A	B10
GND_F	J1	NC	A14	SC0B	E9
GND_G	H10	NC	E8	SC1A	C10
GND_G	L13	NC	P1	SC1B	D9
GND_H	A7	NC	P14	SC2A	D10
GND_K	B14	$\overline{\text{OE}}$	K3	SC2B	B9
GND_P	P9	PCAP	L9	SCK	D7
GND_{P1}	N10	PSTAT0	C13	SCKA	B11
GND_Q	C7	PSTAT1	B13	SCKB	C8
GND_Q	J10	PSTAT2	B12	SENSE	P8
GND_Q	J5	PSTAT3	C11	SIMCLK	L7
GND_Q	N8	PWR_EN	K7	SIMDATA	M9
INT0	L12	R/$\overline{\text{W}}$	K4	$\overline{\text{SIMRESET}}$	N9
INT1	N14	$\overline{\text{RESET\_IN}}$	L10	SIZ0	D12

Table 1-2 DSP56651 PBGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
SIZ1	C14	TOUT0	A3	V_{CCF}	K2
SPICS0	E7	TOUT1	C4	V_{CCG}	H11
SPICS1	B6	TOUT2	B4	V_{CCG}	L11
SPICS2	E6	TOUT3	A4	V_{CCH}	C6
SPICS3	D6	TOUT4	D5	V_{CCHQ}	A8
SPICS4	A6	TOUT5	C5	V_{CCHQ}	G12
SRDA	A12	TOUT6	A5	V_{CCHQ}	J3
SRDB	A10	TOUT7	B5	V_{CCHQ}	P7
STDA	A13	$\overline{TRST}$	F14	V_{CCK}	C12
STDB	C9	TxD	E14	V_{CCP}	K9
STO	P11	V_{CCA}	C1	V_{CCQ}	B7
TCK	F11	V_{CCA}	F1	V_{CCQ}	J2
TDI	F13	V_{CCB}	L8	V_{CCQ}	H12
TDO	F10	V_{CCC}	L3	V_{CCQ}	M8
TEST	E13	V_{CCD}	M5		
TMS	G14	V_{CCE}	D11		

DSP56651 SIGNAL DESCRIPTION

DSP56651 signals are organized into nineteen functional groups as summarized in **Table 1-3**. **Figure 1-3** is a diagram of DSP56651 signals by functional group.

Table 1-3 Signal Functional Group Allocations

Functional Group		Number of Signals	Detailed Description
Power (V_{CCX})		20	**Table 1-4**
Ground (GND_X)		17	**Table 1-5**
Substrate ground (GND)		20	
PLL and clocks		5	**Table 1-6**
Address bus	External Interface Module (EIM)	22	**Table 1-7**
Data bus		16	**Table 1-8**
Bus control		4	**Table 1-9**
Chip selects		6	**Table 1-10**
Reset, mode, and multiplexer control		5	**Table 1-11**
External interrupts		9	**Table 1-12**
Timers		8	**Table 1-13**
Keypad port		16	**Table 1-14**
Serial data port (UART)		4	**Table 1-15**
Serial control port (QSPI)		8	**Table 1-16**
Smart Card port (SIM)		5	**Table 1-17**
Serial audio codec port (SAP)		6	**Table 1-18**
Baseband codec port		6	**Table 1-19**
Emulation port	Develop-ment and Test	6	**Table 1-20**
Debug control port		2	**Table 1-21**
JTAG test access port (TAP)		6	**Table 1-22**

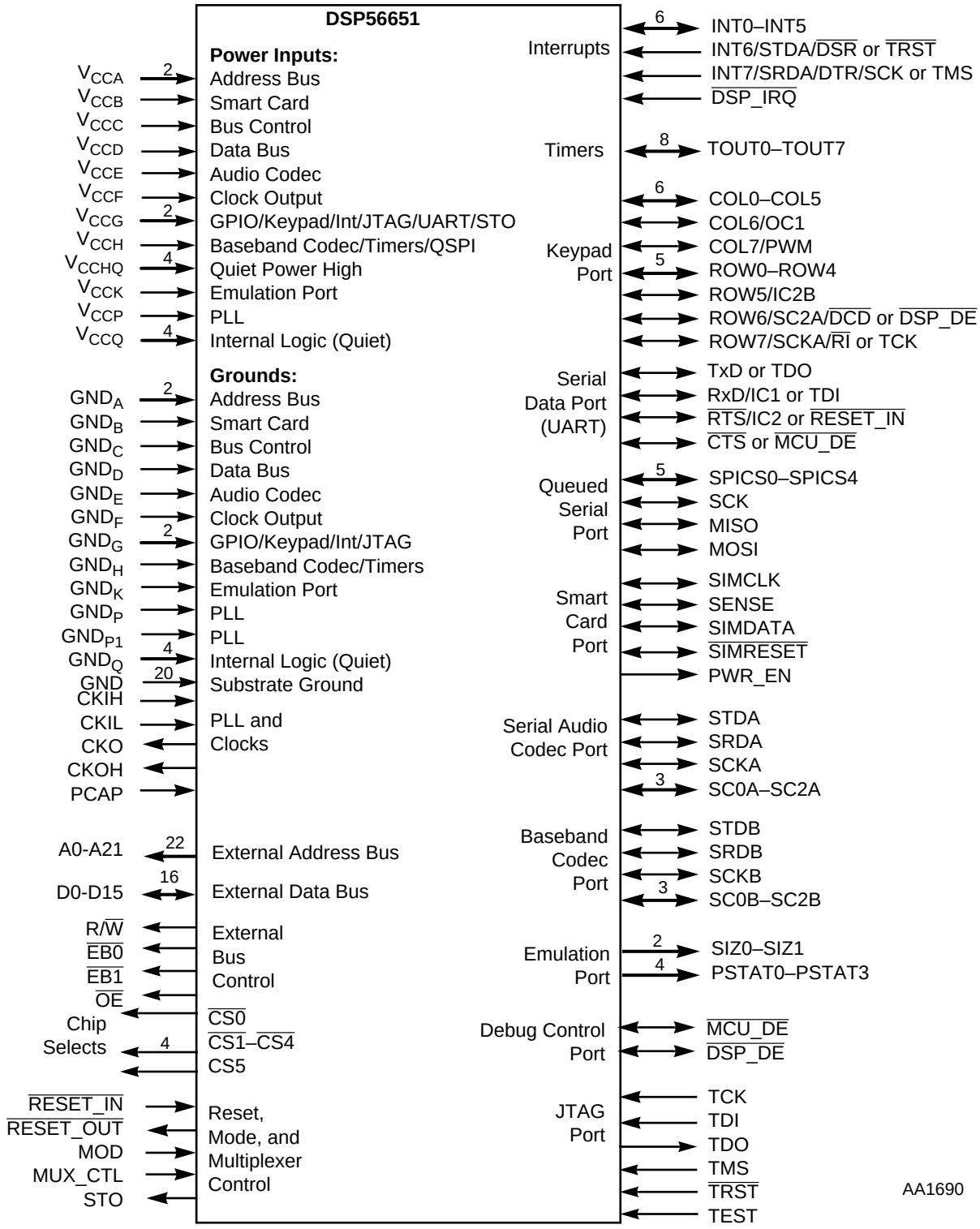


Figure 1-3 Signals Identified by Functional Group

Power

Table 1-4 Power

Power Names	Description
V_{CCA}	**Address Bus power**—These lines supply power to the address bus.
V_{CCB}	**Smart Card interface power**—This line supplies isolated power for Smart Card Interface I/O drivers.
V_{CCC}	**Bus control power**—This line supplies power to the bus control logic.
V_{CCD}	**Data bus power**—These lines supply power to the data bus.
V_{CCE}	**Audio codec port power**—This line supplies power to audio codec I/O drivers.
V_{CCF}	**Clock output power**—This line supplies a quiet power source for the CKOUT output. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{CCF} line and the GND_F line.
V_{CCG}	**GPIO power**—This line supplies power to the GPIO, keypad, data port, interrupts, STO, and JTAG I/O drivers.
V_{CCH}	**Baseband codec and timer power**—This line supplies power to the baseband codec, timer and QSPI I/O drivers.
V_{CCHQ}	**Quiet power high**—These lines supply a quiet power source to the pre-driver voltage converters. This value should be greater than or equal to the maximum value of the power supplies of the chip I/O drivers (i.e., the maximum of V_{CCA}, V_{CCB}, V_{CCC}, V_{CCD}, V_{CCE}, V_{CCF}, V_{CCG}, V_{CCH}, and V_{CCK}).
V_{CCK}	**Emulation port power**—This line supplies power to the emulation port I/O drivers.
V_{CCP}	**Analog PLL circuit power**—This line is dedicated to the analog PLL circuits and must remain noise-free to ensure stable PLL frequency and performance. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the V_{CCP} line and the GND_P and GND $_{P1}$ lines.
V_{CCQ}	**Quiet power**—These lines supply a quiet power source to the internal logic circuits. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{CCQ} lines and the GND_Q lines.

Ground

Table 1-5 Ground

Ground Names	Description
GND_A	**Address Bus ground**—These lines connect system ground to the address bus.
GND_B	**Smart Card interface ground**—These lines connect system ground to the Smart Card bus.
GND_C	**Bus control ground**—This line connects ground to the bus control logic.
GND_D	**Data bus ground**—These lines connect system ground to the data bus.
GND_E	**Audio codec port ground**—These lines connect system ground to the audio codec port.
GND_F	**Clock output ground**—This line supplies a quiet ground connection for the clock output drivers. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{CCF} line and the GND_F line.
GND_G	**GPIO ground**—These lines connect system ground to GPIO, keypad, data port, interrupts, STO, and JTAG I/O drivers.
GND_H	**Baseband codec and timer ground**—These lines connect system ground to the baseband codec, timer and QSPI I/O drivers.
GND_K	**Emulation port ground**—These lines connect system ground to the emulation port I/O drivers.
GND_P	**Analog PLL circuit ground**—This line supplies a dedicated quiet ground connection for the analog PLL circuits and must remain relatively noise-free to ensure stable PLL frequency and performance. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the V_{CCP} line and the GND_P line.
GND_{P1}	**Analog PLL circuit ground**—This line supplies a dedicated quiet ground connection for the analog PLL circuits and must remain relatively noise-free to ensure stable PLL frequency and performance. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the V_{CCP} line and the GND_P line.
GND_Q	**Quiet ground**—These lines supply a quiet ground connection for the internal logic circuits. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{CCQ} line and the GND_Q line.
GND	**Substrate ground**—These lines must be tied to ground.

PLL and Clock

Table 1-6 PLL and Clock Signals

Signal Name	Signal Type	State during Reset	Signal Description
CKIH	Input	Input	**High frequency clock input**—This signal provides the high frequency input clock. This clock may be other a CMOS square wave or sinusoid input.
CKIL	Input	Input	**Low frequency clock input**—This signal provides the low frequency input clock and should be less than or equal to the frequency of CKIH. This is the default input clock after reset.
CKO	Output	Driven low	**DSP/MCU output clock**—This signal provides an output clock synchronized to the DSP or MCU core internal clock phases, according the selected programming option. The choices of clock source and enabling / disabling the output signal are software selectable.
CKOH	Output	Driven low	**High frequency clock output**—This signal provides an output clock derived from the CKIH input. This signal can be enabled or disabled by software.
PCAP	Input / Output	Indeter-minate	**PLL capacitor**—This signal is used to connect the required external filter capacitor to the PLL filter. Connect one end of the capacitor to PCAP and the other to V_{CCP}. The value of the capacitor is specified in **Section 2** of this data sheet.

Address Bus

Table 1-7 Address Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
A0–A21	Output	Driven low	**Address bus—**These signals specify the address for external memory accesses. If there is no external bus activity, A0–A21 remain at their previous values to reduce power consumption.

Data Bus

Table 1-8 Data Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
D0–D15	Input/ Output	Input	**Data bus**—These signals provide the bidirectional data bus for external memory accesses. D0–D15 are held in the previous logic state when there is no external bus activity and during hardware reset. This is done with weak "keepers" inside the I/O buffers.

Bus Control

Table 1-9 Bus Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
R/$\overline{W}$	Output	Driven high	**Read/write—**This signal indicates the bus access type. A high signal indicates a bus read. A low signal indicates a write to the bus. When accessing memory it can also be used as write enable ($\overline{WE}$) signal. When accessing a peripheral chip, the signal acts as a read/write.
$\overline{EB0}$	Output	Driven high	**Enable byte 0**—When driven low, this signal indicates access to data byte 0 (D8–D15) during a read or write cycle. This pin may also act as a write byte enable, if so programmed. This output is used when accessing 16-bit wide SRAM.
$\overline{EB1}$	Output	Driven high	**Enable byte 1**—When driven low, this signal indicates access to data byte 1 (D0–D7) during a read or write cycle. This pin may also act as a write byte enable, if so programmed. This output is used when accessing 16-bit wide SRAM.
$\overline{OE}$	Output	Driven high	**Bus select—**When driven low, this signal indicates that the current bus access is a read cycle and enables slave devices to drive the data bus with a read.

Chip Selects

Table 1-10 Chip Select Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{CS0}$	Output	Chip-driven	**Chip select 0—**This signal is asserted low based on the decode of the internal address bus bits A[31:24] and is typically used as the external flash memory chip select. After reset, accesses using this CS have a default of 15 wait states.
$\overline{CS1}$–$\overline{CS4}$	Output	Driven high	**Chip select 1–chip select 4—**These signals are asserted low based on the decode of the internal address bus bits A[31:24] of the access address. When not selected as chip select signals, these signals become general purpose outputs (GPOs). After reset, these signals are GPOs that are driven high.
CS5	Output	Driven low	**Chip select 5—**This signal is asserted high based on the decode of the internal address bus bits A[31:24] of the access address. When not selected as a chip select signal, this signal becomes a GPO. After reset, this signal is a GPO that is driven low.

Reset, Mode, and Multiplexer Control

Table 1-11 Reset, Mode, and Multiplexer Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{RESET\_IN}}$	Input	Input	**Reset input**—This signal is an active low Schmitt trigger input that provides a reset signal to the internal circuitry. The input is valid if it is asserted for at least three CKIL clock cycles. This pin has a 47kΩ pull-up resistor. Note: If MUX_CTL is held high, the $\overline{\text{RTS}}$ signal of the serial data port (UART) becomes the $\overline{\text{RESET\_IN}}$ input line. (See **Table 1-15** on page 1-26.)
$\overline{\text{RESET\_OUT}}$	Output	Pulled low	**Reset output**—This signal is asserted low for at least seven CKIL clock cycles under one of the following conditions: • $\overline{\text{RESET\_IN}}$ is pulled low for at least three CKIL clock cycles • The alternate $\overline{\text{RESET\_IN}}$ signal is enabled by MUX_CTL and is pulled low for at least three CKIL clock cycles • The watchdog count expires This signal is asserted immediately after the qualifier detects a valid $\overline{\text{RESET\_IN}}$ signal, remains asserted during $\overline{\text{RESET\_IN}}$ assertion, and is stretched for at least seven more CKIL clock cycles after $\overline{\text{RESET\_IN}}$ is deasserted. Three CKIL clock cycles before $\overline{\text{RESET\_OUT}}$ is deasserted, the MCU boot mode is latched from the MOD signal.
MOD	Input	Input	**Mode select**—This signal selects the MCU boot mode during hardware reset. If MOD is driven low at least four CKIL clock cycles before $\overline{\text{RESET\_OUT}}$ is deasserted, then the internal MCU ROM ignores the first access and the M•CORE fetches the first word from the first location the external flash memory. If MOD is driven high four CKIL clock cycles before $\overline{\text{RESET\_OUT}}$ deassertion, then the internal MCU ROM is enabled and the M•CORE fetches the first word from the first location in the internal ROM.

Table 1-11 Reset, Mode, and Multiplexer Control Signals (Continued)

<table>
<tr><th>Signal Name</th><th>Signal Type</th><th>State during Reset</th><th>Signal Description</th></tr>
<tr><td>MUX_CTL</td><td>Input</td><td>Input</td><td>Multiplexer control—This input allows the designer to select an alternate set of pins to be used for RESET_IN, the debug control port signals, and the JTAG signals as defined below:
<table>
<tr><th colspan="2">Normal (MUX_CTL low)</th><th>Alternate (MUX_CTL high)</th></tr>
<tr><td rowspan="2">Interrupt signals (See Table 1-12)</td><td>INT6 / STDA / $\overline{\text{DSR}}$</td><td>$\overline{\text{TRST}}$</td></tr>
<tr><td>INT7 / SRDA / DTR / SCLK</td><td>TMS</td></tr>
<tr><td rowspan="2">Keypad signals (See Table 1-14 on page 1-22)</td><td>ROW6 / SC2A / $\overline{\text{DCD}}$</td><td>$\overline{\text{DSP\_DE}}$</td></tr>
<tr><td>ROW7 / SCKA / $\overline{\text{RI}}$</td><td>TCK</td></tr>
<tr><td rowspan="4">Serial Data Port (UART) signals (See Table 1-15 on page 1-26)</td><td>TxD</td><td>TDO</td></tr>
<tr><td>RxD / IC1</td><td>TDI</td></tr>
<tr><td>$\overline{\text{RTS}}$ / IC2A</td><td>$\overline{\text{RESET\_IN}}$</td></tr>
<tr><td>$\overline{\text{CTS}}$</td><td>$\overline{\text{MCU\_DE}}$</td></tr>
</table>
If MUX_CTL is driven low, the normal functions are selected. If MUX_CTL is driven high, the alternate functions are selection.

Note: The user is responsible to ensure that transition between normal and alternate functions are made smoothly. No provisions are made in the on-chip hardware to assure such a smooth switch. The external command converter uses to drive this signal must ensure that critical pins (such as the JTAG TMS and $\overline{\text{TRST}}$ signals and $\overline{\text{RESET\_IN}}$) are driven with inactive values during and after the switch.

The MUX_CTL signal has an internal 100 kΩ pull-down resistor.</td></tr>
<tr><td>STO</td><td>Output</td><td>Chip driven</td><td>Soft turn off—This is a general purpose output pin. Its logic state is not affected by reset.</td></tr>
</table>

For Reset, mode, and MUX control signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Interrupts

Table 1-12 Interrupt Signals

Signal Name	Signal Type	State during Reset	Signal Description
INT0–INT3	Input or Output	Input	**Interrupt 0–interrupt 3**—These signals can be programmed as interrupt inputs or GPIO signals. The signals have on-chip 100 kΩ pull-up resistors. As Schmitt trigger interrupt inputs the signals can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases. The signals are GPIOs when not programmed as interrupts. After reset, the default state for these signals is general purpose input (GPI).
INT4–INT5	Input or Output	Input	**Interrupt 4–interrupt 5**—These signals can be programmed as interrupt inputs or GPIO signals, and have 10-27kΩ pull-up resistors. As Schmitt trigger interrupt inputs, the signals can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases. The signals are GPIOs when not programmed as interrupts. After reset, the default state for these signals is GPI.

Table 1-12 Interrupt Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
Normal:	**MUX_CTL driven low**		
INT6	Input or Output	Input	**Interrupt 6**—When selected, this signal can be programmed as an interrupt input or a GPIO signal, and has a 47kΩ pull-up resistor. As a Schmitt trigger interrupt input, the signal can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases.
STDA	Output		**Audio codec serial transmit data** (alternate)—When programmed as STDA, this signal transmits data from the serial transmit shift register in the serial audio codec port. Note: When this signal is used as STDA, the primary STDA signal is disabled. (See **Table 1-18** on page 1-31.)
$\overline{\text{DSR}}$	Output		**Data set ready**—When programmed as GPIO output, this signal can be used as the $\overline{\text{DSR}}$ output for the serial data port. (See **Table 1-15** on page 1-26) The signal is a GPIO when not programmed as one of the above functions. After reset, the default state for this signal is GPI.
Alternate:	**MUX_CTL driven high**		
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—When selected, this signal acts as the $\overline{\text{TRST}}$ input for the JTAG TAP controller. The signal is a Schmitt trigger input that asynchronously initializes the JTAG test controller when asserted. Note: When this signal is enabled, the primary $\overline{\text{TRST}}$ signal is disconnected from the TAP controller. (See **Table 1-22**.)

Table 1-12 Interrupt Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
Normal:	**MUX_CTL driven low**		
INT7	Input or Output	Input	**Interrupt 7**—When selected, this signal can be programmed as an interrupt input or a GPIO signal, and has a 47kΩ pull-up resistor. As a Schmitt trigger interrupt input, the signal can be programmed to be level sensitive, positive edge-triggered, or negative edge-triggered. When edge-triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal; however, as signal fall time of the interrupt signal increases, the probability of generating multiple interrupts due to this noise also increases.
SRDA	Input		**Audio codec serial receive data** (alternate)—When programmed as SRDA, this signal receives data into the serial receive shift register in the serial audio codec port. Note: When this signal is used as SRDA, the primary SRDA signal is disabled. (See **Table 1-18** on page 1-31.)
$\overline{\text{DTR}}$	Input		**Data terminal ready**—When programmed as GPIO, this signal is used as the $\overline{\text{DTR}}$ positive and negative edge-triggered interrupt input for the serial data port. (See **Table 1-15** on page 1-26.)
SCLK	Input		**Serial clock**–When so programmed, this signal provides the input clock for the serial data port (UART). (See **Table 1-15** on page 1-26.) The signal is a GPIO when not programmed as one of the above functions. After reset, the default state for this signal is GPI.
Alternate:	**MUX_CTL driven high**		
TMS	Input	Input	**Test mode select**—When selected, this signal acts as the TMS input for the JTAG TAP controller. The signal is used to sequence that TAP controller state machine. The TMS is sampled on the rising edge of TCK. Note: When this signal is enabled, the primary TMS signal is disconnected from the TAP controller. (See **Table 1-22** on page 1-36.)

Table 1-12 Interrupt Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{DSP\_IRQ}}$	Input	Input	**DSP external interrupt request**—This active low Schmitt trigger input can be programmed as a level-sensitive or negative edge-triggered maskable interrupt request input during normal instruction processing. If the DSP is in the stop state and DSP_IRQ is asserted, the DSP exits the stop state. This signal has an on-chip 47 kΩ pull-up resistor.

For Interrupt signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Timers

Table 1-13 Timer Signals

Signal Name	Signal Type	State during Reset	Signal Description
TOUT0–TOUT7	Input or Output	Input	**Timer output 0–7—**These are timer output signals. After reset, the default state for these signals is GPI. Note: These signals are GPIOs when not used as timer outputs.

Keypad Port

Table 1-14 Keypad Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
COL0–COL5	Input or Output	Input	**Column strobe 0–5—**These signals function as keypad column strobes that can be programmed as regular or open-drain outputs. When not used as column strobe signals, these are GPIO signals. After reset, the default state is GPI.

Table 1-14 Keypad Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
COL6 OC1	Input or Output Output	Input	**Column strobe 6—**This signal functions as a keypad column strobe that can be programmed as a regular or open-drain output. **MCU timer 1 output compare** —When programmed as OC1, this is the MCU Timer 1 output compare signal. When not programmed as OC1 and not used as a column strobe signal, this is a GPIO signal. After reset, the default state is GPI
COL7 PWM	Input or Output Output	Input	**Column strobe 7—**This signal functions as a keypad column strobe that can be programmed as a regular or open-drain output. **Pulse width modulator output**—When so programmed, this is the pulse width modulator output. When not programmed as PWM and not used as a column strobe signal, this is a GPIO signal. After reset, the default state is GPI
ROW0–ROW4	Input or Output	Input	**Row sense 0–4—**These signals function as keypad row senses. When not used as Row Sense signals, these are GPIO signals. After reset, the default state is GPI. These signals have on-chip 22 kΩ pull-up resistors.
ROW5 IC2B	Input or Output Input	Input	**Row sense 5—**This signal functions as a keypad row sense. **MCU input compare 2 timer**—When so programmed, this signal can be the input capture for the MCU input compare 2 timer. When not programmed as IC2B and not used as a row sense signal, this is a GPIO signal. After reset, the default state is GPI.

Table 1-14 Keypad Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
Normal:	**MUX_CTL driven low**		
ROW6	Input or Output	Input	**Row sense 6—**This signal functions as a keypad row sense and is equipped with an on-chip 100kΩ pull-up resistor.
SC2A	Input or Output		**Audio codec serial control 2** (alternate)—When programmed as SC2A, this signal provides I/O frame synchronization for the serial audio codec port. In synchronous mode, the signal provides the frame sync for both the transmitter and receiver. In asynchronous mode, the signal provides the frame sync for the transmitter only. As SC2A, this pin has a 100kΩ pull-down resistor. Note: When this signal is used as SC2A, the primary SC2A signal is disabled. (See **Table 1-18** on page 1-31.)
$\overline{\text{DCD}}$	Output		**Data Carrier Detect**—When programmed as GPIO output, this signal can be used as the $\overline{\text{DSR}}$ output for the serial data port. (See **Table 1-15** on page 1-26.) After reset, the default state is GPI.
Alternate:	**MUX_CTL driven high**		
$\overline{\text{DSP\_DE}}$	Input	Input	**Digital signal processor debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknowledges that the DSP has entered the debug mode. When programmed as DSP_DE, this signal has an open-drain 100kΩ pull-up.
	Output		When the DSP enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{DSP\_DE}}$ as an output signal for three clock cycles. Note: When this signal is enabled, the primary $\overline{\text{DSP\_DE}}$ signal is disabled. (See **Table 1-21** on page 1-35.)

Table 1-14 Keypad Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
Normal:	**MUX_CTL driven low**		
ROW7	Input or Output	Input	**Row sense 7—**This signal functions as a keypad row sense.
SCKA	Input		**Audio codec serial clock** (alternate)—When programmed as SCKA, this signal provides the serial bit rate clock for the serial audio codec port. In synchronous mode, the signal provides the clock input or output for both the transmitter and receiver. In asynchronous mode, the signal provides the clock for the transmitter only. Note: When this signal is used as SCKA, the primary SCKA signal is disabled. (See **Table 1-18** on page 1-31.)
$\overline{RI}$	Output		**Ring indicator**—When programmed as GPIO output, this signal can be used as the $\overline{RI}$ output for the serial data port. (See **Table 1-15**.) After reset, the default state is GPI.
Alternate:	**MUX_CTL driven high**		
TCK	Input	Input	**Test clock**—When selected, this signal provides the TCK input for the JTAG TAP controller. The signal is used to synchronize the JTAG test logic. This signal is equipped with a 47kΩ pull-up resistor. Note: When this signal is enabled, the primary TCK signal is disconnected from the TAP controller. (See **Table 1-22** on page 1-36.)

For keypad port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Serial Data Port (UART)

Table 1-15 Serial Data Port (UART) Signals

Signal Name	Signal Type	State during Reset	Signal Description
Normal:	**MUX_CTL driven low**		
TxD	Input or Output	Input	**UART transmit—**This signal transmits data from the UART. The signal is a GPIO when not programmed as the TxD signal. After reset, the default state for this signal is GPI.
Alternate:	**MUX_CTL driven high**		
TDO	Output		**Test data output**—When selected, this signal provides the TDO serial output for test instructions and data from the JTAG TAP controller. TDO is a tri-state signal that is actively driven in the shift-IR and shift-DR controller states. Note: When this signal is enabled, the primary TDO signal is disconnected from the TAP controller. (See **Table 1-22** on page 1-36.)
Normal:	**MUX_CTL driven low**		
RxD	Input or Output	Input	**UART receive—**This signal receives data into the UART.
IC1	Input		**Input compare 1**—When so programmed, the signal connects to an input capture / output compare timer used for autobaud mode support. The signal is a GPIO when not programmed as one of the above functions. This signal has an on-chip 47 kΩ pull-up resistor. After reset, the default state for this signal is GPI.
Alternate:	**MUX_CTL driven high**		
TDI	Input	Input	**Test data in**—When selected, this signal provides the TDI serial input for test instructions and data for the JTAG TAP controller. TDI is sampled on the rising edge of TCK. Note: When this signal is enabled, the primary TDI signal is disconnected from the TAP controller. (See **Table 1-22** on page 1-36.)

Table 1-15 Serial Data Port (UART) Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
Normal:	**MUX_CTL driven low**		
$\overline{\text{RTS}}$	Input or Output	Input	**Request to send—**This signal functions as the UART $\overline{\text{RTS}}$ signal.
IC2A	Input		**Input compare 2 A**—When so programmed, this signal connects to an input capture timer channel. The signal is a GPIO when not programmed as one of the above functions. After reset, the default state for this signal is GPI.
Alternate:	**MUX_CTL driven high**		
$\overline{\text{RESET\_IN}}$	Input	Input	**Reset input**—This signal is an active low Schmitt trigger input that provides a reset signal to the internal circuitry. The input is valid if it is asserted for at least three CKIL clock cycles. Note: When this signal is enabled, the primary $\overline{\text{RESET\_IN}}$ signal is disabled. (See **Table 1-11** on page 1-17.)

Table 1-15 Serial Data Port (UART) Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
Normal:	**MUX_CTL driven low**		
$\overline{\text{CTS}}$	Input or Output	Input	**Clear to send—**This signal functions as the UART $\overline{\text{CTS}}$ signal, and is equipped with a 47kΩ pull-up. After reset, the default state for this signal is GPI. Note: The signal is a GPIO when not used as $\overline{\text{CTS}}$.
Alternate:	**MUX_CTL driven high**		
$\overline{\text{MCU\_DE}}$	Input Output	Input	**Microcontroller debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknowledges that the MCU has entered the debug mode. The signal is equipped with an open-drain 47kΩ pull-up resistor. When the MCU enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{MCU\_DE}}$ as an output signal for several clock cycles. Note: When this signal is enabled, the primary $\overline{\text{MCU\_DE}}$ signal is disabled. (See **Table 1-21**.)

Note: There are four additional signals that support UART operation, provided as follows:
- $\overline{\text{DSR}}$—data set ready. This is an alternate function for the INT6 signal. (See **Table 1-12** on page 1-19.)
- $\overline{\text{DTR}}$—data terminal ready. This is an alternate function for the INT7 signal. (See **Table 1-12** on page 1-19.)
- $\overline{\text{DCD}}$—data carrier detect. This is an alternate function for the ROW6 signal. (See **Table 1-14** on page 1-22.)
- $\overline{\text{RI}}$—ring indicator. This is an alternate function for the ROW7 signal. (See **Table 1-14** on page 1-22.)

For serial data port (UART) signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Serial Control Port

Table 1-16 Serial Control Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
SPICS0–SPICS3	Output Input or Output	Input	**Synchronous peripheral chip select 0–3**—The output signals provide chip select signals for the queued serial peripheral interface (QSPI). The signals are programmable as active high or active low. Each signal has an on-chip 100 kΩ pull-up resistor. These are GPIO signals when the chip select functions are not being used. After reset, the default state for each signal is GPI.
SPICS4	Output Input or Output	Input	**Synchronous peripheral chip select 4**—This output signal provides a chip select signal for the QSPI. This signal is programmable as active high or active low. This signal has an on-chip 100 kΩ pull-down resistor. This is a GPIO signal when the chip select function is not being used. After reset, the default state is GPI.
SCK	Output Input or Output	Input	**Serial clock** — This output signal provides the serial clock from the QSPI for the accessed peripherals. There is a programmable number of clock cycles delay between the assertion of the chip select signal and the first transmission of the serial clock. The polarity and phase of SCK are programmable. This is a GPIO signal when the SCK function is not being used. After reset, the default state is GPI.
MISO	Input Input or Output	Input	**Synchronous master in slave out**—This input signal provides serial data input to the QSPI. Input data can be sampled on the rising or falling edge of SCK and received in QSPI RAM MSB or LSB first. This is a GPIO signal when the function is not being used. After reset, the default state is GPI.
MOSI	Output Input or Output	Input	**Synchronous master out slave in**—This output signal provides serial data from the QSPI. Output data can be sampled on the rising or falling edge of SCK and transmitted MSB or LSB first. This is a GPIO signal when the function is not being used. After reset, the default state is GPI.

For serial control port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Smart Card Port

After rest, the default state of all Smart Card port pins is GPI. For Smart Card port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 1-17 Smart Card Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
SIMCLK	Output Input or Output	Input	**SIM clock—**This signal is an output clock from the Smart Card port to the Smart Card. This signal is a GPIO signal when the Smart Card Port is not being used.
SENSE	Input Input or Output	Input	**SIM sense—**This signal is a Schmitt trigger input that signals when a Smart Card is inserted or removed. This signal is a GPIO signal when the Smart Card port is not being used. The signal has an on-chip 100 kΩ pull-down resistor.
SIMDATA	Input/ Output Input or Output	Input	**SIM data—**This bidirectional signal is used to transmit data to and receive data from the Smart Card. In the output state, the signal is open-drain. This signal is a GPIO signal when the Smart Card port is not being used. The signal has an on-chip 47 kΩ pull-up resistor.
$\overline{\text{SIMRESET}}$	Output Input or Output	Input	**SIM reset—**This signal is an output reset signal from the Smart Card port to the Smart Card. The Smart Card port can activate the reset of an attached Smart Card by driving $\overline{\text{SIMRESET}}$ low. This signal is a GPIO signal when the Smart Card port is not being used.
PWR_EN	Output Input or Output	Input	**SIM power enable—**This active high output enables the external device that supplies V_{CC} to the Smart Card. If this pin is driven high, the external device supplies power to the Smart Card. Driving the signal low cuts off power to card. This permits effective power management and power sequencing for Smart Card enable/disable. This signal is a GPIO signal when the Smart Card port is not being used. This signal has an on-chip 100 kΩ pull-down resistor.

Serial Audio Codec Port

After reset, the default state of all serial audio codec pins is Hi-Z. For serial audio codec port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 1-18 Serial Audio Codec Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
STDA	Input or Output	Input	**Audio codec transmit data**— This output signal transmits serial data from the audio codec serial transmitter shift register. It is equipped with a 100kΩ pull-up resistor. This is a GPIO signal when STDA is not being used. Note: This signal is disabled if the alternate STDA function on INT6 is selected. (See **Table 1-12** on page 1-19.)
SRDA	Input or Output	Input	**Audio codec receive data** — This input signal receives serial data and transfers the data to the audio codec receive shift register. It is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SRDA is not being used. Note: This signal is disabled if the alternate SRDA function on INT7 is selected. (See **Table 1-12** on page 1-19.)
SCKA	Input or Output	Input	**Audio codec serial clock** — This bidirectional signal provides the serial bit rate clock when only one clock is being used or the TxD clock otherwise. It is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when the serial audio codec port is not being used. Note: This signal is disabled if the alternate SCKA function on ROW7 is selected. (See **Table 1-14** on page 1-22.)
SC0A	Input or Output	Input	**Audio codec serial clock 0—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receive clock I/O This is a GPIO signal when SC0A is not being used.
SC1A	Input or Output	Input	**Audio codec serial clock 1—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receiver frame sync I/O This is a GPIO signal when SC1A is not being used.

Table 1-18 Serial Audio Codec Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SC2A	Input or Output	Input	**Audio codec serial clock 2—**This signal's function is determined by the SCLK mode. • Synchronous mode—transmitter and receiver frame sync I/O • Asynchronous mode—transmitter frame sync I/O It is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SC2A is not being used. Note: This signal is disabled if the alternate SC2A function on ROW6 is selected. (See **Table 1-14** on page 1-22.)

Baseband Codec Port

After reset, the default state of the baseband codec port pins is Hi-Z. For baseband codec port signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 1-19 Baseband Codec Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
STDB	Output Input or Output	Input	**Baseband codec transmit data**— This output signal transmits serial data from the baseband codec serial transmitter shift register. This signal is equipped with a 100 pull-up resistor. This is a GPIO signal when STDB is not being used.
SRDB	Input Input or Output	Input	**Baseband codec receive data** — This input signal receives serial data and transfers the data to the baseband codec receive shift register. This signal is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SRDB is not being used.
SCKB	Input or Output	Input	**Baseband codec serial clock** — This bidirectional signal provides the serial bit rate clock when only one clock is being used or the TxD clock otherwise. This signal is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when the serial baseband codec port is not being used.

Table 1-19 Baseband Codec Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SC0B	Input or Output	Input	**Baseband codec serial clock 0—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receive clock I/O This signal is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SC0B is not being used.
SC1B	Input or Output	Input	**Baseband codec serial clock 1—**This signal's function is determined by the SCLK mode. • Synchronous mode—serial I/O flag 0 • Asynchronous mode—receiver frame sync I/O This signal is equipped with a 100KkΩ pull-down resistor. This is a GPIO signal when SC1B is not being used.
SC2B	Input or Output	Input	**Baseband codec serial clock 2—**This signal's function is determined by the SCLK mode. • Synchronous mode—transmitter and receiver frame sync I/O • Asynchronous mode—transmitter frame sync I/O This signal is equipped with a 100kΩ pull-down resistor. This is a GPIO signal when SC2B is not being used.

Emulation Port

After reset, the default state for the emulation port pins is GPI.

Table 1-20 Emulation Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
SIZ0–SIZ1	Input or Output	Input	**Data size 0–1—**These signals encode the data size for the current MCU access. When not programmed as data size signals, these are GPIO signals. The signals have on-chip 100 kΩ pull-up resistors.
PSTAT0–PSTAT3	Input or Output	Input	**Pipeline state 0–3—**These signals encode the internal MCU execution unit status. When not programmed as pipeline state signals, these are GPIO signals. The signals have on-chip 100 kΩ pull-up resistors.

Debug Port Control

If the MUX_CTL signal is driven high, the alternate $\overline{\text{MCU\_DE}}$ and $\overline{\text{DSP\_DE}}$ signal locations are selected, and this interface is disabled. For debug port control signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output

Table 1-21 Debug Port Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{MCU\_DE}}$	Input	Input	**Microcontroller debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknowledges that the MCU has entered the debug mode. This signal is equipped with an open-drain 47kΩ pull-up resistor.
	Output		When the MCU enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{MCU\_DE}}$ as an output signal for three clock cycles.
$\overline{\text{DSP\_DE}}$	Input	Input	**Digital signal processor debug event**—As an input signal, this signal provides a means to enter the debug mode of operation from an external command converter. An an output signal, it acknowledges that the DSP has entered the debug mode.This signal is equipped with an open-drain 4kΩ K pull-up resistor.
	Output		When the DSP enters the debug mode due to a debug request or as the result of meeting a breakpoint condition, it asserts $\overline{\text{DSP\_DE}}$ as an output signal for three clock cycles.

JTAG Port

When the bottom connector pins are selected as a debug port by holding the MUX_CTL pin at a logic high, the dedicated JTAG pins become inactive. That is, they are disconnected from the JTAG TAP controller. For JTAG signals equipped with resistors, all pull-ups and pull-downs are automatically disconnected when the pin is an output.

Table 1-22 JTAG Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
TMS	Input	Input	**Test mode select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: INT7 is connected to the JTAG TAP controller and functions as TMS, see **Table 1-12** on page 1-19.)
TDI	Input	Input	**Test data input**—TDI is a serial test data input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: RxD is connected to the JTAG TAP controller and functions as TDI, see **Table 1-15** on page 1-26.)
TDO	Output	Tri-stated	**Test data output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK. **MUX_CTL high**: TxD is connected to the JTAG TAP controller and functions as TDO, see **Table 1-15** on page 1-26.)
TCK	Input	Input	**Test clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: ROW7 is connected to the JTAG TAP controller and functions as TCK, see **Table 1-14** on page 1-22.)
$\overline{\text{TRST}}$	Input	Input	**Test reset**—$\overline{\text{TRST}}$ is an active-low Schmitt-trigger input signal used to asynchronously initialize the test controller. $\overline{\text{TRST}}$ has an internal 47 kΩ pull-up resistor. **MUX_CTL high**: INT6 is connected to the JTAG TAP controller and functions as $\overline{\text{TRST}}$, see **Table 1-12** on page 1-19.)
TEST	Input	Input	**Factory test mode**—Selects factory test mode. Reserved. This pin MUST be connected to ground.

SECTION 2

SPECIFICATIONS

GENERAL CHARACTERISTICS

The DSP56651 is fabricated in high-density CMOS. The DSP56651 specifications are preliminary from design simulations and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Absolute Maximum Ratings (GND = 0 V)

Rating	Symbol	Value	Unit
Internal supply voltage	V_{CCI}	–0.3 to +2.75	V
External supply voltage	V_{CCE}	–0.3 to +3.6	V
Operating temperature range	T_A	–40 to +85	°C
Storage temperature	T_{STG}	–55 to +125	°C

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	BGA Value[3]	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	TBD	°C / W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	TBD	°C / W
Thermal characterization parameter	Ψ_{JT}	TBD	°C / W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal-single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111)
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are measured values; testing is not complete. Values were measured on a non-standard four-layer thermal test board (two internal planes) at one watt in a horizontal configuration.

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
Internal supply voltage	V_{CCI}	2.3	—	2.5	V
External supply voltage	V_{CCE}	V_{CCI}	—	3.4	V
I/O predriver supply voltage	V_{CCHQ}	V_{CCE}	—	3.4	V
Input high voltage	V_{IH}	$0.7 \times V_{CCE}$	—	$V_{CCE} + 0.2$	V
Input low voltage	V_{IL}	–0.3	—	$0.2 \times V_{CCE}$	V
Input leakage current	I_{IN}	–10	—	10	µA
Output high voltage (I_{OH} = –400 µA)	V_{OH}	$0.75 \times V_{CCE}$	—	V_{CCE}	V
Output low voltage (I_{OL} = 800 µA)	V_{OL}	0	—	$0.18 \times V_{CCE}$	V
Total stop mode (DSP and MCU stopped, PLL powered down, timers disabled)	I_{CC_STOP}	—	60	—	µA
DSP run current at 58.8 MHz (MCU stopped, timers disabled, DSP running algorithm from internal memory, BBP and SAP active)	I_{CCDSP_RUN}	—	35	—	mA
PLL supply current (16.8 MHz input, DSP freq = 58.8 MHz, MCU clock = 16.8 MHz)	I_{CC_PLL}	—	1.6	—	mA
DSP wait current at 58.8 MHz (MCU stopped, timers disabled, BBP and SAP active)	$I_{CC\_DSP\_WAIT}$	—	4.5	—	mA
MCU run current at 16.8 MHz (DSP and DSP PLL stopped, timers disabled, MCU peripherals active)	$I_{CC\_MCU\_RUN}$	—	9	—	mA
MCU doze current at 16.8 MHz (DSP and DSP PLL stopped, timers disabled, MCU peripherals active)	$I_{CC\_MCU\_DOZE}$	—	3	—	mA
MCU wait current at 16.8 MHz (DSP and DSP PLL stopped, timers disabled, MCU peripherals active)	$I_{CC\_MCU\_WAIT}$	—	3	—	mA
Timer current (MCU and DSP stopped; 16.8 MHz to timer)	I_{CC_TIMER}	—	500	—	µA
Input capacitance per pin	C_{IN}	—	—	TBD	pF
Pull-up resistor value[1]	—	50%	100%	180%	—

Note: 1. Applies to 22 K and 47 K resistors.

CLOCK REQUIREMENTS

Table 2-4 Clock Requirements

Characteristics	Symbol	Min	Typ	Max	Units
CKIH input frequency	f_1	0	—	16.8	MHz
CKIL input frequency	f_2	0	32.768	f_1	kHz
MCU internal frequency	$f_{MCU-CLK}$	0	—	16.8	MHz
DSP internal frequency	$f_{DSP-CLK}$	—	—	58.8	MHz
CKIH input amplitude	V_{I-CKIH}	500	—	—	mV_{PP}
CKIL input low voltage	$V_{IL-CKIL}$	-0.3	—	$0.2xV_{CCE}$	V
CKIL input high voltage	$V_{IH-CKIL}$	V_{CCI}	—	2.77	V
CKIH input impedance	R_{I-CKIH}	High TBD	—	—	MΩ

EXTERNAL BUS INTERFACE REQUIREMENTS

When the MCU is operating at 16.8 MHz, the bus interface can access 100 ns access time external memory with one wait state or 15 ns access time external memory with no wait states.

AC ELECTRICAL CHARACTERISTICS

The characteristics listed in this section are given for V_{DDI} = 2.4 V and V_{DDE} = 3.3 V with a capacitive load of 50 pF.

INTERNAL CLOCKS

For each occurrence of T_{DH}, T_{DL}, T_{DC}, or I_{DCYC}, substitute with the numbers in **Table 2-6**. DF, MF, and PDF are the DSP PLL division, multiplication, and pre-division factors set in registers.

Table 2-5 DSP Clocks

Characteristics	Symbol	Min	Max	Unit
DSP PLL input frequency	EfD	0	16.8	MHz
DSP PLL input clock cycle time • with PLL disabled • with PLL enabled	ET_{DC}	 59.5 59.5	 ∞ 273100	 ns ns

Table 2-6 Internal DSP Clocks

Characteristics	Symbol	Expression
Internal DSP operation frequency with PLL enabled	fD	(EfD × MF) / (PDF × DF)
Internal DSP operation frequency with PLL disabled	fD	EfD / 2
Internal DSP clock high period • with PLL disabled • with PLL enabled and MF ≤ 4 • with PLL enabled and MF > 4	T_{DH}	 ET_{DC} (Min) $0.49 \times ET_{DC} \times PDF \times DF / MF$ (Max) $0.51 \times ET_{DC} \times PDF \times DF / MF$ (Min) $0.47 \times ET_{DC} \times PDF \times DF / MF$ (Max) $0.53 \times ET_{DC} \times PDF \times DF / MF$
Internal clock low period • with PLL disabled • with PLL enabled and MF ≤ 4 • with PLL enabled and MF > 4	T_{DL}	 ET_{DC} (Min) $0.49 \times ET_{DC} \times PDF \times DF / MF$ (Max) $0.51 \times ET_{DC} \times PDF \times DF / MF$ (Min) $0.47 \times ET_{DC} \times PDF \times DF / MF$ (Max) $0.53 \times ET_{DC} \times PDF \times DF / MF$
Internal clock cycle time with PLL enabled	T_{DC}	$ET_{DC} \times PDF \times DF / MF$
Internal clock cycle time with PLL disabled	T_{DC}	$2 \times ET_{DC}$
DSP instruction cycle time	I_{DCYC}	T_{DC}

Table 2-7 MCU Clocks

Characteristics	Symbol	Min	Max	Unit
Frequency of the internal MCU-CLK clock	fM	0	16.8	MHz
Internal MCU-CLK clock cycle time	T_{MC}	59.5	∞	ns

PHASE-LOCKED LOOP (PLL) CHARACTERISTICS

Table 2-8 Phase-Locked Loop (PLL) Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled[1]	MF × EfD × 2 / PDF	30	120	MHz
PLL external capacitor (PCAP pin to V_{CCP}) • MF ≤ 4 • MF > 4	C_{PCAP} [2]	(680 • MF-120) recommended (580 • MF-100) minimum (780 • MF-140) maximum (1100 • MF) recommended (830 • MF) minimum (1470 • MF) maximum		pF

Notes: 1. The VCO output is further divided by 2 when PLL is enabled. If the division factor (DF) is 1, the operating frequency is $\frac{VCO}{2}$.

2. C_{PCAP} is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}). (The recommended value for Cpcap is (680 × MF – 120) pF for MF ≤ 4 and (1100 × MF) pF for MF > 4.)

RESET, MODE SELECT, AND INTERRUPT TIMING

Table 2-9 Reset, Mode Select, and Interrupt Timing

Num	Characteristics	Expression	MCU @16.8 MHz DSP @58.8 MHz		Unit
			Min	Max	
1	$\overline{\text{RESET\_IN}}$ duration to guarantee reset	$3 \times T_{CKIL} + 0.05$	91.6	—	µs
2	Delay from $\overline{\text{RESET\_IN}}$ assertion to $\overline{\text{RESET\_OUT}}$ assertion	min: $4.5 \times T_{CKIL}$ max: $5.5 \times T_{CKIL}$	137.33	167.85	µs
3	Duration of $\overline{\text{RESET\_OUT}}$ assertion	$7 \times T_{CKIL}$	213.62	—	µs
4	Delay from $\overline{\text{RESET\_IN}}$ assertion to all pins at Reset Value (periodically sampled and not 100% tested)	min: $4.5 \times T_{CKIL}$ max: $5.5 \times T_{CKIL}$	137.33	167.85	µs µs
5	MOD select setup time	$3.5 \times T_{CKIL} + 0.02$	107	—	µs
6	MOD select hold time	—	0	—	ns
7	Minimum edge-triggered $\overline{\text{DSP\_IRQ}}$ assertion width	—	10	—	ns
8	Minimum edge-triggered $\overline{\text{DSP\_IRQ}}$ deassertion width	—	10	—	ns

Table 2-9 Reset, Mode Select, and Interrupt Timing (Continued)

Num	Characteristics	Expression	MCU @16.8 MHz DSP @58.8 MHz		Unit
			Min	Max	
9	Minimum edge-triggered INTn width high	—	TBD	—	ns
10	Minimum edge-triggered INTn width low	—	TBD	—	ns

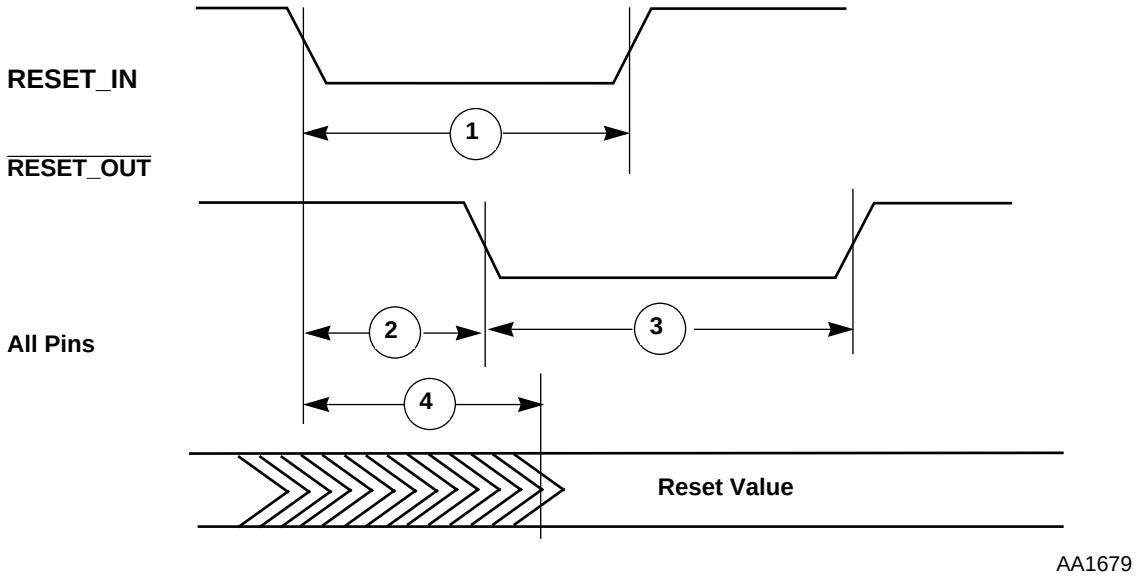


Figure 2-1 Reset Timing

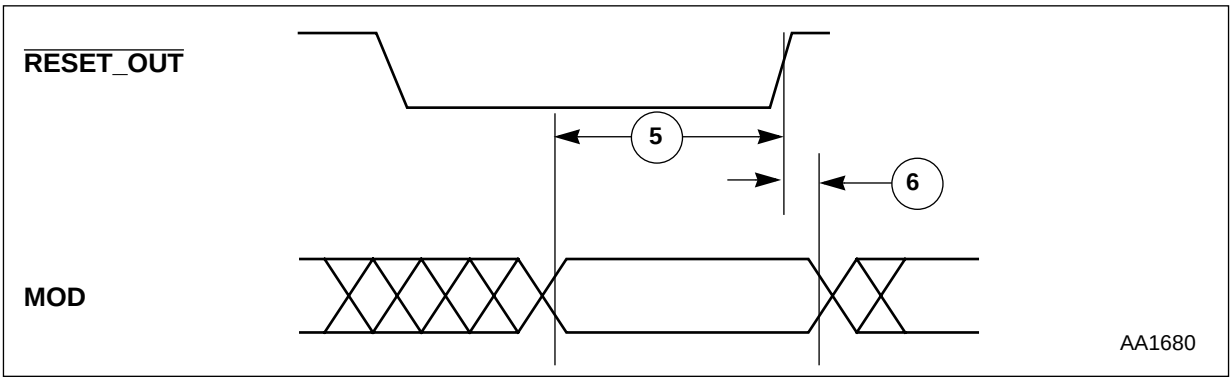


Figure 2-2 Operating Mode Select Timing

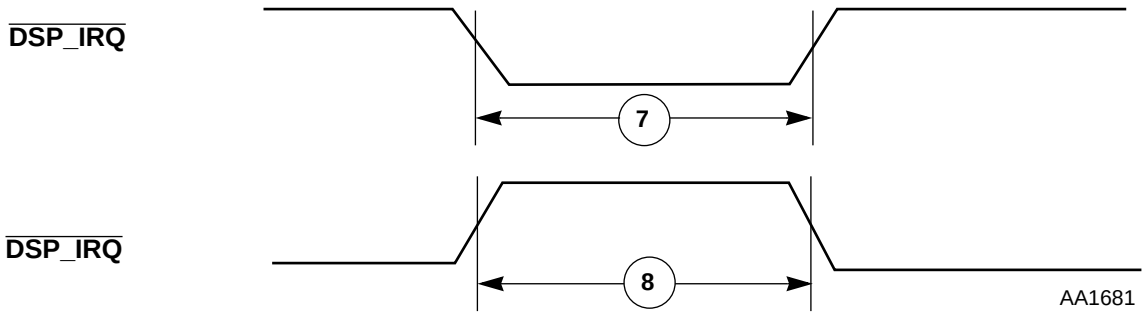


Figure 2-3 DSP External Interrupt Timing (Negative Edge-Triggered)

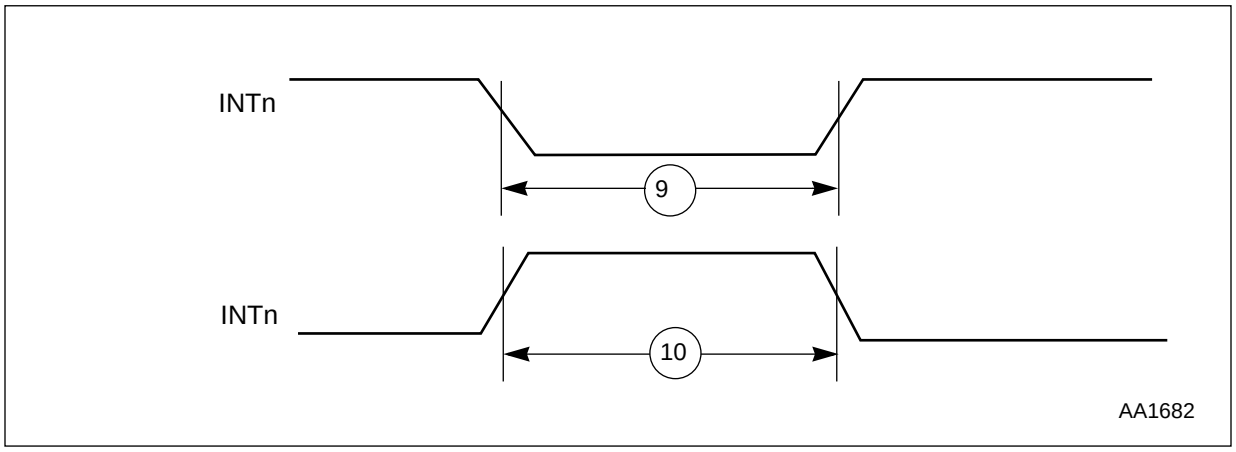


Figure 2-4 INT0-INT7 External Interrupt Timing

EXTERNAL INTERFACE MODULE (EIM) TIMING

The EIM provides the bus interface between the DSP56651 and external memory and peripherals. It uses the external address bus, data bus, bus control signals, and the chip select signals.

Table 2-10 EIM External Bus Output AC Timing Specifications[1]

Num	Characteristics	MCU @16.8 MHz		Unit
		Min	Max	
11	MCU_CLK rise to address and R/$\overline{W}$ valid[2]	—	4	ns
12	MCU_CLK rise to address and R/$\overline{W}$ invalid (output hold)	0	—	ns
13	MCU_CLK rise to CS asserted	—	4	ns
14	MCU_CLK rise to CS deasserted (output hold)	0	—	ns
15	MCU_CLK fall to $\overline{OE}$, $\overline{EB}$ asserted (read, OEA = 0), $\overline{EB}$ asserted (write)[3]	—	4	ns
16	MCU_CLK rise to $\overline{OE}$, $\overline{EB}$ asserted (read, OEA = 1)[3]	—	4	ns
17	MCU_CLK rise to $\overline{OE}$, $\overline{EB}$ deasserted (output hold) (read)[3]	0	—	ns
	MCU_CLK rise to $\overline{EB}$ deasserted (output hold) (write, WEN = 0)	0	—	ns
18	MCU_CLK fall to $\overline{EB}$ deasserted (output hold) (write, WEN = 1)	0	—	ns
19	MCU_CLK fall to $\overline{OE}$, $\overline{EB}$ asserted (WSC = 0)[3]	—	4	ns
20	MCU_CLK rise to $\overline{OE}$, $\overline{EB}$ deasserted (output hold) (WSC = 0)[3]	0	—	ns
21	Data-in valid to MCU_CLK rise (setup)	15	—	ns
22	MCU_CLK rise to data-in invalid (hold)	0	—	ns
23	MCU_CLK rise to data-out valid	—	4	ns
24	MCU_CLK rise to data-out invalid (output hold)	0	—	ns
25	MCU_CLK rise to data-out high impedance	—	4	ns
26	MCU_CLK fall to data-out valid (WSC = 0)	—	6	ns
27	MCU_CLK rise to data-out invalid (output hold) (WSC = 0)	0	—	ns
28	MCU_CLK rise to data-out high impedance (WSC = 0)	—	6	ns

Note: 1. The following notes apply to this table:
- Output timing is measured at the pin. The specifications assume a capacitive load of 50 pF.
- R/$\overline{W}$, $\overline{EB}$, and CS deassertion to address change is 0 ns minimum.
- MCU_CLK can be viewed on the CKO pin by programming the clock control register (CKCTL).

2. Address setup to R/$\overline{W}$ and CS assertion is 0 ns minimum.
3. $\overline{EB}$ outputs are asserted for reads if the EBC bit in the corresponding CS control register is clear.

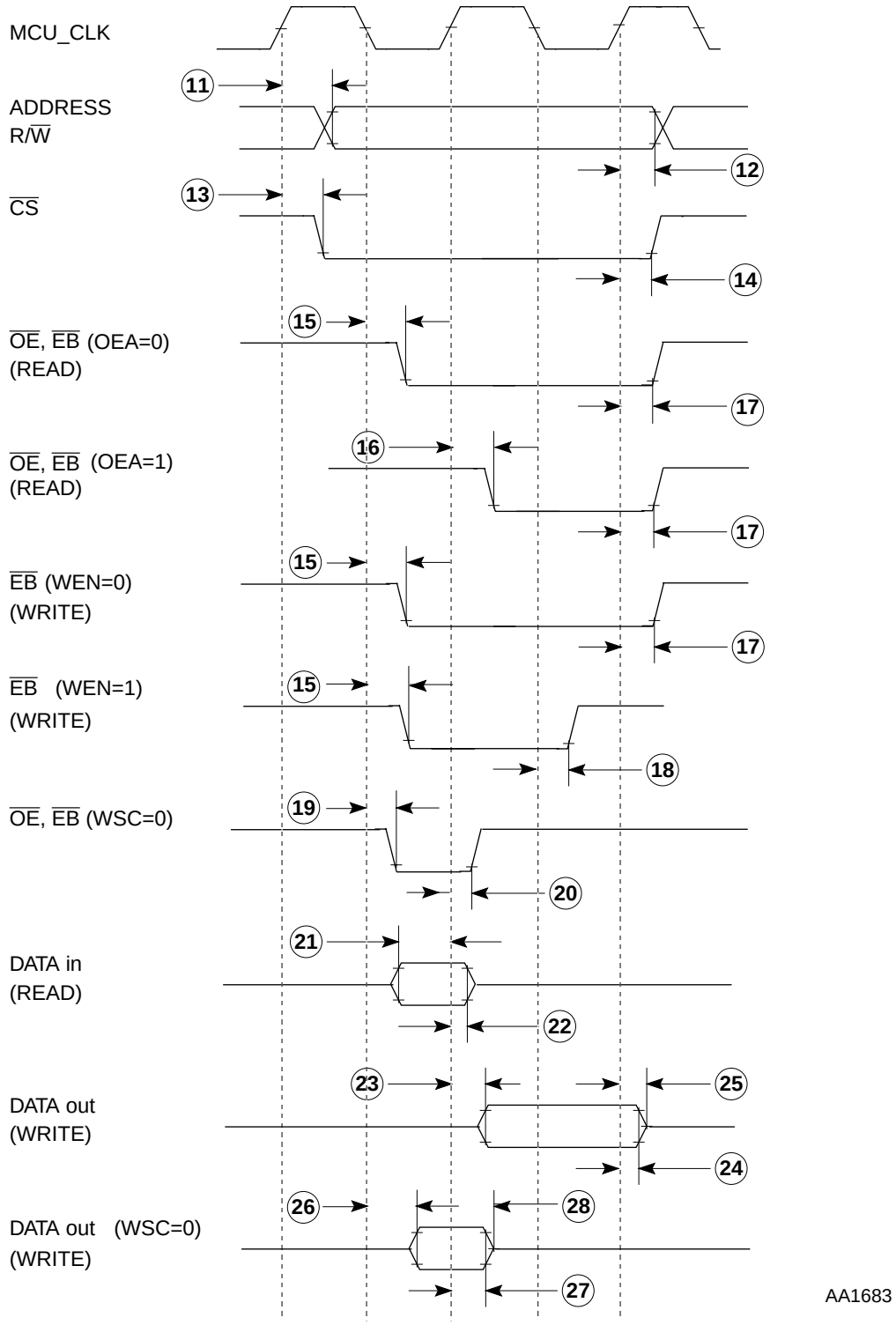


Figure 2-5 EIM Read / Write Timing

SMART CARD TIMING

Table 2-11 Smart Card Port to Smart Card AC Timing

Num	Characteristics	CKIH @16.8 MHz		Unit
		Min	Max	
31	$\overline{\text{SIMRESET}}$ low to SIMCLK low	1.18	200 / f	µs
32	SIMCLK deactivated to SIMDATA tri-state to low	1.18	200 / f	µs
33	SIMDATA low to PWR_EN low	1.18	200 / f	µs
34	$\overline{\text{SIMRESET}}$ low	40000 / f	—	ns
35	SENSE high to $\overline{\text{SIMRESET}}$ low	57	76	µs
Note: "f" is CKIH / 4 (for 5 V sims) or CKIH / 5 (for 3 V sims), as programmed in the Smart Card port.				

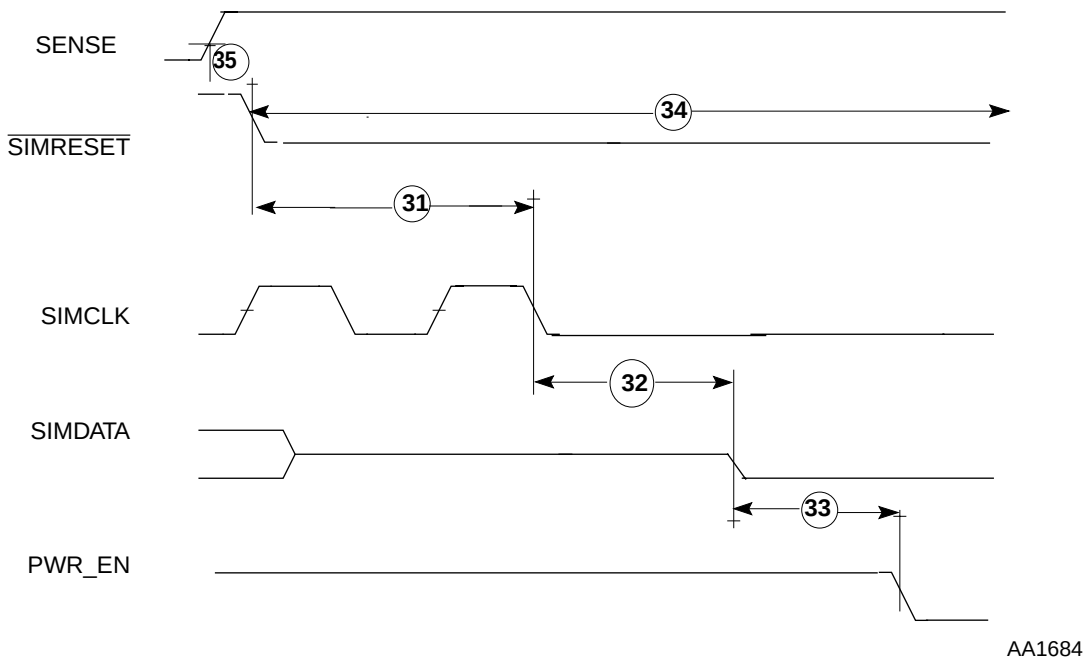


Figure 2-6 Smart Card Interface Power Down AC Timing

QSPI TIMING

The QSPI uses the signals in the serial control port to select individual serial peripherals (using the SPI chip select signals) and transfer data between peripherals and the DSP56651.

Table 2-12 QSPI Timing

Num	Characteristics	Symbol	Expression	MCU_CLK @ 16.8 MHz		Unit
				Min	Max	
301	Cycle time	T_{QCYC}	—	1	504	T_{MC}
302	Clock (SCK) high or low time	T_{SW}	—	—	252	T_{MC}
303	Chip-select lag time	T_{LAG}	—	1	∞	T_{QCYC}
304	Inter-queue transfer delay	T_{TD}	—	1	∞	T_{QCYC}
305	Chip-select lead time	T_{LEAD}	—	1	128	T_{QCYC}
306	Data setup time (inputs)	T_{SU}	—	0	—	nS
307	Data hold time (inputs)	T_{HI}	—	0.5	—	T_{QCYC}
308	Data valid (after SCK edge)	T_V	—	—	6	nS
309	Data hold time (outputs)	T_{HO}	—	–2	—	nS
310	Rise time	T_I	—	—	10	nS
311	Fall time	T_F	—	—	10	nS

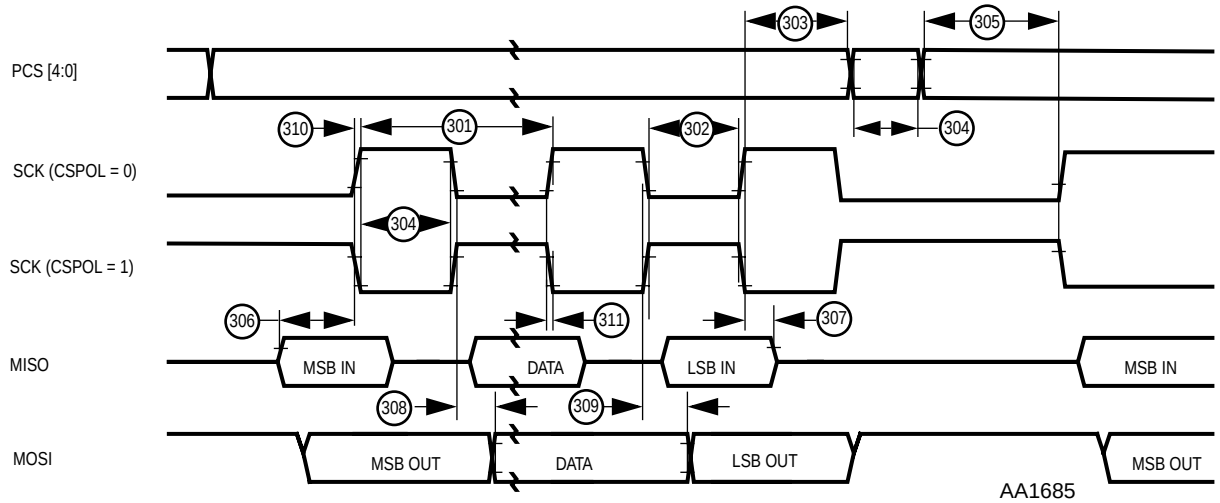


Figure 2-7 QSPI Timings for CPHA = 0

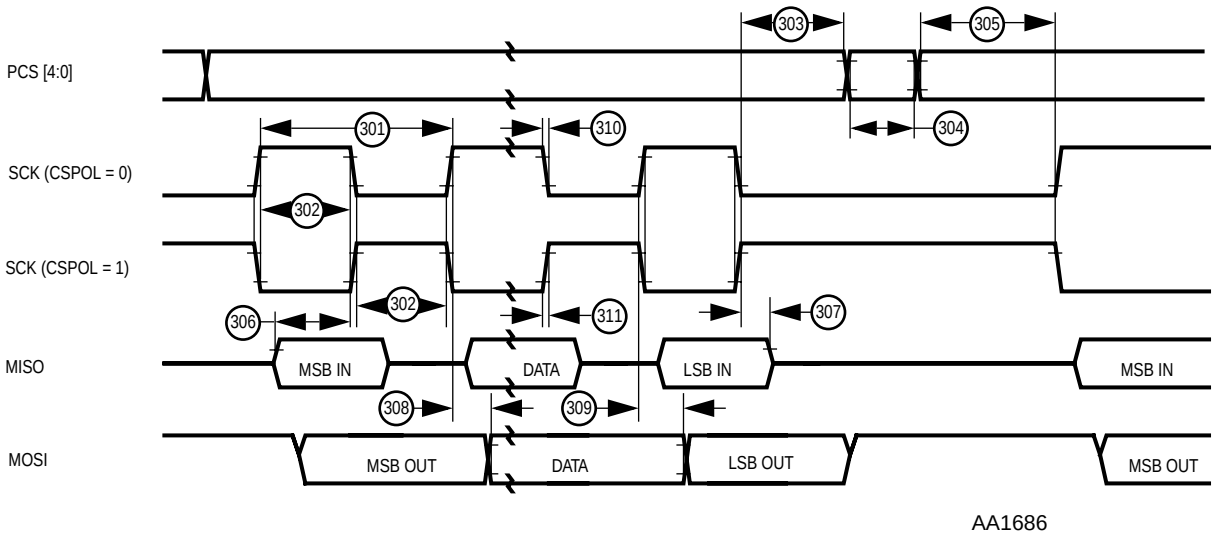


Figure 2-8 QSPI Timings for CPHA = 1

AUDIO SERIAL CODEC AND BASEBAND SERIAL CODEC TIMING

The audio serial codec port (also called the serial audio port or SAP) and the baseband serial codec port (also called the baseband port or BBP) have the same timing specifications. The timing table uses the following acronyms to describe the signal parameters:

tSSICC	=	BBP / SAP clock cycle time
TXC (SCKA / SCKB Pin)	=	Transmit clock
RXC (SC0A / SC0B or SCKA / SCKB Pin)	=	Receive clock
FST (SC2A / SC2B Pin)	=	Transmit frame sync
FSR (SC1A / SC1B or SC2A / SC2B Pin)	=	Receive frame sync
ick	=	Internal clock
xck	=	External Clock
icka	=	Internal clock, asynchronous mode (asynchronous implies that TXC and RXC are two different clocks)
icks	=	Internal clock, synchronous mode (synchronous implies that TXC and RXC are the same clock)
bl	=	Bit length
wl	=	Word length
wr	=	Word length relative

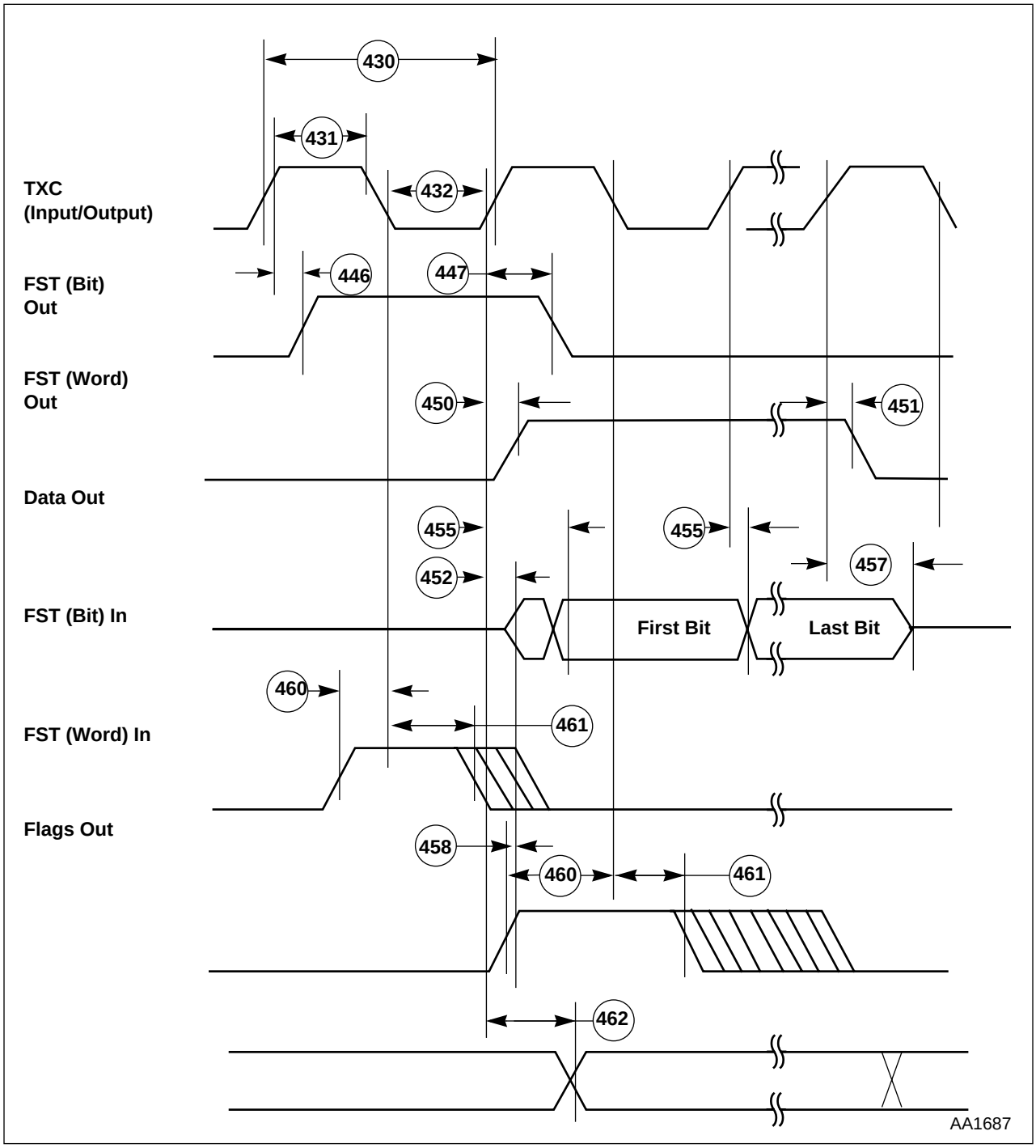
Table 2-13 SAP and BBP Timing

Num	Characteristics	Symbol	Expression	DSP @ 58.8 MHz		Case	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$4 \times T_{DC}$ $3 \times T_{DC}$	68 51	— —	i ck x ck	ns ns
431	Clock high period for internal clock for external clock	—	 $2 \times T_{DC} - 12.2$ $1.5 \times T_{DC}$	 21.8 25.5	 — —	 ick xck	 ns ns
432	Clock low period for internal clock for external clock	—	 $2 \times T_{DC} - 12.2$ $1.5 \times T_{DC}$	 21.8 25.5	 — —	 ick xck	 ns ns
433	RXC rising edge to FSR out (bl) high	—	—	— —	45.1 26.8	x ck i ck a	ns ns
434	RXC rising edge to FSR out (bl) low	—	—	— —	45.1 26.8	x ck i ck a	ns ns
435	RXC rising edge to FSR out (wr) high[2]	—	—	— —	47.6 29.3	x ck i ck a	ns ns
436	RXC rising edge to FSR out (wr) low[2]	—	—	— —	47.6 29.3	x ck i ck a	ns ns
437	RXC rising edge to FSR out (wl) high	—	—	— —	45.9 25.6	x ck i ck a	ns ns
438	RXC rising edge to FSR out (wl) low	—	—	— —	45.1 26.8	x ck i ck a	ns ns
439	Data in setup time before RXC (SCK in synchronous mode) falling edge	—	—	0.0 23.2	— —	x ck i ck	ns ns
440	Data in hold time after RXC falling edge	—	—	6.1 3.6	— —	x ck i ck	ns ns
441	FSR input (bl, wr) high before RXC falling edge[2]	—	—	1.2 28.0	— —	x ck i ck a	ns ns
442	FSR input (wl) high before RXC falling edge	—	—	1.2 28.0	— —	x ck i ck a	ns ns
443	FSR input hold time after RXC falling edge	—	—	3.6 0.0	— —	x ck i ck a	ns ns
444	Flags input setup before RXC falling edge	—	—	0.0 23.2	— —	x ck i ck s	ns ns
445	Flags input hold time after RXC falling edge	—	—	7.3 0.0	— —	x ck i ck s	ns ns

Table 2-13 SAP and BBP Timing (Continued)

Num	Characteristics	Symbol	Expression	DSP @ 58.8 MHz		Case	Unit
				Min	Max		
446	TXC rising edge to FST out (bl) high	—	—	— —	35.4 18.3	x ck i ck	ns ns
447	TXC rising edge to FST out (bl) low	—	—	— —	37.8 20.7	x ck i ck	ns ns
448	TXC rising edge to FST out (wr) high[2]	—	—	— —	37.8 20.7	x ck i ck	ns ns
449	TXC rising edge to FST out (wr) low[2]	—	—	— —	40.3 23.2	x ck i ck	ns ns
450	TXC rising edge to FST out (wl) high	—	—	— —	36.6 19.5	x ck i ck	ns ns
451	TXC rising edge to FST out (wl) low	—	—	— —	37.8 20.7	x ck i ck	ns ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	37.8 20.7	x ck i ck	ns ns
454	TXC rising edge to data out valid	—	$35 + 0.5 \times T_{DC}$	— —	43.5 25.6	x ck i ck	ns ns
455	TXC rising edge to data out high impedance[3]	—	—	— —	37.8 19.5	x ck i ck	ns ns
457	FST input (bl, wr) setup time before TXC falling edge[2]	—	—	2.0 21.0	— —	x ck i ck	ns ns
458	FST input (wl) to data out enable from high impedance[3]	—	—	—	32.9	—	ns
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	x ck i ck	ns ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	x ck i ck	ns ns
462	Flag output valid after TXC rising edge	—	—	— —	39.0 22.0	x ck i ck	ns ns

Note:
1. For internal clock, external clock cycle is defined by I_{CYC} and BBP / SAP control register.
2. Word relative frame sync signal wave form, relates to clock, as the bit length frame sync signal wave form, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
3. Periodically sampled and not 100% tested.



Note: In the network mode, output flag transitions can occur at the start of each time slot within the frame. In the normal mode, the output flag state is asserted for the entire frame period.

Figure 2-9 BBP and SAP Transmitter Timing

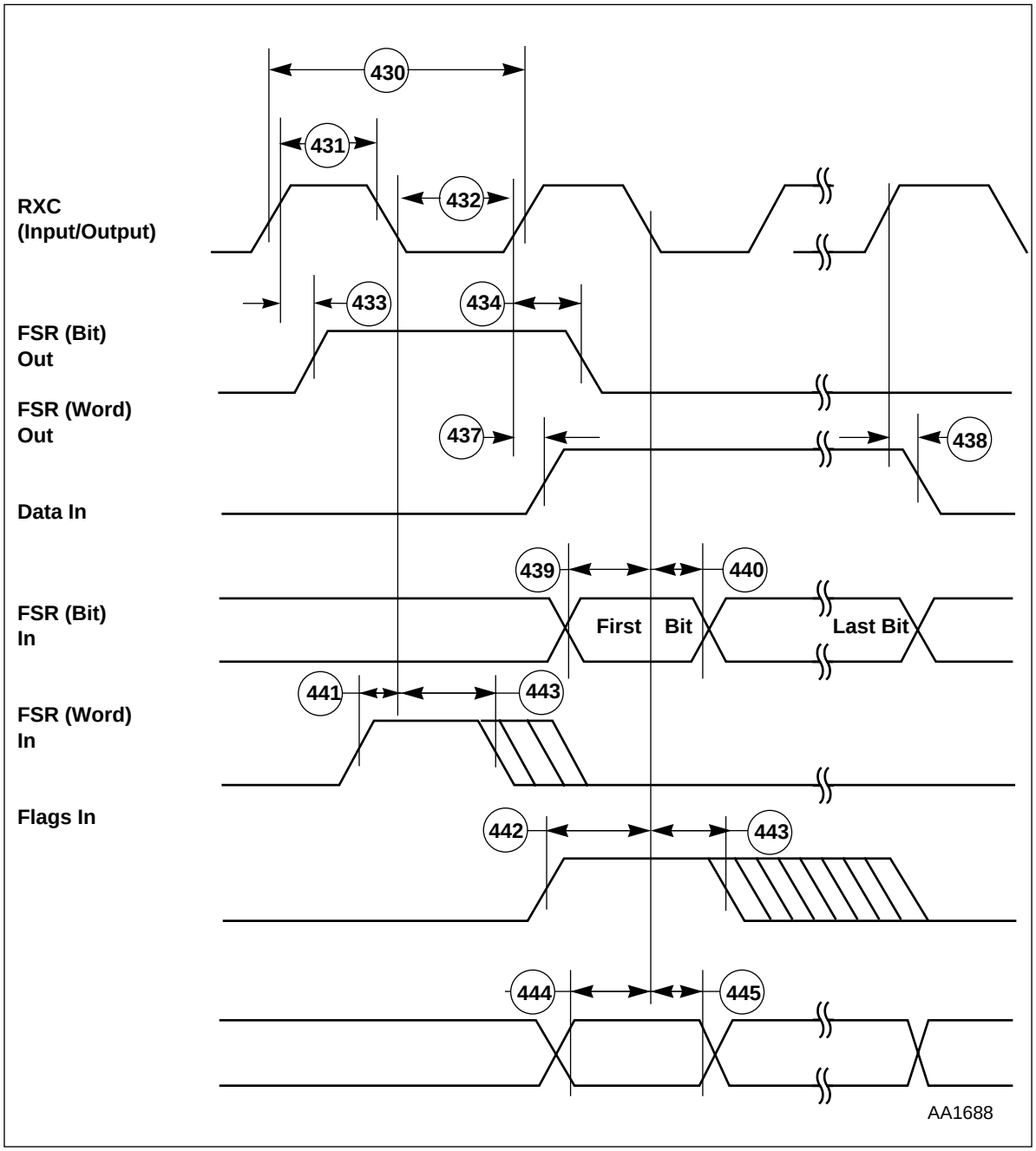


Figure 2-10 BBP And SAP Receiver Timing

JTAG PORT TIMING

Table 2-14 JTAG Timing

Num	Characteristics	Expression	DSP @ 58.8 MHz		Unit
			Min	Max	
500	TCK frequency of operation	$1/(3 \times T_{DC})$	0.0	19.6	MHz
501	TCK cycle time in crystal mode	—	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	—	20.0	—	ns
503	TCK rise and fall times	—	0.0	3.0	ns
504	Boundary scan input data setup time	—	5.0	—	ns
505	Boundary scan input data hold time	—	24.0	—	ns
506	TCK low to output data valid	—	0.0	40.0	ns
507	TCK low to output high impedance	—	0.0	40.0	ns
508	TMS, TDI data setup time	—	5.0	—	ns
509	TMS, TDI data hold time	—	25.0	—	ns
510	TCK low to TDO data valid	—	0.0	44.0	ns
511	TCK low to TDO high impedance	—	0.0	44.0	ns
512	TRST assert time	—	100.0	—	ns
513	TRST setup time to TCK low	—	40.0	—	ns

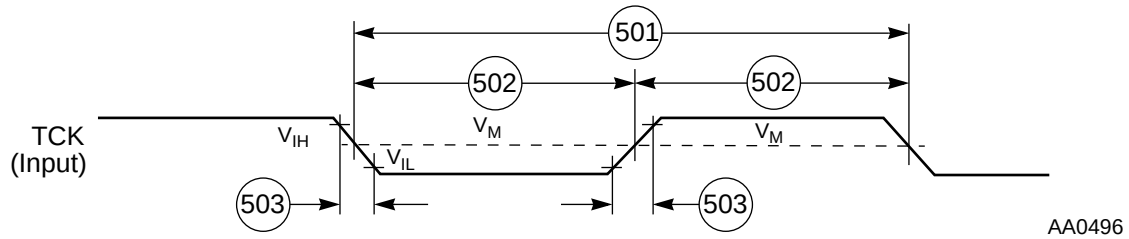


Figure 2-11 Test Clock Input Timing Diagram

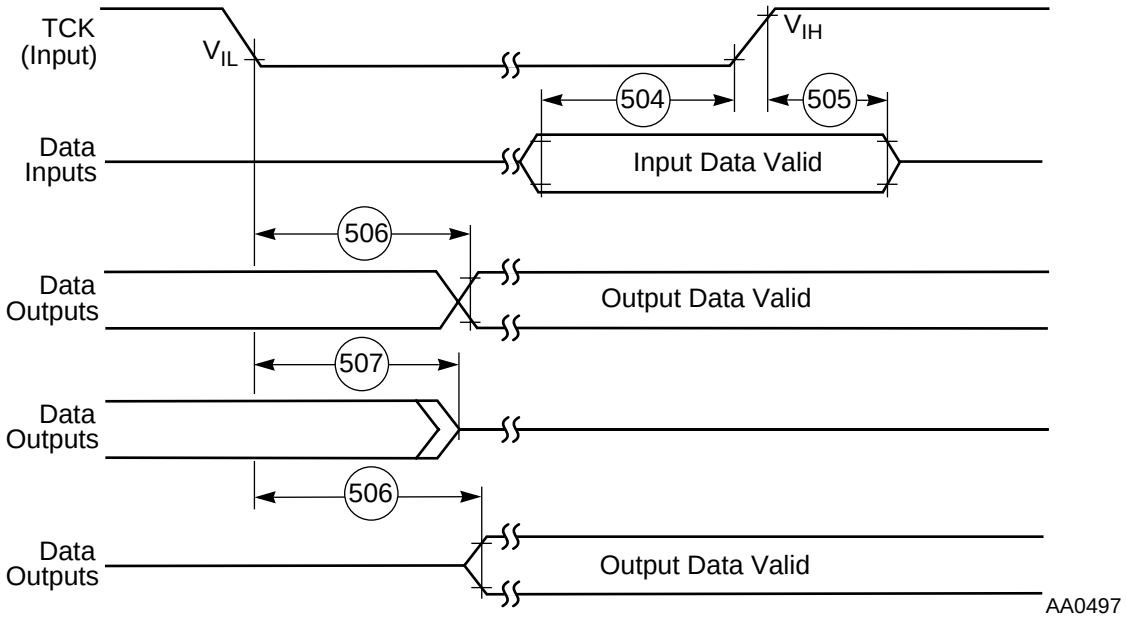


Figure 2-12 Boundary Scan (JTAG) Timing Diagram

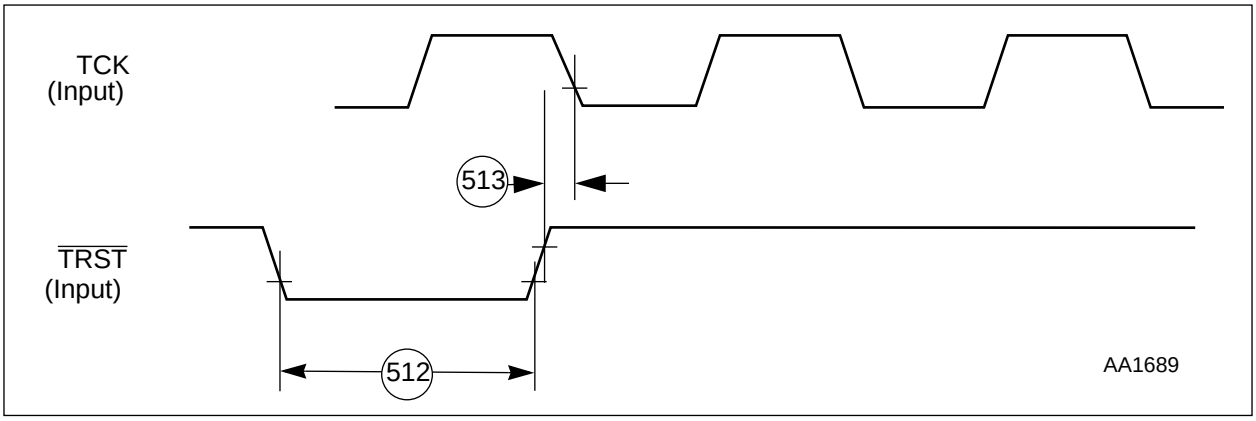


Figure 2-13 $\overline{\text{TRST}}$ Timing Diagram

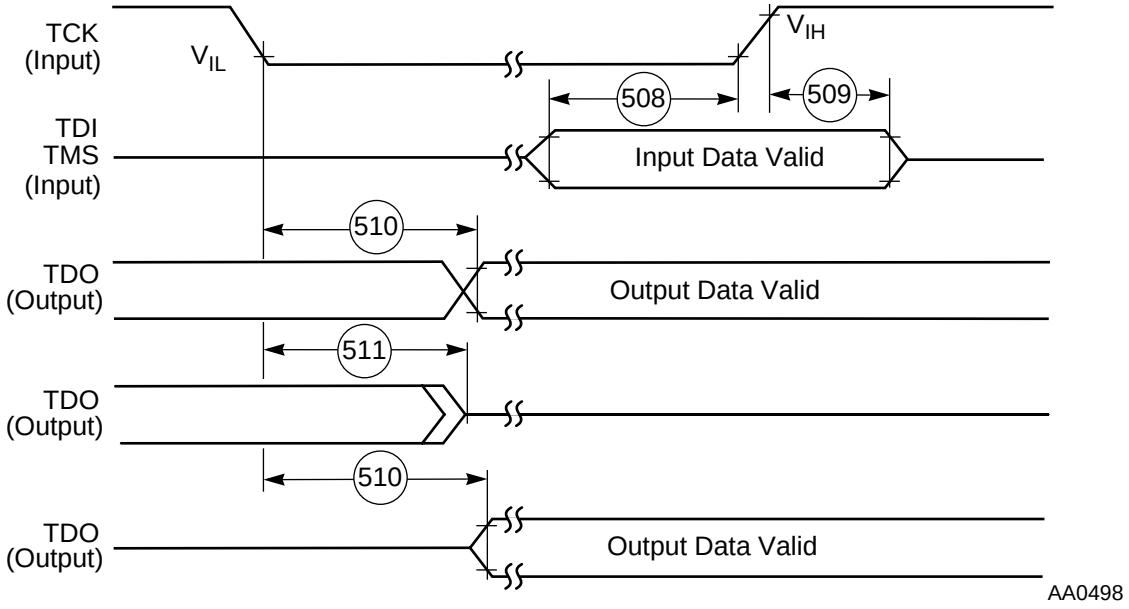


Figure 2-14 Test Access Port Timing Diagram

SECTION 3

PACKAGING

PACKAGE INFORMATION

This section provides information about the available packages for this product. The DSP56651 is available in a 196-pin plastic ball grid array (PBGA) package.

The DSP56651 part (RAM-based DSP program memory) is delivered in a 17-mm (outline) PBGA package having a solder-ball footprint identical to that of the 15 mm PBGA. Compatibility between the footprints of the two packages is maintained to minimize impact to the customer's application board routing, such that the same board can be used for both the DSP56651 and DSP56652.

196 PBGA (GT), 17 x 17 mm, with Footprint of 15-mm PBGA

The DSP56651 is offered in the non-JEDEC standard, 17-mm PBGA package. The package is "non-standard" in that the single outermost row of solder balls in the array is removed, leaving a 14 x 14 array (196) of solder balls. This package footprint is identical to that of the JEDEC standard 15 mm (outline) 196 PBGA. The pitch of the solder balls is 1 mm. Refer to the following table and figure for package drawing and dimensions.

PBGA PACKAGE DIMENSIONS

Table 3-1 Dimensions for 196 PBGA (17-mm Outline)

DIM	MILLIMETERS	
	MIN	MAX
A	1.32	1.75
A1	0.27	0.47
A2	0.30	0.40
A3	0.75	0.88
b	0.35	0.65
D	17.00	BASIC
D1	13.00	BASIC
D2	TBD	17.00
E	17.00	BASIC
E1	13.00	BASIC
E2	TBD	17.00
e	1.00	BASIC
R1	—	2.50

PBGA PACKAGE MECHANICAL DRAWING

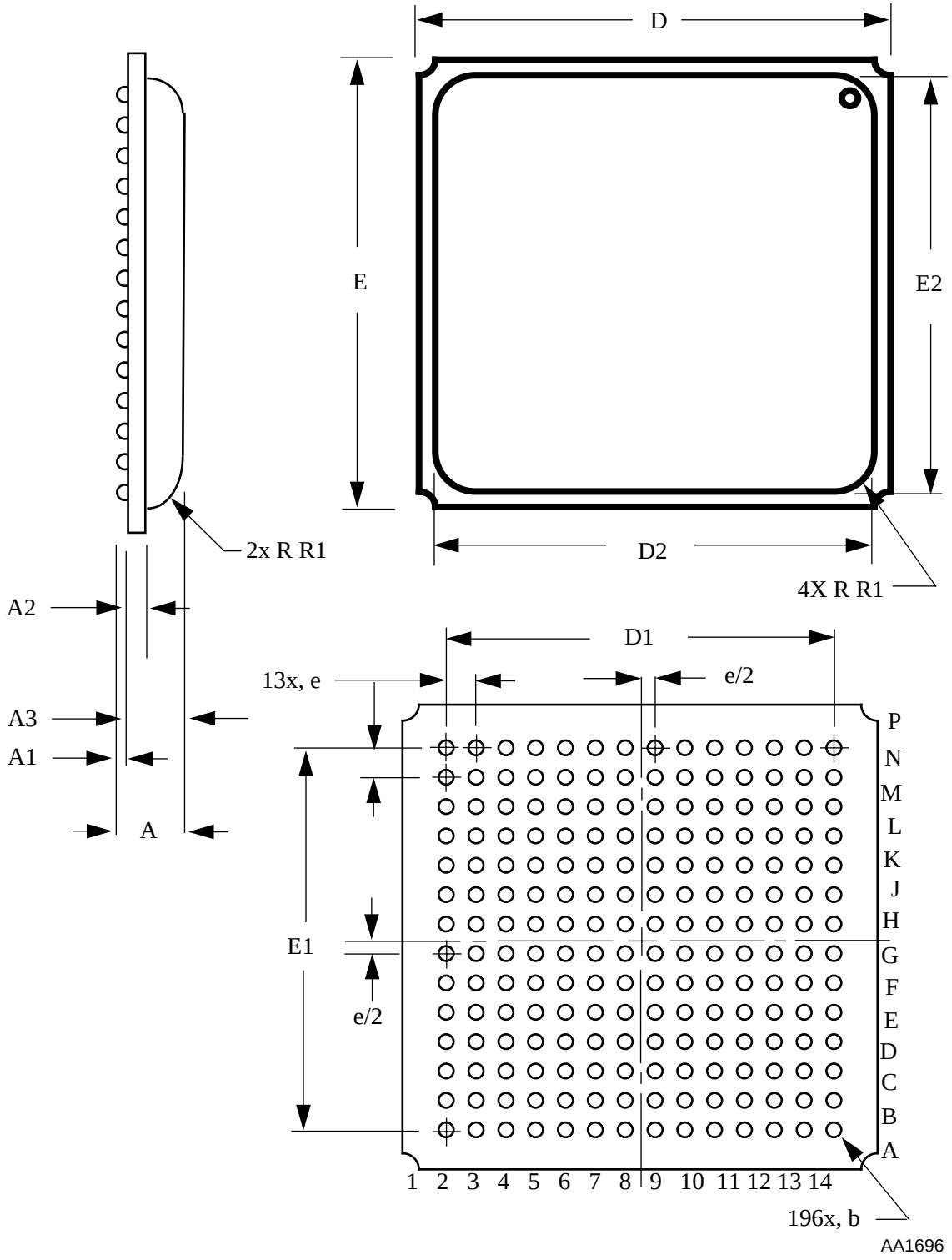


Figure 3-1 DSP56651 Mechanical Drawing

Preliminary

ORDERING DRAWINGS

Complete mechanical information regarding DSP56651 packaging is available by facsimile through Motorola's Mfax system. Call the following number to obtain information by facsimile:

(602) 244-6591

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's personal identification number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56651 196-pin PBGA package mechanical drawing is referenced as Case 1128-01 Rev. D.

SECTION 4

DESIGN CONSIDERATIONS

HEAT DISSIPATION

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature ˚C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance ˚C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ˚C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board. This model is most useful for ceramic packages with heat sinks; Ninety percent of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the

estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) as determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, this value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

Note: **Table 2-2** on page 2-2 of this document contains the package thermal values for this chip.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least four 0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer printed circuit board (PCB) with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the R/$\overline{W}$, $\overline{DSP\_IRQ}$, and INT0–INT7 signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the PLL supply pins (both V_{CC} and GND).

SECTION 5

ORDERING INFORMATION

Table 5-1 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 5-1 DSP56651 Ordering Information

Part	Package Type	Pin Count	Order Number
DSP56651	Plastic ball grid array (PBGA)	196	PC56651GC

How to reach us:

USA/Europe/Locations Not Listed:
Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
1 (800) 441-2447 (within US)
1 (303) 675-2140 (outside US)
1 (303) 675-2150 (direct FAX)

Mfax™:
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609

Asia/Pacific:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-2662928

Technical Resource Center:
1 (800) 521-6274

DSP Helpline
dsphelp@dsp.sps.mot.com

Japan:
Nippon Motorola Ltd.
SPD, Strategic Planning Office, 141
4-32-1, Nishi-Gotanda
Shinagawa-ku, Tokyo, Japan
81-3-5487-8488

Internet:
www.motorola-dsp.com

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