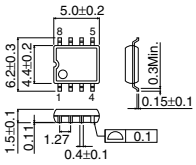
DDR-SDRAM Termination Regulator
BD3531F

●Description

BD3531F is a regulator developed as termination power supply of standard DDR-SDRAM that is used for PC.
Industry's highest speed of transient response characteristic is realized. The built-in FET can sink and source load current of 1.5A(max.)
Waveform quality when data is transferred at high speed can't be deteriorated.
BD3531F meets the bus line standards SSTL-2 of DDR-SDRAM.
High-reliability can be realized for any applications using DDR-SDRAM.

●Dimension (Unit : mm)



SOP8

●Features

1) Built-in push-pull regulator for termination(VTT)
2) Built-in reference voltage circuit(VREF)
3) Built-in enable function
4) Built-in under voltage lock out circuit
5) Package SOP8
6) Built-in thermal shut down circuit

●Applications

Note personal computer, Desktop personal computer

●Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Limits	Unit
Input voltage	VCC	7 ＊1	V
Termination input voltage	VTT_IN	7 ＊1	V
VDDQ reference voltage	VDDQ	7 ＊1	V
Power dissipation 1	Pd1	560 ＊2	mW
Power dissipation 2	Pd2	690 ＊3	mW
Operating temperature range	Topr	−10 ～ +100	˚C
Storage temperature range	Tstg	−55 ～ +150	˚C

＊1 Should not exceed Pd.
＊2 Reduced by 4.48mW for each increase in Ta of 1˚C over 25˚C(With no heat sink).
＊3 Reduced by 5.52mW for each increase in Ta of 1˚C over 25˚C(PCB(70mm×70mm×1.6mm)glass epoxy mounting.)

●Recommended Operating Conditions（Ta=25˚C）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage	VCC	4.5	—	5.5	V
Termination input voltage	VTT_IN	1.7	—	2.6	V

*This product is designed for protection against radioactive rays.

●Electrical characteristics (Unless otherwise noted, Ta=25˚C, VCC=5V, VEN=3V, VDDQ=2.5V, VTT_IN=2.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Standby current	IST	—	0.8	1.6	mA	VEN=0V
Bias current	ICC	—	2	4	mA	
<Termination>						
Termination voltage	VTT	VREF−30mV	VREF	VREF+30mV	V	Io=-3A to 3A, Ta=0℃ to 100℃ *
Source current	ITT+	1.5	—	—	A	
Sink current	ITT−	—	—	−1.5	A	
Upper side ON resistance	HRON	—	0.4	0.8	Ω	
Lower side ON resistance	LRON	—	0.4	0.8	Ω	
<Reference voltage>						
Output voltage	VREF	1/2× VDDQ-50mV	1/2× VDDQ	1/2× VDDQ+50mV	V	IREF=-10mA to 10mA Ta=0℃ to 100℃ *
Source current	IREF+	10	20	—	mA	
Sink current	IREF−	—	−20	−10	mA	
<UVLO>						
UVLO OFF voltage	VUVLO	4.2	4.35	4.5	V	VCC : Sweep up
Hysteresis voltage	ΔVUVLO	100	160	220	mV	VCC : Sweep down

* Design Guarantee

●Application Circuit