PTF041501E
PTF041501F

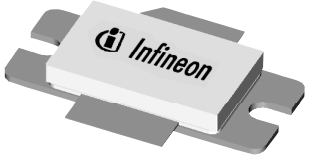
green Product

Thermally-Enhanced High Power RF LDMOS FETs
150 W, 450 – 500 MHz

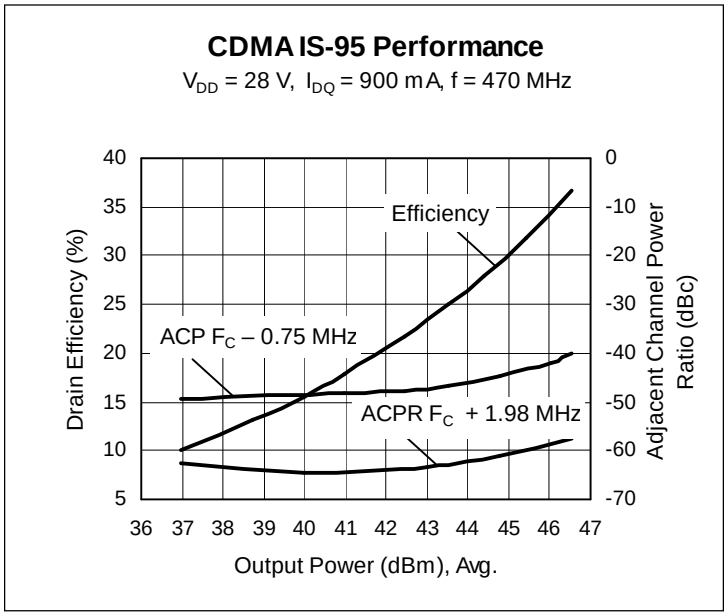
Description

The PTF041501E and PTF041501F are thermally-enhanced, 150-watt, internally-matched *GOLDMOS*® FETs intended for ultra-linear CDMA applications. They are characterized for CDMA and CDMA2000 operation from 450 to 470 MHz. Thermally-enhanced packaging provides the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.

PTF041501E
Package H-30260-2



PTF041501F
Package H-31260-2



Features

- Thermally-enhanced packages
- Broadband internal matching
- Typical CDMA performance at 470 MHz, 28 V
  - Average output power = 32 W
  - Linear Gain = 21 dB
  - Efficiency = 31%
- Typical CW performance, 470 MHz, 28 V
  - Output power at P–1dB = 165 W
  - Efficiency = 61%
- Integrated ESD protection: Human Body Model, Class 1 (minimum)
- Excellent thermal stability
- Low HCI drift
- Capable of handling 5:1 VSWR @ 28 V, 150 W (CW) output power

RF Characteristics

3-carrier CDMA2000 Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 900 mA, P_{OUT} = 60 W average, f = 470 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	21	—	dB
Drain Efficiency	η_D	—	42	—	%
Adjacent Channel Power Ratio	ACPR	—	–45	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 900 mA, P_{OUT} = 150 W PEP, f = 470 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	20.0	21	—	dB
Drain Efficiency	η_D	45	46	—	%
Intermodulation Distortion	IMD	—	–30	–29	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.07	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 900 mA	V_{GS}	2	2.9	4	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	625	W
Above 25°C derate by		3.57	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 150 W CW)	$R_{\theta JC}$	0.28	°C/W

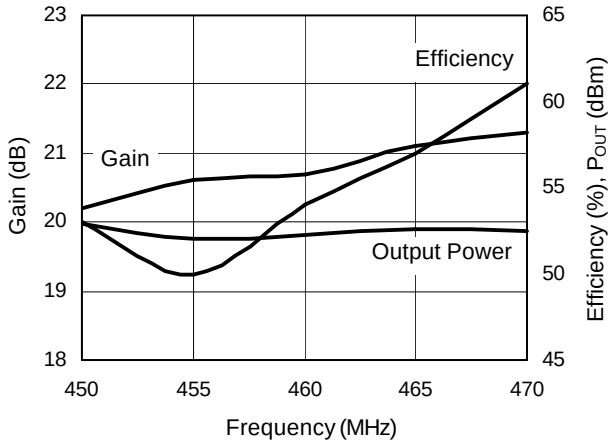
Ordering Information

Type	Package Outline	Package Description	Marking
PTF041501E	H-30260-2	Thermally-enhanced slotted flange, single-ended	PTF041501E
PTF041501F	H-31260-2	Thermally-enhanced earless flange, single-ended	PTF041501F

Typical Performance (data taken in a production test fixture)

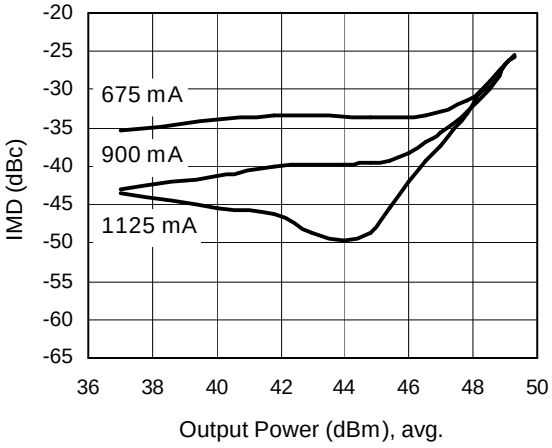
P_{OUT}, Gain & Efficiency (at P-1dB) vs. Frequency

V_{DD} = 28 V, I_{DQ} = 900 mA



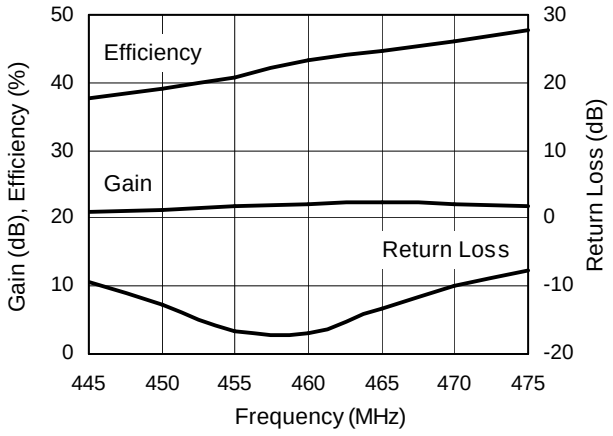
IM3 vs. Output Power at Selected Biases

V_{DD} = 28 V, f_1 = 469, f_2 = 470 MHz



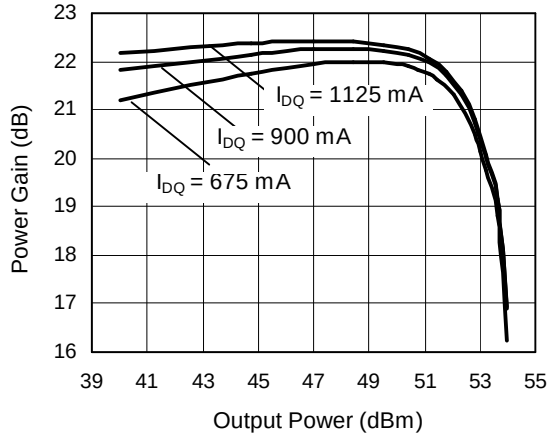
Broadband Circuit Performance

V_{DD} = 28 V, I_{DQ} = 900 mA, P_{OUT} avg.. = 48.75 dBm



Power Sweep

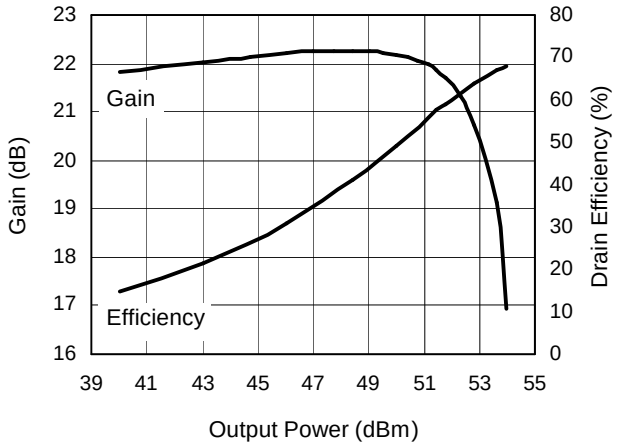
V_{DD} = 28 V, f = 470 MHz



Typical Performance (cont.)

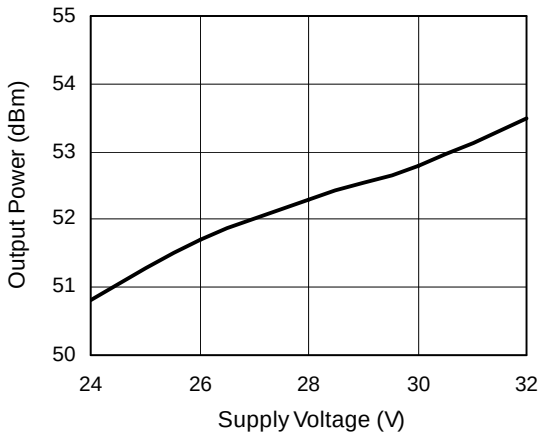
Gain & Efficiency vs. Output Power

V_{DD} = 28 V, I_{DQ} = 900 mA, f = 470 MHz



Output Power (at 1 dB Compression) vs. Supply Voltage

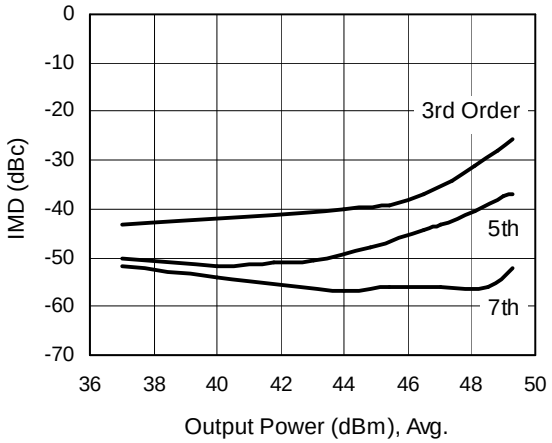
I_{DQ} = 900 mA, f = 470 MHz



Intermodulation Distortion vs. P_{OUT}

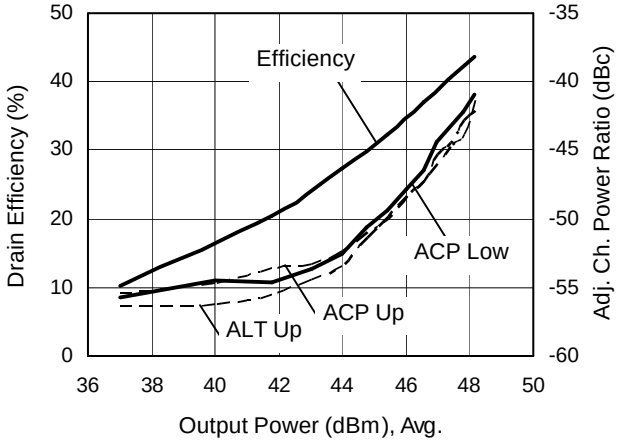
(in a broadband circuit)

V_{DD} = 28 V, I_{DQ} = 900 mA, f_1 = 469 MHz, f_2 = 470 MHz

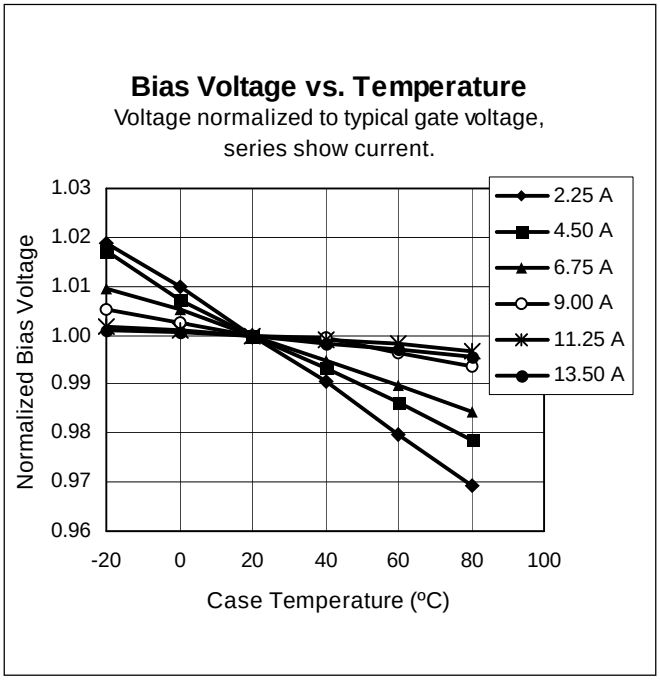


Three-carrier CDMA 2000 Performance

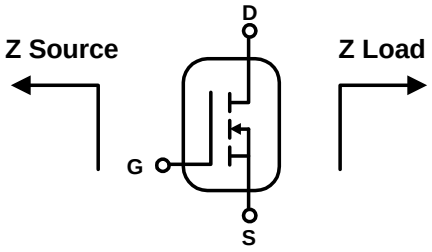
V_{DD} = 28 V, I_{DQ} = 900 mA, f = 470 MHz

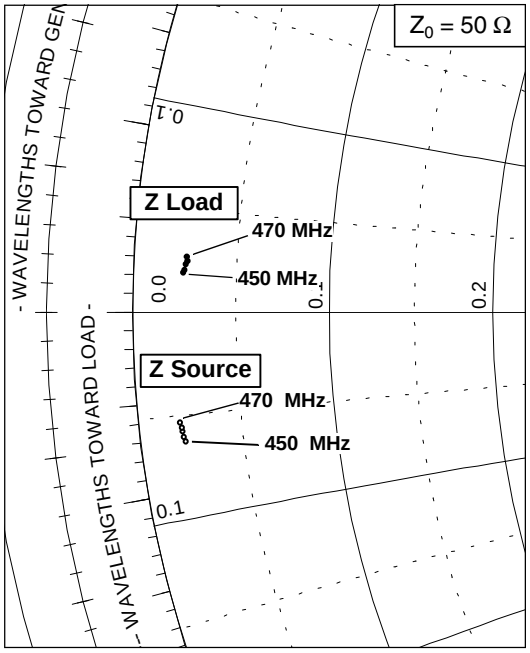


Typical Performance (cont.)



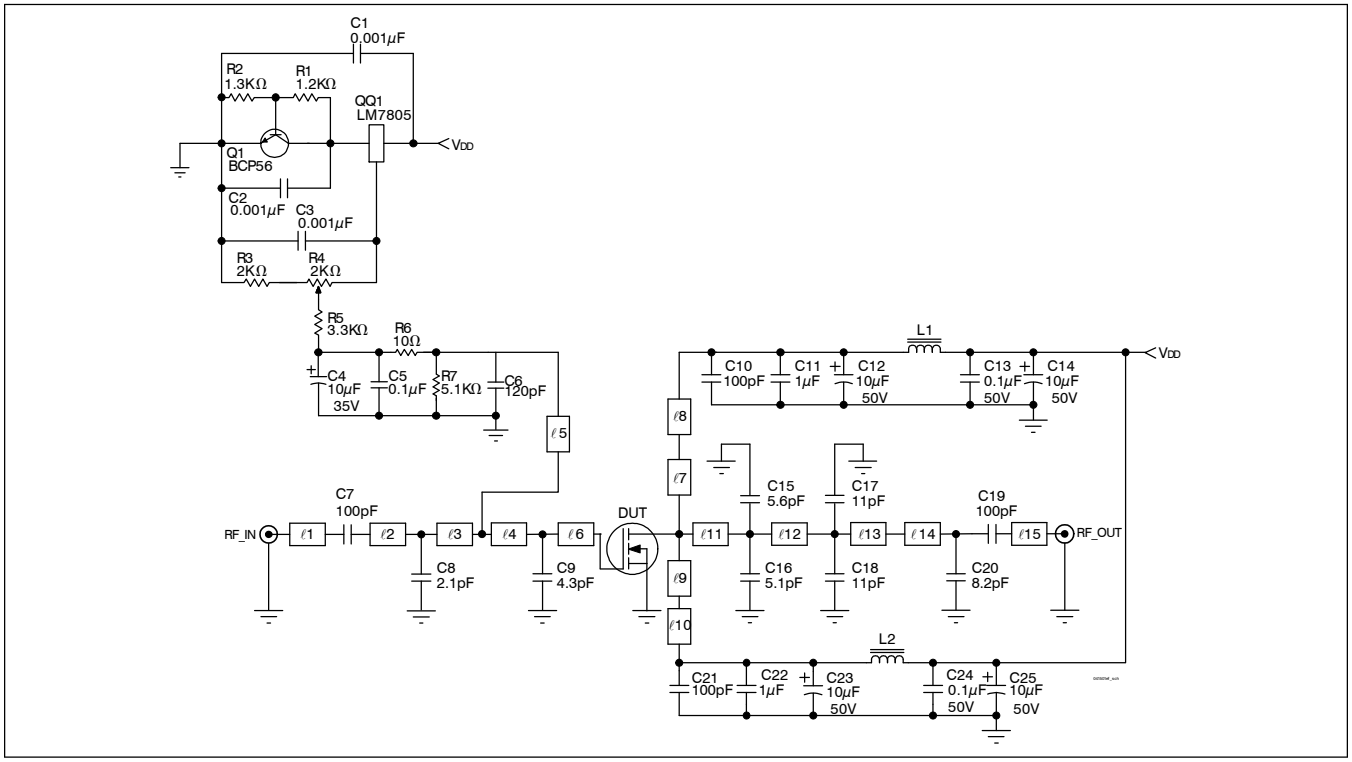
Broadband Circuit Impedance





Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
450	1.07	–3.15	1.18	0.96
455	1.03	–3.04	1.21	1.03
460	1.02	–2.89	1.24	1.17
465	1.01	–2.80	1.28	1.25
470	0.99	–2.67	1.26	1.36

Reference Circuit



Reference circuit schematic for f = 460 MHz

Circuit Assembly Information			
DUT	PTF041501E or PTF041501F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 9.2	Rogers TMM10	2 oz. copper

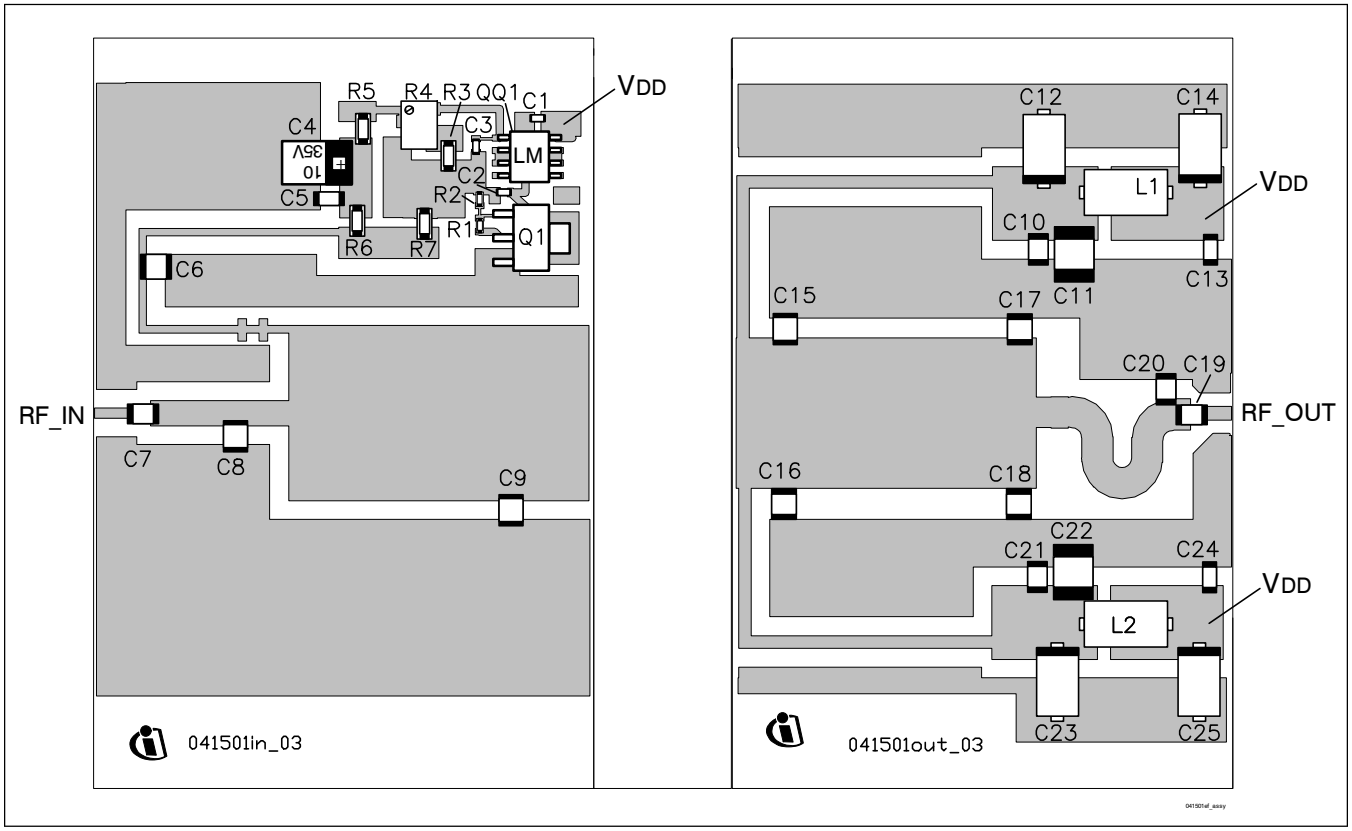
Microstrip	Electrical Characteristics at 460 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.016 λ, 50.0 Ω	4.32 x 0.71	0.170 x 0.028
ℓ2	0.033 λ, 24.0 Ω	8.13 x 2.54	0.320 x 0.100
ℓ3	0.025 λ, 24.0 Ω	6.10 x 2.54	0.240 x 0.100
ℓ4	0.097 λ, 4.8 Ω	21.59 x 17.78	0.850 x 0.700
ℓ5	0.081 λ, 50.0 Ω	21.59 x 0.71	0.850 x 0.028
ℓ6	0.040 λ, 4.8 Ω	8.89 x 17.78	0.350 x 0.700
ℓ7	0.158 λ, 38.0 Ω	40.64 x 1.27	1.600 x 0.050
ℓ8	0.030 λ, 10.9 Ω	5.59 x 7.11	0.220 x 0.280
ℓ9	0.158 λ, 38.0 Ω	40.64 x 1.27	1.600 x 0.050
ℓ10	0.030 λ, 10.9 Ω	5.59 x 7.11	0.220 x 0.280
ℓ11	0.025 λ, 5.6 Ω	5.59 x 15.24	0.220 x 0.600
ℓ12	0.105 λ, 5.6 Ω	23.62 x 15.24	0.930 x 0.600
ℓ13	0.006 λ, 5.6 Ω	1.27 x 15.24	0.050 x 0.600
ℓ14	0.104 λ, 21.3 Ω	25.40 x 3.05	1.000 x 0.120
ℓ15	0.014 λ, 50.0 Ω	3.81 x 0.71	0.150 x 0.028

[1] Electrical characteristics are rounded.

Reference Circuit (cont.)

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	PCS6106TR-ND
C5, C13, C24	Capacitor, 0.1 µF	Digi-Key	P4525-ND
C6	Ceramic capacitor, 120 pF	ATC	100B 121
C7, C10, C19, C21	Ceramic capacitor, 100 pF	ATC	100B 101
C8	Ceramic capacitor, 2.1 pF	ATC	100B 2R1
C9	Ceramic capacitor, 4.3 pF	ATC	100B 4R3
C11, C22	Capacitor, 1.0 µF	ATC	920C105
C12, C14, C23, C25	Capacitor, 10 µF, 50 V	Garrett Electronics	TPS106K050R0400
C15	Ceramic capacitor, 5.6 pF	ATC	100B 5R6
C16	Ceramic capacitor, 5.1 pF	ATC	100B 5R1
C17, C18	Ceramic capacitor, 11 pF	ATC	100B 110
C20	Ceramic capacitor, 8.2 pF	ATC	100B 8R2
L1, L2	Ferrite, 6 mm	Ferroxcube	53/3/4.6-452
Q1	Transistor	Infineon	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3	Chip resistor, 2 k-ohms	Digi-Key	P2.0KECT-ND
R4	Potentiometer, 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5	Chip resistor, 3.3 k-ohms	Digi-Key	P3.3KECT-ND
R6	Chip resistor, 10 ohms	Digi-Key	P10ECT-ND
R7	Chip resistor, 5.1 k-ohms	Digi-Key	P5.1KECT-ND

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

**Gerber Files for this circuit available on request*

Package Outline Specifications

Package H-30260-2

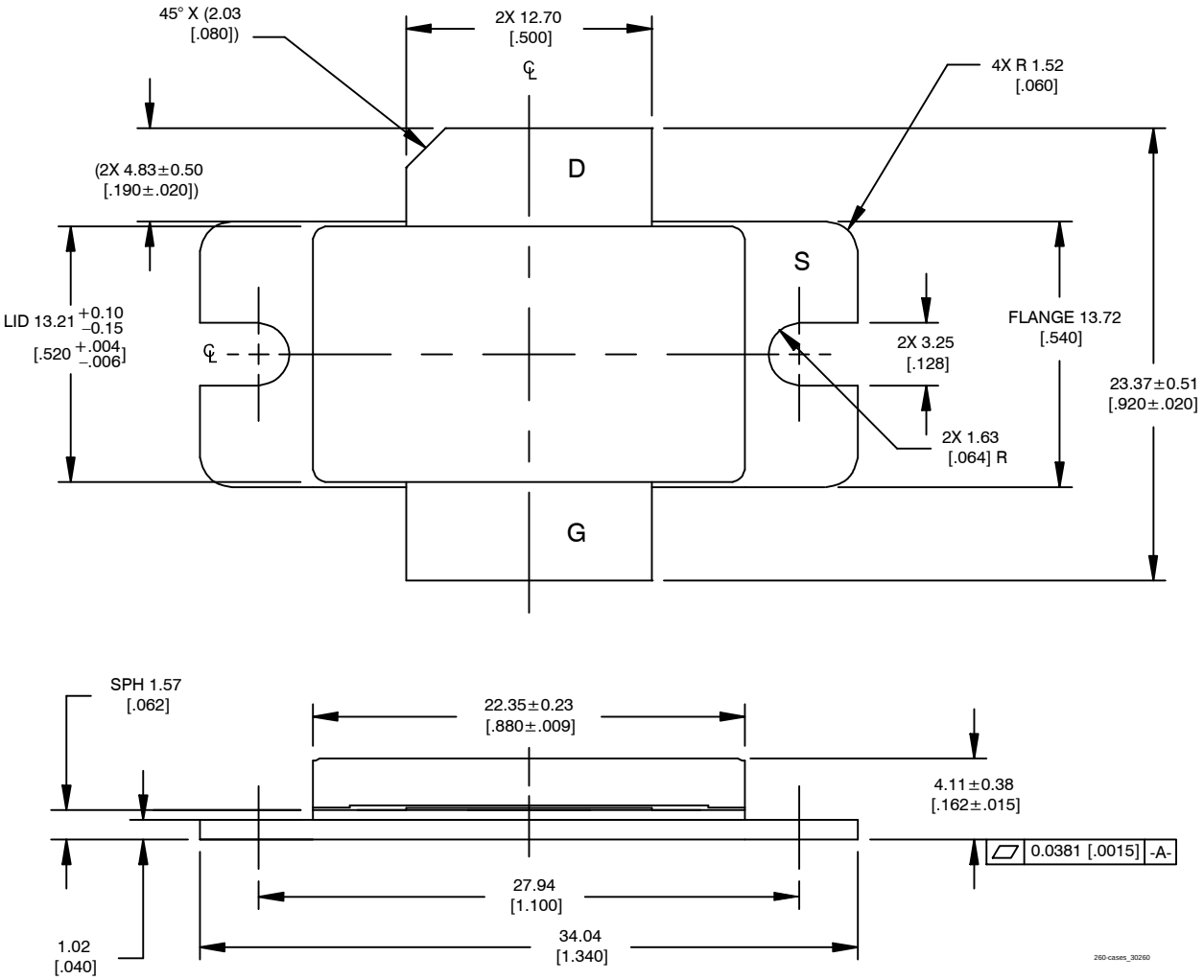


Diagram Notes:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S - flange: 2.54 micron [100 microinch] (min)
   D, G - leads: 1.14 micron ± 0.38 micron [45 microinch ± 15 microinch]

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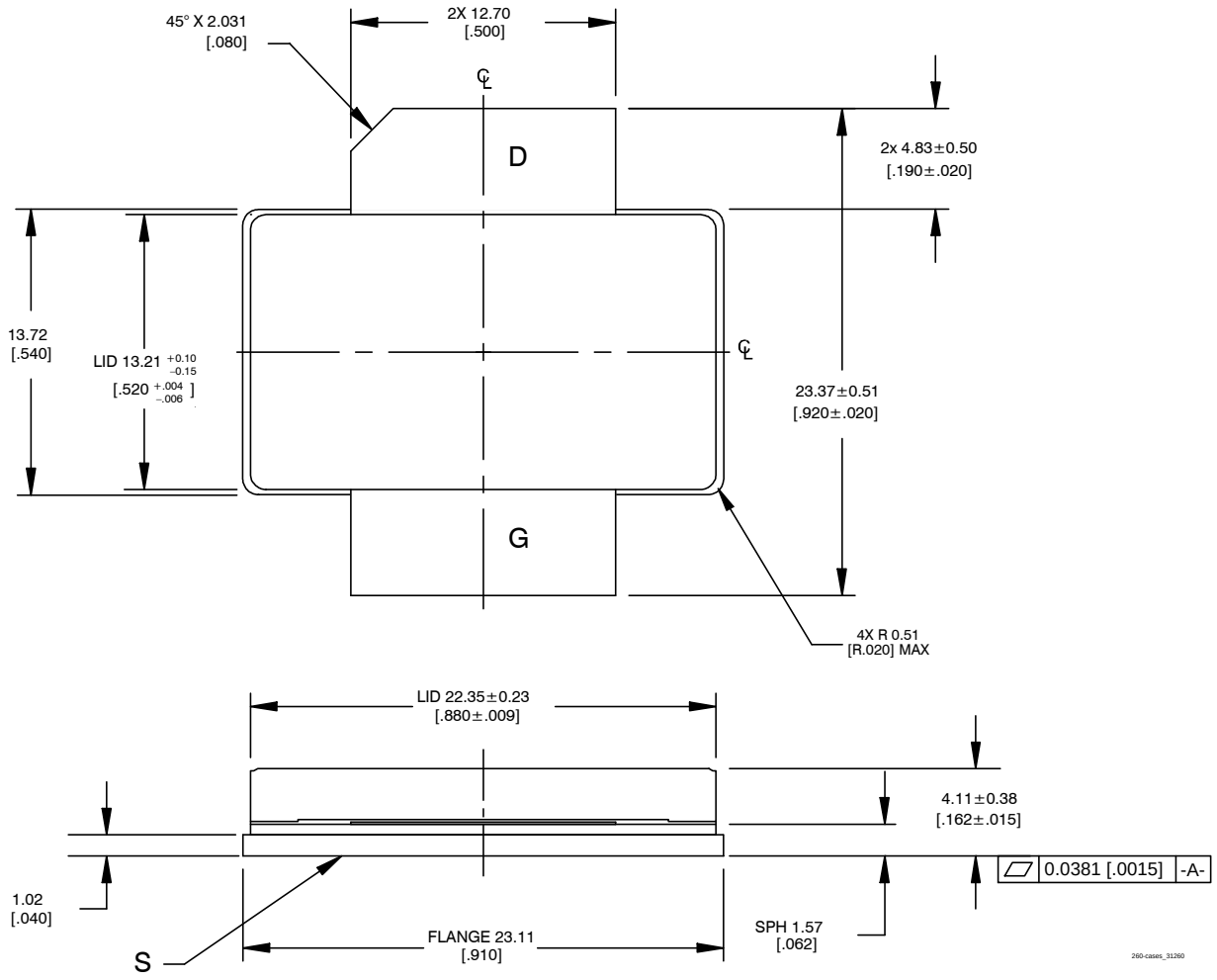
Package Outline Specifications (cont.)

Package H-31260-2



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Revision History:	**2007-08-01**	Data Sheet
Previous Version:	2005-04-15, Data Sheet	
Page	Subjects (major changes since last revision)	
6	Corrected circuit information	
all	Updated company information	

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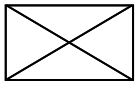

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