

## Single, Dual, and Quad Micropower, Zero-Drift, RRIO Operational Amplifiers

The ISL28133, ISL28233 are single and dual micropower, zero-drift operational amplifiers that are optimized for single supply operation from 1.65V to 5.5V. Their low supply current of 18μA and wide input range enable the ISL28133 to be an excellent general purpose op amp for a range of applications. The ISL28133 is ideal for handheld devices that operates off 2 AA or single Li-Ion batteries.

The ISL28133 is available in the 5 Ld SOT-23, the 5 Ld SC70 and the 6 Ld 1.6mmx1.6mm μTDFN packages. All devices operates over the extended temperature range of -40°C to +125°C.

## Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28133FHZ-T7* (Note 1)	BCFA	5 Ld SOT-23	MDP0038
<i>Coming Soon</i> ISL28133FHZ-T7A* (Note 1)	BCFA	5 Ld SOT-23	MDP0038
<i>Coming Soon</i> ISL28133FEZ-T7* (Note 1)	BHA	5 Ld SC70	P5.049
<i>Coming Soon</i> ISL28133FEZ-T7A* (Note 1)	BHA	5 Ld SC70	P5.049
<i>Coming Soon</i> ISL28133FRUZ-T7* (Note 2)	T8	6 Ld μTDFN	L6.1.6x1.6C
<i>Coming Soon</i> ISL28233FUZ (Note 1)	8233Z	8 Ld MSOP	MDP0043
<i>Coming Soon</i> ISL28233FUZ-T7* (Note 1)	8233Z	8 Ld MSOP	MDP0043
<i>Coming Soon</i> ISL28233FRTZ-T7* (Note 1)	TBD	8 Ld TDFN	TBD
<i>Coming Soon</i> ISL28433FVZ (Note 1)	TBD	14 Ld TSSOP	M14.173

\*Please refer to TB347 for details on reel specifications.

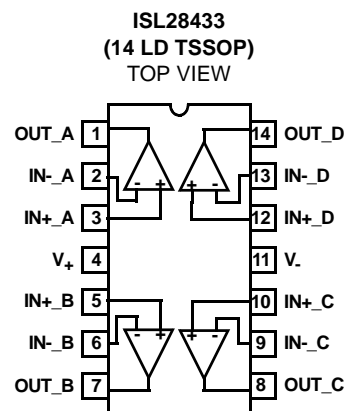
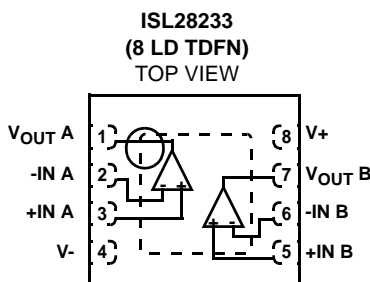
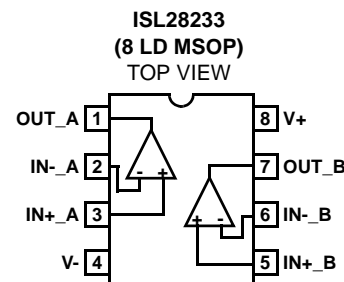
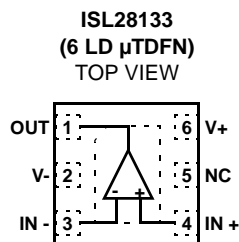
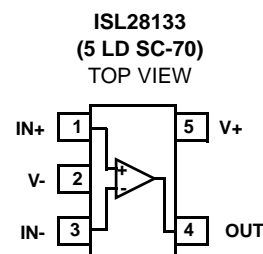
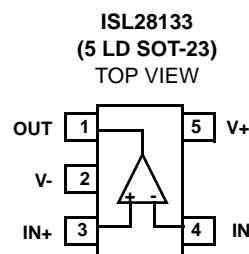
### NOTES:

- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

- Low Input Offset Voltage . . . . . 8μV, Max.
- Low Offset Drift. . . . . 0.075μV/°C, Max
- Quiescent Current . . . . . 18μA, Typ.
- Wide Supply Range . . . . . 1.65V to 5.5V
- Low Output Noise (0.01Hz to 10Hz). . . . . 1.1μV<sub>P-P</sub>, Typ.
- Rail-to-Rail Inputs and Output
- Input Bias Current . . . . . 300pA, Max.
- Operating Temperature Range. . . . . -40°C to +125°C

## Pinouts



## Absolute Maximum Ratings

Max Supply Voltage $V_+$ to $V_-$	5.75V
Max Voltage $V_{IN}$ to GND	-0.5V to 5.75V
Max Input Differential Voltage	5.75V
Max Input Current	20mA
Max Voltage $V_{OUT}$ to GND (10s)	5.75V
ESD Rating	
Human Body Model	3000V
Machine Model	200V
Charged Device Model	1500V

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
5 Ld SOT-23	225
5 Ld SC70	206
6 Ld $\mu$ TDFN	133
Maximum Storage Temperature Range	-65°C to +150°C
Pb-Free Reflow Profile	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

## Operating Conditions

Temperature Range	-40°C to +125°C
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CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$ , unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
DC SPECIFICATIONS						
V <sub>OS</sub>	Input Offset Voltage		-8	±2	8	μV
			-15.5		15.5	μV
TCV <sub>OS</sub>	Input Offset Voltage Temperature Coefficient			0.02	0.075	μV/°C
I <sub>OS</sub>	Input Offset Current			-60		pA
I <sub>B</sub>	Input Bias Current		-300	±30	300	pA
			-600		600	pA
Common Mode Input Voltage Range		V+ = 5.0V, V- = GND	-0.1		5.1	V
CMRR	Common Mode Rejection Ratio	V <sub>CM</sub> = -0.1V to 5.0V	118	125		dB
			115			dB
PSRR	Power Supply Rejection Ratio	V <sub>S</sub> = 2V to 5.5V	110	138		dB
			110			dB
V <sub>OH</sub>	Output Voltage Swing, High	R <sub>L</sub> = 10kΩ	4.965	4.981		V
V <sub>OL</sub>	Output Voltage Swing, Low			18	35	mV
A <sub>OL</sub>	Open Loop Gain	R <sub>L</sub> = 1MΩ		200		dB
V <sub>+</sub>	Supply Voltage	(Note 5)	1.65		5.5	V
I <sub>S</sub>	Supply Current	R <sub>L</sub> = OPEN		18	25	μA
					35	μA
I <sub>SC+</sub>	Output Source Short Circuit Current	R <sub>L</sub> = Short to ground or V+	13	17	26	mA
I <sub>SC-</sub>	Output Sink Short Circuit Current		-26	-19	-13	mA
AC SPECIFICATONS						
GBWP	Gain Bandwidth Product f = 50kHz	A <sub>V</sub> = 100, R <sub>F</sub> = 100kΩ, R <sub>G</sub> = 1kΩ, R <sub>L</sub> = 10kΩ to V <sub>CM</sub>		400		kHz
e <sub>N</sub> V <sub>P-P</sub>	Peak-to-Peak Input Noise Voltage	f = 0.01Hz to 10Hz		1.1		μV <sub>P-P</sub>
e <sub>N</sub>	Input Noise Voltage Density	f = 1kHz		65		nV/√(Hz)

**Electrical Specifications**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$ , unless otherwise specified. **Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+125^\circ C$ .** (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
i <sub>N</sub>	Input Noise Current Density	f = 1kHz		72		fA/√(Hz)
		f = 10Hz		79		fA/√(Hz)
C <sub>in</sub>	Differential Input Capacitance	f = 1MHz		1.6		pF
	Common Mode Input Capacitance			1.12		pF
TRANSIENT RESPONSE						
SR	Positive Slew Rate	V <sub>OUT</sub> = 1V to 4V, R <sub>L</sub> = 10kΩ		0.2		V/μs
	Negative Slew Rate			0.1		V/μs
t <sub>r</sub> , t <sub>f</sub> , Small Signal	Rise Time, t <sub>r</sub> 10% to 90%	A <sub>V</sub> = +1, V <sub>OUT</sub> = 0.1V <sub>P-P</sub> , R <sub>F</sub> = 0Ω, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 1.2pF		1.1		μs
	Fall Time, t <sub>f</sub> 10% to 90%			1.1		μs
t <sub>r</sub> , t <sub>f</sub> Large Signal	Rise Time, t <sub>r</sub> 10% to 90%	A <sub>V</sub> = +1, V <sub>OUT</sub> = 2V <sub>P-P</sub> , R <sub>F</sub> = 0Ω, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 1.2pF		8		μs
	Fall Time, t <sub>f</sub> 10% to 90%			10		μs
t <sub>s</sub>	Settling Time to 0.1%, 2V <sub>P-P</sub> Step	A <sub>V</sub> = +1, R <sub>F</sub> = 0Ω, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 1.2pF		35		μs

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Parts are 100% tested with a minimum operating voltage of 1.65V to a VOS limit of  $\pm 15\mu V$ .

**Typical Performance Curves**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ .

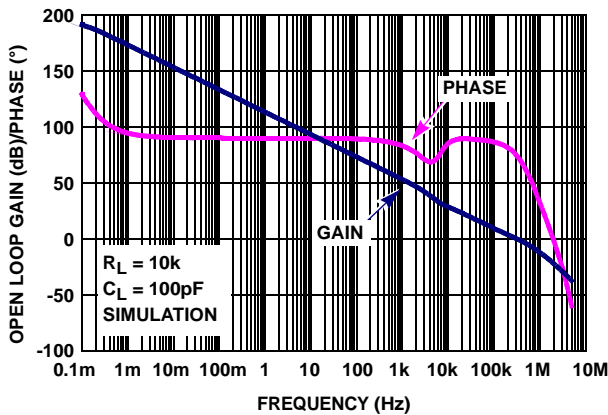


FIGURE 1. FREQUENCY RESPONSE vs OPEN LOOP GAIN,  
 $R_L = 10k$

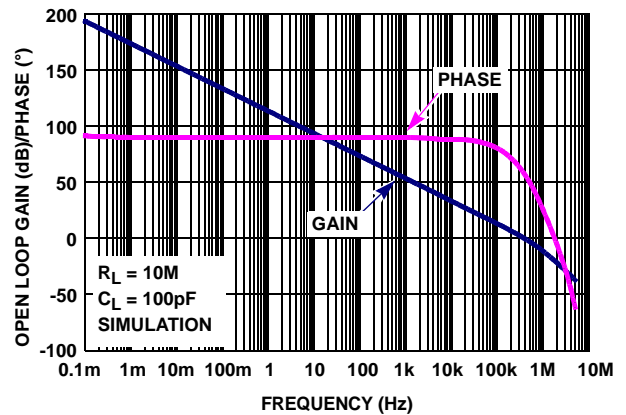


FIGURE 2. FREQUENCY RESPONSE vs OPEN LOOP GAIN,  
 $R_L = 10M$

## Typical Performance Curves

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ . (Continued)

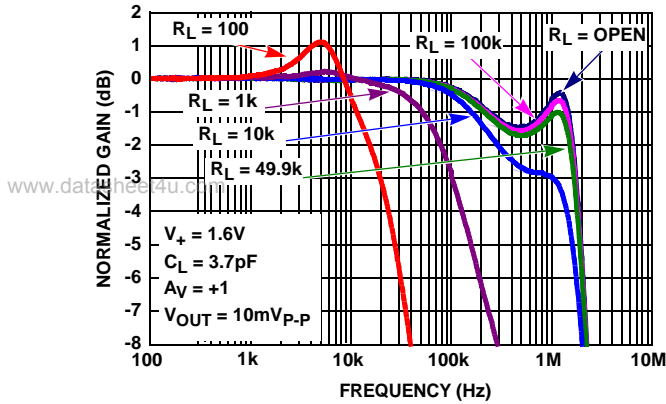


FIGURE 3. GAIN vs FREQUENCY vs  $R_L$ ,  $V_S = 1.6V$

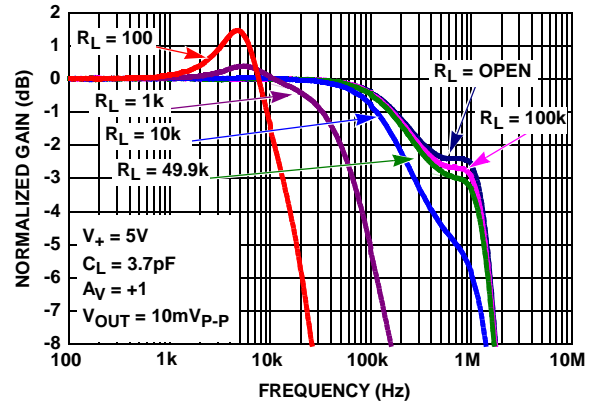


FIGURE 4. GAIN vs FREQUENCY vs  $R_L$ ,  $V_S = 5V$

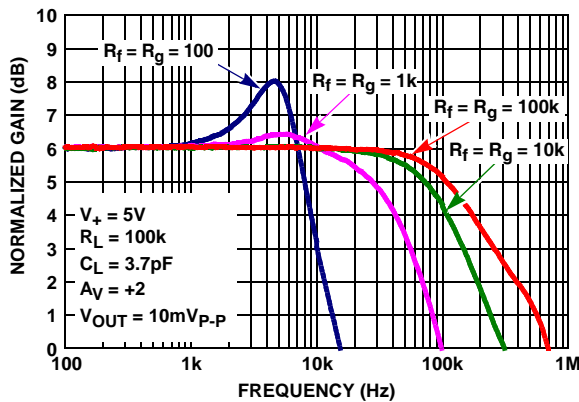


FIGURE 5. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES  $R_f/R_g$

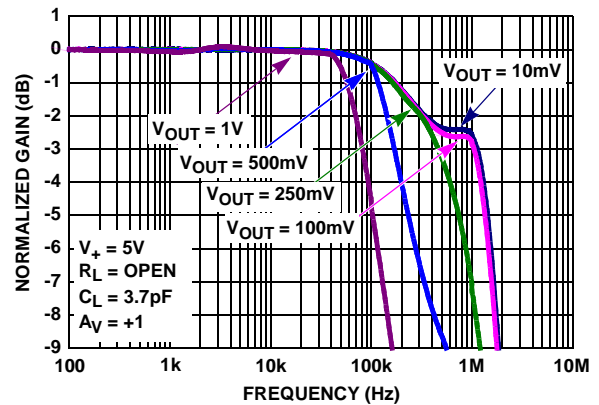


FIGURE 6. GAIN vs FREQUENCY vs  $V_{OUT}$ ,  $R_L = \text{OPEN}$

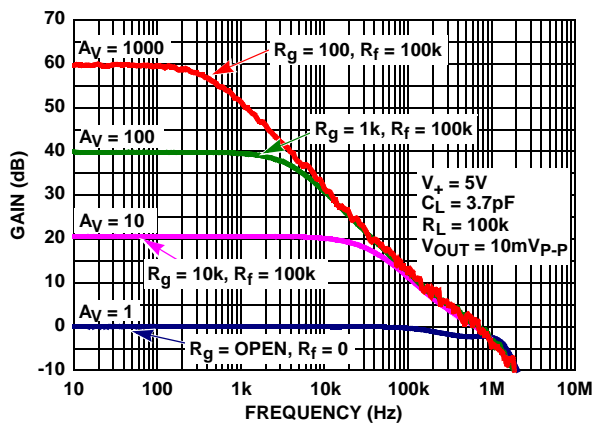


FIGURE 7. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

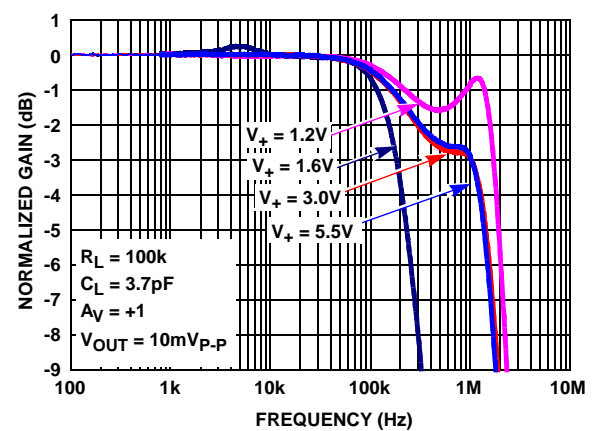


FIGURE 8. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

## Typical Performance Curves

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ . (Continued)

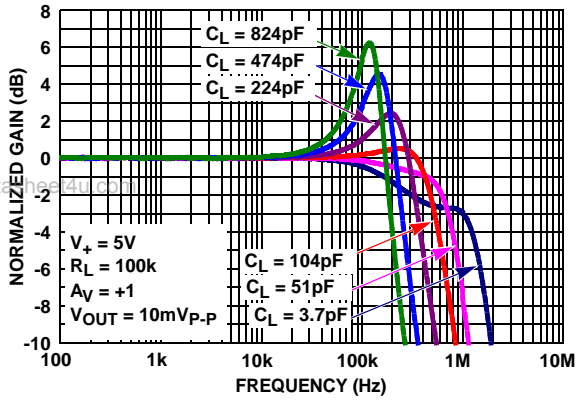


FIGURE 9. GAIN vs FREQUENCY vs  $C_L$

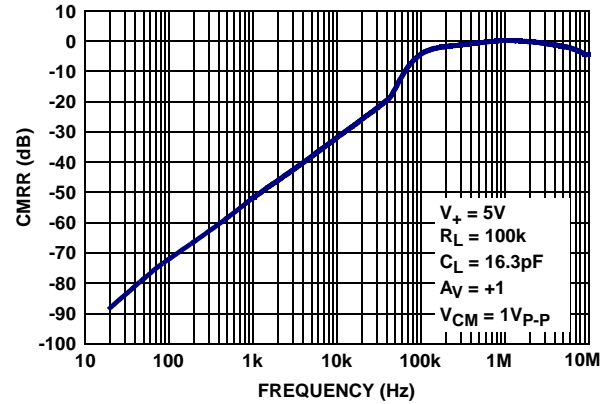


FIGURE 10. CMRR vs FREQUENCY,  $V_S = 5V$

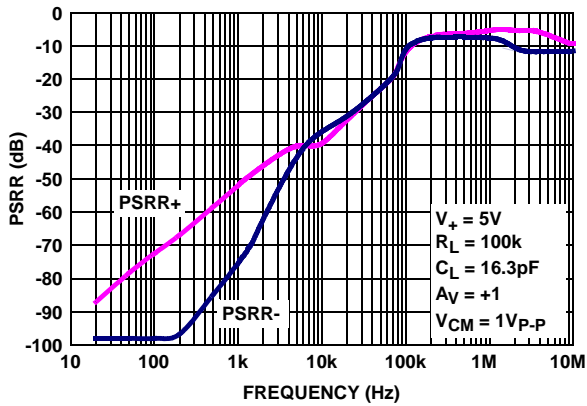


FIGURE 11. PSRR vs FREQUENCY,  $V_S = 5V$

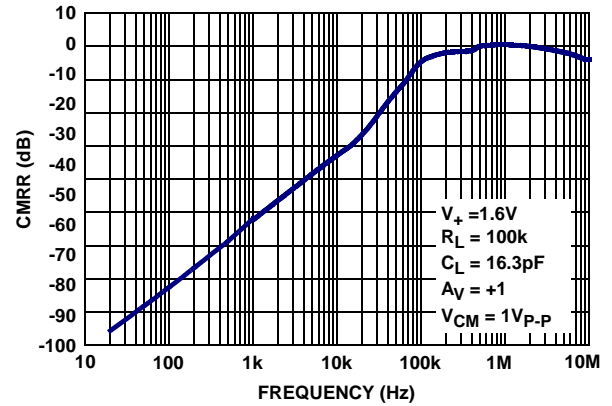


FIGURE 12. CMRR vs FREQUENCY,  $V_S = 1.6V$

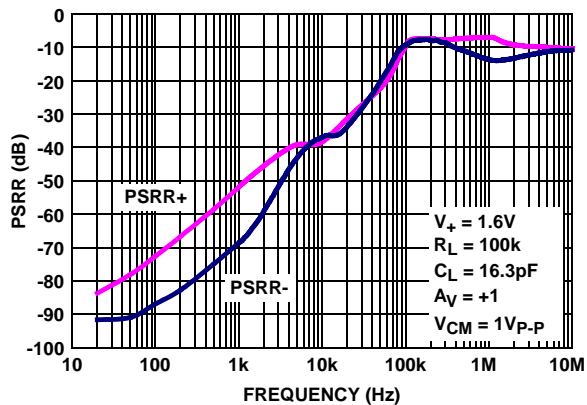


FIGURE 13. PSRR vs FREQUENCY,  $V_S = 1.6V$

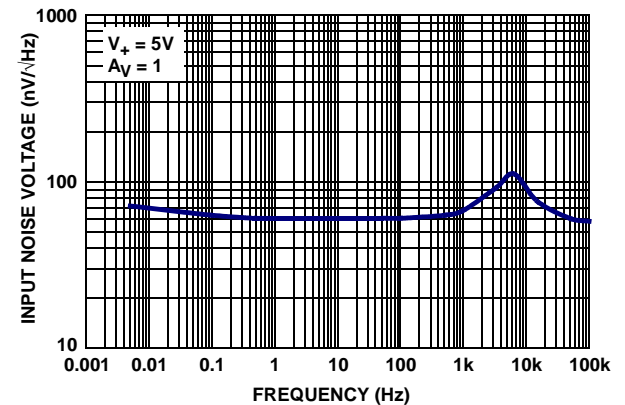


FIGURE 14. INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

# Typical Performance Curves

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ . (Continued)

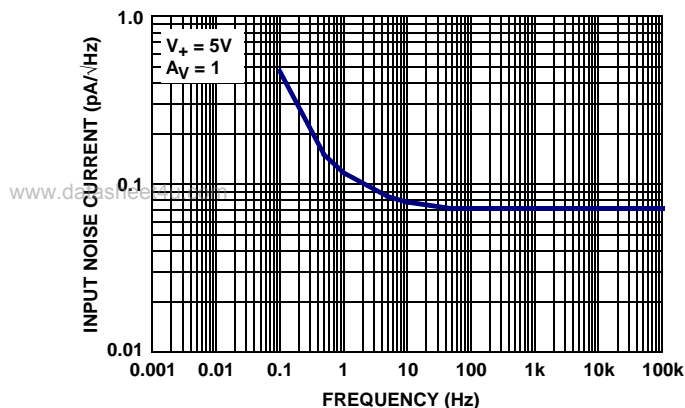


FIGURE 15. INPUT NOISE CURRENT DENSITY vs FREQUENCY

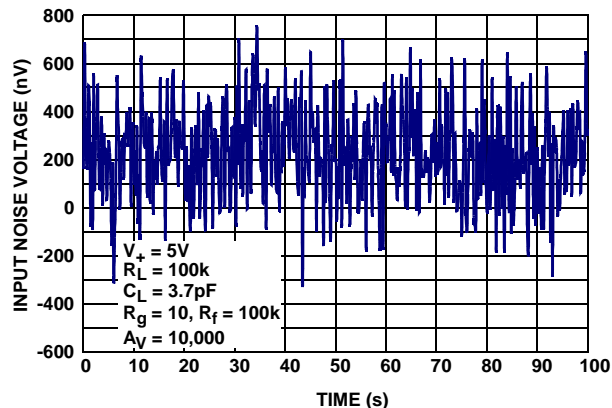


FIGURE 16. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

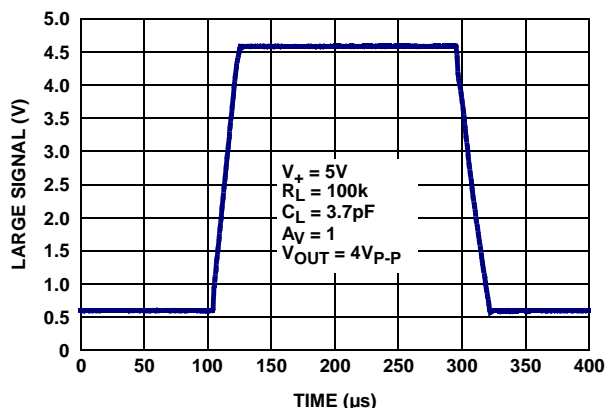


FIGURE 17. LARGE SIGNAL STEP RESPONSE (4V)

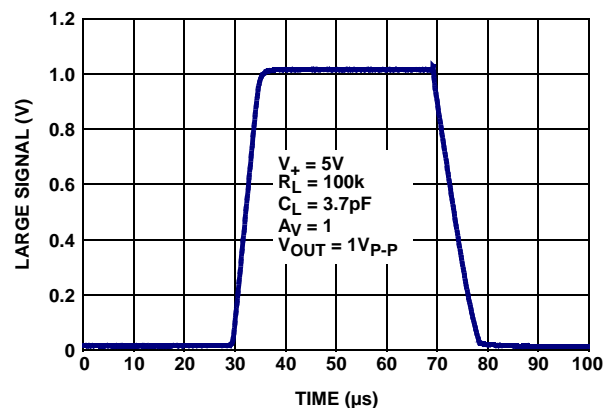


FIGURE 18. LARGE SIGNAL STEP RESPONSE (1V)

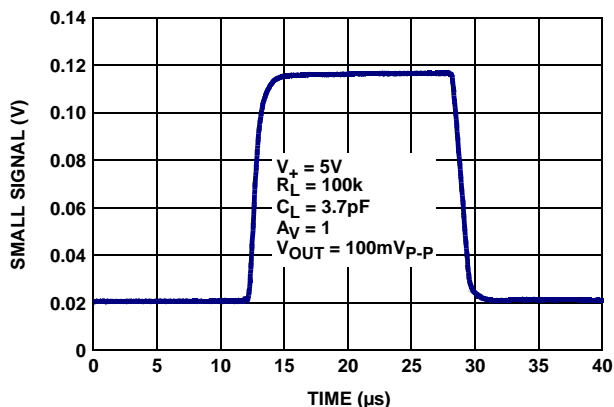


FIGURE 19. SMALL SIGNAL STEP RESPONSE (100mV)

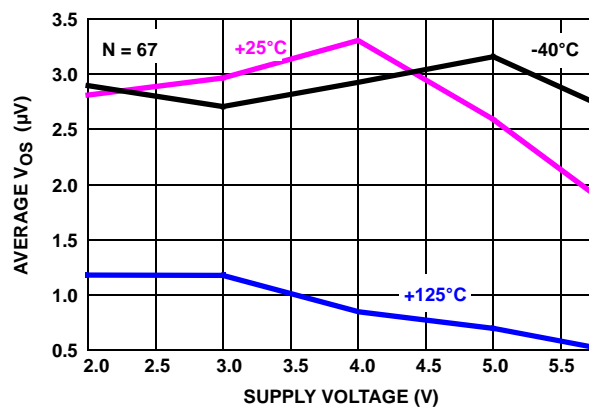


FIGURE 20. AVERAGE INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

## Typical Performance Curves

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ . (Continued)

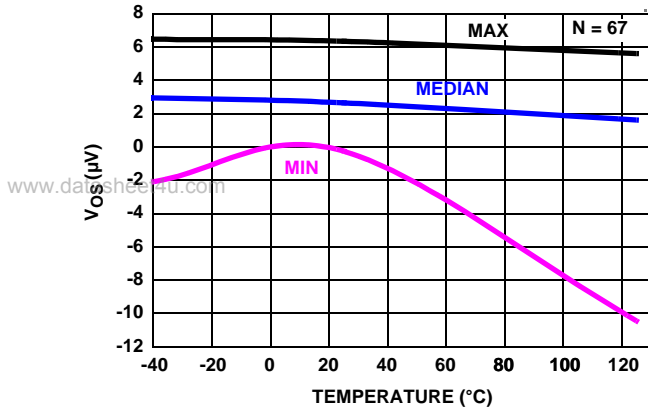


FIGURE 21.  $V_{OS}$  vs TEMPERATURE,  $V_S = \pm 1.0V$ ,  $V_{IN} = 0V$ ,  $R_L = \text{INF}$

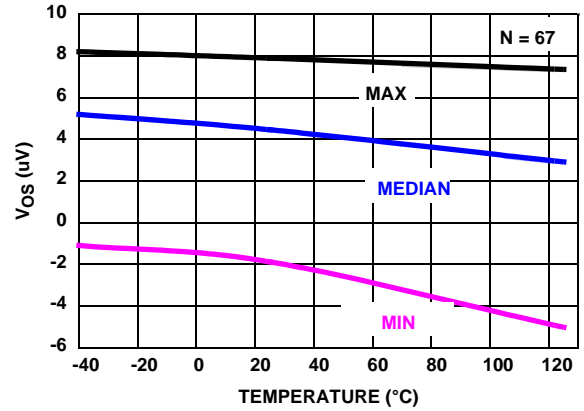


FIGURE 22.  $V_{OS}$  vs TEMPERATURE,  $V_S = \pm 2.5V$ ,  $V_{IN} = 0V$ ,  $R_L = \text{INF}$

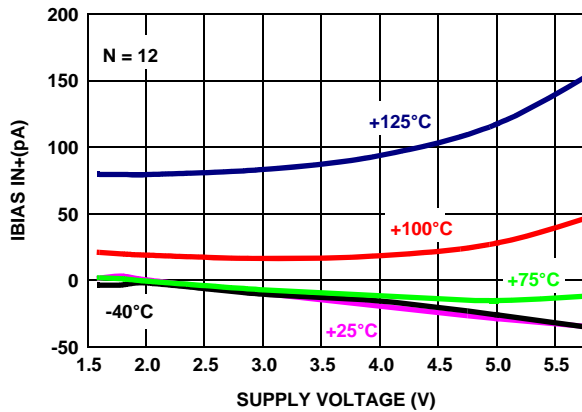


FIGURE 23. AVERAGE NON-INVERTING INPUT BIAS CURRENT vs SUPPLY VOLTAGE vs TEMPERATURE

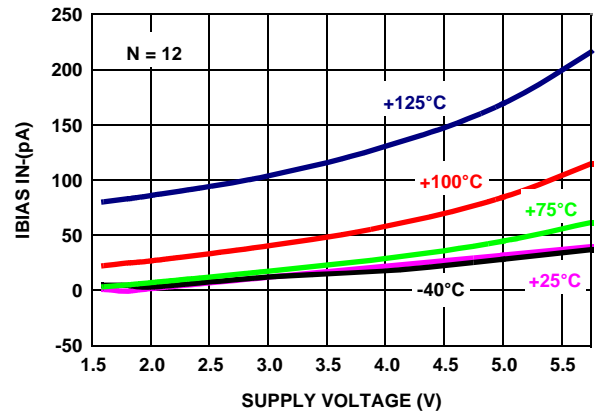


FIGURE 24. AVERAGE INVERTING INPUT BIAS CURRENT vs SUPPLY VOLTAGE vs TEMPERATURE

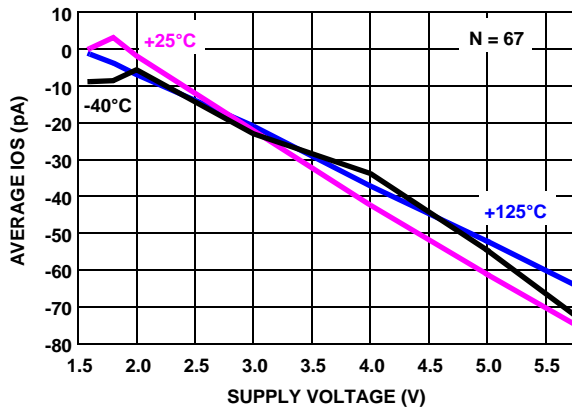


FIGURE 25.  $I_{OS}$  vs SUPPLY VOLTAGE vs TEMPERATURE

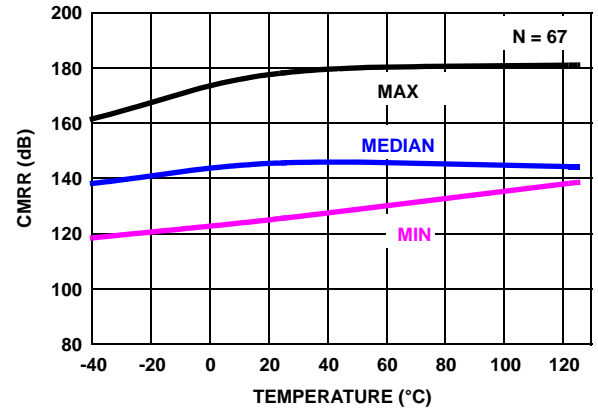


FIGURE 26. CMRR vs TEMPERATURE,  $V_{CM} = -2.5V$  TO  $+2.5V$ ,  $V_+ = \pm 2.5V$

## Typical Performance Curves

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ . (Continued)

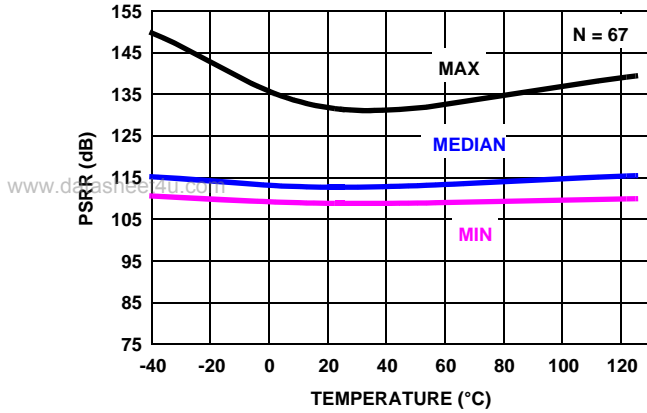


FIGURE 27. PSRR vs TEMPERATURE,  $V_+ = 2V$  TO  $5.5V$

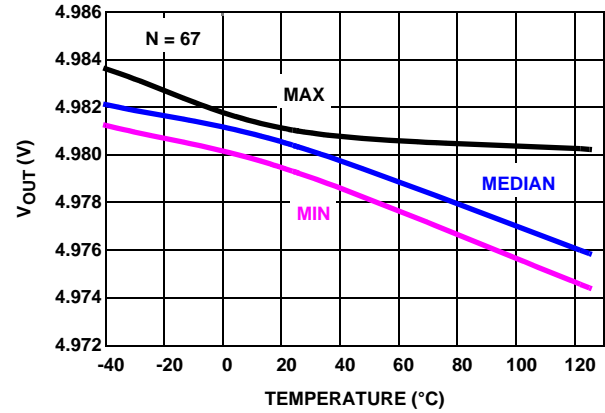


FIGURE 28.  $V_{OUT}$  HIGH vs TEMPERATURE,  $R_L = 10k$ ,  $V_S = \pm 2.5V$

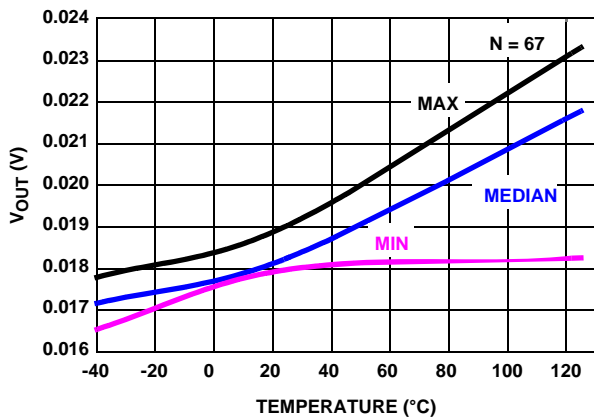


FIGURE 29.  $V_{OUT}$  LOW vs TEMPERATURE,  $R_L = 10k$ ,  $V_S = \pm 2.5V$

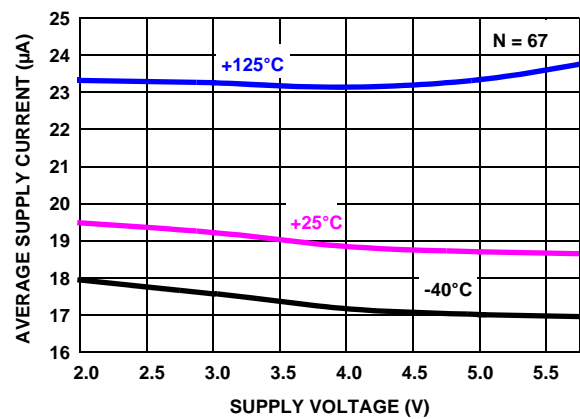


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

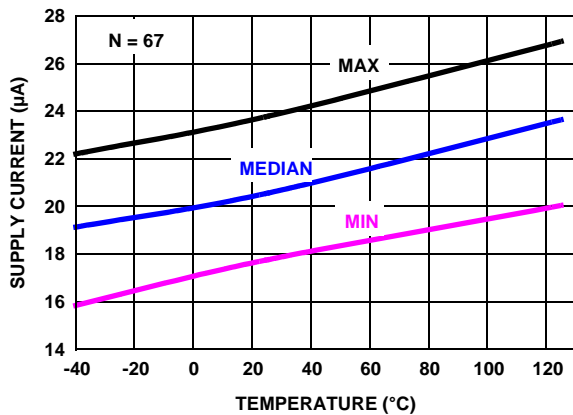


FIGURE 31.  $V_+$  SUPPLY CURRENT vs TEMPERATURE,  
 $V_S = \pm 0.8V$ ,  $V_{IN} = 0V$ ,  $R_L = \text{INF}$

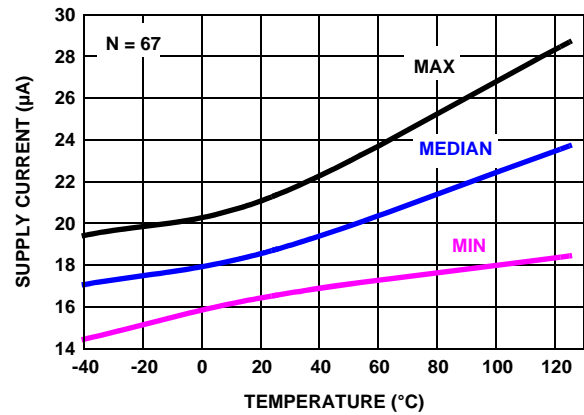


FIGURE 32.  $V_+$  SUPPLY CURRENT vs TEMPERATURE,  
 $V_S = \pm 2.5V$ ,  $V_{IN} = 0V$ ,  $R_L = \text{INF}$



## Typical Performance Curves

$V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ . (Continued)

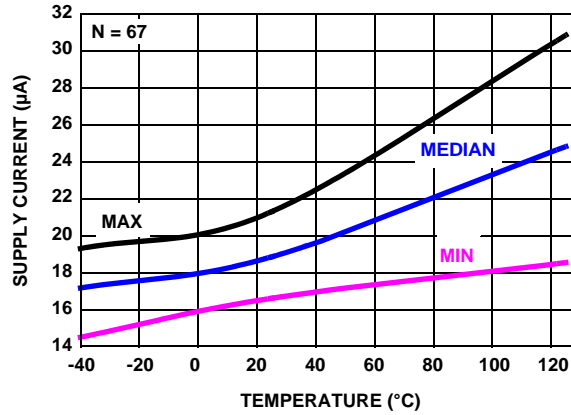


FIGURE 33.  $V_+$  SUPPLY CURRENT vs TEMPERATURE,  $V_S = \pm 3.0V$ ,  $V_{IN} = 0V$ ,  $R_L = \text{INF}$

## Pin Descriptions

ISL28133 (5 Ld SOT23)	ISL28133 (5 Ld SC70)	ISL28133 (6 Ld $\mu$ TDFN)	ISL28233 (8 Ld MSOP, 8 Ld TDFN)	ISL28433 (14 Ld TSSOP)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
3	1	4	3(A) 5(B)	3(A) 5(B) 10(C) 12(D)	IN+	Non-inverting input	<p>Circuit 1</p>
2	2	2	4	11	V-	Negative supply	
4	3	3	2(A) 6(B)	2(A) 6(B) 9(C) 13(D)	IN-	Inverting input	(See Circuit 1)
1	4	1	1(A) 7(B)	1(A) 7(B) 8(C) 14(D)	OUT	Output	<p>Circuit 2</p>
5	5	6	8	4	V+	Positive supply	
		5			NC	Not connected	Not internally connected

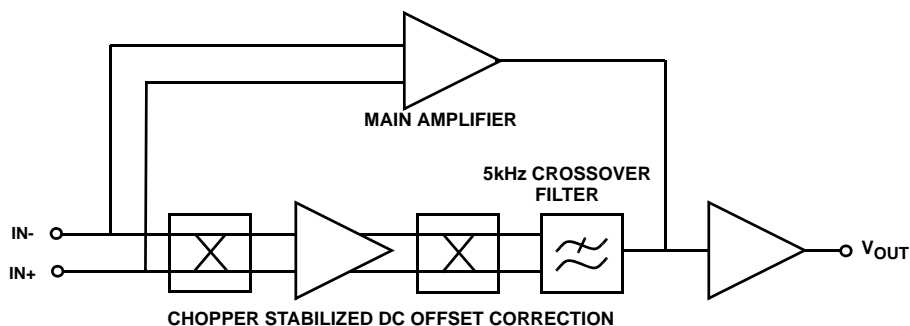


FIGURE 34. ISL28X33 FUNCTIONAL BLOCK DIAGRAM

## Applications Information

### Functional Description

The ISL28133 uses a proprietary auto-zero architecture (Figure 34) that combines a 400kHz main amplifier with a very high open loop gain (200dB) chopper stabilized amplifier to achieve very low offset voltage and drift ( $2\mu\text{V}$ ,  $0.02\mu\text{V}/^\circ\text{C}$  typical) while consuming only  $18\mu\text{A}$  of supply current per channel.

This multi-path amplifier architecture contains a time continuous main amplifier whose input DC offset is corrected by a parallel-connected, high gain chopper stabilized DC correction amplifier operating at 100kHz. From DC to  $\sim 5\text{kHz}$ , both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5kHz crossover filter cuts off the low frequency amplifier path leaving the main amplifier active out to the 400kHz gain-bandwidth product of the device.

The key benefits of this architecture for precision applications are very high open loop gain, very low DC offset, and low  $1/f$  noise. The noise is virtually flat across the frequency range from a few millihertz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency (5kHz).

### Rail-to-rail Input and Output (RRIO)

The RRIO CMOS amplifiers use parallel input PMOS and NMOS that enable the inputs to swing  $100\text{mV}$  beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and are capable of maintaining high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with  $17\text{mA}$  current limit and the capability to swing to within  $20\text{mV}$  of either rail while driving a  $10\text{k}\Omega$  load.

### IN+ and IN- Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications

where either input is expected to exceed the rails by  $0.5\text{V}$ , an external series resistor must be used to ensure the input currents never exceed  $20\text{mA}$  (Figure 35).

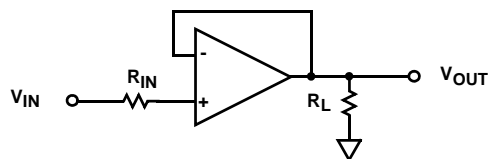


FIGURE 35. INPUT CURRENT LIMITING

### Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28X33 amplifiers, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 36 shows how the guard ring should be configured. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well.

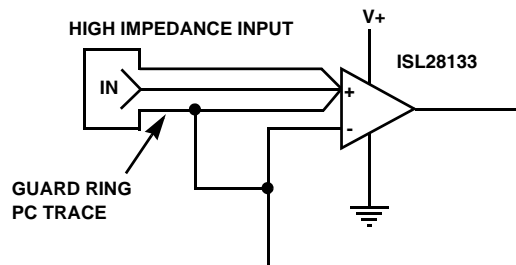


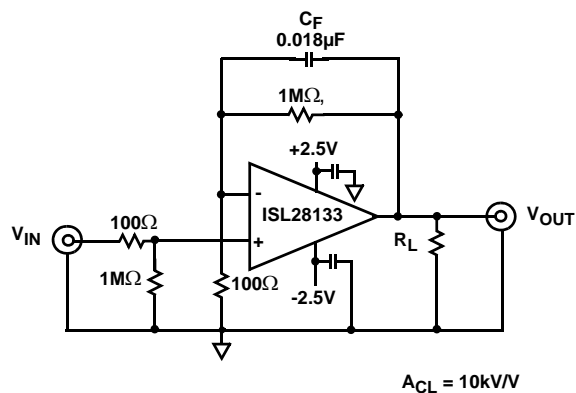
FIGURE 36. USE OF GUARD RINGS TO REDUCE LEAKAGE

### High Gain, Precision DC Coupled Amplifier

The circuit in Figure 37 implements a single-stage DC coupled amplifier with an input DC sensitivity of under  $100\text{nV}$  that is only possible using a low VOS amplifier with high open loop gain. High gain DC amplifiers operating from low

voltage supplies are not practical using typical low offset precision op amps. For example, the typical  $\pm 100\mu\text{V}$   $V_{OS}$  and offset drift  $0.5\mu\text{V}/^\circ\text{C}$  of a low offset op amp would produce a DC error of  $>1\text{V}$  with an additional  $5\text{mV}/^\circ\text{C}$  of temperature dependent error making it difficult to resolve DC input voltage changes in the micro-volt range.

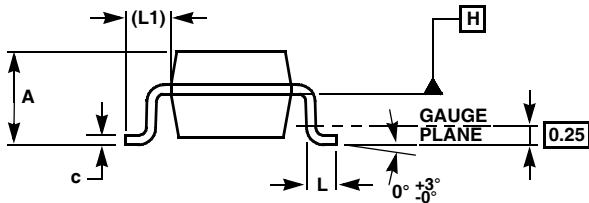
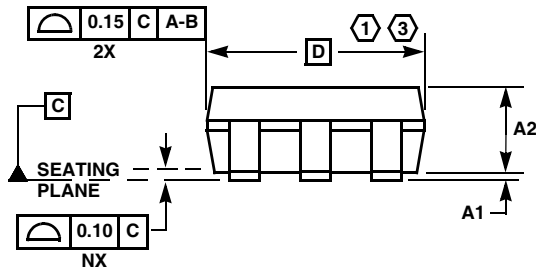
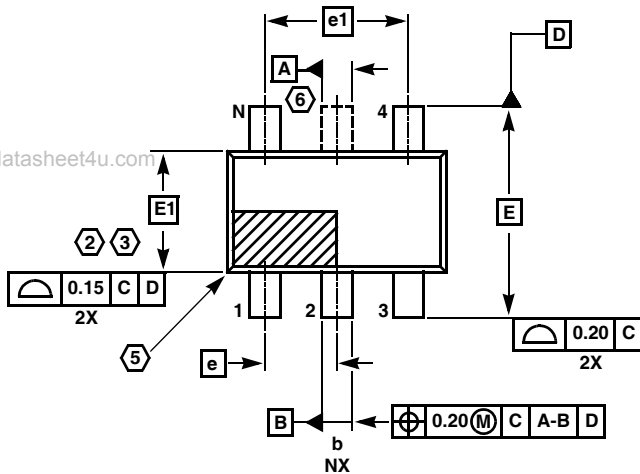
The  $\pm 8\mu\text{V}$  max  $V_{OS}$  and  $0.075\mu\text{V}/^\circ\text{C}$  of the ISL28133 produces a temperature stable maximum DC output error of only  $\pm 80\text{mV}$  with a maximum temperature drift of  $0.75\mu\text{V}/^\circ\text{C}$ . The additional benefit of a very low  $1/f$  noise corner frequency and some feedback filtering enables DC voltages and voltage fluctuations well below  $100\text{nV}$  to be easily detected with a simple single stage amplifier.



**FIGURE 37. HIGH GAIN, PRECISION DC COUPLED AMPLIFIER**

# SOT-23 Package Family

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## MDP0038

### SOT-23 PACKAGE FAMILY

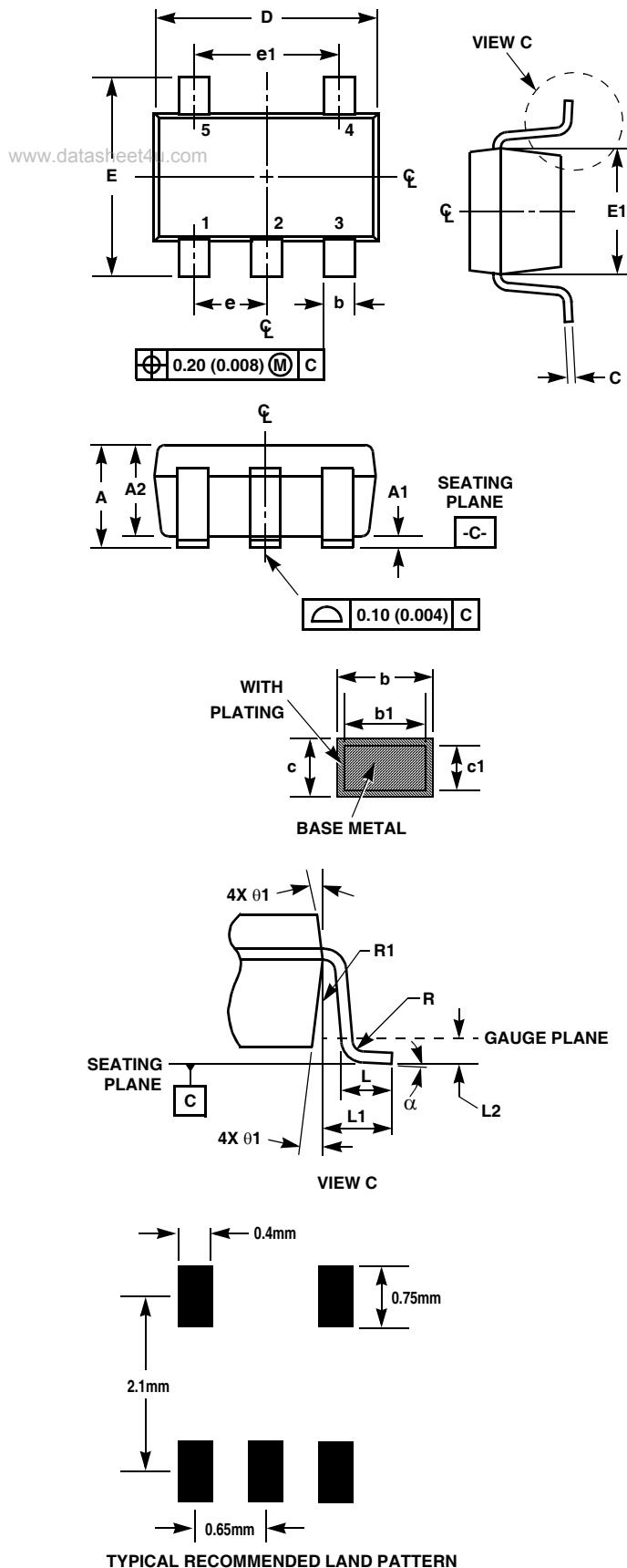
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

#### NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

# Small Outline Transistor Plastic Packages (SC70-5)



## P5.049

### 5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	-
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		-
α	0°	8°	0°	8°	-
N	5		5		5
R	0.004	-	0.10	-	-
R1	0.004	0.010	0.15	0.25	-

Rev. 3 7/07

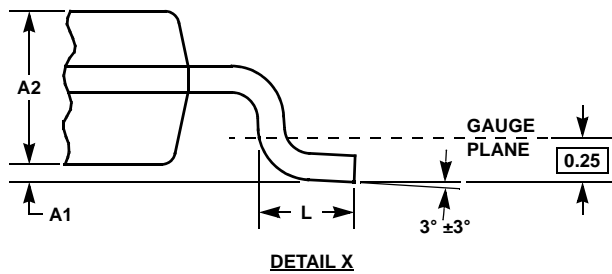
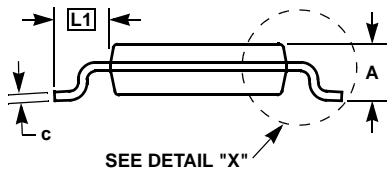
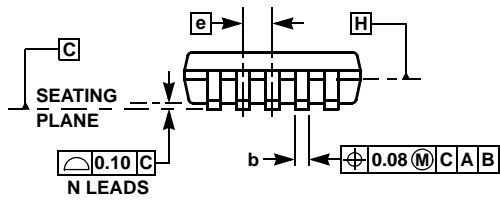
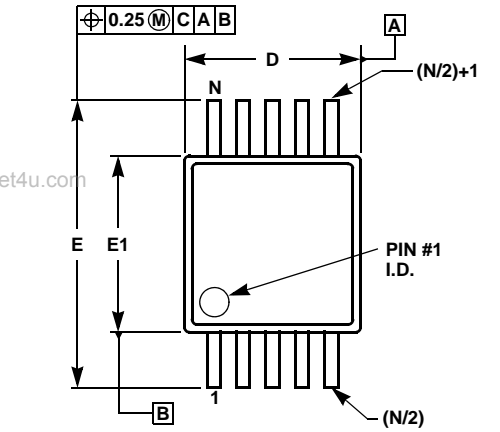
#### NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.



# Mini SO Package Family (MSOP)

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## MDP0043

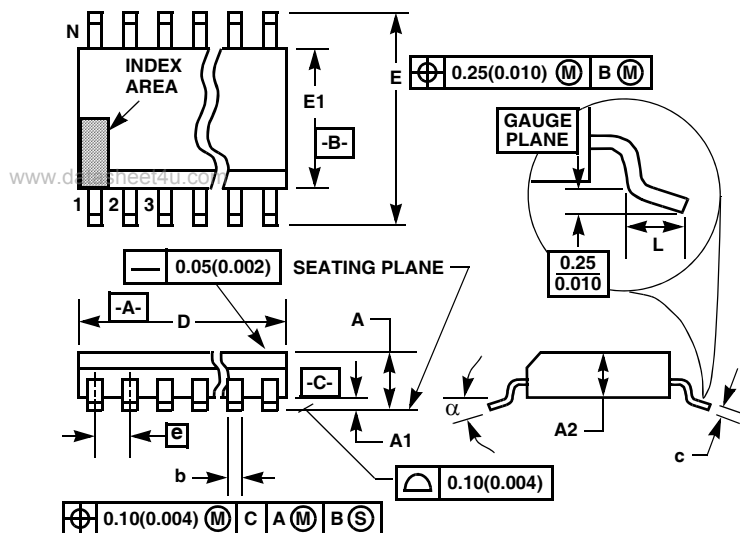
### MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

#### NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

**Thin Shrink Small Outline Plastic Packages (TSSOP)****NOTES:**

- These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

**M14.173****14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0°	8°	0°	8°	-

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