mosaic
semiconductor, inc.

11403 West Bernado Court, Suite 100, San Diego, CA 92127.
Tel No: (619) 674 2233, Fax No: (619) 674 2230

1M x 32 SRAM MODULE

PUMA 84S32000 - 70/85/10

Issue 2.1 : January 1999

Description

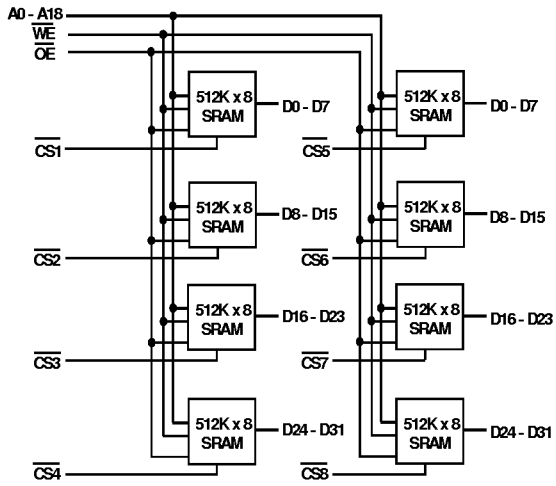
The PUMA 84S32000 is a 32Mbit CMOS Static RAM organised as 1M x 32 in a JEDEC 84 pin surface mount J-leaded PLCC, available with access times of 70, 85, and 100ns. The output width is user configurable as 8, 16 or 32 bits using eight Chip Selects ($\overline{CS1}$~8).

The PUMA 84S32000 offers a dramatic space saving advantage over eight standard 512Kx8 devices. The -L version has data retention capability and can be used in battery backup applications.

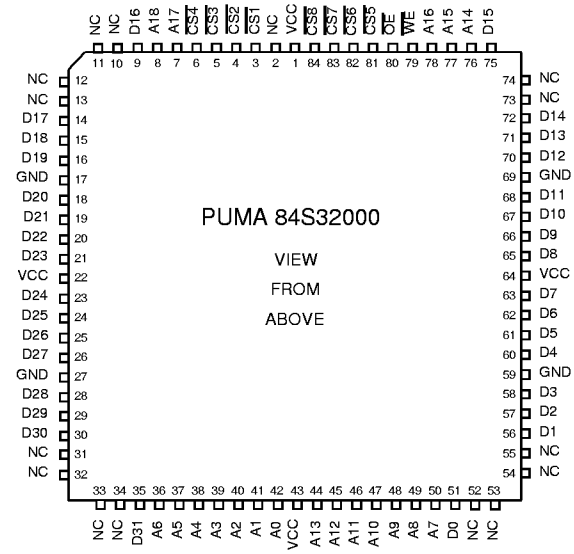
Features

- Access times of 70/85/100 ns.
- High Density Package
- JEDEC 84 'J' leaded plastic Surface Mount Package.
- Single 5.0 V±10% Power supply.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power (32-BIT) 2.51 W (max)
  Low Power Standby (-L) 8.25 mW (max)
- Fully Static operation.
- Data Retention Capability (-L version only).
- Multiple ground pins for maximum noise immunity.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 ~ A18**
Data Input/Output	**D0 ~ D31**
Chip Select	**$\overline{CS1}$ ~ 8**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
No Connect	**NC**
Power (+5V)	**V_{cc}**
Ground	**GND**

Package Details

Plastic 84 J-Leaded JEDEC PLCC

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Voltage on any pin relative to GND	V_T	-0.3V to 7.0	V
Power Dissipation	P_T	4.5	W
Storage Temperature	T_{STG}	-55 to +125	℃

Notes (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*Units*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
Input Low Voltage	V_{IL} (1)	-0.3	-	0.8	V	
Operating Temperature	T_A	0	-	70	℃	
	T_{AI}	-40	-	85	℃	(Suffix **I**)

Notes: (1) Pulse width: -3.0V for less than 40ns.

DC Electrical Characteristics (V_{CC}=5V±10%,T_A=-40°C to +85°C)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current		I_{LI1}	V_{IN}=0V to V_{CC}	-8	-	8	µA
Output Leakage Current		I_{LO}	$V_{I/O}$=0V to V_{CC}	-8	-	8	µA
Operating Supply Current(2)	32 bit	I_{CC32}	Cycle time = min 100% duty $I_{I/O}$=0mA				
			CS=V_{IL} V_{IN} = V_{IH} or V_{IL}	-	-	456	mA
	16 bit	I_{CC16}	As above.	-	-	244	mA
	8 bit	I_{CC8}	As above.	-	-	138	mA
Standby Supply Current	(TTL)	I_{SB}	$\overline{CS}$(1)=V_{IH}, V_{IN}=V_{IL}or V_{IH}	-	-	32	mA
-L Version	(CMOS)	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V,Other inputs = 0~V_{CC}	-	-	2	mA
Output Voltage Low		V_{OL}	I_{OL} = 2.1mA,V_{CC}=Min	-	-	0.4	V
Output Voltage High		V_{OH}	I_{OH} = -1.0mA,V_{CC}=Min	2.2	-	-	V

Notes: (1) $\overline{CS1\sim4}$ or $\overline{CS5\sim8}$ inputs operate simultaneously for 32 bit mode.

Capacitance (V_{CC}=5V, T_A=25°C, F=1Mhz)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Capacitance Address,$\overline{OE}$,$\overline{WE}$	C_{IN1}	V_{IN}=0V	-	-	64	pF
Output Capacitance 8-bit mode (worst case)	$C_{I/O}$	$V_{I/O}$=0V	-	-	80	pF

Note: These parameters are calculated, not measured.

AC Test Conditions

*Input pulse levels: 0.8V to 2.4V

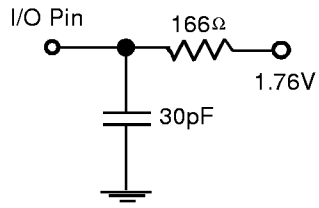
*Input rise and fall times: 5 ns

*Input and Output timing reference levels: 1.5V

*V_{cc}=5V±10%

*PUMA module is tested in 32 bit mode.

Output Load



Operation Truth Table

Below is the truth table which applies to each individual SRAM on the module. When operating the module care should be taken to prevent any two SRAM components which are connected to the same data byte from driving the bus simultaneously. This will prevent bus contention occurring on the module. Please refer to the block diagram on the front page of this datasheet.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*V_{cc} Current*	*I/O Pin*	*Reference Cycle*
Not Selected	1	X	X	I_{SB1},I_{SB2}	High Z	Power Down
Output Disable	0	1	1	I_{CC1}	High Z	
Read	0	0	1	I_{CC1}	D_{OUT}	Read Cycle
Write	0	X	0	I_{CC1}	D_{IN}	Write Cycle

1 = V_{IH}, 0 = V_{IL}, X = Don't Care

Low V_{CC} Data Retention Characteristics - L version only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$=V_{CC}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1} (1)	V_{CC} = 3.0VA, $\overline{CS}$ > V_{CC}-0.2V, V_{IN} >0V	-	-	1.5	mA
Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

AC OPERATING CONDITIONS

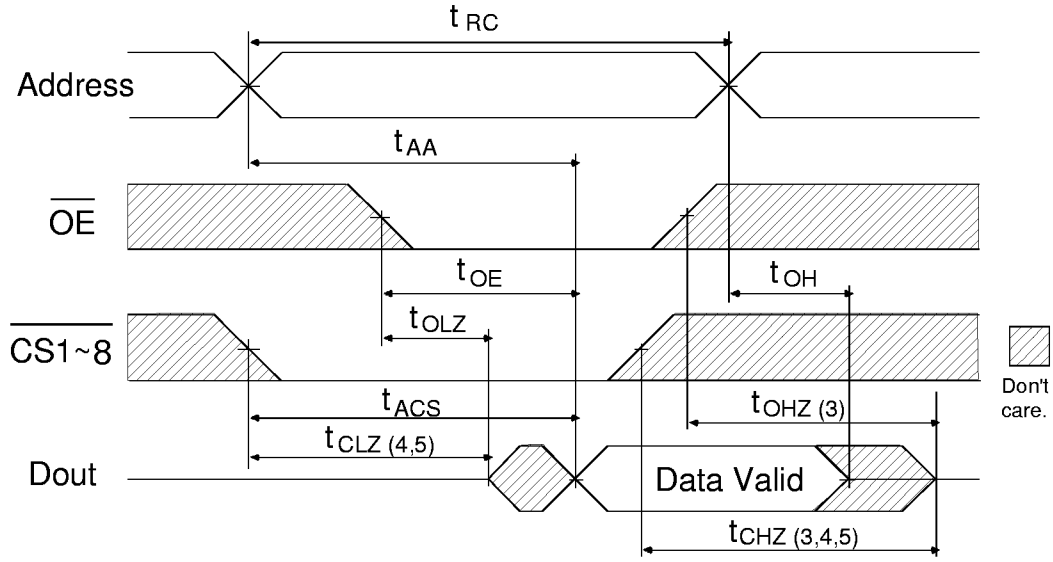
Read Cycle

		70		85		10		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Units*
Read Cycle Time	t_{RC}	70	-	85	-	100	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	ns
Chip Select Access Time	t_{ACS}	-	70	-	85	-	100	ns
Output Enable to Output Valid	t_{OE}	-	35	-	45	-	50	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	15	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns
Output Disable to Output in High Z	t_{OHZ}	0	25	0	25	0	30	ns
Chip Disable to Output in High Z	t_{CHZ}	0	25	0	25	0	30	ns
Chip Enable to Output in Low Z	t_{CLZ}	10	0	10	0	10	0	ns

Write Cycle

		70		85		10		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Units*
Write Cycle Time	t_{WC}	70	-	85	-	100	-	ns
Chip Selection to End of Write	t_{CW}	60	-	70	-	80	-	ns
Address Valid to End of Write	t_{AW}	60	-	70	-	80	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	50	-	60	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	30	-	35	-	40	-	ns
Output Active from End of Write	t_{OW}	3	-	3	-	3	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Write to Output High Z	t_{WHZ}	0	25	0	25	0	30	ns

Read Cycle Timing Waveform [1,2]



AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

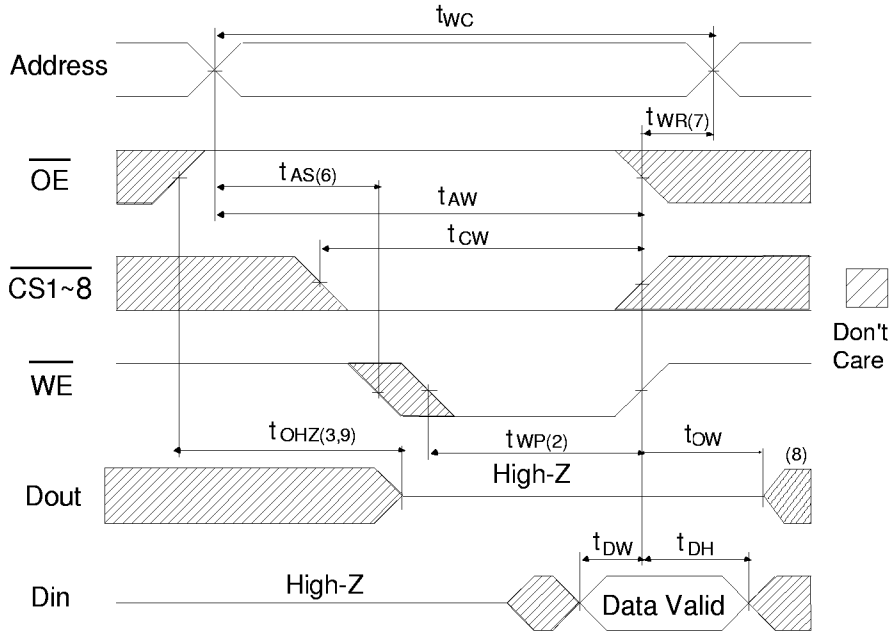
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

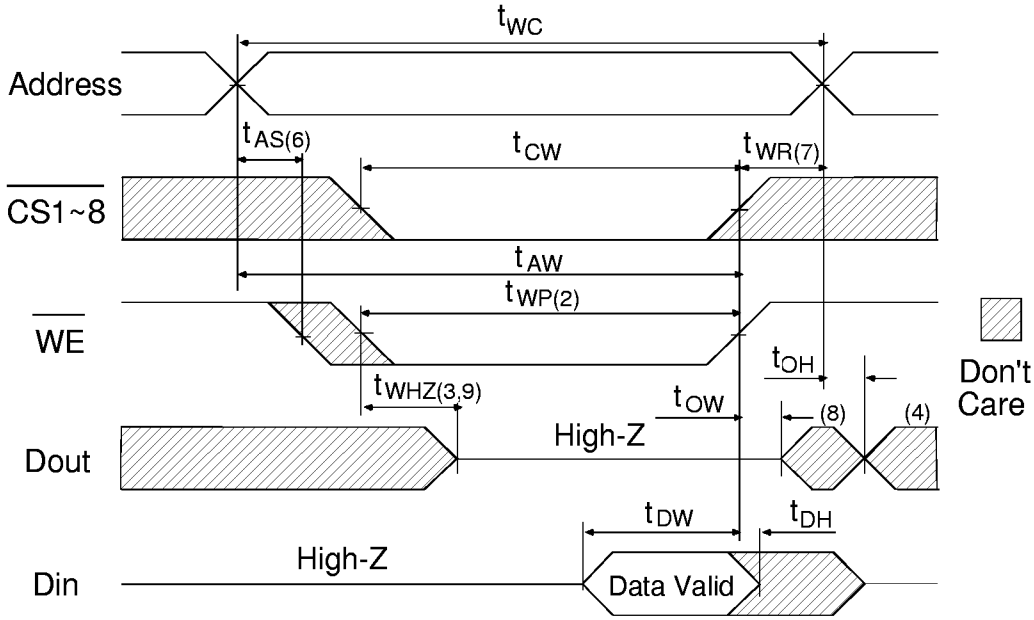
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform [1,4]



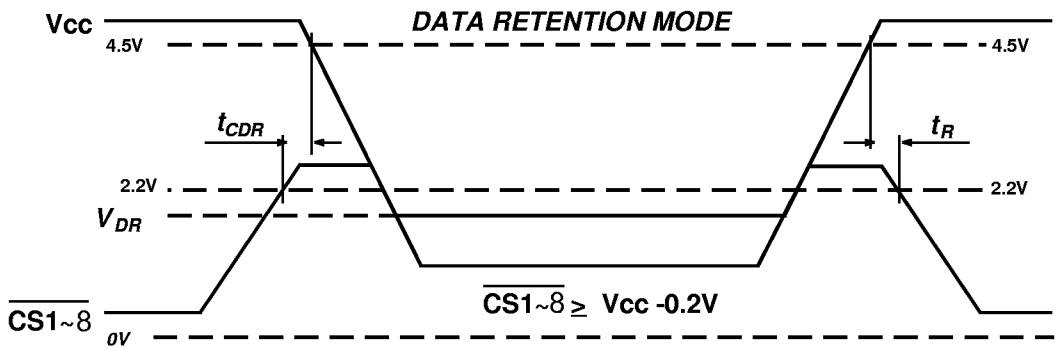
Write Cycle No.2 Timing Waveform (1,5)



AC Write Characteristics Notes

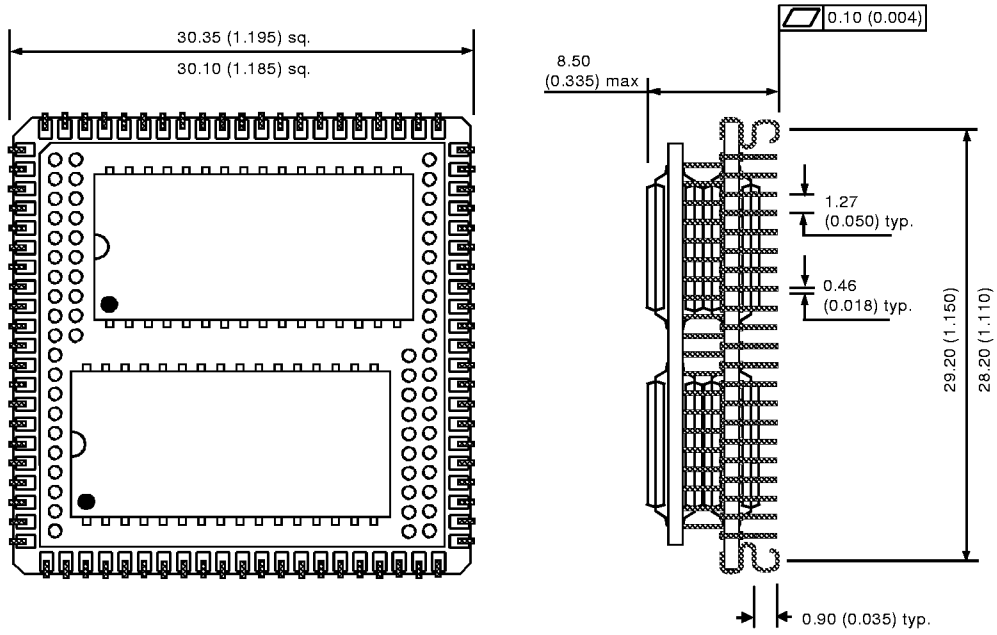
(1) All write cycle timing is referenced from the last valid address to the first transition address.
(2) All writes occur during the overlap of $\overline{CS1\sim8}$ and $\overline{WE}$ low.
(3) If $\overline{OE}$, $\overline{CS1\sim8}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
(4) Dout is the Read data of the new address.
(5) $\overline{OE}$ is continuously low.
(6) Address is valid prior to or coincident with $\overline{CS1\sim8}$ and $\overline{WE}$ low, too avoid inadvertant writes.
(7) $\overline{CS1\sim8}$ or $\overline{WE}$ must be high during address transitions.
(8) When CS is low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Data Retention Waveform



Package Information Dimensions in mm(inches)

Plastic 84 Pin JEDEC Surface mount PLCC



Ordering Information

PUMA 84S32000LI - 70

Speed	70	=	70 ns
	85	=	85 ns
	10	=	100 ns
Temperature Range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
Power Consumption	Blank	=	Standard
	L	=	Low Power
Organisation	32000	=	1M x 32 SRAM configurable as 2M x 16 and 4M x 8
Memory Type	S	=	Asynchronous SRAM 5V
Package	PUMA 84	=	Memory Stack 84 pin 'J' Leaded

Note :

Although this data is believed to be accurate, the information contained herein, is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.

Our products are subject to a constant process of development. Data may be changed at any time without notice.

Products are not authorised for use as critical components in life support devices without the express approval of a company director.