T-42-05
1.1

CELL FAMILY ARCHITECTURE

The CAB Standard Cells are designed in a 1.25μ double-metal, single-poly, twin-tub CMOS process using p- wafer starting material. They are intended primarily for 5V (± 10%) applications but will operate between 2.5V and 5.5V.

Cell layout has been done using Gould's Silicon Compiler cell generator development system (SCORE). All physical, electrical, and simulation data are automatically generated by the system. The cells are designed such that when they are abutted and interconnect is placed on a grid, no design rule violations will occur. Note that a GDS-II version of the cell layouts has been automatically generated and is available for use with STREAM-type systems.

1.1.1 Library Options

Four separate libraries are contained in sections later in this book. Cells from these libraries can be used together in the same design. Basic Functions contains cell types from simple inverters to decoders, multiplexers, and counters. The Basic Function library should be chosen and supplemented by Interface Functions, MSI Functions, and 7400 Functions.

Core Cells are the gates, flip-flops, MSI functions, amplifiers, ect. that are used to accomplish the desired circuit function. Vdd and Vss are routed horizontally in metal-1 through the cell near the top and bottom. In metal-2, all signal input and output lines enter or exit the cell along both the top and bottom.

Pad cells are used to interface the core circuits to the outside world. Included in these cells are input buffers, output buffers, I/O buffers, power pads, ect. There are several types of pad cells for each input or output function. Each pad cell offers a fixed height, variable width design.

Vdd and Vss are routed horizontally through each pad cell in metal-2. These power lines are much more substantial than those found in the core cells, as they must conduct the current required by numerous banks of core cells as well as the pad cells. Unlike the core cells, the signal I/O is routed into or out of the cell in metal-1. The pad cells' signal I/O is found only on the interior side of the cell.

Table 1–1
LIBRARY FUNCTIONS AND USAGE

LIBRARY	SECTION	USAGE
BASIC FUNCTIONS	2	Use with any other library
INTERFACE FUNCTIONS	3	Use with any other library
MSI FUNCTIONS	4	Use with any other library
7400 FUNCTIONS	5	Use with any other library

1.1.1.1 Basic Functions

This library contains functions that are relatively simple. The cells are designed for a variety of speeds and are optimized for minimum power and area.

1.1.1.2 Interface Functions

This library contains all of the cells which interface the circuit to the rest of the system, input cells, output cells, and I/O cells.

1.1.1.3 MSI Functions

These functions are made from cells (soft) in the Basic Function section and are more complex.

1.1.1.4 7400 Functions

Over 200 of the most popular standard parts used when designing with 7400 TTL components are contained here. These functions range from simple NAND gates to reasonably complex ALU's, comparators, and counter-registers. Look to this library when the design time is to be optimized and the designer is familiar with standard parts and system level design. Many of these cells are made by combining cells (soft) from the Basic Functions section.

1.1.2 Data Sheet Overview

For each Standard Cell circuit, there is a data sheet that contains all the information required to use the cell in an IC design. Included are:

- The *CELL NAME* (in the upper right-hand corner of the data sheet).
- A brief description of the cell *FUNCTION* and/or *FEATURES*.
- Two *AREA* figures of merit are included: the cell area relative to the area of the 2-input, speed 3, *NAND* gate (NA023) and *EQ.GATES*, which is the number of equivalent 2-input gates in the cell.
- The *BOLT SYNTAX* used to call the cell in the *BOLT* circuit description.
- The *TRUTH TABLE* description of the cell's logical function.
- The table of the *CAPACITIVE LOADS* presented by each of the cell's inputs. Capacitance information for 3-state cell outputs is also given. This data is used during timing analysis.
- A *LOGIC SYMBOL* drawing (to ensure standardized logic schematics).
- A table summarizing the cell's *AC PARAMETERS*. Data is included for 5.0V and 25°C operation with nominal process parameters. Derating curves are provided in Section 1.3.2.2 that make it possible to tailor this data to specific application environments.
- A *LOGIC SCHEMATIC* of the cell. A logic schematic is included for all complex cells.

Note: the following characteristics are discussed in Section 1.3, Interpreting the Data Sheets, voltage levels, power dissipation and DC characteristics of the I/O cell.

1.1.3 Package Availability

Table 1–2 lists the types of packages that are available from Gould. Table 1–3 indicates the thermal temperature coefficient for each package type, (see Section 1.3.6 for correct usage).

Table 1–2
GOULD PACKAGE OFFERING

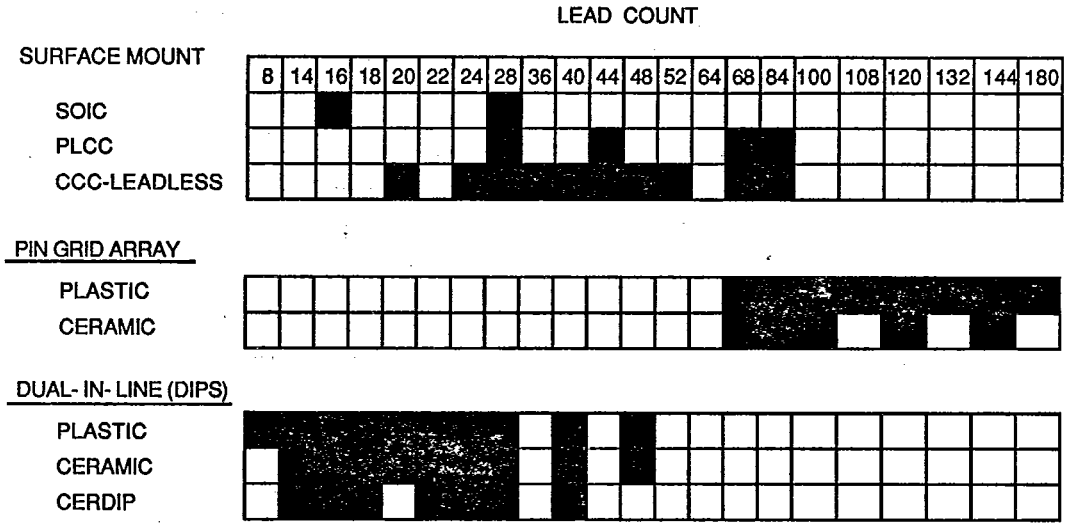

Table 1–3
THERMAL TEMPERATURE

	LEAD COUNT																				
SURFACE MOUNT	8	14	16	18	20	22	24	28	36	40	44	48	52	64	68	84	100	108	120	132	144	180
SOIC			71					68														
PLCC								58			53				45	42						
CCC-LEADLESS					62		58	56	49	46	44	41	39		33	27						
PIN GRID ARRAY																						
PLASTIC															–	–	–	–	–	–	–	–
CERAMIC															27	26	24		23		22	
DUAL- IN- LINE (DIPS)																						
PLASTIC	91	80	75	73	68	66	63	59		50		47										
CERAMIC		73	68	66	63	59	57	53		47		46										
CERDIP		96	87	80		66	58	49		44												

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