XR-1015/1016

Seventh Order Elliptic Low Pass Filters

EXAR ...the analog plus company™

September 1996-4

FEATURES

- Greater than 70 dB Stopband Rejection
- Operation at +5 VDC
- Precise Filter Positioning
- Low Power Consumption
- No External Components Required for Filter

APPLICATIONS

- General Purpose Filtering
- Anti-alias Filters (for analog-to-digital converters)
- Reconstruction Filters (for digital-to-analog converters)
- Band Limiting of Voice
- Digital Signal Processing Front End
- Filtering of Voice for Music for Special Effects (echo, phasing, etc.)

GENERAL DESCRIPTION

The XR-1015 and XR-1016 are seven pole and six zero elliptic low pass switched capacitor filters. The position of the passband of the filter is set by the frequency of the clock which allows for easy adjustment. The use of switched capacitor filters reduces the amount of variation in the filter response that occurs with discrete use of capacitors, inductors and resistors. The XR-1015 and XR-1016 also provide synchronized sampled inputs and outputs that allows the device to be cascaded without the need of an additional sample-and-hold. The XR-1015 and XR-1016 are produced with a 3 µm polysilicon gate dual metal CMOS process for low power consumption.

The XR-1015 is an eight pin device that can operate from +3 -2.0 VDC to ±5VDC. The device can also be biased so that it can be operated with a single +5 to +10 VDC supply. It is pin-for-pin compatible with the Reticon R5609 with the added advantage of operating to +5 VDC single supply. The clock to corner ratio of the XR-1015 is fixed at 100:1.

The XR-1016 is a 14 pin device which provides two uncommitted operational amplifiers for use as a reconstruction filter, anti-aliasing filters or for additional pre-filter gain. The XR-1016, as does the XR-1015, provides a clock output with the voltage output from rail to rail. The XR-1016 has the ability to change the clock to corner ratio from 100:1 to 50:1. The output clock can be used to strobe an analog-to-digital converter or to synchronize any additional circuits in the system.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1015CN	8 Lead 300 Mil CDIP	0°C to 70°C
XR-1015CP	8 Lead 300 Mil PDIP	0°C to 70°C
XR-1016CN	14 Lead 300 Mil CDIP	0°C to 70°C
XR-1016CP	14 Lead 300 Mil PDIP	0°C to 70°C
XR-1016CD	16 Lead 300 Mil JEDEC SOIC	0°C to 70°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

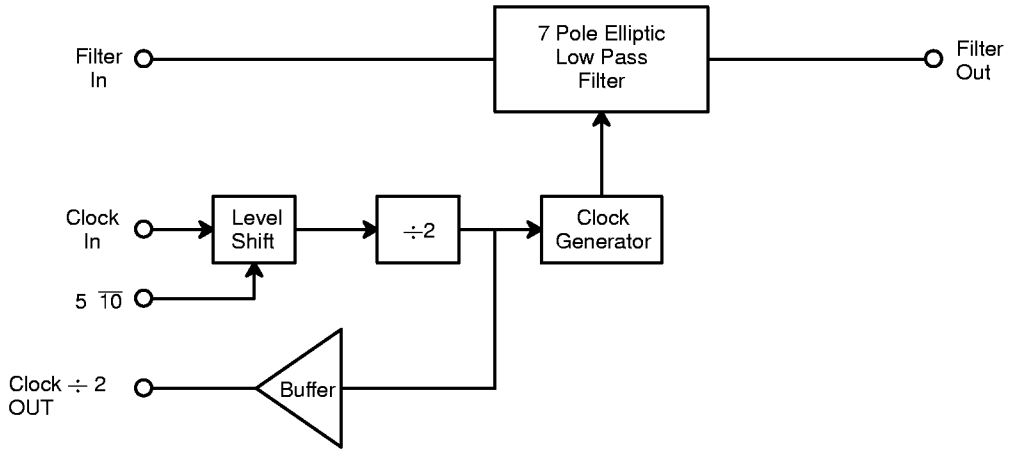
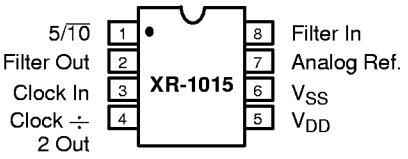
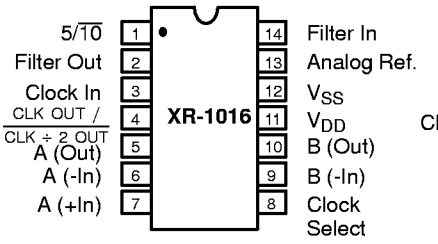


Figure 1. XR-1015 Block Diagram

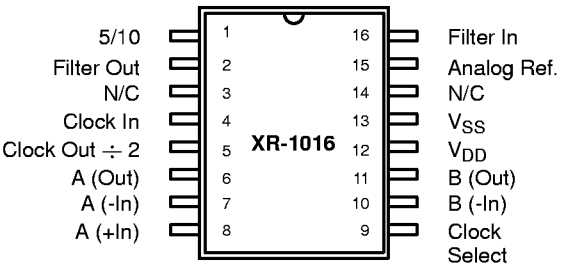
PIN CONFIGURATION



8 Lead PDIP, CDIP (0.300")



14 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

1015 Pin #	1016 Pin #	Symbol	Description
1	1	5/10	This controls the reference level of the internal level shifters of the XR-1015 or XR-1016 in order to determine the point at which the device considers the digital inputs to be a logic 1 or a logic 0. When this input is at V_{SS}, the decision level is at 2/3 of the sum of the magnitudes of the V_{DD} and V_{SS} levels relative to V_{SS}. When the 5/10 pin is tied high, then the decision level is set for 2/3 of the sum of the magnitudes of the V_{DD} and V_{SS} in voltage relative to V_{DD}. Table 1 shows some of the possibilities of the input logic thresholds. The level at pin 1 does not affect the clock output amplitude. This output is always from near V_{DD} to near V_{SS} in amplitude.
2	2	OUTPUT	The filter output. This output will drive a 10kΩ load. The signal will be centered around the voltage set by ANALOG REFERENCE.
3	-	CLOCKIN	The input clock is applied at this point. The input clock controls the position of the corner frequency of the filter using the ratio: $\frac{f_{CLOCK}}{f_{COMER}} = 100 : 1$ The logic threshold level needed at this point is controlled by pin 1, 5/10. Please see the pin description of 5/10 for details.
-	3	CLOCKIN	The input clock is applied to this point. The XR-1016 has an internal divider which provides either a clock to corner ratio of 100:1 or 50:1. This is controlled by pin 8 (CLOCK SELECT). If CLOCKIN is low, fclock/fcorner = 100:1.

V_{DD}/V_{SS}	Level at Pin 1	Logic Decision Level
+5/-5 VDC	-5 VDC	1.8 VDC
	+5	-1.8 VDC
+5/0 VDC	0	3.7 VDC
	+5	1.8 VDC
+2.5/-2.5 VDC	-2.5	1.2 VDC
	+2.5	-0.7 VDC
+10/0 VDC	0	6.8 VDC
	+10	3.2 VDC

Table 1.

PIN DESCRIPTION (CONT'D)

1015 Pin #	1016 Pin #	Symbol	Description
4	4	CLOCK/2	This output is the same frequency as the sampling frequency of the XR-1015 or XR-1016. It can be used to synchronize an analog-to-digital converter to the filter's output. The failing edge of the CLOCK/2 output is the edge which the output (pin 2) should be sampled in order to ensure that the output has settled.
-	5	A (OUT)	Operational amplifier A output. This is provided for creating additional filtering if desired. This output can drive a load of typically 10kΩ.
-	6	A (-INPUT)	Operational amplifier A negative input. This is a CMOS gate input with virtually infinite input impedance.
-	7	A (+INPUT)	Operational amplifier A positive input. This is a CMOS gate input with virtually infinite input impedance.
-	8	CLOCK SELECT	This pin on the XR-1016 will select the clock to corner ratio of the filter. When this pin is at logic 0, the filter will have a clock to corner of 100:1. When this pin is tied to a logic 1, the clock to corner ratio will be 50:1. The CLOCK/CLOCK÷2 will always represent the sampling frequency of the XR-1016. The logic level control of this digital input is controlled by pin 1 5/10 as described under that pin description.
-	9	B (-INPUT)	Operational amplifier B negative input. Notice that the positive input of this operational amplifier 8 is tied internally to the ANALOG REFERENCE.
-	10	B (OUT)	Operational amplifier B output.
5	11	V_{DD}	Positive supply input. The range of voltages of this point is from +2.5 VDC to +5 VDC when used with dual supplies of equal magnitude. If a single supply is used, the range is from +5 VDC to +10 VDC. It is recommended that a 0.47µF capacitor be tied from this pin to ground to decouple the noise on the supply line which can degrade the performance of the filter. If very low clock frequencies are used, then the size of the capacitor should be increased to keep the noise on the supply at a minimum. This capacitor should be located as close to the V_{DD} pin as possible. It is suggested that a 10Ω resistor from the positive supply to V_{DD} be used to filter system supply noise from the filter.
6	12	V_{SS}	Negative supply input. The range of the input is from -5 VDC to 0 VDC depending on the voltage present at V_{DD}. It is recommended that the pin be decoupled with a 0.47µF capacitor located as physically close as possible to the V_{SS} pin and tied from V_{SS} to ground. It is recommended that a 10Ω resistor from the negative supply to V_{SS} be used to filter system supply noise from the filter.
7	13	ANALOG REF.	This pin provides the level at which the analog signals will be referenced. If equal split supplies are used, then this point is tied to ground. If unequal supplies or a single supply is used, then this point should be tied to a resistor divider circuit to provide a voltage at the analog reference pin that is 1/2 of the algebraic sum of the two supplies. Since this point is used as analog ground inside the device, it is recommended that a 0.47µF capacitor be tied from this pin to ground. As with the V_{DD} and V_{SS} decoupling, the size of this capacitor should be made larger if the clock frequency is decreased.
8	14	FILTER IN	Filter input: The signal that needs to be filtered is applied to this point. It has an input impedance of 4MΩ at 1MHz clock frequency. It should be noted that any signal applied to this input greater than 1/2 of the sampling frequency will be aliased into the band of interest.

ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = 5 VDC, V- = -5 VDC, f_{CLOCK} = 2MHz, R_L = 1 MΩ, C_L = 40pF, T_A = 25°C Unless Otherwise Specified.

Symbol	Parameters	XR-1015			XR-1016			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
General Characteristics									
	Supply Voltage								
	Single Supply	5		10.5				V	See *Figure 2.*
					5		10.5	V	See *Figure 4.*
	Split Supply	+3, -2		15.25				V	See *Figure 3.*
					+3, -2		±5.25	V	See *Figure 5.*
	Supply Current								
	Single Supply		10	11				mA	See *Figure 2.*
						10	11	mA	See *Figure 4.*
	Split Supply								
	Positive		10	12				mA	See *Figure 3.*
	Negative		10	12				mA	
	Positive					10	12	mA	See *Figure 5.*
	Negative					10	12	mA	
Filter Section									
f_{CLOCK}	Upper Frequency Limit	2	2.5					MHz	See *Figure 3.*
					2	2.5		MHz	See *Figure 5.*
$f_{CLOCKMIN}$	Lowest Practical		1					kHz	See *Figure 3.*
							1	kHz	See *Figure 5.*
	Input Impedance								
	Pin 8		1					mΩ	See *Figure 3.*, f_{CLOCK} = 1MHz
	Pin 14					1			See *Figure 5.* f_{CLOCK} = 1MHz
tpw	Minimum f_{CLOCK} Pulse Width	200						ns	See *Figure 3.*
					200			ns	See *Figure 5.*
THD	Total Harmonic Distortion								V_{IN} = 2 Vpp
			0.02%			0.02%			f_{CLOCK} = 500kHz
			0.1%			0.1%			f_{CLOCK} = 2MHz
	Clock Feedthrough		30			30		mVpp	
V_{INMAX}	Maximum Input Voltage			8			8	Vpp	Above which distortion increases.
	Corner Freq. Accuracy		±0.5	±1		±0.5	±1	%	f_{CLOCK} = 2MHz

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameters	XR-1015			XR-1016			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
A_V	Passband Gain	-0.5	0	+0.5	-0.5	0	+0.5	dB	Tested at f_{IN} = 293Hz, 3.9kHz, 8.6kHz, 12.1kHz
		-1	0	+1	-1	0	+1	dB	Tested at f_{IN} = 15.3kHz, 17.1kHz
	Ripple Passband		±0.1			±0.1		dB	f_{CLOCK} = 500kHz
			±0.5	1		±0.5	1	dB	f_{CLOCK} = 2MHz
V_{OS}	Voltage Offset	-0.5	-0.2	+0.5	-0.5	-0.2	+0.5	VDC	
	Output Noise		0.6			0.6		mVrms	1Hz-20Hz, *Figure 9.*
Operation Amplifier									
	Unity Gain Bandwidth		1.2			1.2		MHz	
CMRR	Common Mode Rejection Ratio (2 Vpp Input)		50			50		dB	
V_{IO}	Input Offset Voltage	-30		30	-30		30	mV	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 14V
Input Signal Level . . . . . V+ +0.3 to V- ±0.3V
Power Dissipation - XR-1016 (Package Limitation) . .
Ceramic Package 1000mW
Derate Above T_A = +25°C . . . . . 6mW/°C
Plastic Package 800mW
Derate Above T_A = +25°C . . . . . 7mW/°C
Power Dissipation - XR-1015 . . . . . .
Ceramic Package 385mW
Derate Above T_A = +25°C . . . . . 8.3mW/°C
Plastic Package 300mW
Derate Above T_A = +25°C . . . . . 8.3mW/°C
Storage Temperature . . . . . -55°C to +150°C

SYSTEM DESCRIPTION

The XR-1015 and XR-1016 General Purpose Seventh Order Elliptic Switched Capacitor Low Pass Filters are usually used as the first or last stage in any sampled signal system.

Any signal from the -3dB point of the low pass response to 1/2 of the sampling frequency (1/4 of the clock frequency) will be attenuated by typically 75dB, referenced to the passband. This allows its use with analog-to-digital converters to prevent the A-to-D from aliasing signals that are above 1/2 of the sampling frequency of the analog-to-digital converter. A simple second order active filter can be used in front of the XR-1015 or XR-1016 if it is known that some input signals will be above the Nyquist frequency of the XR-1015 or XR-1016.

The reverse of the above circuit can be used for digital-to-analog converters, to prevent the sampling frequency from causing difficulties with other stages in the system.

Application Information

The XR-1015 and XR-1016 are fabricated in P-well CMOS. This uses a N-substrate and requires the V_{DD} to be applied first before V_{SS} in order to prevent latchup of the device.

In addition to the above caution, the input signals should not be applied above the power supply levels, to prevent latchup. The same is true of the input clock.

The input signal should not have any traces or wires near the clock or other system clocks. The same is true of the output. This will help to reduce the clock feedthrough and provide measurements equal to the datasheet values, or better.

PRINCIPLES OF OPERATION

The XR-1015 and XR-1016 are switched capacitor filters with seven poles and six zeros with an elliptic response. With the elliptic response of the filter, the stop band rejection is greater than 75dB. The elliptic filter response is called an equal-ripple response, where the ripple in the stop band is an approximation of the ripple in the pass band. In this way the rolloff of the filter response is very fast as shown in *Figure 6.*

The use of zeros to obtain the stop band attenuation does cause some change in the linearity of the group delay of the elliptic filter. The rapid change in group delay occurs near the corner frequency as shown in *Figure 7.* This would only be a factor in situations where the output signal must not be delayed by different times for different input frequencies. For applications where the distortion of the phase information is important, the corner frequency of the filter can be placed higher in frequency so that the linear portion of the group delay response of the filter can be located within the information band.

Since the XR-1015 and XR-1016 are sample data filters in that they divide the continuous time signal into an amount of charge at a given time, certain limitations must be made on the signals placed on the input of the filters. The frequency of the signal applied to this input must have a period so that at least two samples of the signal are made during the period of the signal. This is true even if the signal is in the stop band response of the filter. The reason for this is that it would take a minimum of two samples of the frequency being applied to establish the period of the signal as well as an approximation of the amplitude. If this sampling criteria is not followed, then the output of the filter will be an aliased signal of the input since the period of the signal would be not accurately known and the frequency would not be known.

If this situation may occur, a simple second order filter can be added to the input. With the XR-1016, operational amplifier A could be used to create this filter. The precision of the location of the corner frequency of the filter is not critical in this situation so that precision resistors and capacitors would not be needed.

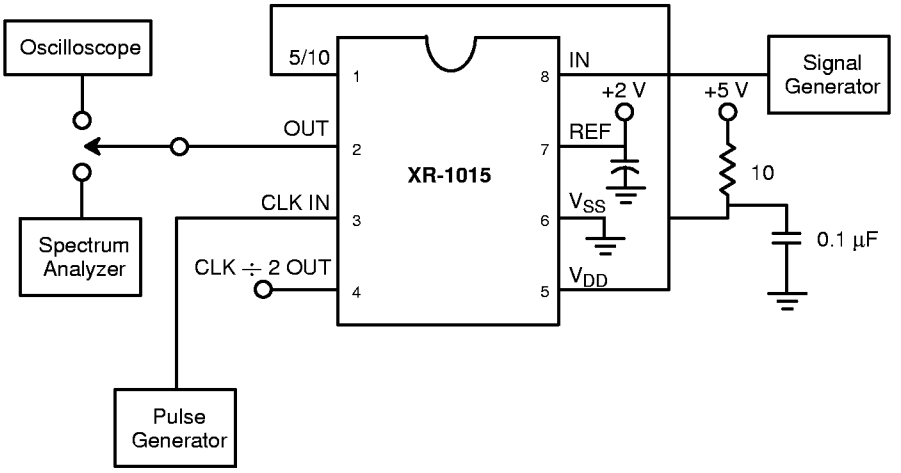


Figure 2. XR-1015 Test Circuit: 5 V Operation (V_{DD} = +5 V, V_{SS} = 0 V, Ref = +2 V)

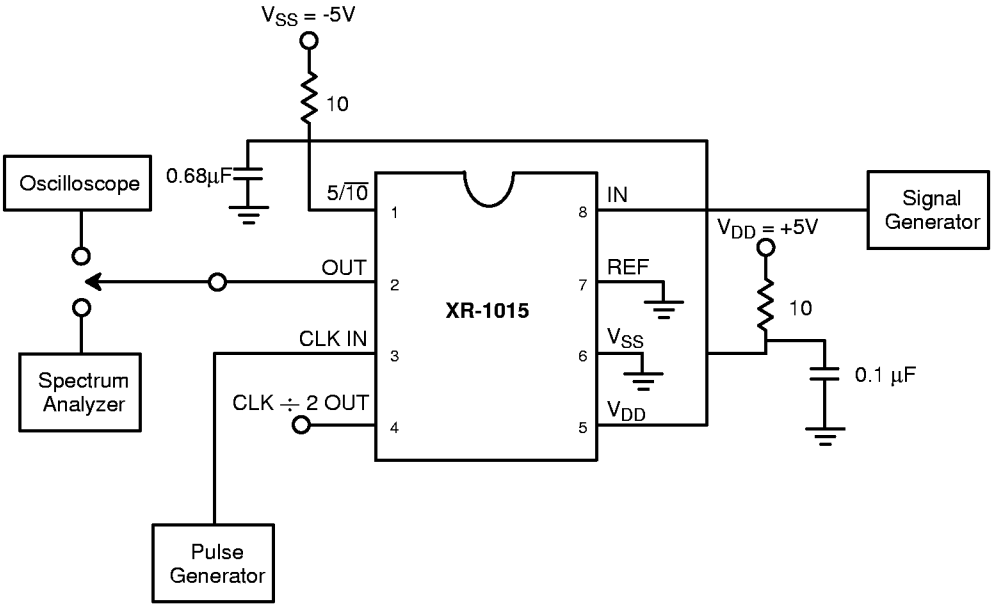


Figure 3. XR-1015 Test Circuit: 10 V Operation (V_{DD} = +5 V, V_{SS} = -5 V)

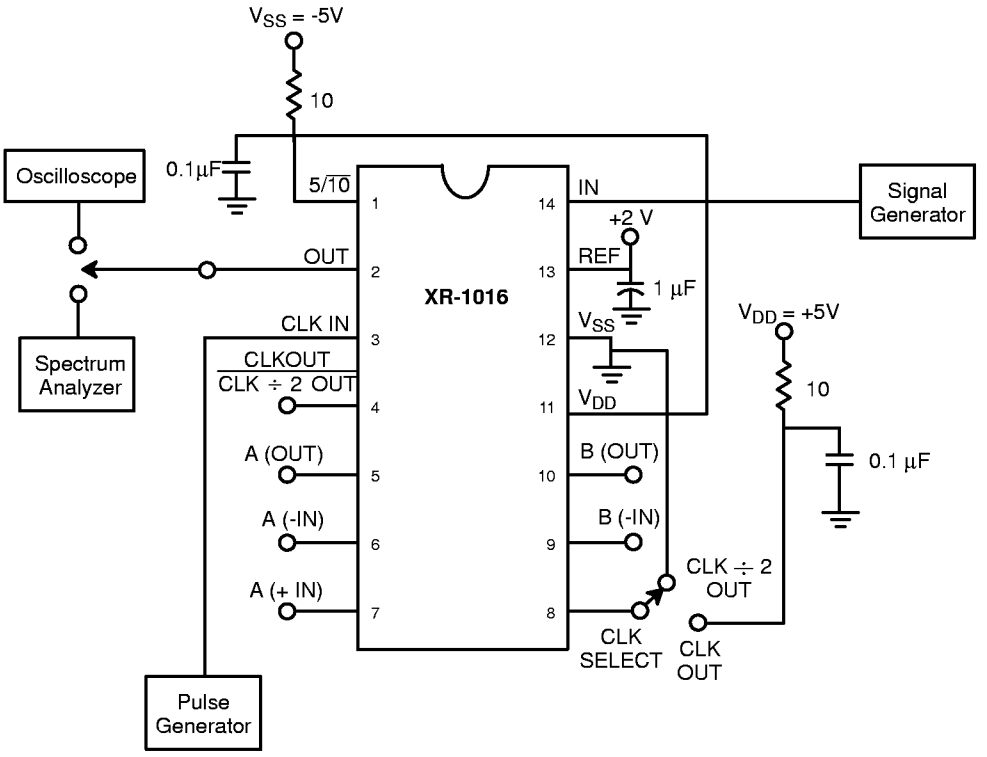


Figure 4. XR-1016 Test Circuit: 5 V Operation (V_{DD} = +5 V, V_{SS} = 0 V, Ref = +2 V)

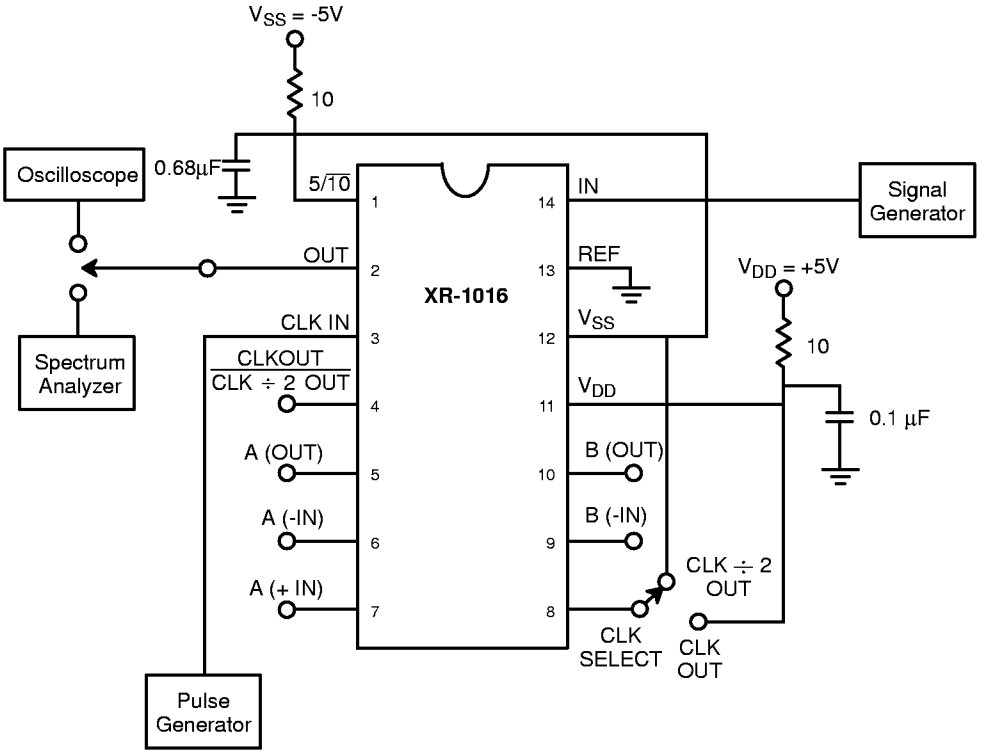


Figure 5. XR-1016 Test Circuit: 10 V Operation (V_{DD} = +5 V, V_{SS} = -5VDC)

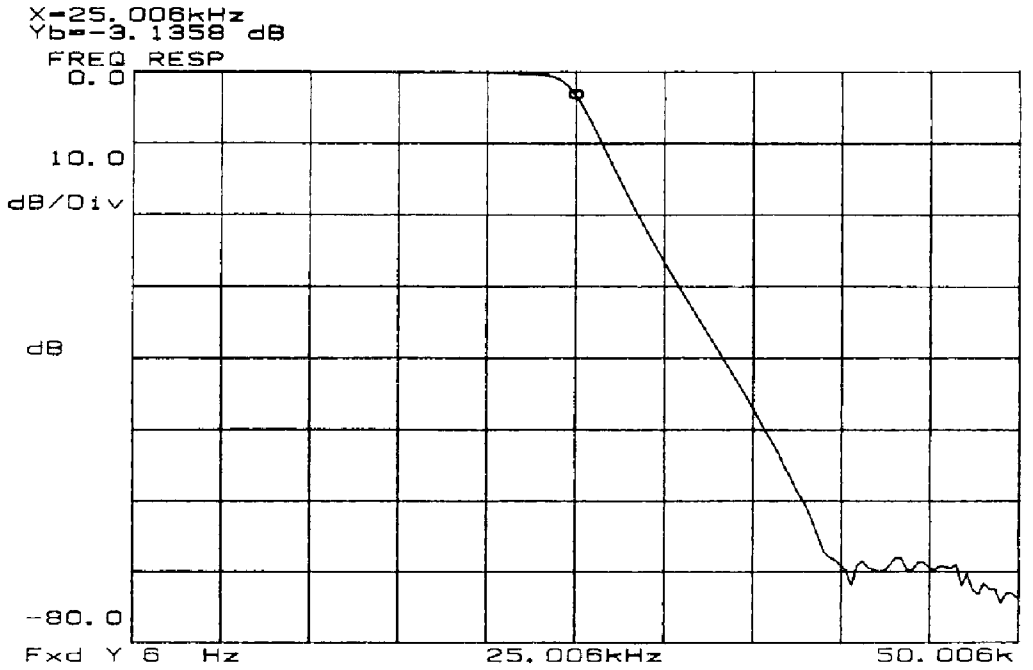


Figure 6. Amplitude Response

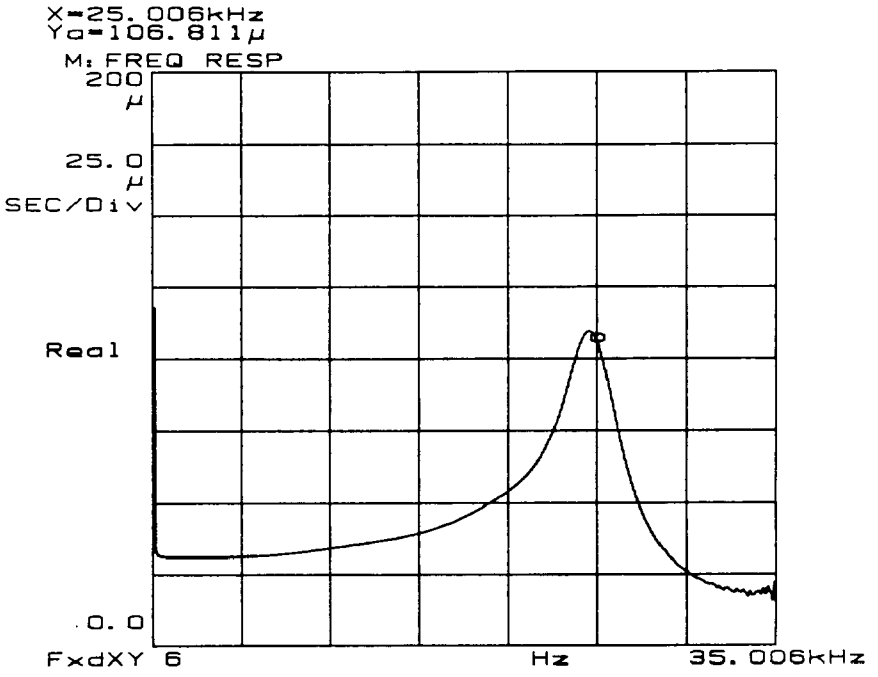


Figure 7. Group Delay Response

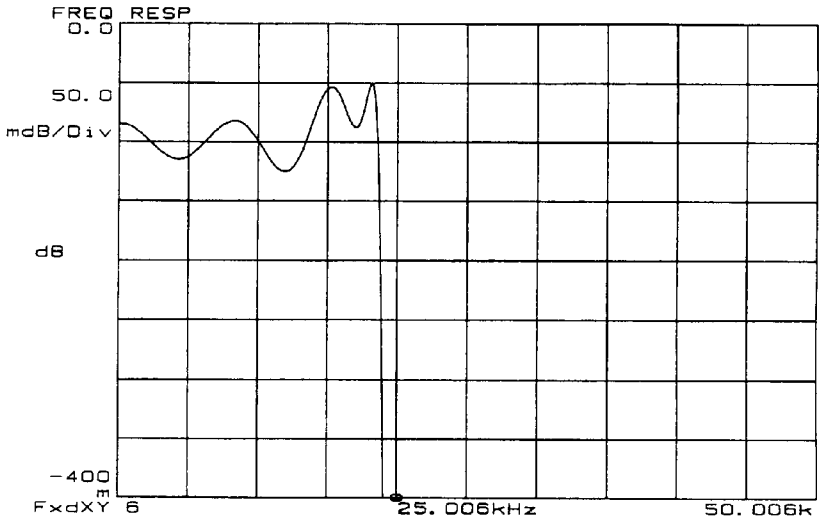


Figure 8. Typical Passband Ripple

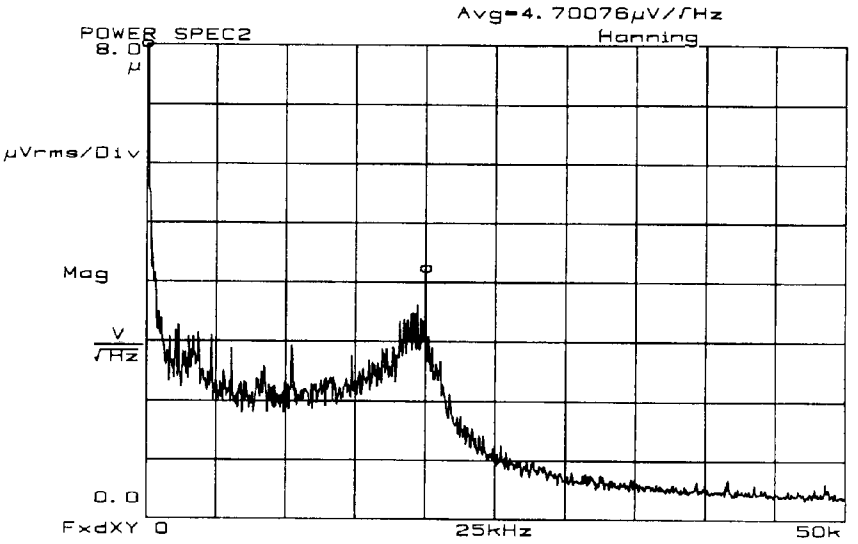


Figure 9. Typical Output Noise

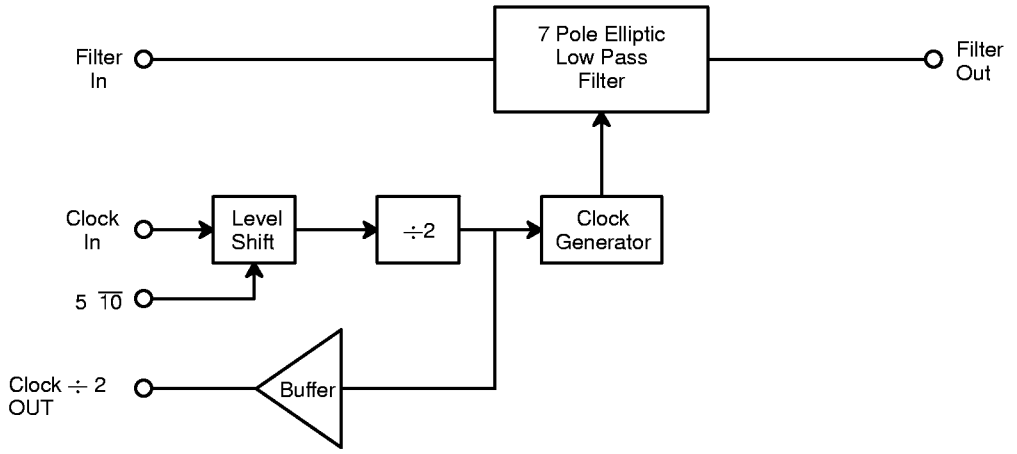


Figure 10. XR-1015 Block Diagram

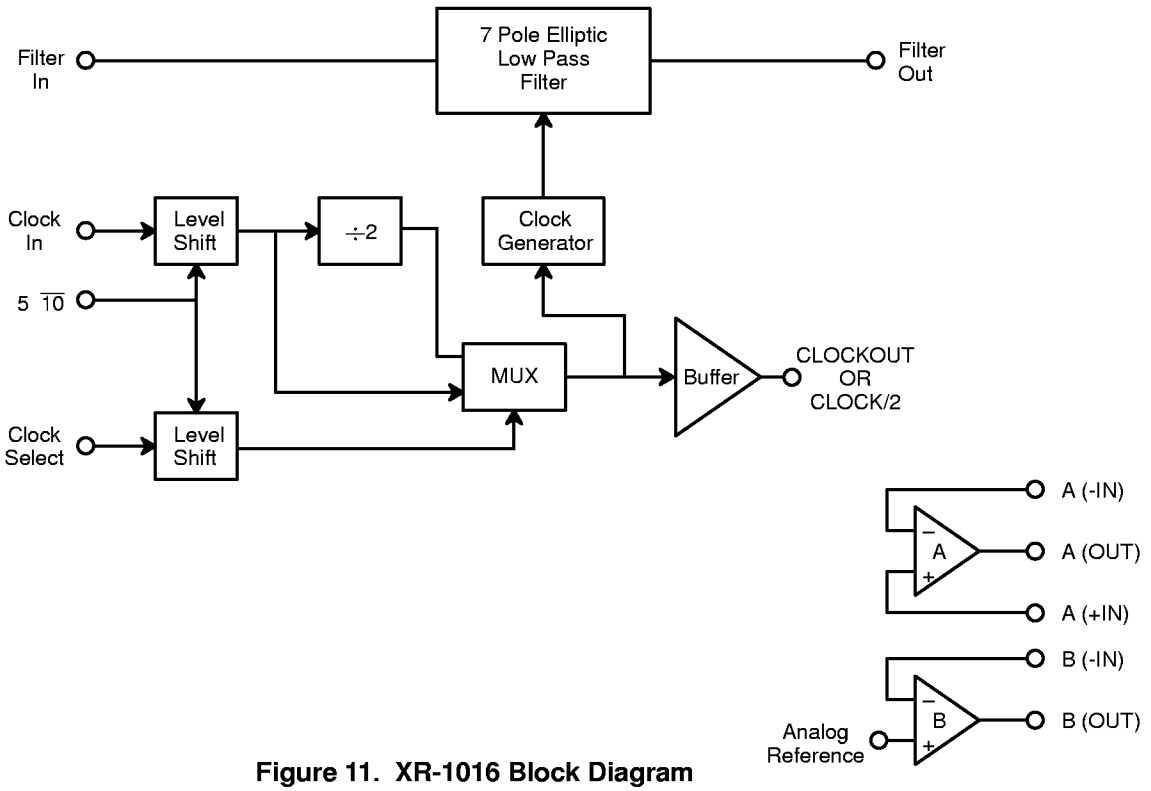
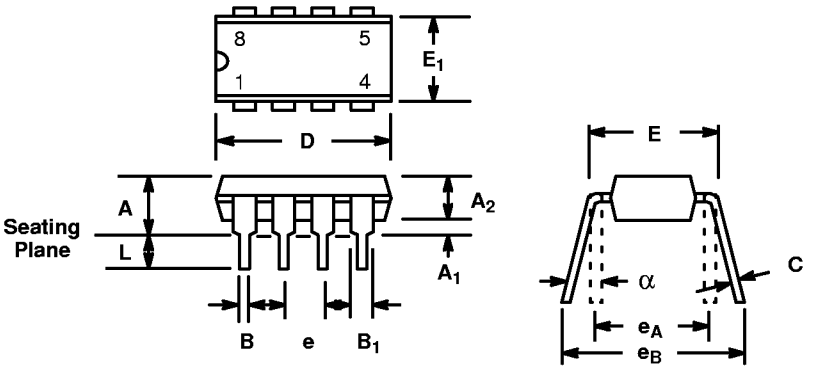


Figure 11. XR-1016 Block Diagram

8 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

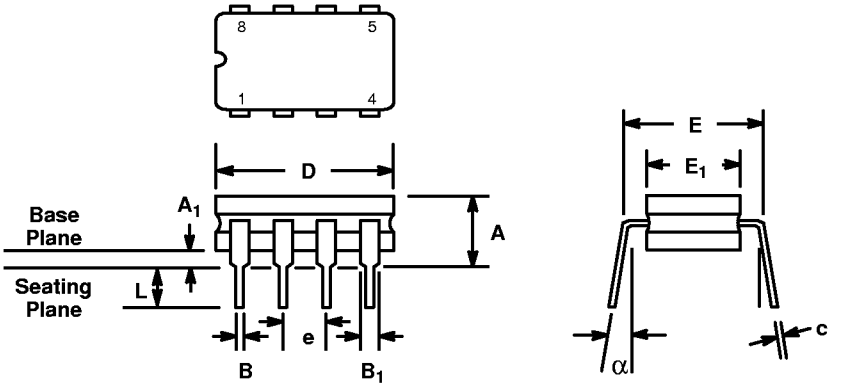


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.015	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.348	0.430	8.84	10.92
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

8 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

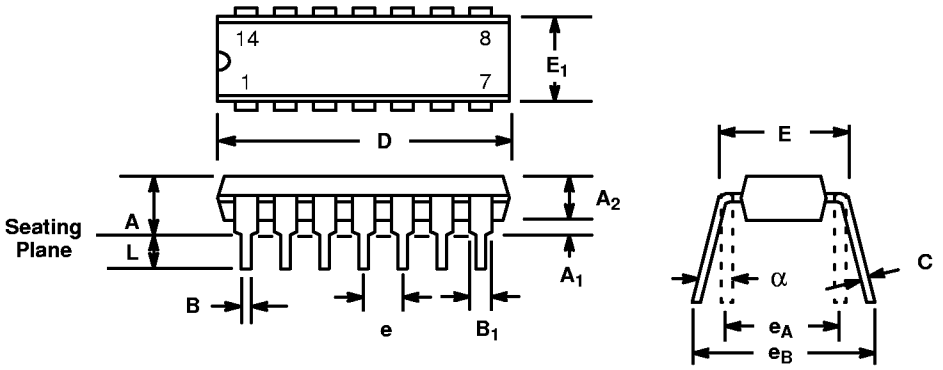


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.305	0.405	7.75	10.29
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

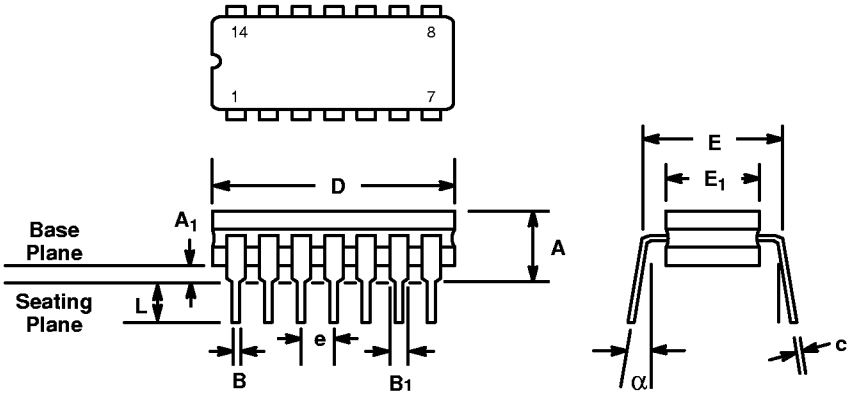


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

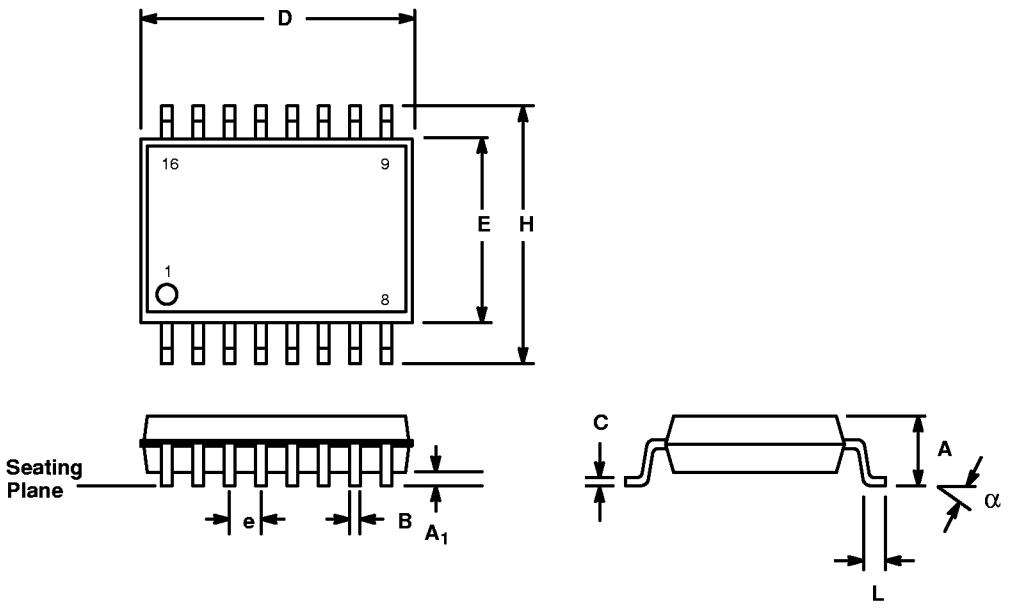


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.685	0.785	17.40	19.94
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column