8 Mbit / 16 Mbit (x8) Multi-Purpose Flash

SST39LF080 / SST39LF016 / SST39VF080 / SST39VF016

Data Sheet

FEATURES:

- **Organized as 1M x8 / 2M x8**
- **Single Voltage Read and Write Operations**
  - 3.0-3.6V for SST39LF080/016
  - 2.7-3.6V for SST39VF080/016
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 15 mA (typical)
  - Standby Current: 4 µA (typical)
  - Auto Low Power Mode: 4 µA (typical)
- **Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Block-Erase Capability**
  - Uniform 64 KByte blocks
- **Fast Read Access Time:**
  - 55 ns for SST39LF080/016
  - 70 and 90 ns for SST39VF080/016
- **Latched Address and Data**
- **Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    15 seconds (typical) for SST39LF/VF080
    30 seconds (typical) for SST39LF/VF016
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 40-Pin TSOP (10mm x 20mm)
  - 48-Ball TFBGA (6mm x 8mm)

PRODUCT DESCRIPTION

The SST39LF/VF080 and SST39LF/VF016 devices are 1M x8 / 2M x8 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39LF080/016 write (Program or Erase) with a 3.0-3.6V power supply. The SST39VF080/016 write (Program or Erase) with a 2.7-3.6V power supply. They conform to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39LF/VF080 and SST39LF/VF016 devices provide a typical Byte-Program time of 14 µsec. The devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39LF/VF080 and SST39LF/VF016 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. They also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39LF/VF080 and SST39LF/VF016 are offered in 40-pin TSOP and 48-ball TFBGA packaging. See Figures 1 and 2 for pinouts.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

The SST39LF/VF080 and SST39LF/VF016 also have the **Auto Low Power** mode which puts the device in a near standby mode after data has been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 15 mA to typically 4 µA. The Auto Low Power mode reduces the typical I_{DD} active read current to the range of 1 mA/MHz of read cycle time. The device exits the Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty. Note that the device does not enter Auto Low Power mode after power-up with CE# held steadily low until the first address transition or CE# is driven high.

Read

The Read operation of the SST39LF/VF080 and SST39LF/VF016 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 3).

Byte-Program Operation

The SST39LF/VF080 and SST39LF/VF016 are programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 20 µs. See Figures 4 and 5 for WE# and CE# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

Sector/Block-Erase Operation

The Sector- (or Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST39LF/VF080 and SST39LF/VF016 offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 4 KByte. The Block-Erase mode is based on uniform block size of 64 KByte. The Sector-Erase operation is initiated by executing a six-byte-command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte-command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 9 and 10 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

Chip-Erase Operation

The SST39LF/VF080 and SST39LF/VF016 provide a Chip-Erase operation, which allows the user to erase the entire memory array to the “1” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 8 for timing diagram, and Figure 19 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Write Operation Status Detection

The SST39LF/VF080 and SST39LF/VF016 provide two software means to detect the completion of a write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST39LF/VF080 and SST39LF/VF016 are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Data# Polling timing diagram and Figure 17 for a flowchart.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 1's and 0's, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Toggle Bit timing diagram and Figure 17 for a flowchart.

Data Protection

The SST39LF/VF080 and SST39LF/VF016 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39LF/VF080 and SST39LF/VF016 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST39LF/VF080 and SST39LF/VF016 devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode within T_{RC}.

Common Flash Memory Interface (CFI)

The SST39LF/VF080 and SST39LF/VF016 also contain the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must write three-byte sequence, same as product ID entry command with 98H (CFI Query command) to address 5555H in the last byte sequence. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in tables 5 through 7. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Product Identification

The Product Identification mode identifies the device as the SST39LF080, SST39VF080, SST39LF016 and SST39VF016 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST39LF/VF080 and SST39LF/VF016. Users may wish to use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the Software ID Entry and Read timing diagram and Figure 18 for the Software ID Entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST39LF/VF080	0001H	D8H
SST39LF/VF016	0001H	D9H

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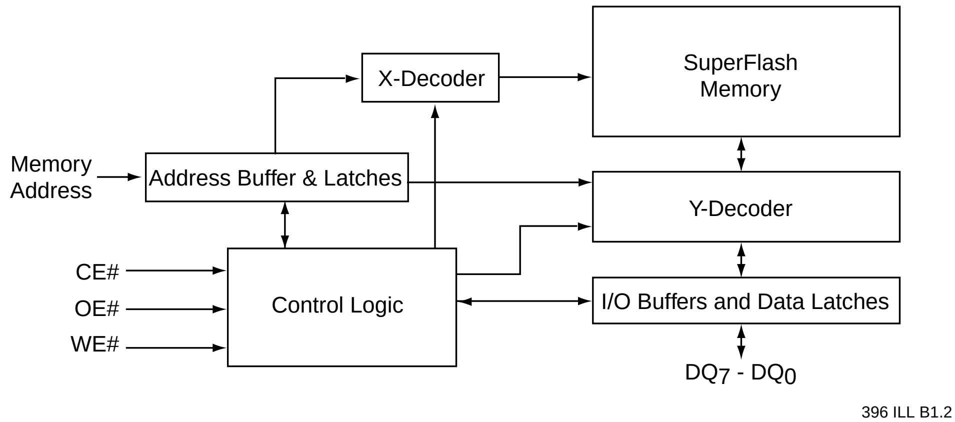
Product Identification Mode Exit/CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 13 for timing waveform and Figure 18 for a flowchart.

Functional Block Diagram



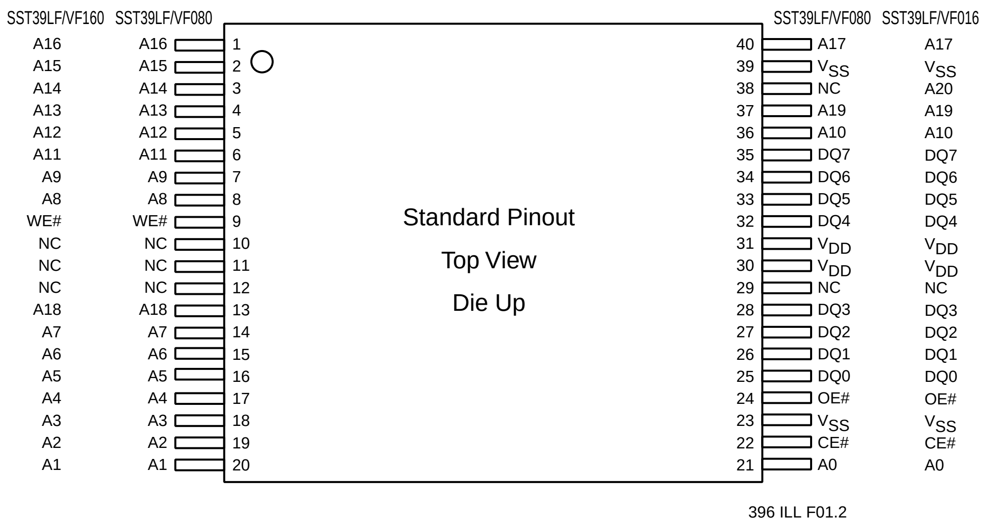


Figure 1: Pin Assignments for 40-pin TSOP

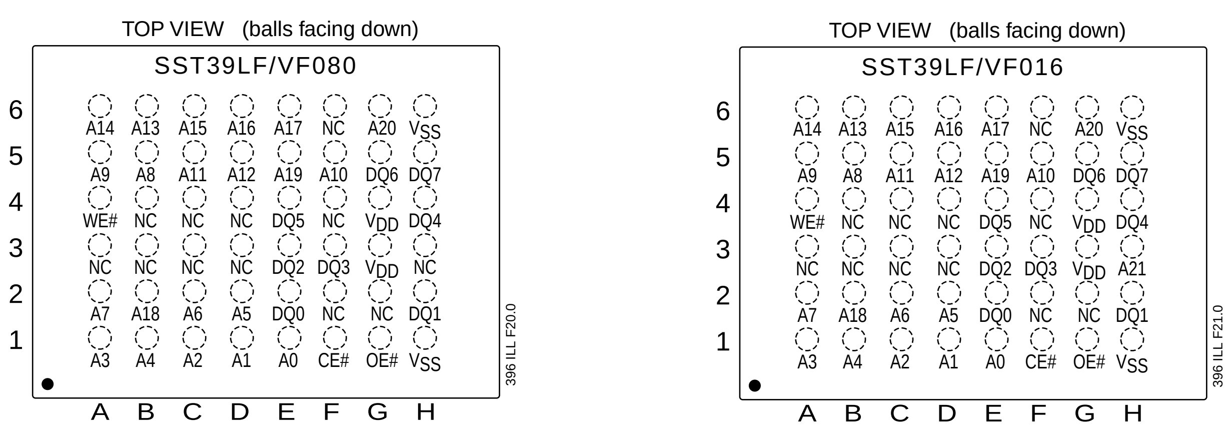


Figure 2: Pin Assignments for 48-ball TFBGA

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}-A_0	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS}-A_{12} address lines will select the sector. During Block-Erase A_{MS}-A_{16} address lines will select the block.
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide power supply voltage: 3.0-3.6V for SST39LF080/016 2.7-3.6V for SST39VF080/016
Vss	Ground	
NC	No Connection	Unconnected pins.

Note: A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	A9	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X	X	Sector or block address, XXH for Chip-Erase
Standby	V_{IH}	X	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	X	High Z/ D_{OUT}	X
	X	X	V_{IH}	X	High Z/ D_{OUT}	X
Product Identification						
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer's ID (BFH) Device ID (1)	$A_{MS}^{(2)}$ - A_1 = V_{IL}, A_0 = V_{IL} $A_{20}^{(2)}$ - A_1 = V_{IL}, A_0 = V_{IH}
Software Mode	V_{IL}	V_{IL}	V_{IH}	A_{IN}		See Table 4

Notes: (1) Device ID D8H for SST39LF/VF080 and D9H for SST39LF/VF016
(2) A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

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TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data	Addr(1)	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA(3)	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_x(2)	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA_x(2)	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
CFI Query Entry	5555H	AAH	2AAAH	55H	5555H	98H						
Software ID Exit/ CFI Exit	XXH	F0H										
Software ID Exit/ CFI Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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Notes: (1) Address format A_{14}-A_0 (Hex),
Addresses A_{15}, A_{16}, A_{17}, A_{18} and A_{19} are "Don't Care" for Command sequence for SST39LF/VF080.
Addresses A_{15}, A_{16}, A_{17}, A_{18}, A_{19} and A_{20} are "Don't Care" for Command sequence for SST39LF/VF016.

(2) SA_x for Sector-Erase; uses A_{MS}-A_{12} address lines
BA_x, for Block-Erase; uses A_{MS}-A_{16} address lines
A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

(3) WA = Program byte address

(4) Both Software ID Exit operations are equivalent

Notes for Software ID Entry Command Sequence

1. With A_{MS} -A_1 = 0; SST Manufacturer's ID = BFH, is read with A_0 = 0,
   SST39LF/VF080 Device ID = D8H, is read with A_0 = 1.
   SST39LF/VF016 Device ID = D9H, is read with A_0 = 1.

   A_{MS} = Most significant address

   A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.
2. The device does not remain in Software Product ID Mode if powered down.

TABLE 5: CFI QUERY IDENTIFICATION STRING[1] FOR SST39LF/VF080 AND SST39LF/VF016

Address	Data	Data
10H 11H 12H	51H 52H 59H	Query Unique ASCII string "QRY"
13H 14H	01H 07H	Primary OEM command set
15H 16H	00H 00H	Address for Primary Extended Table
17H 18H	00H 00H	Alternate OEM command set (00H = none exists)
19H 1AH	00H 00H	Address for Alternate OEM extended Table (00H = none exits)

Note 1: Refer to CFI publication 100 for more details.

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TABLE 6: SYSTEM INTERFACE INFORMATION FOR SST39LF/VF080 AND SST39LF/VF016

Address	Data	Data
1BH	27H(1) 30H(1)	V_{DD} Min. (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1CH	36H	V_{DD} Max. (Program/Erase) DQ7-DQ4: Volts, DQ3-DQ0: 100 millivolts
1DH	00H	V_{PP} min. (00H = no V_{PP} pin)
1EH	00H	V_{PP} max. (00H = no V_{PP} pin)
1FH	04H	Typical time out for Byte-Program 2^N µs (2^4 = 16 µs)
20H	00H	Typical time out for min. size buffer program 2^N µs (00H = not supported)
21H	04H	Typical time out for individual Sector/Block-Erase 2^N ms (2^4 = 16 ms)
22H	06H	Typical time out for Chip-Erase 2^N ms (2^6 = 64 ms)
23H	01H	Maximum time out for Byte-Program 2^N times typical (2^1 x 2^4 = 32 µs)
24H	00H	Maximum time out for buffer program 2^N times typical
25H	01H	Maximum time out for individual Sector/Block-Erase 2^N times typical (2^1 x 2^4 = 32 ms)
26H	01H	Maximum time out for Chip-Erase 2^N times typical (2^1 x 2^6 = 128 ms)

Note (1) 30H for SST39LF080/016 and 27H for SST39VF080/016

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TABLE 7A: DEVICE GEOMETRY INFORMATION FOR SST39LF/VF080

Address	Data	Data
27H	14H	Device size = 2^N Bytes (14H = 20; 2^{20} = 1M Bytes)
28H 29H	00H 00H	Flash Device Interface description; 0000H = x8-only asynchronous interface
2AH 2BH	00H 00H	Maximum number of byte in multi-byte write = 2^N (00H = not supported)
2CH	02H	Number of Erase Sector/Block sizes supported by device
2DH 2EH 2FH 30H	FFH 00H 10H 00H	Sector Information (y + 1 = Number of sectors; z x 256B = sector size) y = 255 + 1 = 256 sectors (00FFH = 255) z = 16 x 256 Bytes = 4 KBytes/sector (0010H = 16)
31H 32H 33H 34H	0FH 00H 00H 01H	Block Information (y + 1 = Number of blocks; z x 256B = block size) y = 15 + 1 = 16 blocks (000FH = 15) z = 256 x 256 Bytes = 64 KBytes/block (0100H = 256)

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TABLE 7B: DEVICE GEOMETRY INFORMATION FOR SST39LF/VF016

Address	Data	Data
27H	15H	Device size = 2^N Byte (15H = 21; 2^{21} = 2M Bytes)
28H 29H	00H 00H	Flash Device Interface description; 0000H = x8-only asynchronous interface
2AH 2BH	00H 00H	Maximum number of byte in multi-byte write = 2^N (00H = not supported)
2CH	02H	Number of Erase Sector/Block sizes supported by device
2DH 2EH 2FH 30H	FFH 01H 10H 00H	Sector Information (y + 1 = Number of sectors; z x 256B = sector size) y = 511 + 1 = 512 sectors (01FFH = 511) z = 16 x 256 Bytes = 4 KBytes/sector (0010H = 16)
31H 32H 33H 34H	1FH 00H 00H 01H	Block Information (y + 1 = Number of blocks; z x 256B = block size) y = 31 + 1 = 32 blocks (001FH = 31) z = 256 x 256 Bytes = 64 KBytes/block (0100H = 256)

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias .... -55°C to +125°C
Storage Temperature .... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential .... -0.5V to V_{DD} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential .... -1.0V to V_{DD} + 1.0V
Voltage on A_9 Pin to Ground Potential .... -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) .... 240°C
Output Short Circuit Current(1) .... 50 mA

Note: (1) Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range for SST39LF080/016

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70 °C	3.0 - 3.6V

Operating Range for SST39VF080/016

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7 - 3.6V
Industrial	-40°C to +85°C	2.7 - 3.6V

AC Conditions of Test

Input Rise/Fall Time .... 5 ns
Output Load .... C_L = 30 pF for SST39LF080/016
.... C_L = 100 pF for SST39VF080/016
See Figures 14 and 15

TABLE 8: DC OPERATING CHARACTERISTICS V_{DD} = 3.0-3.6V FOR SST39LF080/016 AND 2.7-3.6V FOR SST39VF080/016

Symbol	Parameter	Limits Min	Max	Units	Test Conditions
I_{DD}	Power Supply Current				Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{DD}=V_{DD} Max.
	Read		20	mA	CE#=OE#=V_{IL},WE#=V_{IH} , all I/Os open
	Program and Erase		25	mA	CE#=WE#=V_{IL}, OE#=V_{IH}
I_{SB}	Standby V_{DD} Current		20	µA	CE#=V_{IHC}, V_{DD} = V_{DD} Max.
I_{ALP}	Auto Low Power Current		20	µA	CE#=V_{ILC}, V_{DD} = V_{DD} Max. All inputs = V_{IHC} or V_{ILC} WE# = V_{IHC}
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, V_{DD} = V_{DD} Max.
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, V_{DD} = V_{DD} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{DD} = V_{DD} Min.
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	V_{DD} = V_{DD} Max.
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD} = V_{DD} Max.
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD} = V_{DD} Max.
V_{OL}	Output Low Voltage		0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min.
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min.
V_H	Supervoltage for A_9 pin	11.4	12.6	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9 pin		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

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TABLE 9: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$(1)	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$(1)	Power-up to Program/Erase Operation	100	µs

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Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$(1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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TABLE 11: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}(1)	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}(1)	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

396 PGM T12.0

Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 12: READ CYCLE TIMING PARAMETERS
V_{DD} = 3.0-3.6V FOR SST39LF080/016 AND 2.7-3.6V FOR SST39VF080/016

Symbol	Parameter	SST39LF080/016-55		SST39VF080/016-70		SST39VF080/016-90		Units
		Min	Max	Min	Max	Min	Max	
T_{RC}	Read Cycle Time	55		70		90		ns
T_{CE}	Chip Enable Access Time		55		70		90	ns
T_{AA}	Address Access Time		55		70		90	ns
T_{OE}	Output Enable Access Time		30		35		45	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		15		20		30	ns
T_{OHZ}(1)	OE# High to High-Z Output		15		20		30	ns
T_{OH}(1)	Output Hold from Address Change	0		0		0		ns

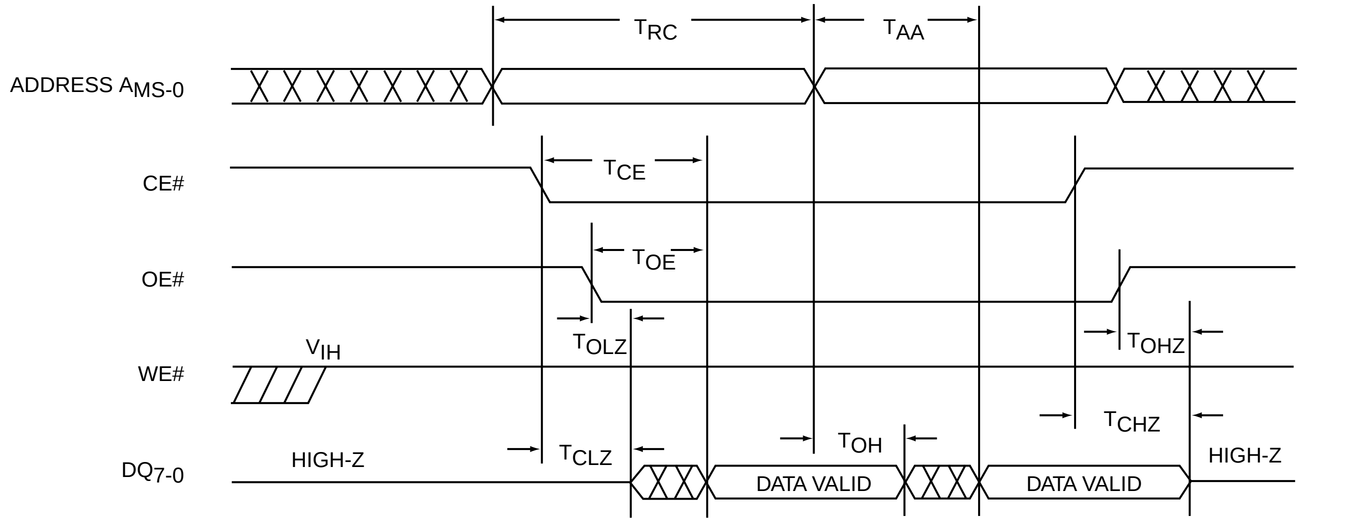
396 PGM T13.2

TABLE 13: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Byte-Program Time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH} (1)	WE# Pulse Width High	30		ns
T_{CPH} (1)	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH} (1)	Data Hold Time	0		ns
T_{IDA} (1)	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms

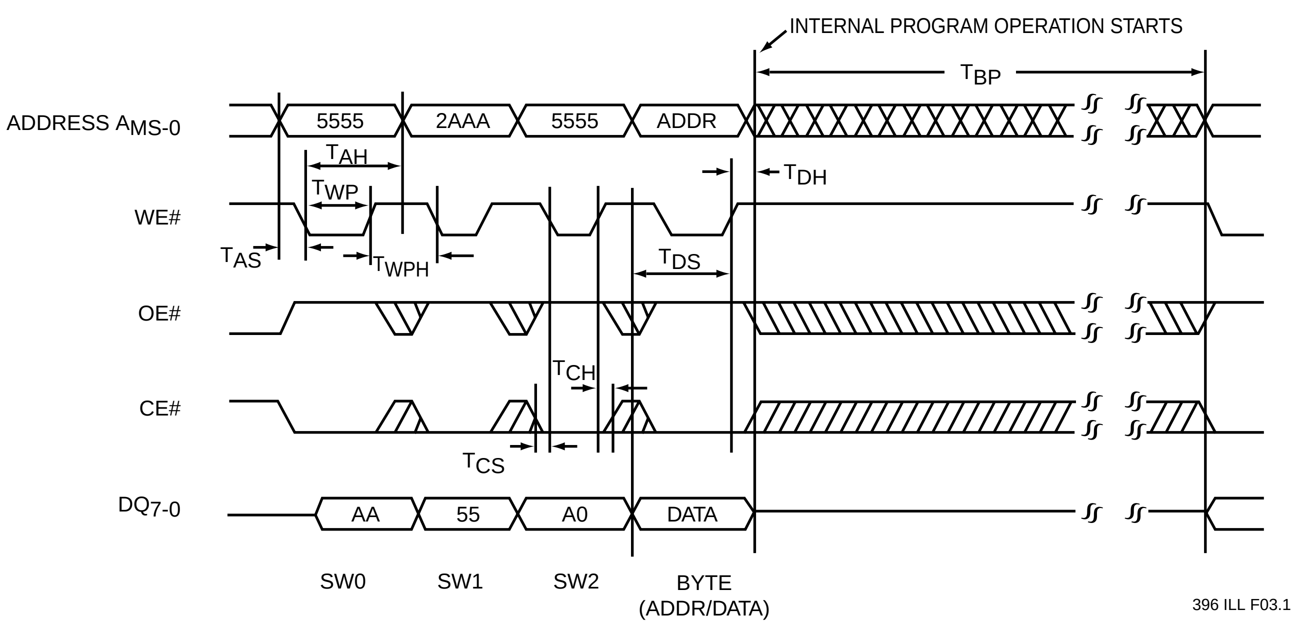
396 PGM T14.0

Note: (1) This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.



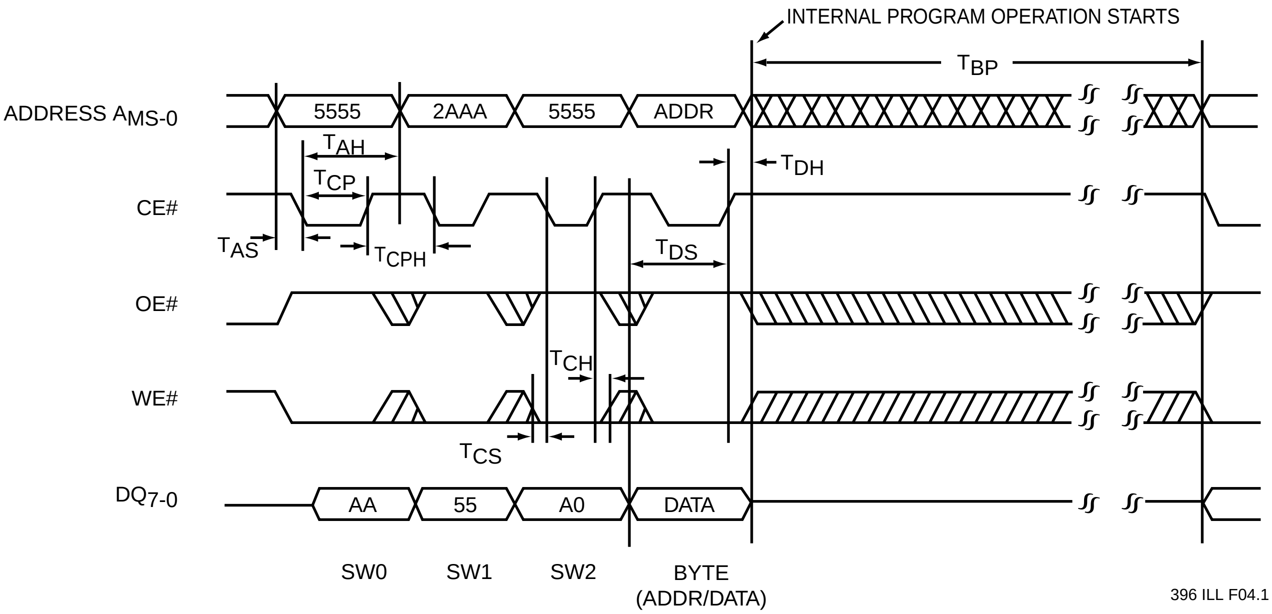
Note: A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

Figure 3: Read Cycle Timing Diagram



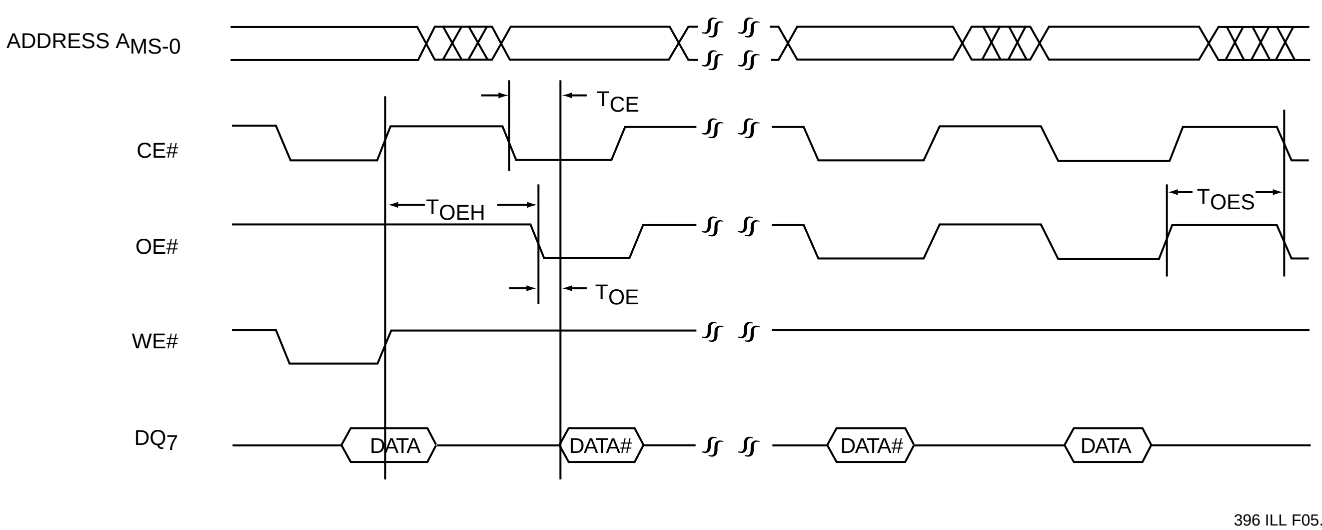
Note: A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

Figure 4: WE# Controlled Program Cycle Timing Diagram



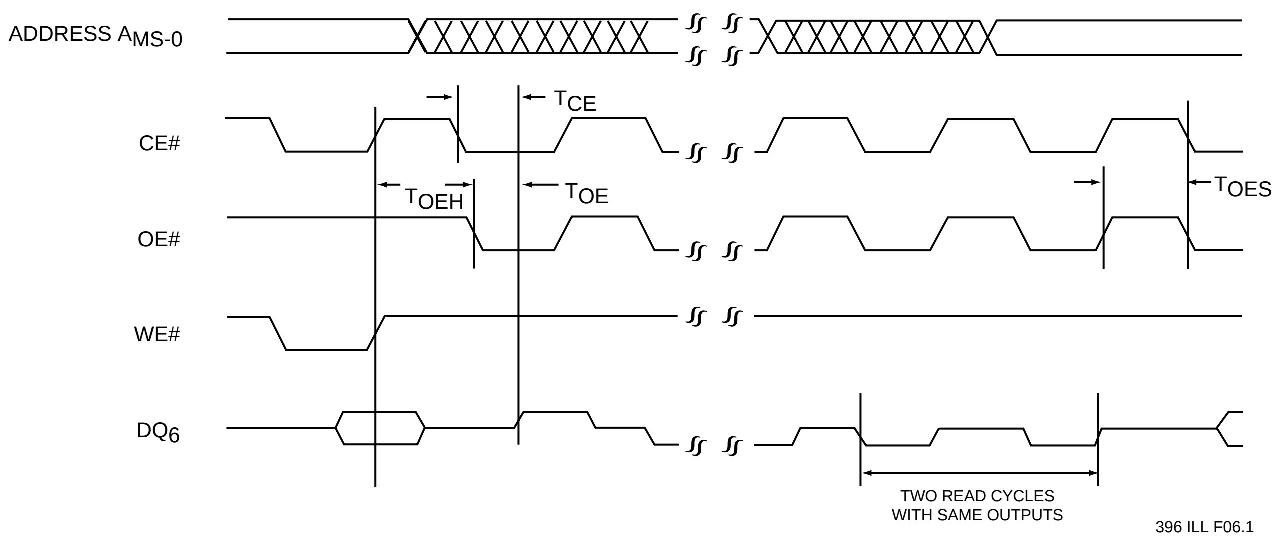
Note: A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

FIGURE 5: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



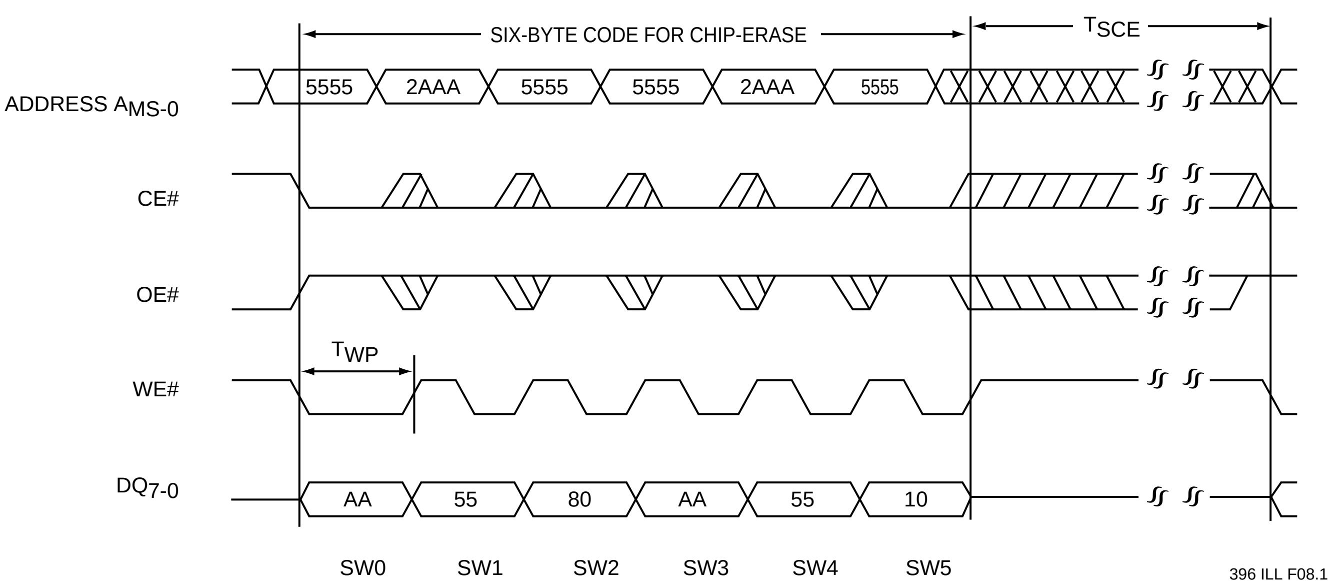
Note: A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

FIGURE 6: DATA# POLLING TIMING DIAGRAM



Note: A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

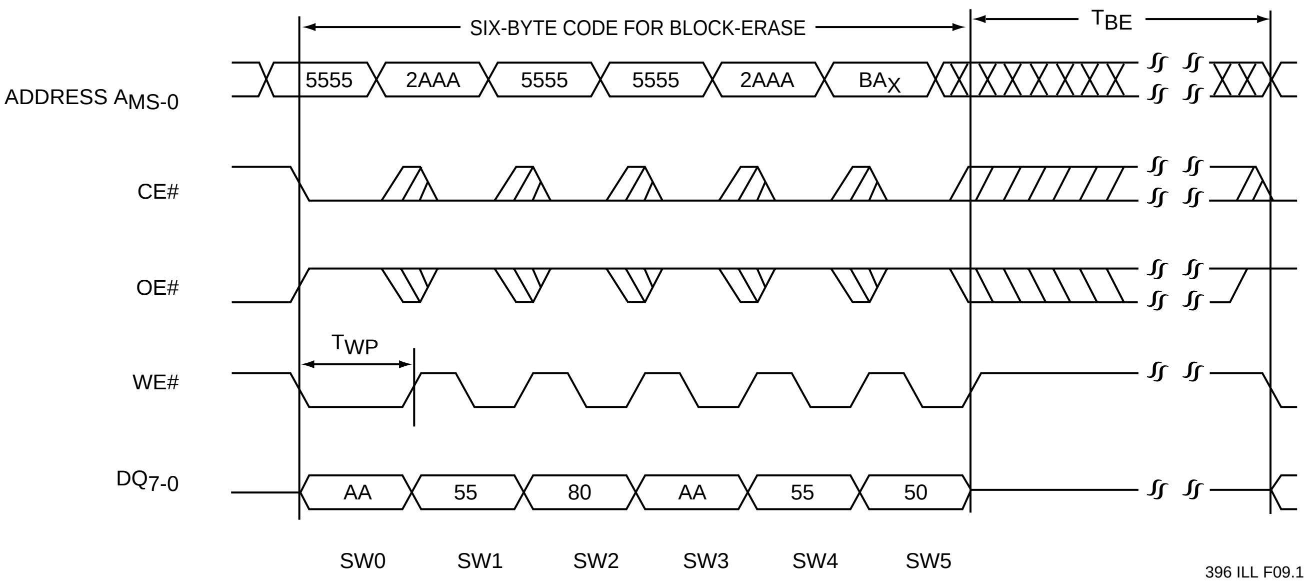
FIGURE 7: TOGGLE BIT TIMING DIAGRAM



Note: The device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)

A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

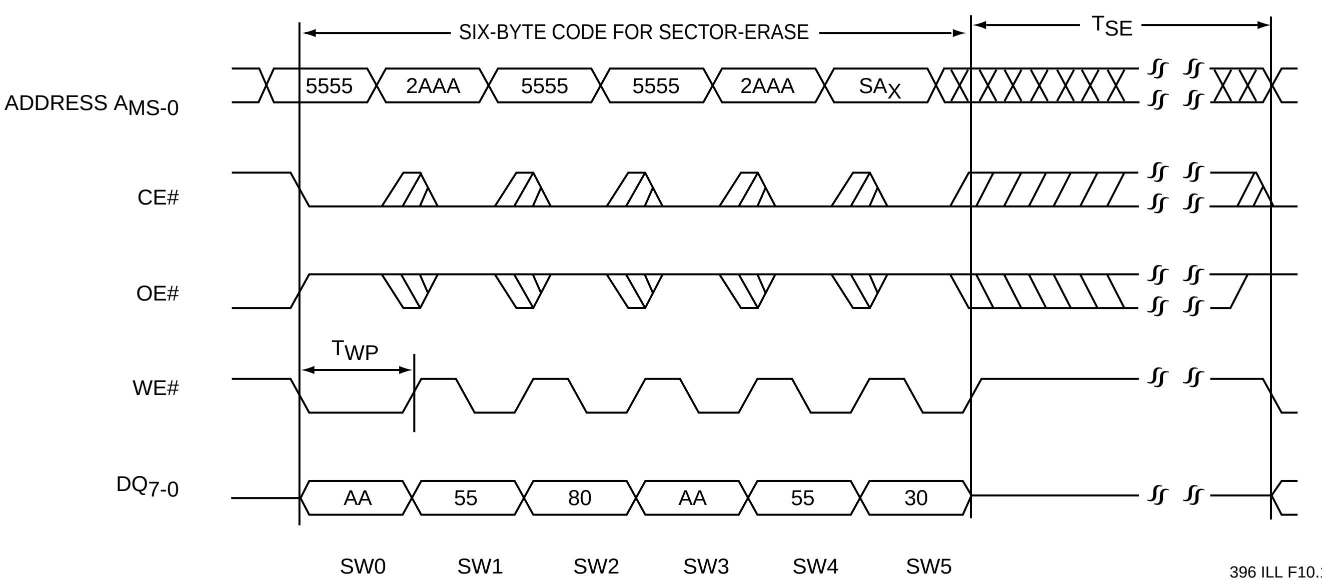
FIGURE 8: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



Note: The device also supports CE# controlled Block-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)

A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

FIGURE 9: WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM



Note: The device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)

A_{MS} = Most significant address
A_{MS} = A_{19} for SST39LF/VF080 and A_{20} for SST39LF/VF016.

FIGURE 10: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM

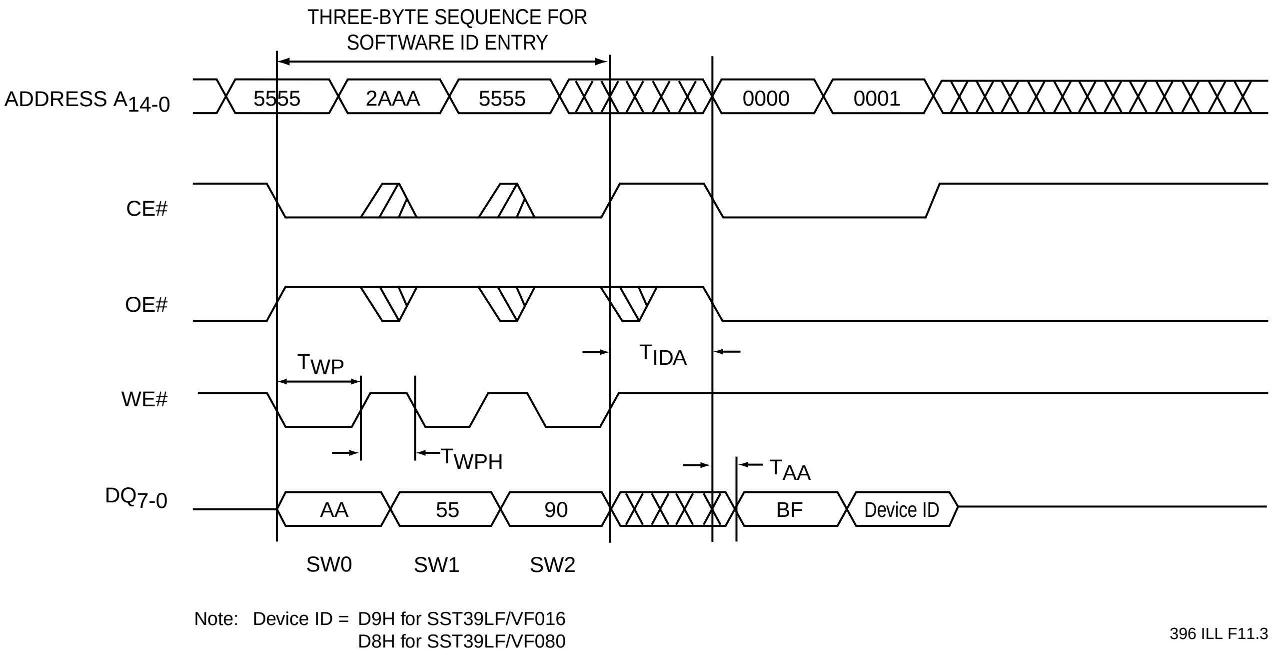


Figure 11: Software ID Entry and Read

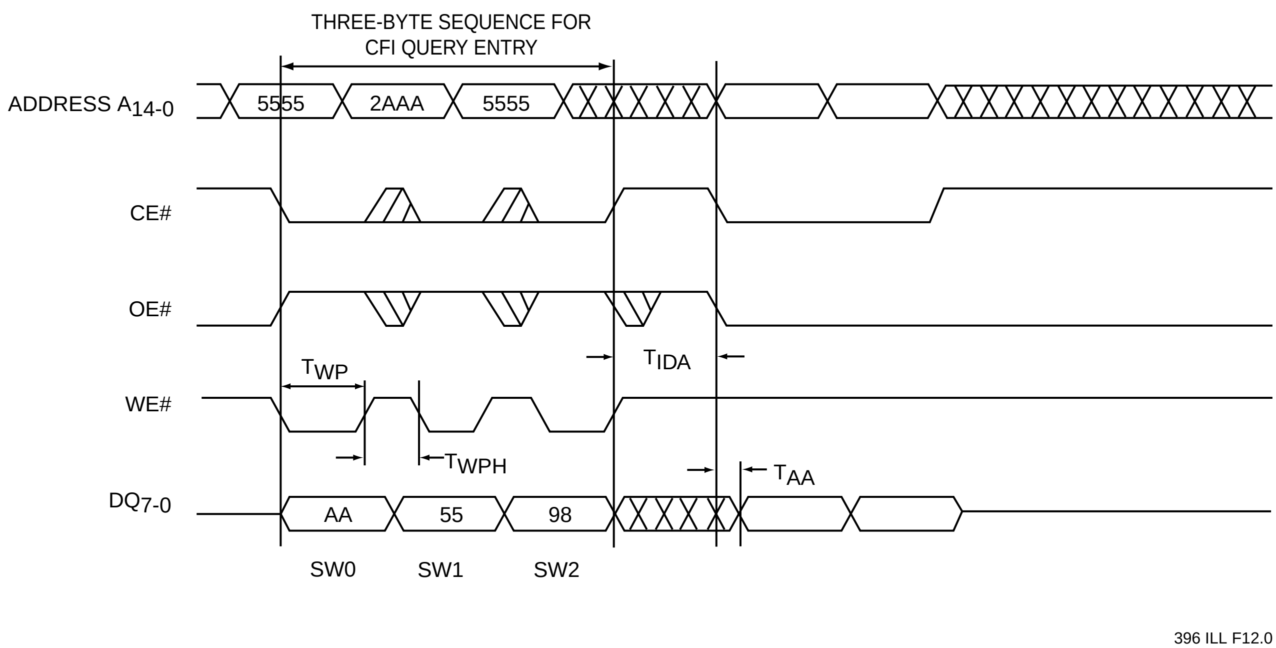


Figure 12: CFI Query Entry and Read

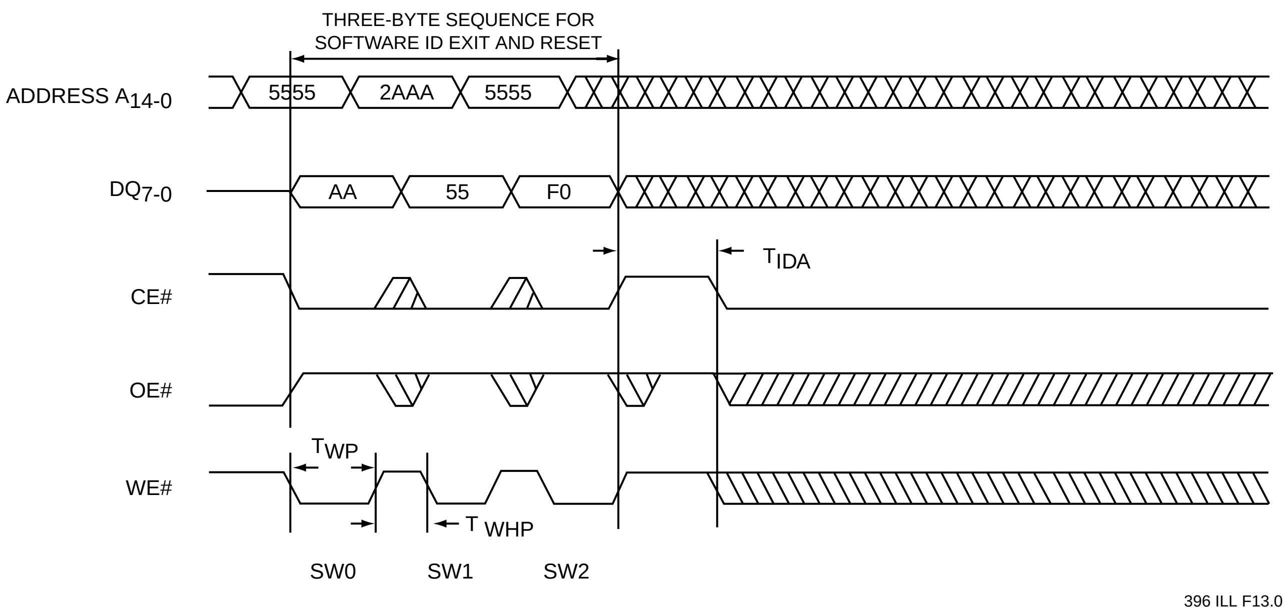
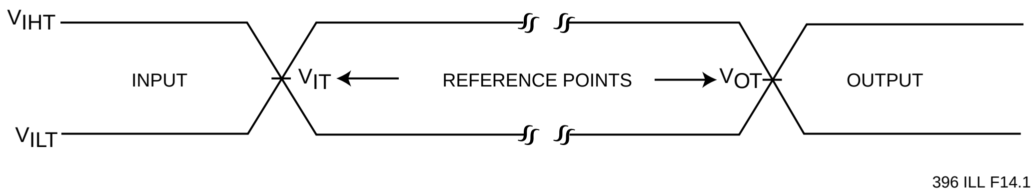


Figure 13: Software ID Exit/CFI Exit



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic “1” and V_{ILT} (0.1 V_{DD}) for a logic “0”. Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Inputs rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT}–V_{INPUT} Test
V_{OT}–V_{OUTPUT} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 14: AC INPUT/OUTPUT REFERENCE WAVEFORMS

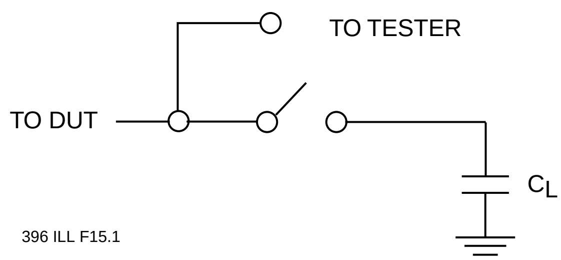


FIGURE 15: A TEST LOAD EXAMPLE

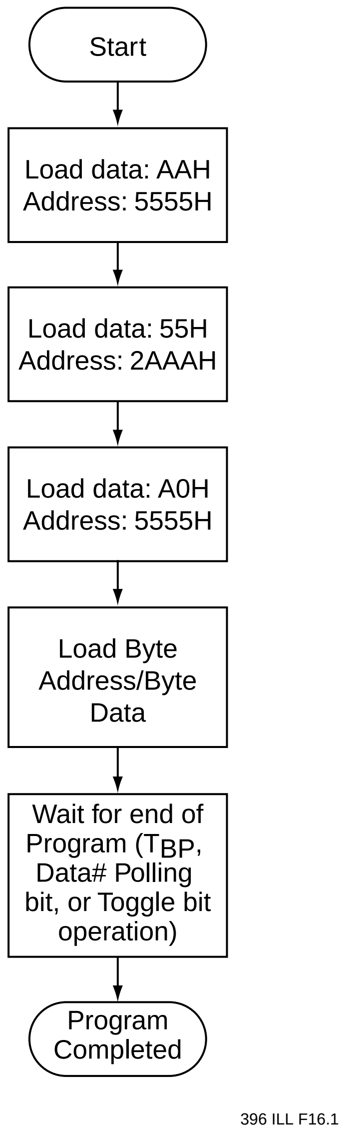


FIGURE 16: BYTE-PROGRAM ALGORITHM

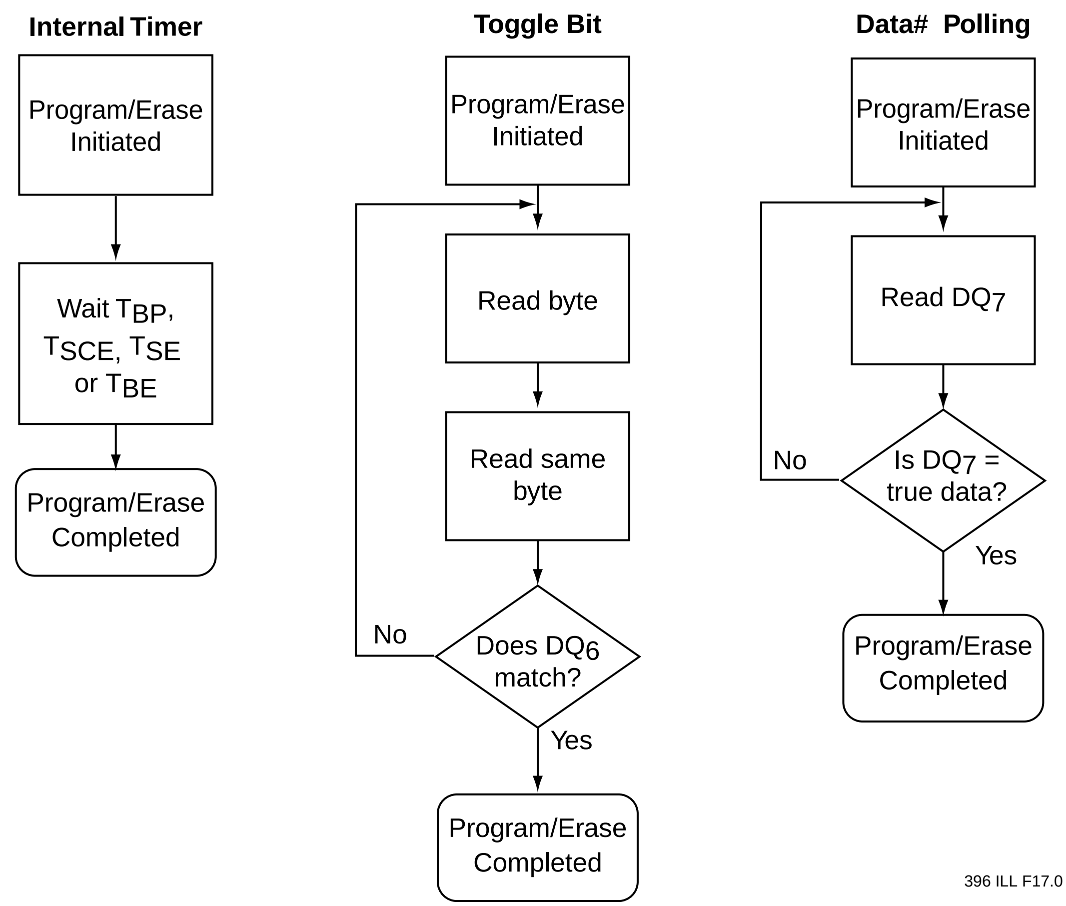


FIGURE 17: WAIT OPTIONS

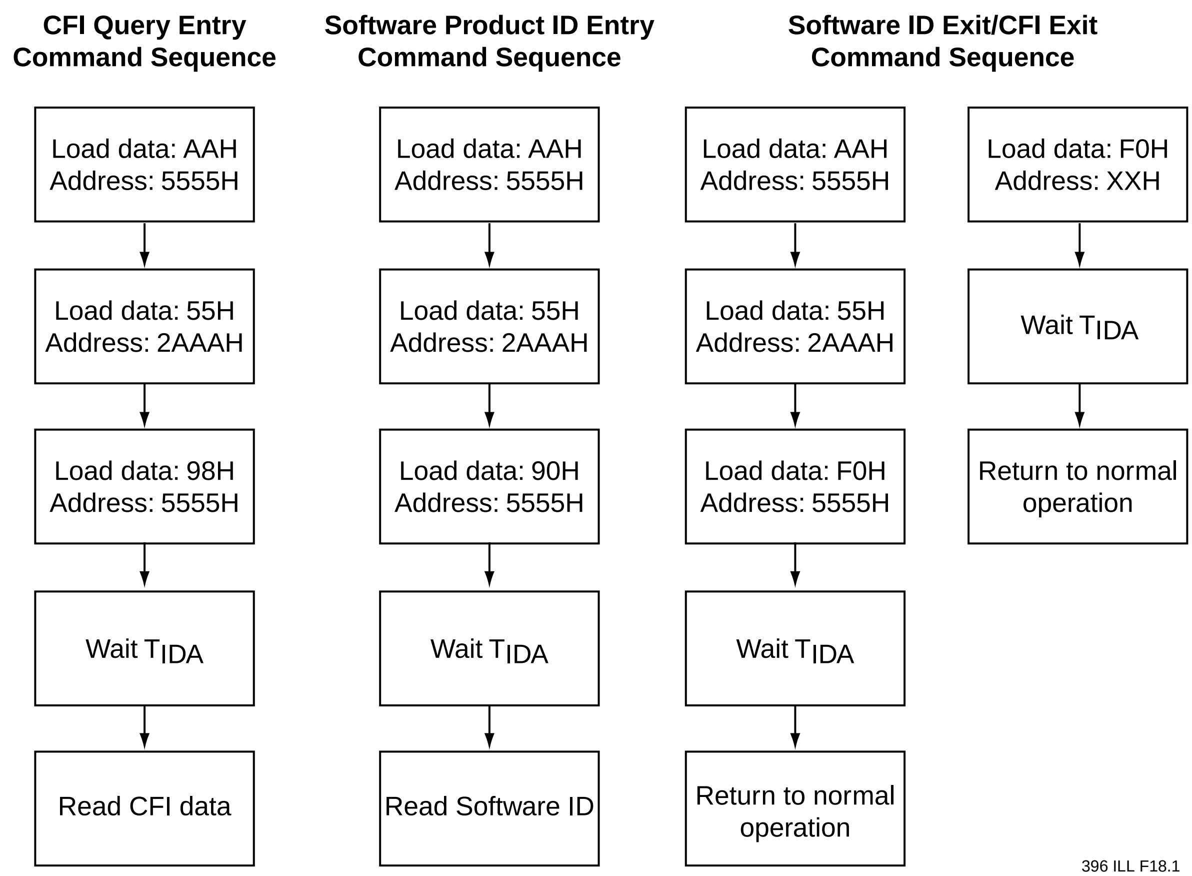


Figure 18: Software Product ID/CFI Command Flowcharts

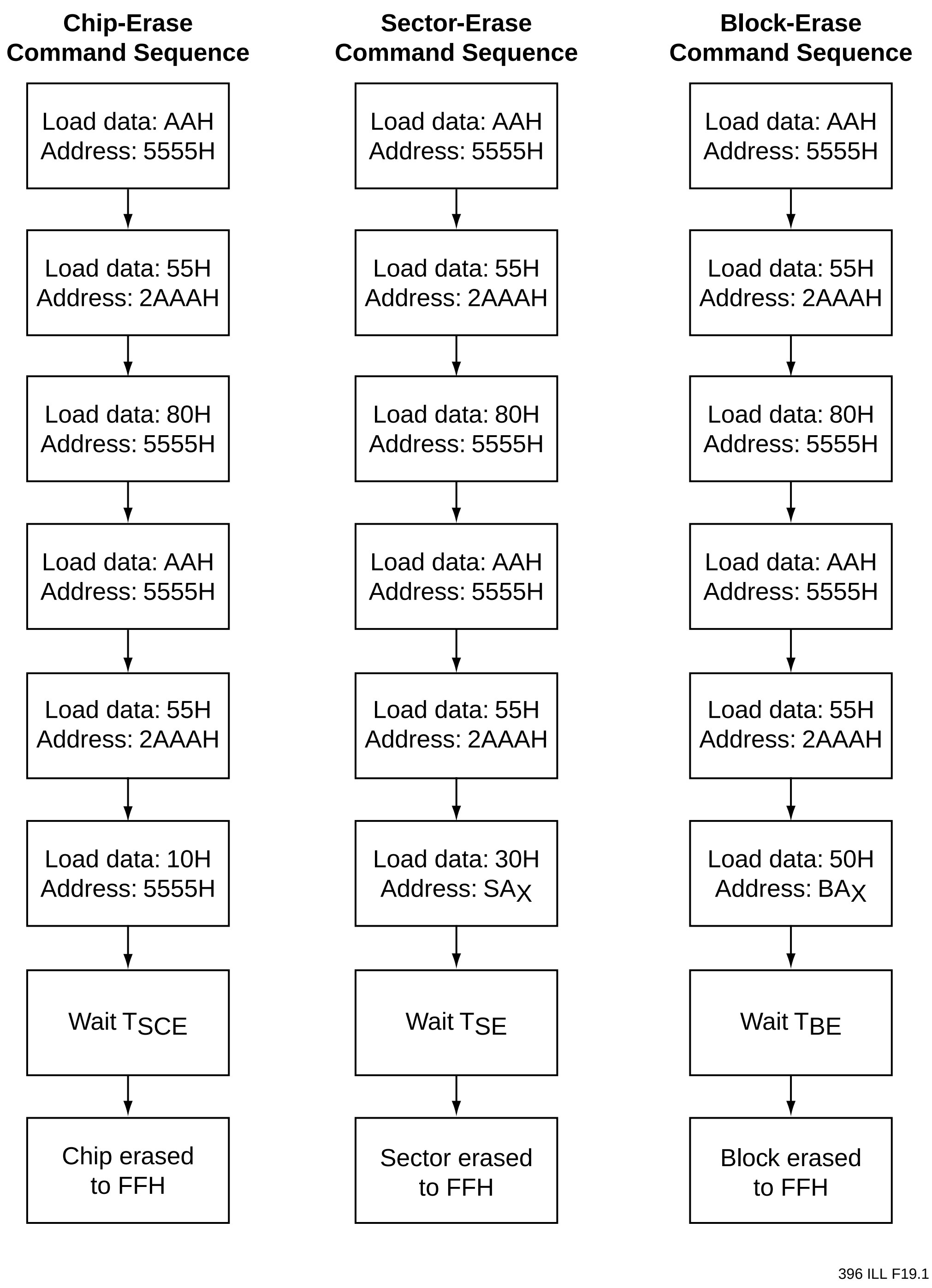


FIGURE 19: ERASE COMMAND SEQUENCE

Device		**Speed**		**Suffix1**		**Suffix2**
SST39xFxxx	-	XXX	-	XX	-	XX

Package Modifier
I = 40 pins
K = 48 pins
Numeric = Die modifier

Package Type
E = TSOP (10mm x 20mm)
B2 = TFBGA (6mm x 8mm)

Temperature Range
C = Commercial = 0°C to +70°C
I = Industrial = -40°C to +85°C

Minimum Endurance
4 = 10,000 cycles

Read Access Speed
55 = 55 ns
70 = 70 ns
90 = 90 ns

Device Density
080 = 8 Megabit
016 = 16 Megabit

Voltage
L = 3.0-3.6V
V = 2.7-3.6V

SST39LF080 Valid combinations

SST39LF080-55-4C-EI	SST39LF080-55-4C-B2K

SST39VF080 Valid combinations

SST39VF080-70-4C-EI	SST39VF080-70-4C-B2K
SST39VF080-90-4C-EI	SST39VF080-90-4C-B2K
SST39VF080-90-4I-EI	SST39VF080-90-4I-B2K

SST39LF016 Valid combinations

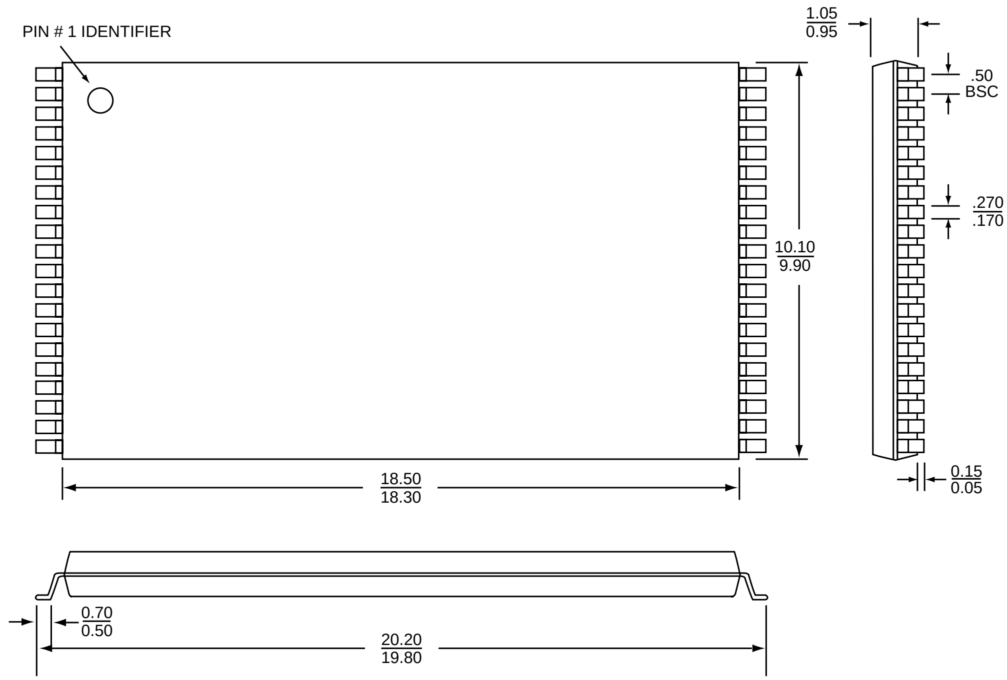
SST39VF016-55-4C-EI	SST39VF016-55-4C-B2K

SST39VF016 Valid combinations

SST39VF016-70-4C-EI	SST39VF016-70-4C-B2K
SST39VF016-90-4C-EI	SST39VF016-90-4C-B2K
SST39VF016-90-4I-EI	SST39VF016-90-4I-B2K

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

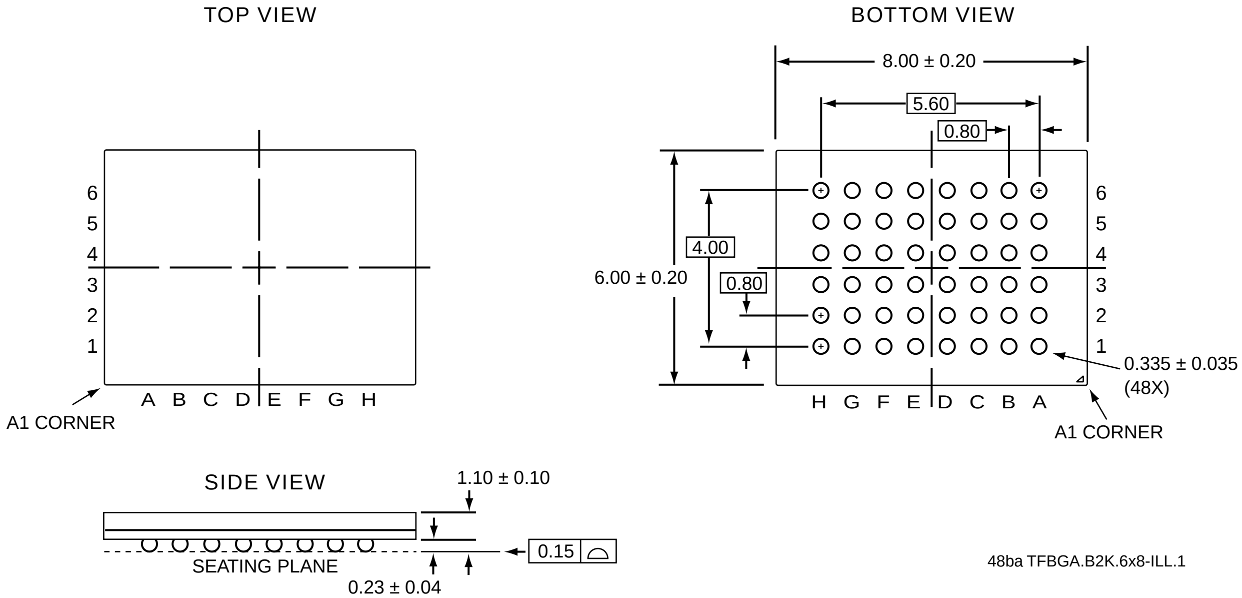
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-142 CD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.

40.TSOP-EI-ILL.3

40-Pin Thin Small Outline Package (TSOP) 10mm x 20mm
SST Package Code: EI



Note: 1. Complies with the general requirements of JEDEC publication 95 MO-210, although some dimensions may be more stringent. (This specific outline variant has not yet been registered)
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.

48-Ball Thin Profile Fine-pitch Ball Grid Array (TFBGA) 6mm x 8mm
SST Package Code: B2K