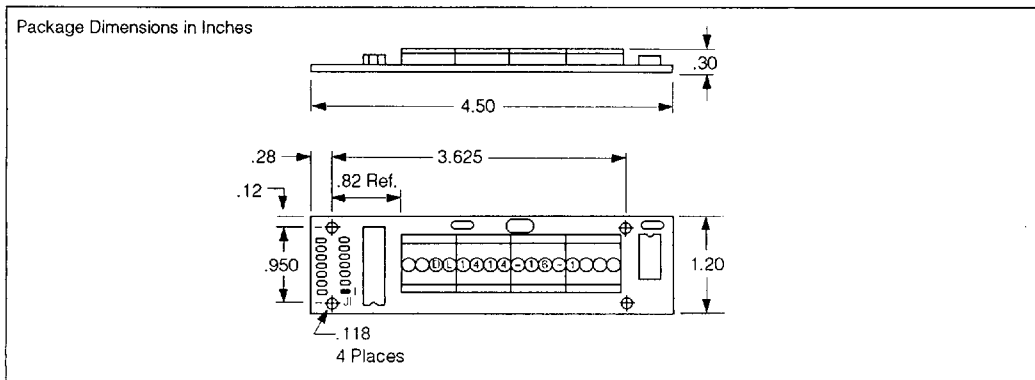


SIEMENS

IDA1414-16

**.112" Red, 17 Segment, 16 Character
DL1414 Intelligent Display® Assembly
IDA1414-16-1 Buffered Input Data Lines**



FEATURES

- **.112" Magnified Monolithic Character**
- **Wide Viewing Angle $\pm 40^\circ$**
- **Complete Alphanumeric Display Assembly Using the DL1414T**
 - Built-in Multiplex and LED Drive Circuitry
 - Built-in Memory
 - Built-in Character Generator
- **64 Character ASCII Set**
- **Direct Access to Each Digit Independently**
- **Single 5.0 Volt Power Supply**
- **TTL Compatible**
- **Easily Interfaced to a Microprocessor**
- **IDA1414-16-1 Buffered Input Data Lines**

DESCRIPTION

The IDA1414-16 assembly is an extension of the DL1414T Intelligent Display. This assembly provides the designer with circuitry for display maintenance. It also minimizes interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

The assembly consists of four DL1414s in a single row, together with decoder and interface buffer on a single printed circuit board. Each DL1414 provides its own memory, ASCII ROM character decoder, multiplexing circuitry, and drivers for the four 17-segment LEDs.

Intelligent Display Assemblies can be used for applications such as data terminals, controllers, instruments, and other products which require an alphanumeric display.

Maximum Ratings

V_{CC}	6.0 V
Voltage, Applied to Any Input	-0.5 to V_{CC} +0.5 Vdc
Operating Temperature	0°C to $+65^\circ\text{C}$
Storage Temperature	-20°C to $+70^\circ\text{C}$
Relative Humidity (non condensing) at 65°C	85%

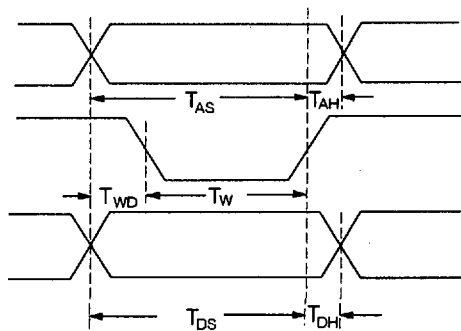
OPTOELECTRONIC CHARACTERISTICS at 25°C

Parameter	Symbol	Min.	Typ.	Max	Units	Conditions
Supply Voltage	V_{CC}	4.75		5.25	V	$V_{CC} = 5.0\text{ V}$ (10 segments/digit)
Supply Current-1 (Total)	I_{CC}			400	mA	
Supply Current-2 (Total)	I_{CC}			380	mA	
Supply Current-1 (Display Blank)	$I_{CC\text{ BLANK}}$			75	mA	$V_{CC} = 5.0\text{ V}, V_{IN} = 0$
Supply Current-2 (Display Blank)	$I_{CC\text{ BLANK}}$			25	mA	
Input Voltage-High -1 (D_0 - $D_8, A_2, A_3, \overline{WR}$) -1 (A_0, A_1)	V_{IH}	2.0 2.7 3.5			V	$V_{CC} = 4.5\text{ V}$ $V_{CC} = 5.5\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 5.5\text{ V}$
-2 (D_0 - D_8, A_0, A_1)	V_{IH}	2.7 3.5			V	
-2 ($A_2, A_3, \overline{WR}$)	V_{IH}	2.0			V	
Input Voltage-Low, All Inputs	V_{IL}			0.8	V	
Input Current-High, Any Input	I_{IH}			20	μA	
Input Current-Low, Any Input	I_{IL}			400	μA	$V_{CC} = 5.5\text{ V}, V_I = 0.4\text{ V}$
Luminous Intensity, Average/Digit	I_V		0.5		mcd	$V_{CC} = 5.0\text{ V}$ (8 segments/digit)
Peak Emission Wavelength	λ_{pk}		660		nm	
Viewing Angle			± 40		Deg.	

SWITCHING CHARACTERISTICS @ 5 V

Parameter	Symbol	0°C Typ.	+25°C Min.	+65°C Typ.	Unit
Write Pulse	T_W	300	325	350	nS
Address/DE Setup Time	T_{AS}	350	400	450	nS
Data Set Up Time	T_{DS}	350	400	450	nS
Write Set Up Time	T_{WD}	50	75	100	nS
Data Hold Time	T_{DH}	50	75	100	nS
Address/DE Hold Time	T_{AH}	50	75	100	nS

TIMING CHARACTERISTICS



Timing Measurement
Voltage Levels

4 volts
— 2 volts
0 volts

Optical Characteristics at 25°C

The IDA1414-16, Intelligent Display Assembly, has 16 alphanumeric characters and operates from just a 5 V supply. Based on the the DL1414T, four character Intelligent Display, the IDA1414-16 adds all the support logic required for direct connection to most microprocessor buses. The system interface takes place through a 14 hole dual in line pattern. Wires may be soldered directly to these holes or contact can be made with a ribbon cable and a connector, such as Berg 65493-006 or Amp 86383-1/86838-2.

System Power Requirements

Operating from a single +5 volt power supply, the IDA1414-16 requires a maximum operating current of 400 mA with ten of the segments lit on each character. With the display blanked, the board circuitry draws 75 mA maximum.

Display Interface

The display interface on the 14 pin dual in line pattern consists of seven data lines (D0 to D6), four address lines (A0 to A3), write pulse, V_{cc} , and GND.

WR (Write, active low) line must be pulsed low for minimum of 325 ns to store a character in the display memory. See the Timing Characteristics diagram for timing and relationships to other signals.

Address lines A0 to A3 are set up so that the right most character is the lowest address. The left most character is the highest address. Data lines are set up so that D0 is the least significant bit and D6 is the most significant bit.

Using The Display Interface

By using memory mapped I/O techniques, the IDA can be treated almost like a memory location—supply the data, address and proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address. After the address has stabilized, the data can change to the desired values. After the data have stabilized, the WR pulse is started and must remain low for at least 325 ns. Signals must be held stable for 75 ns minimum after the rising edge of the WR pulse to ensure correct loading while the addresses must be stable for 400 ns preceding the same rising edge of the WR pulse. Refer to the Timing Characteristics diagram.

System Design Considerations

It is often necessary, because of the nature of displays, to use a ribbon cable from the CPU board. The IDA has a 14 pin dual in line pattern for this purpose. Use IDA1414-16-1 (buffered version) rather than IDA1414-16-2 (non-buffered version) when the ribbon cable is over twelve inches. Voltage transients from noisy systems may couple through the cables into the Intelligent Display and can cause serious damage.

Avoid handling the IDA other than by the edges of the PCB. Static damage can still be a problem, so take the necessary precautions. Keep in conductive material, grounded work areas, etc.

The IDAs should need minimal cleaning, i.e., a gentle wiping with a soft damp cloth. Alcohol should *never* be used on any Intelligent Display device. Always check the chemical composition of any solvent before using on any Intelligent Display device.

Interconnection

Wires may be soldered directly to 14 hole dual in line position or contact can be made with ribbon cable and connector such as Berg 65493-006 or Amp 86838-1/86838-2

CHARACTER SET

	D0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H		
	D1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H		
	D2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H		
	D3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H		
D6	D5	D4	hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L	H	L	2	.	"	#	\$	%	&	'	<	>	*	+	,	-	.	/	
L	H	H	3	0	1	2	3	4	5	6	7	8	9	[	]	{	}	^	~
H	L	L	4	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	
H	L	H	5	p	q	r	s	t	u	v	w	x	y	z	[	\	]	^	_

All other input codes display "blank"

The circuit diagram illustrates a 4-bit parallel adder. It consists of the following components and connections:

- 74LS139 (U2):** A 4-to-16 line decoder. Its inputs are $\overline{A_3}$, $\overline{A_2}$, $\overline{A_1}$, and $\overline{A_0}$. Its outputs are S_3 , S_2 , S_1 , S_0 , and C_{out} (pin 16).
- 74LS244 (U1):** A 6-bit bus buffer. Its inputs are S_3 , S_2 , S_1 , S_0 , and C_{out} . Its outputs are D_3 , D_2 , D_1 , D_0 , and D_{out} .
- Four 74LS141 (DL1414) Decoders:** Labeled ID0, ID1, ID2, and ID3. Each decoder has a 4-bit input (ID3: $\overline{A_3}$, ID2: $\overline{A_2}$, ID1: $\overline{A_1}$, ID0: $\overline{A_0}$) and 16 outputs. The outputs of these decoders are connected to the inputs of the 74LS244 and the 74LS139.
- 74LS244 (U1) Details:** The 74LS244 is configured with its inputs C_1 and C_2 to ground (pin 14) and C_3 to VCC (pin 14). Its output pins are 1, 10, 12, 14, and 16.
- Power and Ground:** Pin 14 is connected to VCC, and pin 7 is connected to GND.

Pin	Function
1	A0 Digit Select
2	A1 Digit Select
3	D4 Data Input
4	D0 Data Input (LSB)
5	D3 Data Input
6	D2 Data Input
7	GND
8	A3 Digit Select
9	WR Write
10	A2 Digit Select
11	D6 Data Input (MSB)
12	D1 Data Input
13	D5 Data Input
14	+VCC