SGS-THOMSON MICROELECTRONICS

EF7333

CEPT PCM TRUNK CONTROLLER

DESCRIPTION

The basic function of the CEPT PCM trunk controller is to synchronize a PCM interface with the local exchange clock. The EF7333 is provided as part of a kit also containing the EF73321 PCM line transceiver. In addition to its basic function, the device also features :

INCOMING LINK PROCESSING FUNCTIONS

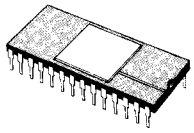
- INPUT SIGNAL HDB3, BINARY OR BIPOLAR DECODING
- FRAME SYNCHRONIZATION WITH LOCAL CLOCK
- LINE JITTER ABSORPTION
- FRAME SKIP/DOUBLING
- RECEIVE ERROR DETECTION AND ALARM GENERATION
- REMOTE ALARM EXTRACTION

OUTGOING LINK PROCESSING FUNCTIONS

- INSERTION OF SYNCHRONIZATION DATA INTO OUTGOING FRAMES
- OUTPUT SIGNAL BINARY, HDB3 OR BIPOLAR CODING
- RECEIVE FAULT ALARM TRANSMISSION

OTHER CHARACTERISTICS

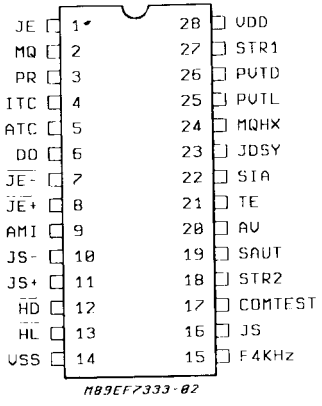
- NMOS TECHNOLOGY
- 5 V SUPPLY
- LOW POWER CONSUMPTION (200 mW)
- CONFORMS TO CCITT RECOMMENDATION G.737
- OPERATES IN STAND-ALONE MODE OR WITH MARKER INTERFACE



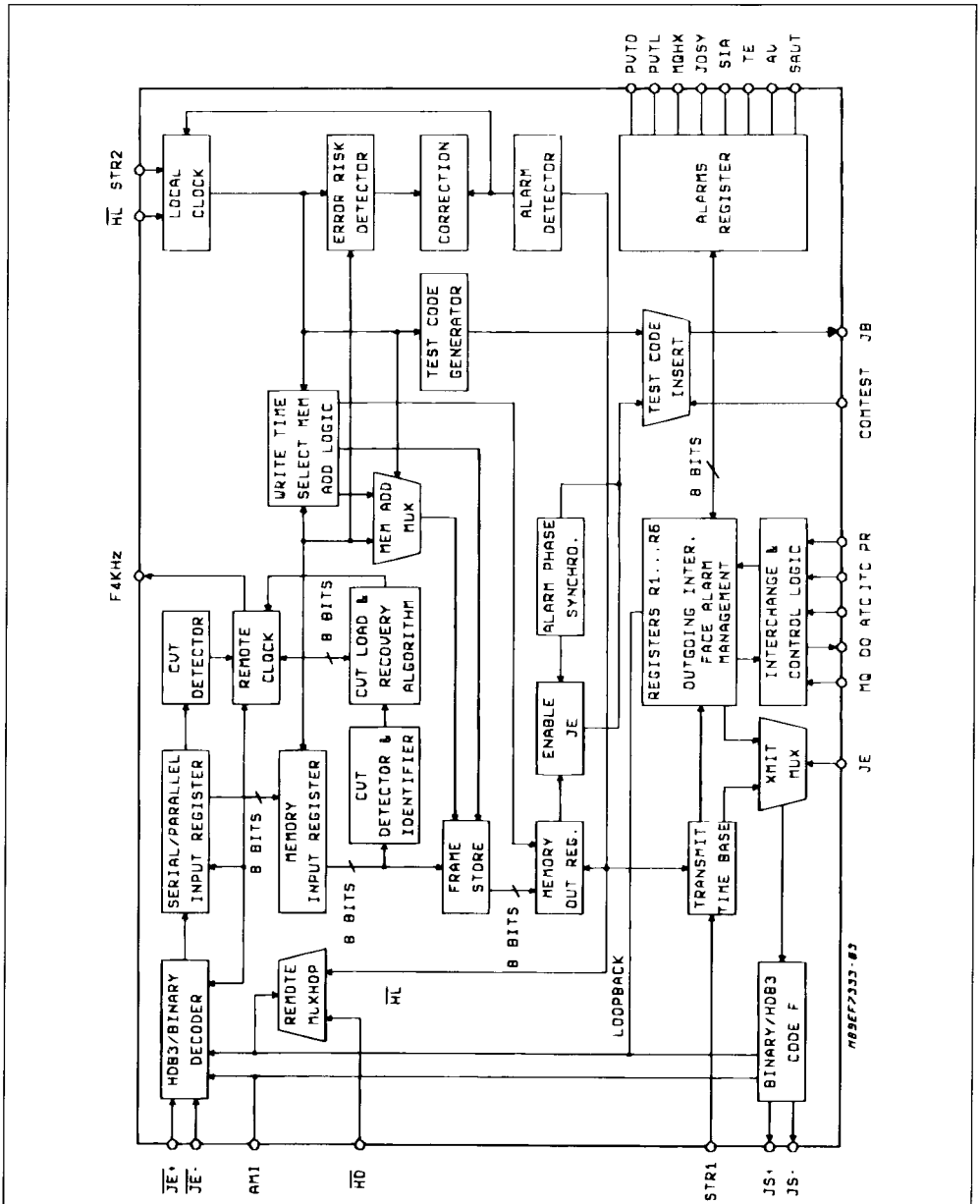
DIP28
(Ceramic)

ORDER CODE : EF7333

PIN CONNECTION



BLOCK DIAGAM



CVT : frame alignment code.

PIN DESCRIPTION

POWER SUPPLY

Name	Pin Type	N°	Function	Description
V_{SS}	Power	14	Ground	Ground
V_{DD}	Power	28	Power Supply	+ 5 V ± 5 %

CLOCKS

Name	Pin Type	N°	Function	Description
$\overline{HD}$	I	12	Distant Clock	Remote clock synchronizing incoming data at $\overline{JE^+}$, $\overline{JE^-}$, frequency 2048 kHz (jitter-free)
$\overline{HL}$	I	13	Local Clock	Local clock synchronizing outgoing data at JS, JS^+, JS^-, frequency 2048 kHz

RECEIVE

Name	Pin Type	N°	Function	Description
STR2	I	18	Synchronization Frame Signal	Local Clock Synchronization Signal Frequency 4 kHz
$\overline{JE^+}$ $\overline{JE^-}$	I I	8 7	Input Trunk	Data from remote interface at frequency of $\overline{HD}$, normally in HDB3 code
JS	O	16	Binary Data Output	Binary data from remote interface, restored to frequency of $\overline{HL}$
JDSY	O	23	Alarm	Loss of interface synchronization alarm : three consecutive frame alignment codes or three consecutive identifier absent.
TE	O	21	Alarm	Error rate alarm, as measured on incoming interface as per CCITT Recommendation G.737
PVTD	O	26	Alarm	Loss of frame alignment at remote end alarm : bit 3 in timeslot TSO of odd frames received from remote interface set to 1
PVTL	O	25	Alarm	Loss of frame alignment alarm : no frame alignment code in timeslot TSO of even frames from incoming interface
SIA	O	22	Alarm	Alarm Indication Signal : more than 75 % bits at 1 in messages received from remote end
MQHX	O	24	Alarm	Remote Clock $\overline{HD}$ Missing
SAUT	O	19	Alarm	Changes of State for Each Frame Skip or doubling Operation
AV	O	20	Alarm	"1" : Frame Skip $\overline{HD}$ Faster than $\overline{HL}$ "0" : Frame Doubling $\overline{HD}$ Slower than $\overline{HL}$
F4kHz	O	15	Remote Clock	Remote Clock Output, Frequency 4 kHz

TRANSMIT

Name	Pin Type	N°	Function	Description
STR1	I	27	Synchronization Frame Signal	Frame Synchronization Signal from Transmit Clock, Frequency 4 kHz
JE	I	1	Binary Data Input	Binary Data from Local Exchange Synchronized by $\overline{HL}$
JS^+ JS^-	O O	11 10	Output Trunk	Transcoding of data received on input JE, synchronization by $\overline{HL}$

CONTROL

Name	Pin Type	N°	Function	Description
AMI	I	9	Mode Select	Selects Transmit/receive Information Coding/decoding Mode
COMTEST	I	17	Test Command	Commands test providing for insertion of a code at the outgoing interface in order to test the network : 10101100 in Even Frame Timeslots 01010011 in Odd Frame Timeslots
PR	I	3	Validation Signal	Signal Validating ATC, ITC, DO
ATC	I	5	Address Register Input	Internal Register Addressing Input (R1...R6)
ITC	I	4	Register Content Input	Data Input for Internal Register Addressed by ATC
DO	O	6	Register Content Output	Data Output for Internal Register Addressed by ATC (in high impedance state when PR = 0)
MQ	I	2	Marker Interface Select	Operation with Marker Interface

FUNCTIONAL DESCRIPTION

NORMAL OPERATION

RECEIVE PATH. The circuit decodes the data received on inputs $\overline{JE}^+$ and $\overline{JE}^-$. There are three decoding modes, selected according to the state of the AMI pin :

- AMI = 0 HDB3code Inputs : $\overline{JE}^+$ and $\overline{JE}^-$
- AMI = 1 Bipolar code Inputs : $\overline{JE}^+$ and $\overline{JE}^-$
- AMI = 1 Binary code Input : $\overline{JE}^+$ and $\overline{JE}^- = 1$ or $\overline{JE}^-$ and $\overline{JE}^+ = 1$

The data are then formatted in eight-bit words corresponding to a timeslot and presented to the frame memory.

The circuit synchronizes the interface by analyzing the content of the channel 0 timeslots (TS0).

The circuit is synchronized when the following have been recognized :

- An even frame alignment code in frame Tn (X0011011),
- An identifier in frame $T_n + 1$ (second bit of TS0 at 1),
- An even frame alignment code in frame $T_n + 2$.

Loss of frame alignment (desynchronization) is declared on detection of the absence of three consecutive even frame alignment codes or three consecutive odd frame identifiers (see appendix 1). In this case, the outgoing interface remains at "1".

The remote clock, slaved to clock $\overline{HD}$, operates when the interface is synchronized. It delivers frame memory write addresses.

The local clock, slaved to clock $\overline{HL}$, is synchronized by signal STR2 which defines the time at which bit 8 of the even or odd frame TS0 is output by the outgoing interface device.

It delivers the frame memory read addresses (frequency 4 kHz). The frame memory capacity is 64 words x 8 bits (double frame).

Jitter absorption : there are two devices within the circuit :

Frame memory write time select.

This provided for absorbing at least ± 1 bit on each time-slot without loss of information at the outgoing interface. Write time selection and detection are instantaneous.

Frame skip or doubling.

This operation is initiated on reading frame memory address 63 (last timeslot of an odd frame Tn) :

- If the write address is between 56 and 63 (write frame Tn + 2) reading is resumed at address 32. The even frame Tn + 1 is skipped on reading.
- If the write address is between 63 and 6 (write frame Tn + 1), reading is resumed at address 32. The odd frame Tn is read again.

Under limiting conditions for this correction operation, the jitter absorbed by the circuit without loss of information is at least ± 8 TS.

The circuit detects the following alarms :

- Remote frame misalignment (PVTD),
- Incoming interface frame alignment code absent (PVTL),
- Incoming interface desynchronized (JDSY),
- Error rate > 10^{-3} (TE),
- Over than 75 % bits at "1" in received data (SIA),
- Remote clock $\overline{Hd}$ absent (MQHX),
- Frame skip or doubling (SAUT),
- Clocks plesiochronous (AV).

Alarms resulting dispositions.

When JDSY, TE or MQHX are set :

- Bit 3 of registers R5 and R2 is set to "1" and immediately transmitted to the odd TSO on the outgoing interface JS (when circuit EF7333 is used without marker interface).
- The outgoing interface JS will remain high.

When the JDSY alarm is set, the TE alarm is disabled and the F4kHz output remains at "0".

TRANSMIT PATH. The transmit multiplexing function provides for insertion at the outgoing interface of even or odd frame timeslots TS0 contained in two internal registers R1 and R2.

The transmit clock, synchronized by signal STR1, controls this multiplexing : Signal STR1 define the time at which bit 8 of the even timeslot TS0 is present at the incoming interface input (frequency 4 kHz).

In this operating mode, the content of the even TS0 is X0011011 (R1) and the content of the odd TS0 is X1XXXXXX (R2).

In the absence of a programmed value, bit 3 of the odd TS0 applies the "OR" operation to the JDSY, TE and SIA alarms.

According to the decoding mode selected for inputs $\overline{JE}$+ and $\overline{JE}$–, the code used for the data on outputs JS+ and JS– will be as follows :

- AMI = 0 HDB3 code Outputs : JS^+ and $\overline{JS}$
- AMI = 1 Bipolar code Outputs : JS^+ and $\overline{JS}$
- AMI = 1 Binary code Output : JS^+ "or" $\overline{JS}$

For proper operation, pins PR, ITC and ATC must be tied to V_{SS} when the marker interface is not selected (MQ = 0).

OPERATION WITH MARKER INTERFACE

Input MQ is at "1" in this case. This operating mode provides access to six internal registers of the circuit. (refer to APPENDIX 3).

To be replaced by the enclosed registers description

The six registers are accessible by programming pins ATC, ITC.

Pin ATC receives the register address and pin ITC receives the content to be written into the addressed register. The last bit of ATC is a read bit and the last bit of ITC is write bit. The register content may be read serially at D0.

These registers are not initialized on powering up the circuit.

BIT	1	2	3	4	5	6	7	8
Content of Register R5	PVTD	PVTL	MQHX	JDSY	SIA	TE	AV	SAUT

CIRCUIT TEST

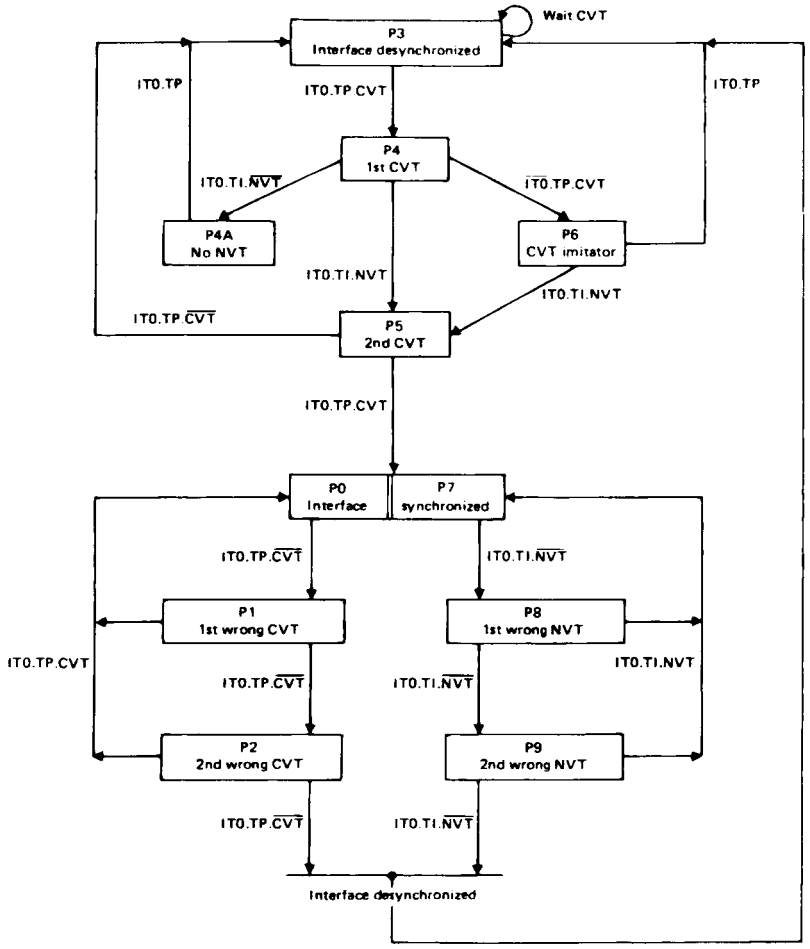
The COMTEST input is used to insert at the outgoing interface a test which is 10101100 for all even frame timeslots and 01010011 for all odd frame timeslots.

The 1-bit register R6 is used to loop the outgoing interface to the incoming interface when set to "1" (JS^+ and JS^- internaly switched to $\overline{JE}$+ and $\overline{JE}$–).

In this case, the remote clock $\overline{HD}$ is internaly switched to the local clock HL. The even and odd timeslots TS0 are then the contents of registers R3 and R4.

APPENDIX 1

FRAME ALIGNMENT LOSS AND RECOVERY ALGORITHM



- CVT : Even frame alignment code correct
- $\overline{CVT}$: Even frame alignment code not recognized
- NVT : Odd frame identifier correct
- $\overline{NVT}$: Odd frame identifier not recognized
- ITO : Channel 0 timeslot
- $\overline{ITO}$: Channels 1 - 31 timeslot
- TP : Even frame
- TI : Odd frame

APPENDIX 2

ERROR RATE ALARM

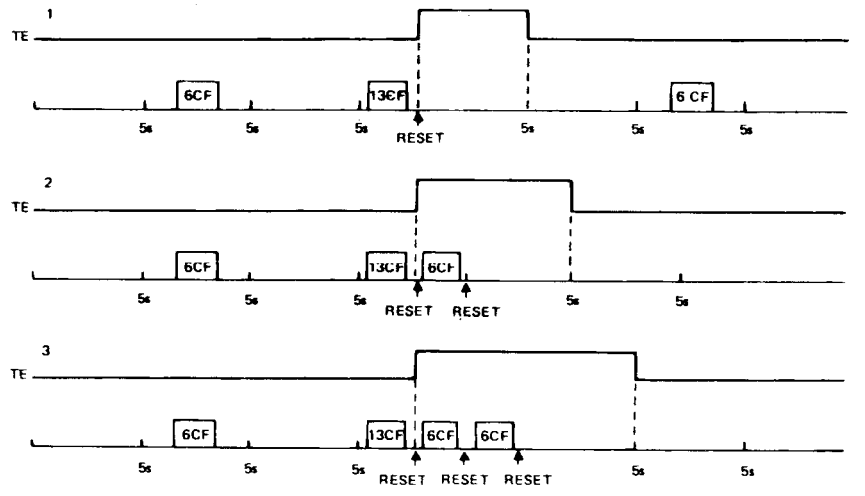
The error rate is calculated over a 5 s period, interrupted as soon as the threshold (13 even frame alignment codes wrong) is reached.

The TE alarm then goes to "1" and is reset only if the number of wrong frame alignment codes is less than six in the next 5 s period.

If not, when the six wrong frame alignment codes threshold is reached a new 5 s count is begun, the TE alarm remaining at "1".

The TE alarm is disabled when the interface is desynchronized (JDSY = 1).

EXAMPLE



CF : Wrong even frame alignment codes

APPENDIX 3

ALARM INDICATION SIGNAL

The frame examination covers 512 bits (1 double-frame), after which the JDSY alarm goes to "1" if the circuit is desynchronized. If the number of "0" bits in the frame during this interval is two or less, the alarm indication signal (SIA) goes to "1".

APPENDIX 3

REGISTERS DESCRIPTION

Register R1 : contains the outgoing junction even frame TSO value.
Only bit 1 can be accessed by the microprocessor interface. The content of this register will be transmitted in line if the circuit is not operating in looped mode.

Register R2 : contains the outgoing junction odd frame TSO value.
Only bit 2 cannot be modified, it remains at "1". Bit 3 can either be at "0" or "1" as a result of a logic OR with the 3 alarms JDSY, TE and MQHX. The content of this register will be transmitted in line only if the circuit is not operating in looped mode.

Register R3 : will contain a value to be introduced into even frame TSO (8 bits). Its content is transmitted in looped mode.

Register R4 : will contain a value to be introduced into odd frame TSO. Its content is transmitted in looped mode.

Register R5 : is a read only register containing the alarms. It is controlled by receive function of EF7333 circuit

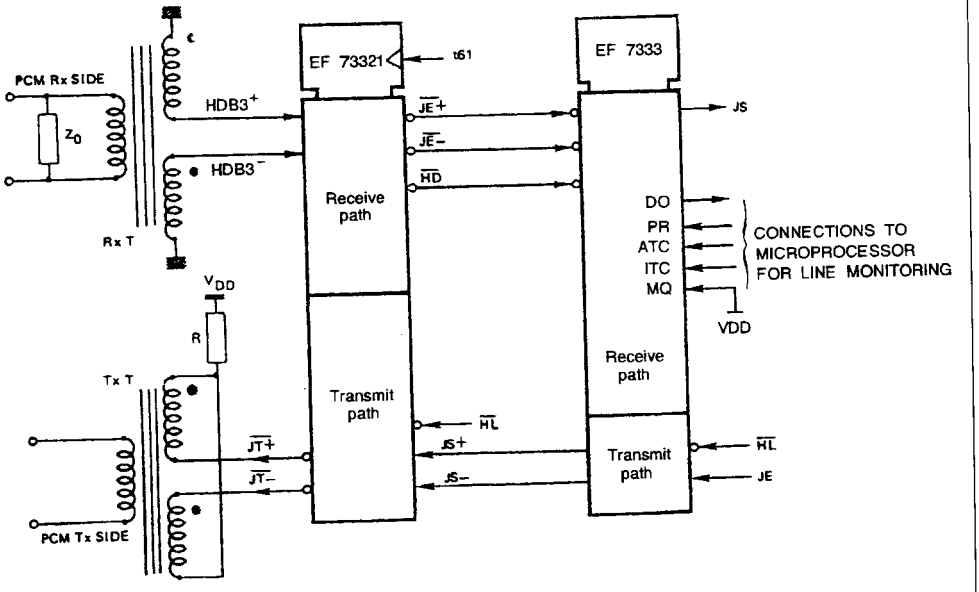
- bit 1 contains the value of bit 3 of incoming junction odd frame TSO. When the value of this bit is "1", this means that the remote end does not control the frame it receives any more. (PVTD alarm - remote frame locking loss).
- bit 2 indicates that the EF7333 synchronous device has found no frame locking code (PVTL alarm - local frame locking loss).
- bit 3 indicates that clock $\overline{HD}$ is missing (MQHX alarm).
  In this application oscillator t61 has stopped operating.
- bit 4 indicates that the synchronous device is no more synchronized (JDSY alarm - synchronization loss).
- bit 5 indicates that a SIA signal is received (SIA alarm - remote alarm indication signal). When JDSY = 0, the junction is synchronized, SIA = 0. When JDSY = 1, the junction is not synchronized, SIA = 1 during two frames.
- bit 6 indicates an excessive error rate higher than 10^{-3} detected on the frame locking codes (TE alarm).
- bit 7 indicates local clock lead or delay compared to remote clock (AV alarm)
  - AV = 1 : frame skip ($\overline{HD}$ faster than $\overline{HL}$)
  - AV = 0 : frame doubling ($\overline{HD}$ slower than $\overline{HL}$)
- bit 8 indicates frame skip or doubling on reading of internal frame memory. Its state changes on each frame skip or doubling operation (SAUT alarm).

Register R6 : contains only 1 bit for selecting the looped mode ;

- If R6 = 0, normal operation, the contents of R1 and R2 are in time.
- If R6 = 1, looped mode operation. JS+ and JS– are internally connected to $\overline{JE}$+ and $\overline{JE}$–, and $\overline{HD}$ is internally connected to $\overline{HL}$. The contents of R3 and R4 are in line.

TYPICAL APPLICATION

Using EF7333 and EF73321 in a 2048 kHz PCM line
For data transmission/reception and frame monitoring



t61 : 16384 kHz clock
R x T : Line receiver transformer
T x T : Line transmit transformer
$\overline{HL}$: Local 2048 kHz clock

Note : EF73321 layout considerations : for correct operation of transmission drivers a 100 nF decoupling capacitor must be connected between V_{DD} and V_{SS} as close as possible to the supply pins.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}, V_{SS}	Supply Voltage	$-0.3\ V < V_{DD}-V_{SS} < 7\ V$	V
V_I	Input Voltage	$V_{SS}-0.3\ V \le V_I \le V_{DD} + 0.3\ V$	V
P	Maximum Power Dissipation	Pmax = 600 mW	mV
T_{stg}	Storage Temperature Range	− 55 °C to 125 °C	°C

STATIC ELECTRICAL CHARACTERISTICS

Ambient Temperature Range : 0 °C to 70 °C–TYPICAL VALUES AT 25 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
P_W	Power Consumption		200	450	mW
C_e	Stray Capacitance between One Input and Ground		5	10	pF
C_s	Stray Capacitance between One Output and Ground		5		pF

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	− 0.3		0.6	V
V_{IH}	Input High Voltage	2.2		V_{DD}+0.3	V
$\|I_{IL}\|$	Input Low Current (V_I = 0 V)			1	µA
I_{IH}	Input High Current ($V_I = V_{DD}$)			1	µA

OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage (I_{OL} = 0.4 mA)			0.4	V
V_{OH}	Output High Voltage (I_{OH} = − 40 µA)	2.5			V
$\|I_Z\|$	DO Output Leakage Current (0.4 V ≤ V_O ≤ 2.4 V)			10	µA

DYNAMIC ELECTRICAL CHARACTERISTICS

Ambient Temperature Range : 0 °C to 70 °C–TYPICAL VALUES AT 25 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Clocks $\overline{HD}$, $\overline{HL}$ (fig. 1)				
T	Period $\overline{HD}$	350	488	2000	ns
t_{WL}	Duration when Low $\overline{HD}$	150			ns
T	Period $\overline{HL}$ (duty cycle = 1/2 ± 5 %)	450	488	2000	ns
t_{TLH}	Rise Time		10	25	ns
t_{THL}	Fall Time		10	25	ns
	Inputs $\overline{JE}^+$, $\overline{JE}^-$/$\overline{HD}$. (fig. 2)				
$t_{set\text{-}up}$	Set-up Time	50			ns
t_{hold}	Hold Time	30			ns
	Inputs STR1, STR2, COMTEST, JE/$\overline{HL}$. (fig. 2)				
$t_{set\text{-}up}$	Set-up Time	50			ns
t_{hold}	Hold Time	30			ns
t_{PLH}	Outputs JS^+, JS^-, JS, F4 kHz (C_L = 50 pF)-(fig. 3)			250	ns
t_{PHL}	Propagation Time			250	ns

Alarms TE, SIA, JDSY, MQHX, PVTD, PVTL, SAUT, AV are held for 512 $\overline{HD}$ or $\overline{HL}$ clock pulses.
Inputs AMI and MQ are wired to a fixed value ("0" or "1") according to the selected operating mode.

Figure 1.

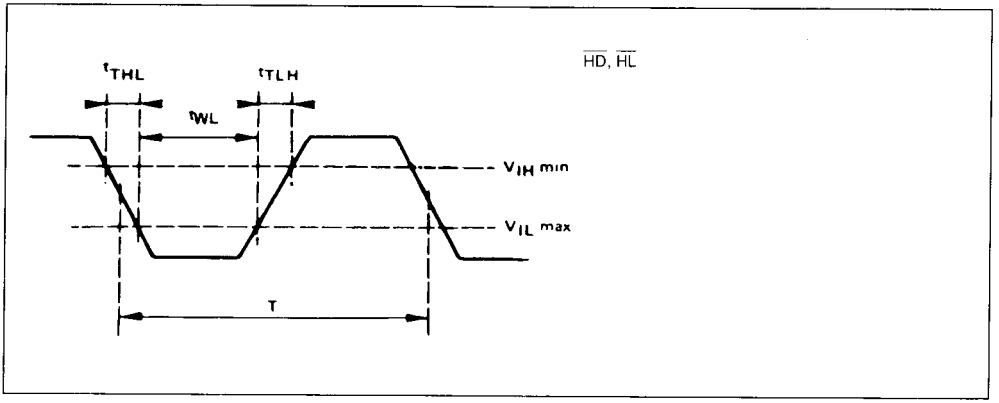


Figure 2.

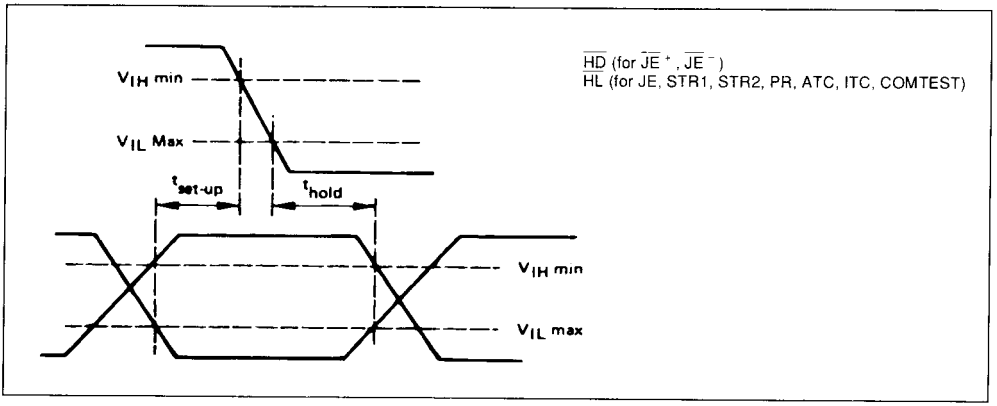
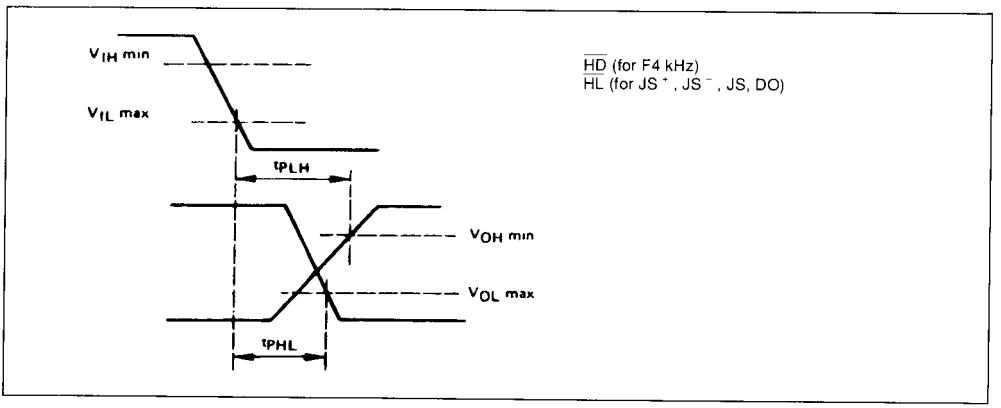


Figure 3.



TIMING DIAGRAMS

Figure 4 : Outgoing Interface Synchronization by STR2.

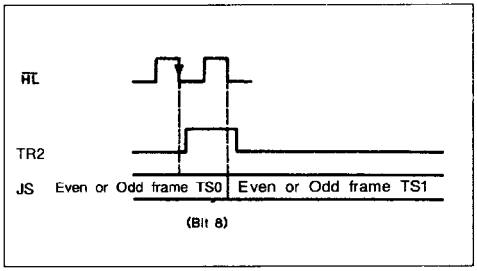


Figure 5 : Incoming Interface Synchronization by STR1.

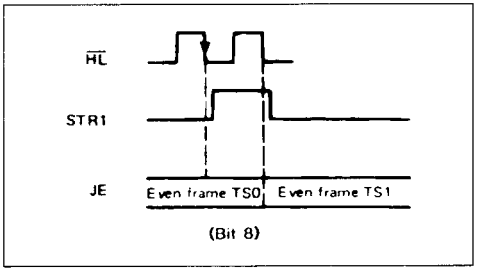


Figure 6 : PVTD alarm.

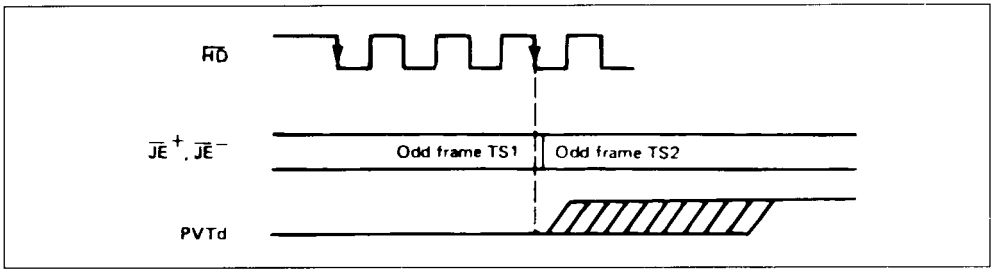


Figure 7 : PVTL alarm.

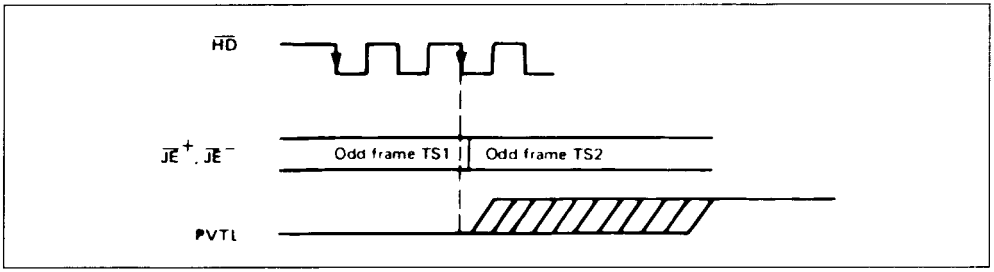


Figure 8 : TE alarm.

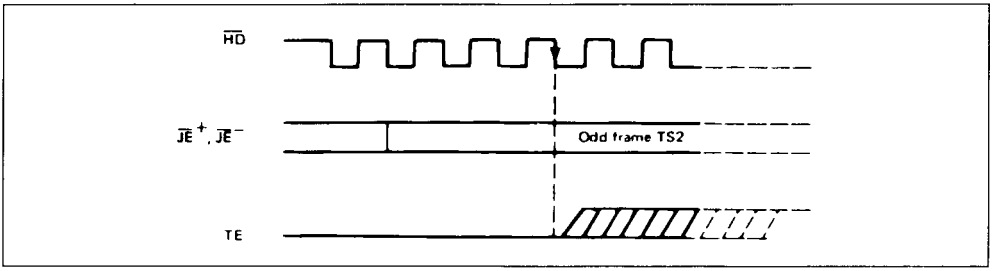


Figure 9 : MQHX alarm.

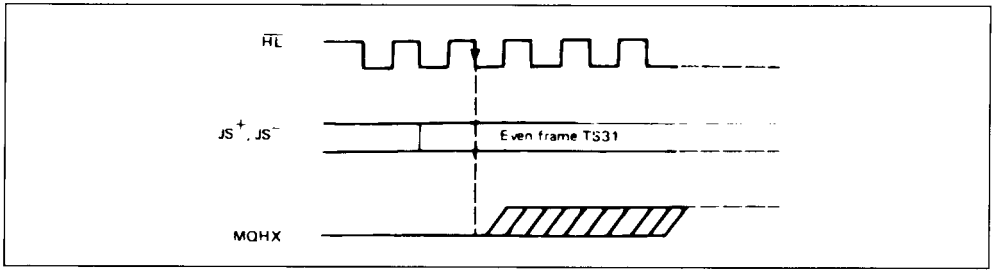


Figure 10 : Frame Doubling.

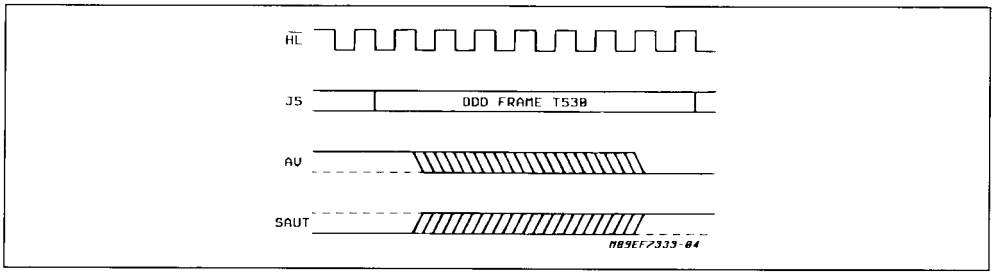


Figure 11 : Frame Skip.

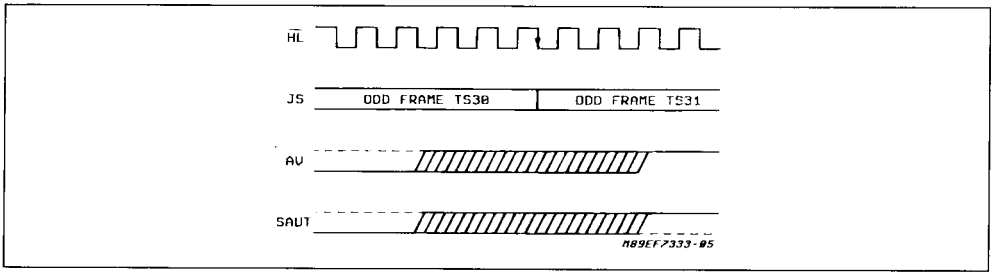


Figure 12 : JDSY alarm

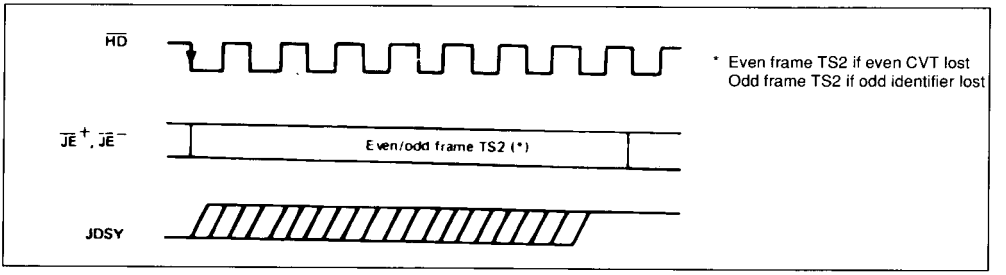
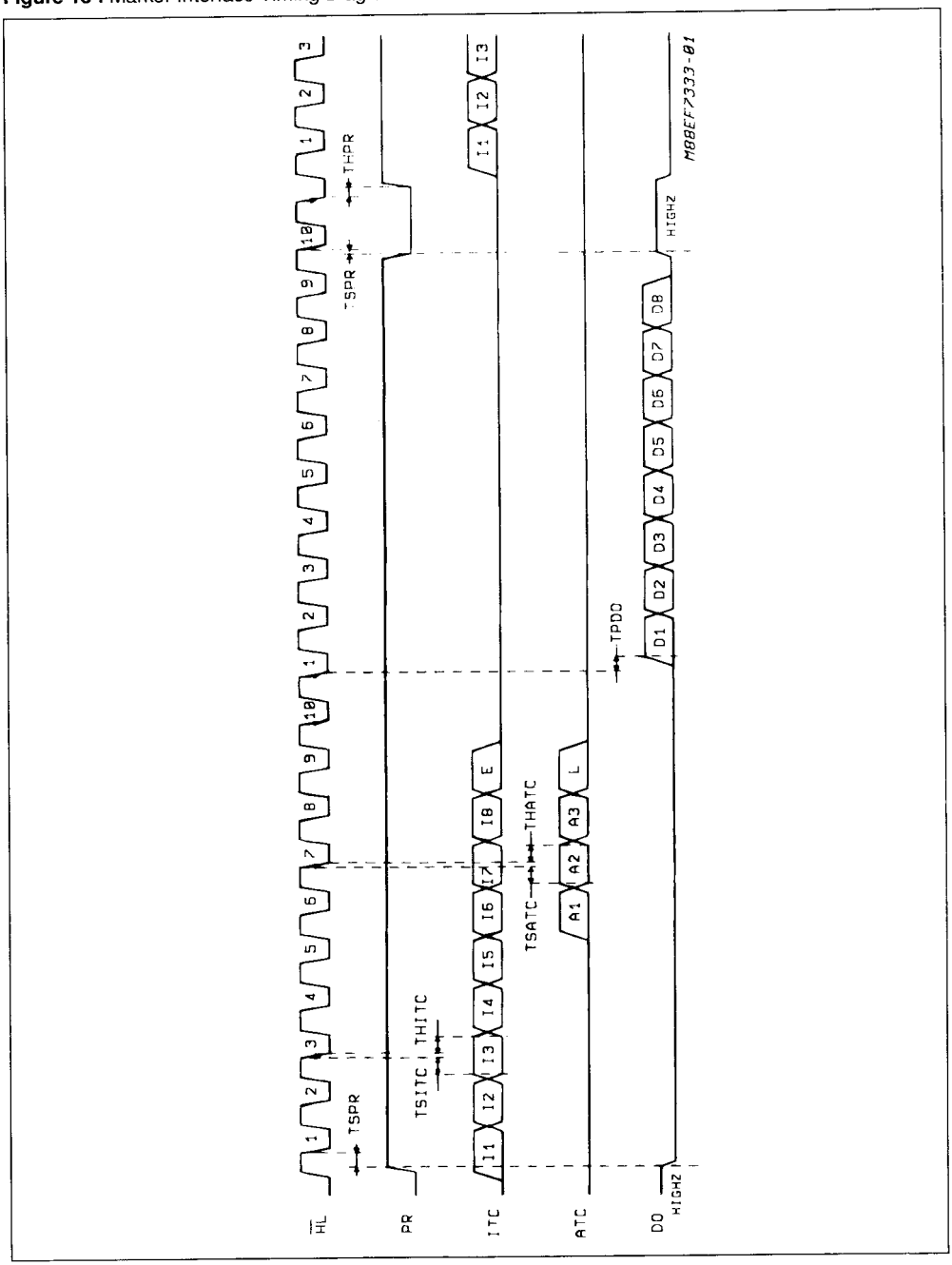


Figure 13 : Marker Interface Timing Diagram.

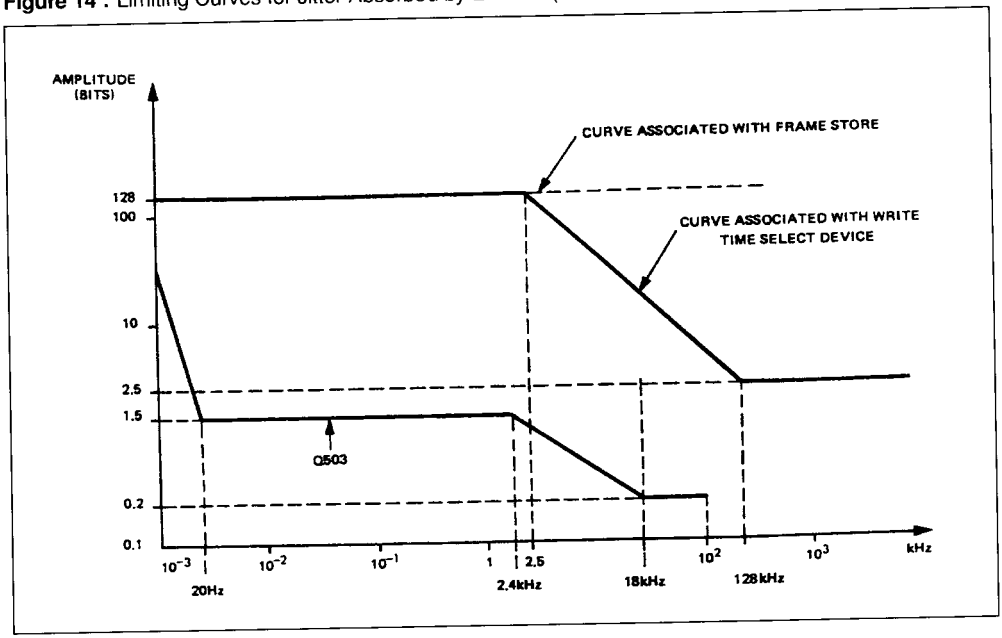


Symbol	Parameter	Min.	Typ.	Max.	Unit
TSPR	Set-up Time	50			ns
THPR	Hold Time	30			ns
TSITC	Set-up Time	50			ns
THITC	Hold Time	30			ns
TSATC	Set-up Time	50			ns
THATC	Hold Time	30			ns
TPDO	Propagation Time (C_L = 50 pF)			300	ns

ADDRESSING			
A1	A2	A3	Addressed Register
1	0	0	R1
0	1	0	R2
1	1	0	R3
0	0	1	R4
1	0	1	R5
0	1	1	R6

L = 1 E = 0 Read
L = 0 E = 1 Write
L = 1 E = 1 Write and then read

Figure 14 : Limiting Curves for Jitter Absorbed by EF7333 (without loss of information or frame skipping).



T-90-20

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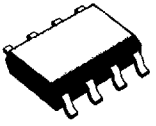
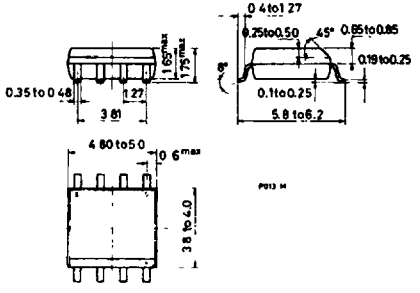
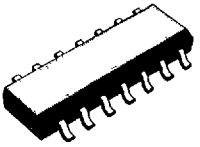
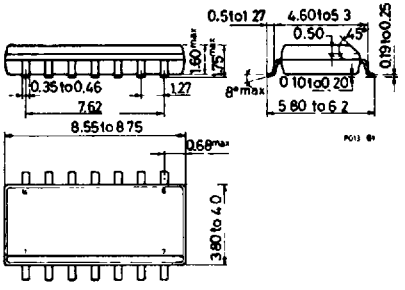
SO-8J



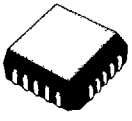


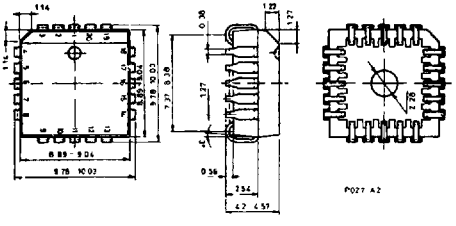
SO-14J



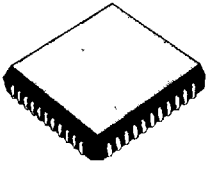


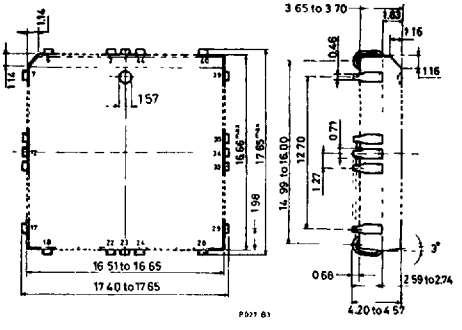
PLCC20



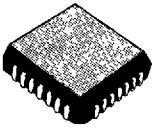


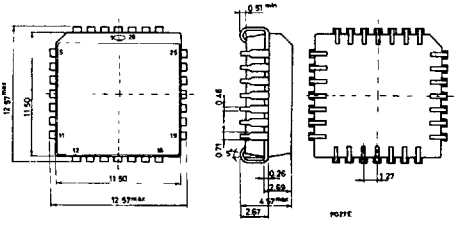
PLCC44



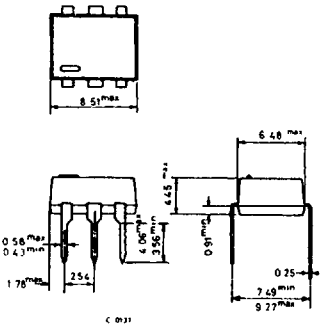


PLCC-28 Plastic Chip Carrier

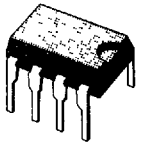


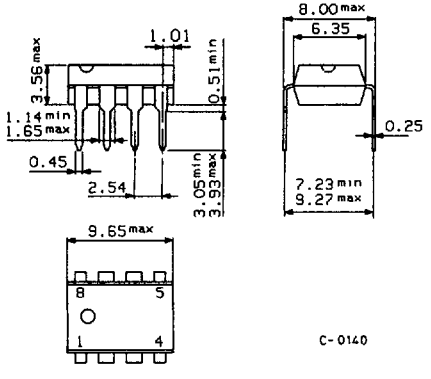


DIP-6

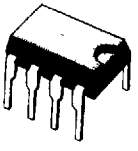


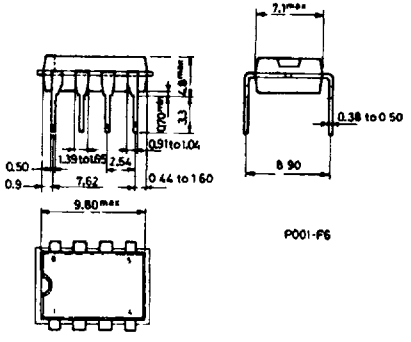
Minidip A Plastic



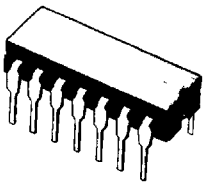


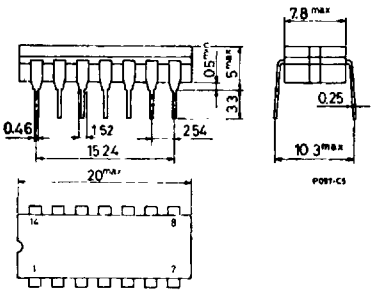
8 lead Plastic Minidip



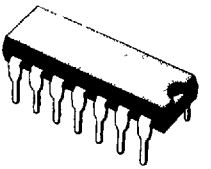


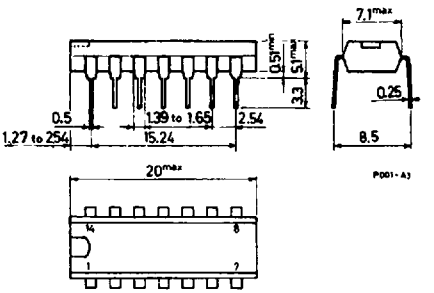
14 lead Ceramic Dip



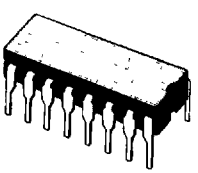


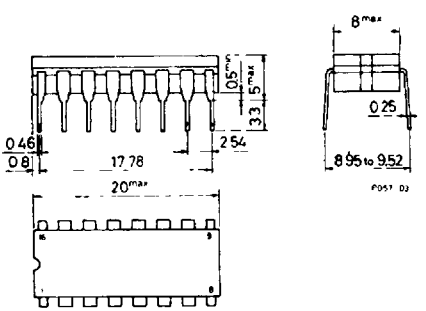
14 lead Plastic Dip



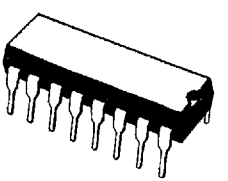


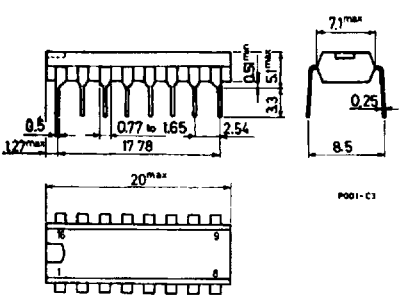
16 lead Ceramic Dip



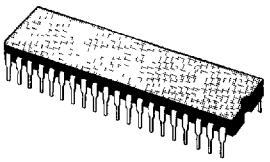


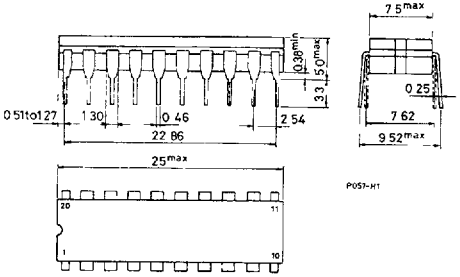
16 lead Plastic Dip (0.25)



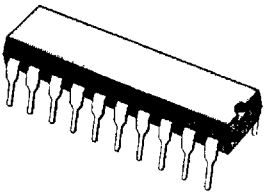


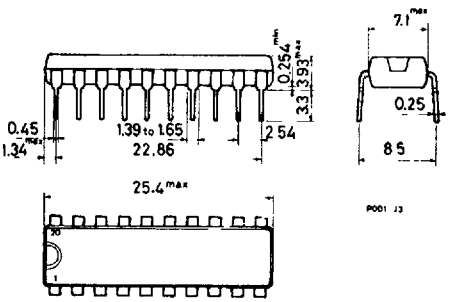
DIP-20 Ceramic



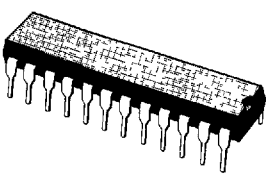


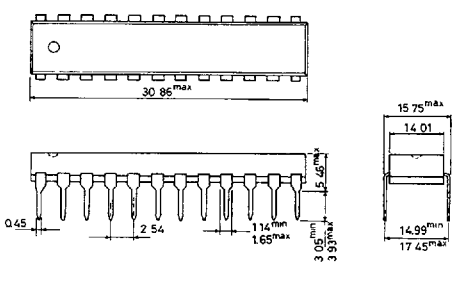
20 lead Plastic Dip (0.25)



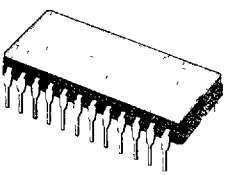


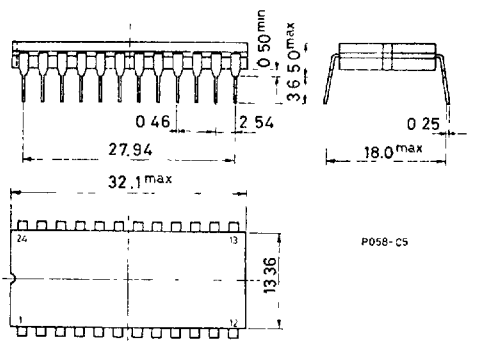
DIP-24 Plastic



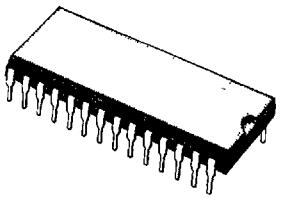


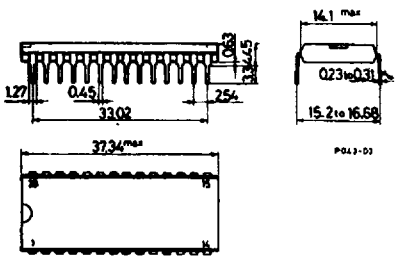
DIP-24 Ceramic (0.25)



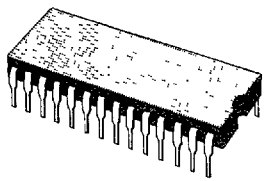


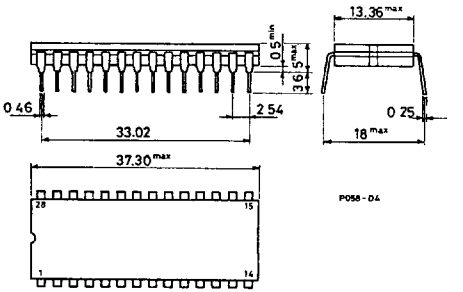
28 lead Plastic Dip



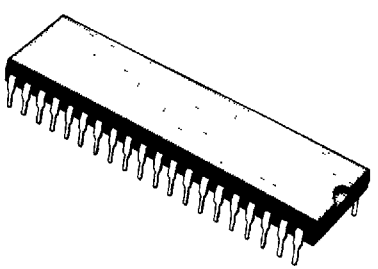


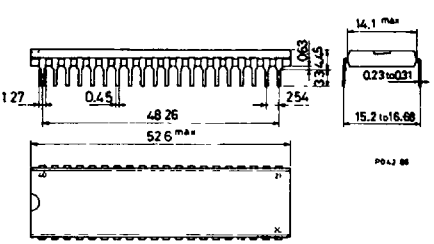
DIP-28 Ceramic (0.25)



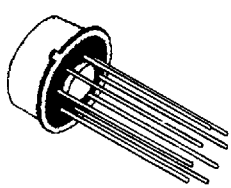


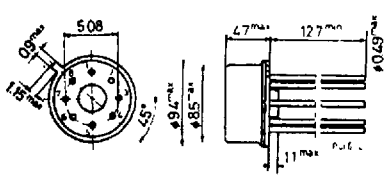
40 lead Plastic Dip





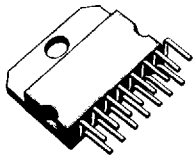
TO-99

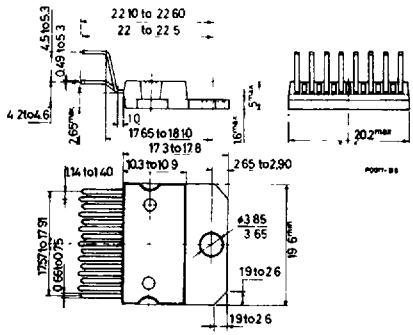




PACKAGES

MULTIWATT-15





FLEXIWATT-15