REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R124-95.	95-04-28	Monica L. Poelking
B	Changes in accordance with NOR 5962-R003-96.	95-10-13	Monica L. Poelking
C	Add device type 03. Update boiler plate, editorial changes throughout.	96-03-12	Monica L. Poelking
D	Changes in accordance with NOR 5962-R300-97.	97-05-15	Monica L. Poelking
E	Changes in accordance with NOR 5962-R347-97.	97-06-19	Monica L. Poelking
F	Add case outlines Z and U. Editorial changes throughout. - LTG	97-09-05	Monica L. Poelking
G	Add device type 04. Editorial changes throughout. - TMH	97-10-20	Monica L. Poelking
H	Changes in accordance with NOR 5962-R170-98.	98-09-14	Monica L. Poelking
J	Device type 01 no longer available from an approved source of supply. Change junction temperature for max ratings. Editorial changes throughout. - GAP	99-11-10	Raymond Monnin

REV																				
SHEET	55	56																		
REV	J	J																		
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
94-08-12

REVISION LEVEL
J

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-94669**

SHEET 1 OF 57

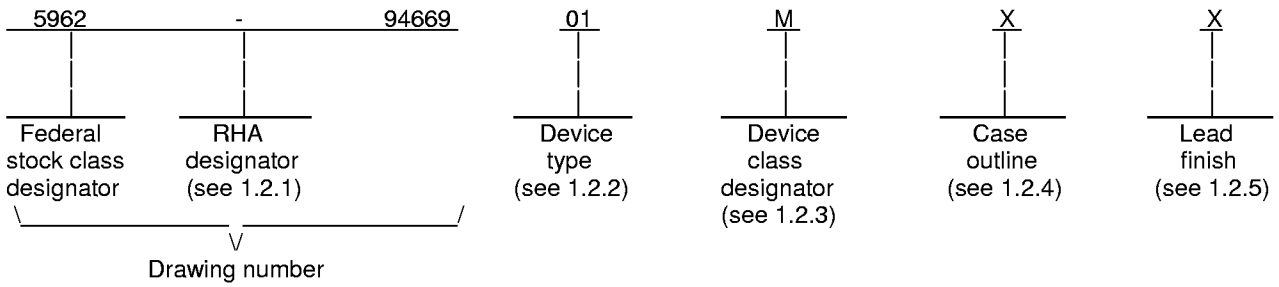
DSCC FORM 2233
APR 97

5962-E031-00

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and Appendix F of MIL-PRF-38535, "General provisions for TAB microcircuits" and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C40-33	Digital signal processor
02	320C40-40	Digital signal processor
03	320C40-50	Digital signal processor
04	320C40-60	Digital signal processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.
Q or V	Certification and qualification to MIL-PRF-38535 and Appendix F of MIL-PRF-38535.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X 1/	See figure 1	325	Pin grid array
Y	See figure 1	352	Quad flat package with non-conductive tie-bar
Z	See figure 1	325	Tape automated bond
U	See figure 1	325	Environmentally protected tape automated bond

1/ Pins in the outer excise area are solder coated. Pins in the inner excise area remain gold.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 and Appendix F of MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535 for device class M.

1.3 Absolute maximum ratings. 1/

Storage Temperature	-65°C to +150°C
Input voltage	-0.3 V to 7 V
Output voltage	-0.3 V to 7 V
Supply voltage	-0.3 V to 7 V
Power dissipation	4.7 W
Lead temperature (soldering, 10 seconds)	260°C
Junction temperature (T_J)	
Case X and Y	150°C
Case Z, U, and bare die designator 9	125°C
Thermal resistance, junction-to-case (θ_{JC})	
Case X	3°C/W
Case Y	2°C/W
Maximum die temperature rise for the die at 100%	
Cases Z and U	0.9°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	
device 01	4.5 V ≤ V_{CC} ≤ 5.5 V
devices 02, 03 and 04	4.75 V ≤ V_{CC} ≤ 5.25 V
High level input voltage (V_{IH}) 2/	
X2/CLKIN, $\overline{\text{CRDYX}}$	2.6 V ≤ V_{IH} ≤ V_{DD} + 0.3 V
$\overline{\text{CSTRBX}}$, $\overline{\text{CREQX}}$, $\overline{\text{CACKX}}$	2.2 V ≤ V_{IH} ≤ V_{DD} + 0.3 V
All other pins	2.0 V ≤ V_{IH} ≤ V_{DD} + 0.3 V
Low level input voltage (V_{IL}) 2/	-0.3 ≤ V_{IL} ≤ 0.8
High level output current (I_{OH})	-300 µA
Low level output current (I_{OL})	2 mA
Maximum operating temperature (T_C)	
devices 01, 02, 03	-55°C to +125°C
device 04	-55°C to +100°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum V_{IH} levels and minimum V_{IL} level are characterized but not tested.
3/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, and Appendix F MIL-PRF-38535 "General provisions for TAB microcircuits", and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, Appendix F of MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A, Appendix F of MIL-PRF-38535 and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundry scan codes. The boundry scan instruction codes shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535 (see 3.1 herein). Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and Appendix F of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. All devices shall be compliant with IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device Type	Limits		Unit
					Min	Max	
DC electricals 2/							
High level output voltage	V_{OH}	V_{DD} = MIN, I_{OH} = MAX	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	V_{DD} = MIN, I_{OL} = MAX	1,2,3	All		0.6	
Three-state current	I_Z	V_{DD} = MAX	1,2,3	All	-20	20	µA
Input current	I_I	V_I = V_{SS} to V_{DD}	1,2,3	All	-10	10	
Input current, TDI, TCK, and TMS	I_{IPU}	V_I = V_{SS} to V_{DD} 3/	1,2,3	All	-400	20	
Input current, $\overline{TRST}$	I_{IPD}	V_I = V_{SS} to V_{DD} 3/	1,2,3	All	-20	400	
Input current, X2/CLKIN only	I_{IC}	V_I = V_{SS} to V_{DD}	1,2,3	All	-50	50	
Supply current	I_{CC}	T_A = 25°C, V_{DD} = MAX, f_x = MAX 4/	4	All		850	mA
Input capacitance	C_I	See 4.4.1c	4	All		15	pF
Output capacitance	C_O	See 4.4.1c	4	All		15	
Functional testing		See 4.4.1b	7,8	All			
CLKIN, H1, H3 timing							
CLKIN fall time	1	See figure 5	9,10,11	All		5 5/	ns
CLKIN low pulse duration, $t_{c(CI)}$ = min	2		9,10,11	01 02 03 04	10 8.5 7 5		
CLKIN high pulse duration, $t_{c(CI)}$ = min	3		9,10,11	01 02 03 04	10 8.5 7 5		
CLKIN rise time	4		9,10,11	All		5 5/	
CLKIN cycle time	5		9,10,11	01 02 03 04	30 25 20 16.67		
H1/H3 fall time	6		9,10,11	All		3	
H1/H3 low pulse duration 6/	7		9,10,11	All		P+6	
H1/H3 high pulse duration 6/	8		9,10,11	All		P+6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
H1/H3 rise time	9	See figure 5	9,10,11	All		4	ns
Delay from H1(H3) low to H3(H1) high	9.1		9,10,11	All		4	
H1/H3 cycle time	10		9,10,11	01 02 03 04	60 50 40 33.3	485 485 485 485	
Memory read/write $\overline{(L)STRB}$ = 0 7/							
Delay time, H1 low to $\overline{(L)STRB}$ low	1	See figure 5	9,10,11	01-03 04	0 5/ 0	10 8	ns
Delay time, H1 low to $\overline{(L)STRB}$ high	2		9,10,11	01-03 04	0 5/ 0	10 8	
Delay time, H1 high to (L)$\overline{R}$/$\overline{W}$ low	3		9,10,11	01-03 04	0 5/ 0	9 8	
Delay time, H1 low to (L)$\overline{A}$ valid	4		9,10,11	01 02 03 04	0 0 0 5/ 0	10 10 9 8	
Setup time, (L)D valid before H1 low (read)	5		9,10,11	01-03 04	15 9		
Hold time, (L)D hold time after H1 low	6		9,10,11	All	0		
Setup time, $\overline{(L)RDY}$ valid before H1 low (read)	7		9,10,11	01-03 04	25 18 5/		
Hold time, $\overline{(L)RDY}$ hold time after H1 low	8		9,10,11	All	0		
Delay time, H1 low to (L)STAT3-(L)STAT0 valid	8.1		9,10,11	01-03 04		10 8	
Delay time, H1 low to (L)$\overline{R}$/$\overline{W}$ high (write)	9		9,10,11	01-03 04	 0 5/	9 8	
(L)D valid after H1 low (write)	10		9,10,11	01-03 04		16 13	
(L)D hold time after H1 high (write)	11		9,10,11	All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
Delay time, H1 high to address valid on back-to-back write cycles	12	See figure 5	9,10,11	01-03 04		13 8	ns
$\overline{DE}$, $\overline{AE}$, and $\overline{CE}$ enable timing							
Delay time, $\overline{(L)DE}$ high to (L)D0-(L)D31 in high-impedance state	1 8/	See figure 5	9,10,11	All	0 5/	15	ns
Delay time, $\overline{(L)DE}$ (L)DE low to (L)D0-(L)D31 valid	2		9,10,11	01-03 04	0 5/ 0	22 16	
Delay time, $\overline{(L)AE}$ high to (L)A0-(L)A31 in high-impedance state	3 8/		9,10,11	All	0 5/	15	
Delay time, $\overline{(L)AE}$ low to (L)A0-(L)A31 valid	4 8/		9,10,11	01-03 04	0 5/ 0	21 16	
Delay time, $\overline{(L)CE}$ high to (L)R/$\overline{W0}$, (L)R/$\overline{W1}$ in high-impedance state	5 8/	See figure 5	9,10,11	All	0 5/	15	ns
Delay time, $\overline{(L)CE}$ low to (L)R/$\overline{W0}$, (L)R/$\overline{W1}$	6		9,10,11	01-03 04	0 5/ 0	21 16	
Delay time, $\overline{(L)CE}$ high to (L)STRB0, (L)STRB1 in high-impedance state	7 8/		9,10,11	All	0 5/	15	
Delay time, $\overline{(L)CE}$ low to (L)STRB0, (L)STRB1 valid	8		9,10,11	01-03 04	0 5/ 0	21 16	
Delay time, $\overline{(L)CE}$ high to (L)PAGE0, (L)PAGE1 in high-impedance state	9 8/		9,10,11	All	0 5/	15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{\text{(L)CE}}$ low to (L)PAGE0, (L)PAGE1 valid	10	See figure 5	9,10,11	01-03 04	0 5/ 0	21 16	ns
$\overline{\text{(L)LOCK}}$ when executing LDFI or LDII							
Delay time H1 low to $\overline{\text{(L)LOCK}}$ low	1	See figure 5	9,10,11	01 02 03 04		11 11 9 8	ns
$\overline{\text{(L)LOCK}}$ when executing STFI or STII							
Delay time H1 low to $\overline{\text{(L)LOCK}}$ low	1	See figure 5	9,10,11	01 02 03 04		11 11 9 8	ns
$\overline{\text{(L)LOCK}}$ when executing SIGI							
Delay time H1 low $\overline{\text{(L)LOCK}}$ low	1	See figure 5	9,10,11	01 02 03 04		11 11 9 8	ns
Delay time H1 low to $\overline{\text{(L)LOCK}}$ low	2		9,10,11	01 02 03 04		11 11 9 8	
(L)PAGE 0, (L)PAGE 1 during memory accesses to a different PAGE							
Delay time H1 low to PAGE high for access to different page	1	See figure 5	9,10,11	01-03 04	0 0	10 8	ns
Delay time H1 low to PAGE low for access to different page	2		9,10,11	01-03 04	0 0	10 8	
Loading IIF registers when configured as output pin							
H1 low to IIOF valid	1	See figure 5	9,10,11	01 02 03 04		18 18 16 14	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
IIOF changing from output to input mode							
IIOF hold time after H1 low	1	See figure 5	9,10,11	All		14 5/	ns
IIOF setup time before H1 low	2		9,10,11	All	11		
IIOF hold time after H1 low	3		9,10,11	All	0		
IIOF changing from input to output mode							
Delay time, H1 low to IIOF switching from input to output	1	See figure 5	9,10,11	01-03 04		16 14	ns
$\overline{\text{RESET}}$							
Setup time for $\overline{\text{RESET}}$ before CLKIN low 6/	1	See figure 5	9,10,11	01-03 04	11 11	P P5/	ns
Delay time, CLKIN high to H1 high	2.1		9,10,11	01 02 03 04	2 2 2 2	12 12 10 10	
Delay time, CLKIN high to H1 low	2.2		9,10,11	01 02 03 04	2 2 2 2	12 12 10 10	
Setup time for $\overline{\text{RESET}}$ high before H1 low and after 10 H1 clock cycles	3		9,10,11	All	13		
Delay time, CLKIN high to H3 low	4.1		9,10,11	01 02 03 04	2 2 2 2	12 12 10 10	
Delay time, CLKIN high to H3 high	4.2		9,10,11	01 02 03 04	2 2 2 2	12 12 10 10	
Delay time, H1 high to (L)D high-impedance	5 8/		9,10,11	All		13 5/	
Delay time, H1 high to (L)A high-impedance	6 8/		9,10,11	All		9 5/	
Delay time, H3 high to control signals high (low for (L)PAGE)	7 8/		9,10,11	All		9 5/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
Delay time, H1 high to $\overline{\text{IACK}}$ high	8 8/	See figure 5	9,10,11	All		9 5/	ns
Delay time, $\overline{\text{RESET}}$ low to asynchronously reset signals high-impedance	9 8/		9,10,11	All		21 5/	
Delay time, $\overline{\text{RESET}}$ low to asynchronously reset signals high	10 8/		9,10,11	All		15 5/	
IIOF3-IIOF0 interrupt response 9/ 10/							
IIOF3-IIOF0 setup time before H1 low	1	See figure 5	9,10,11	01-03 04	11 11 5/		ns
Interrupt pulse duration to assure one interrupt seen 11/	2		9,10,11	All	P	<2P 5/	
$\overline{\text{IACK}}$ 12/							
Delay time, H1 high to $\overline{\text{IACK}}$ low	1	See figure 5	9,10,11	01-03 04		9 7	
Delay time, H1 high $\overline{\text{IACK}}$ high during first cycle of $\overline{\text{IACK}}$ instruction data read	2		9,10,11	01-03 04		9 7	
Communication-port word transfer cycle							
Word transfer period (4 bytes = 1 word) 8/ 13/ 14/ 15/	1	See figure 5	9,10,11	All	1.5P+7	2.5P+170	
$\overline{\text{CRDY}}$ low to $\overline{\text{CSTRB}}$ low between back-to-back write cycles 8/ 13/ 14/	2		9,10,11	All	1.5P+7	2.5P+28	
Communication port BYTE timing (write and read)							
Setup time, data valid before $\overline{\text{CSTRB}}$ (write)	1	See figure 5	9,10,11	All	2		
Delay time, $\overline{\text{CRDY}}$ low $\overline{\text{CSTRB}}$ high (write)	2		9,10,11	All	0 5/	12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
CD hold time after $\overline{\text{CRDY}}$ low (write)	3	See figure 5	9,10,11	All	2		ns
Delay time, $\overline{\text{CRDY}}$ high to $\overline{\text{CSTRB}}$ low for subsequent bytes (write)	4		9,10,11	All	0 5/	12	
Byte period 8/ 16/	5		9,10,11	All		44	
Delay time, $\overline{\text{CSTRB}}$ low $\overline{\text{CRDY}}$ low (read)	6		9,10,11	All	0 5/	10	
Setup time, CD valid after $\overline{\text{CSTRB}}$ (read)	7		9,10,11	All	0		
Hold time, CD valid after $\overline{\text{CRDY}}$ low (read)	8		9,10,11	All	11		
Delay time, $\overline{\text{CSTRB}}$ high $\overline{\text{CRDY}}$ high (read)	9		9,10,11	All	0 5/	10	
Communication token transfer sequence input to an output port 6/							
Delay time, $\overline{\text{CACK}}$ low to $\overline{\text{CSTRB}}$ change from input to a high level output 6/	1 17/	See figure 5	9,10,11	All	0.5P+22	1.5P+22	ns
Delay time, $\overline{\text{CACK}}$ low to start of $\overline{\text{CREQ}}$ going high for token request acknowledge	2 17/		9,10,11	All	P+5	2P+26	
Delay time, start of $\overline{\text{CREQ}}$ going high to $\overline{\text{CREQ}}$ change from output to an input 6/	3		9,10,11	All	0.5P-5	0.5P+13	
Delay time, start of $\overline{\text{CREQ}}$ going high to $\overline{\text{CACK}}$ change from input to an output level high 6/	4		9,10,11	All	0.5P-5	0.5P+13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
Delay time, start of $\overline{\text{CREQ}}$ going high to CD(7-0) change from inputs driven to outputs down 6/	4.1	See figure 5	9,10,11	All	0.5P-5	0.5P+13	ns
Delay time, start of $\overline{\text{CREQ}}$ going high to CRDY change from an output to an input	4.2 6/		9,10,11	All	0.5P-5	0.5P+13	
Delay time, start of $\overline{\text{CREQ}}$ going high to $\overline{\text{CSTRB}}$ low for start of word transfer out	5 6/		9,10,11	All	1.5P-8	1.5P+9	
Delay time, start of $\overline{\text{CREQ}}$ going high to $\overline{\text{CSTRB}}$ low for start of word output	6 6/		9,10,11	All	3.5P+12	5.5P+48	
Communication token transfer sequence output to an input port							
Delay time, $\overline{\text{CREQ}}$ low to start of $\overline{\text{CACK}}$ going low for token request acknowledge	1 6/ 18/	See figure 5	9,10,11	01-03 04	P+5 P+5	2P+26 2P+22	ns
Delay time, $\overline{\text{CRDY}}$ low at end of word transfer out to start $\overline{\text{CACK}}$ going low	2 6/ 18/		9,10,11	All	P+6	2P+27	
Delay time, start of $\overline{\text{CACK}}$ going low to CD7-CD0 change from outputs to inputs	3 6/		9,10,11	All	0.5P-8	0.5P+8	
Communication token transfer sequence output to an input port - Continued.							
Delay time, start of $\overline{\text{CACK}}$ going low to $\overline{\text{CRDY}}$ change from an input to output, high level	4 6/	See figure 5	9,10,11	All	0.5P-8	0.5P+8	ns
Delay time, $\overline{\text{CREQ}}$ high to $\overline{\text{CREQ}}$ change from an input to output, high level	5 18/		9,10,11	All	4	22	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{\text{CREQ}}$ high to $\overline{\text{CACK}}$ change from output to an input	6 18/	See figure 5	9,10,11	All	4	22	ns
Delay time, $\overline{\text{CREQ}}$ high to $\overline{\text{CSTRB}}$ change from output to an input	7 18/		9,10,11	All	4	22	
Delay time, $\overline{\text{CREQ}}$ high to $\overline{\text{CREQ}}$ low for the next token request	8 6/ 18/		9,10,11	All	P-4	2P+8	
Timer pin 19/							
TCLK setup time before H1 low	1	See figure 5	9,10,11	All	10		ns
TCLK hold time after H1 low	2		9,10,11	All	0		
Delay time, TCLK valid after H1 high	3		9,10,11	All		13	
JTAG							
TMS/TDI setup time to TCK high	1	See figure 5	9,10,11	All	10		ns
TMS/TDI hold time from TCK high	2		9,10,11	All	5		
Delay time, TCK low to TD0 valid	3		9,10,11	All	0	15	

See footnotes at end of table.

1/ All testing to be performed using worst-case test conditions. The supply voltage for device 01 is $4.5\ V \le V_{CC} \le 5.5\ V$, for device 02 and 03 is $4.75\ V \le V_{CC} \le 5.25\ V$. The case temperature for devices 01 - 03 is $-55°C \le T_C \le +125°C$, for device 04 is $-55°C \le T_C \le +100°C$.

2/ All input and output voltage levels are TTL compatible.

3/ Pins with internal pullup devices: TDI, TCK, TMS. Pin with internal pulldown device: $\overline{TRST}$.

4/ f_x is the input clock frequency. The maximum value is 40 MHz.

5/ This limit is specified by design but not tested.

6/ P = CLKIN cycle time.

7/ For consecutive reads, (L)$\overline{R}/\overline{W}$ stays high and $\overline{(L)STRB}$ stays low.

8/ This parameter is characterized but not tested.

9/ IIOF is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

10/ For edge-triggered interrupts, only timing parameter 1 applies.

11/ Interrupt pulse duration must be at least 1 P wide (P = one H1 period) to assure it will be seen. It must be less than 2P wide to assure it will be responded to only once. Recommended pulse duration is 1.5 P.

12/ The $\overline{IACK}$ output is active for the entire duration of the bus cycle and is therefore extended if the bus cycle utilizes wait states.

13/ For these timing values, it is assumed that the device receiving data is ready to receive data.

14/ P is the duration of the H1 clock period with a minimum value of 50 ns ($P \ge 50$ ns).

15/ t_{WORD} max = 2.5P + 28 ns + 4 ({6}) + 3 ({2} + {9} + {4}), where boxed numbers refer to the max values for corresponding parameters in the communication port byte timing table on the next page (in other words, {6} means the value under max for parameter 6 in the table --- a value of 10 ns). This timing assumes two devices are connected.

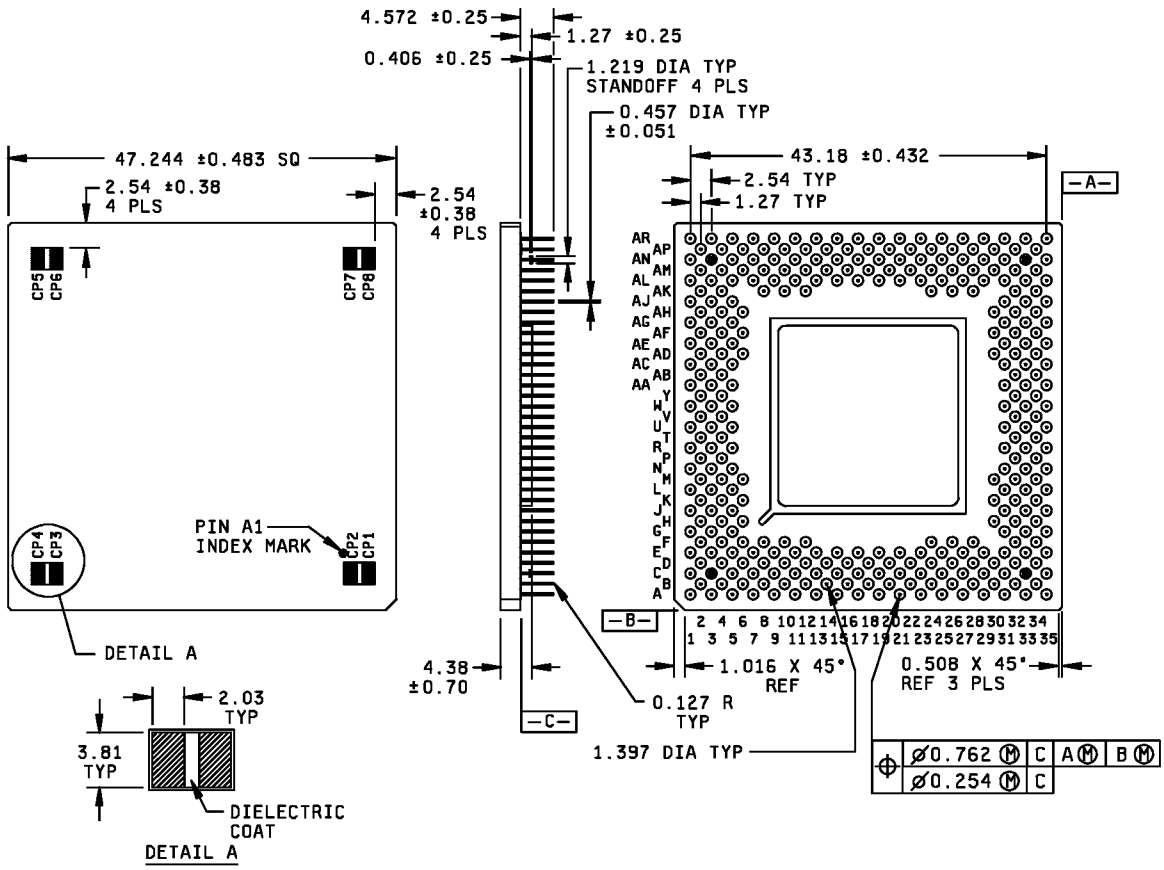
16/ t_{BYTE} max = ({2} + {4} + {6} + {9}) where boxed numbers refer to the max values for corresponding parameters in the above table (in other words, ({6}) means the value under max for parameter 6 in table --- a value of 10 ns). This assumes two devices are connected.

17/ These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.

18/ These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.

19/ Period and polarity of valid logic level are specified by contents of internal control registers.

Case X



Millimeters	Inches	Millimeters	Inches
47.244	1.860	43.18	1.700
4.572	0.180	3.683	0.145
2.54	0.100	3.81	0.150
2.03	0.080	1.397	0.055
1.27	0.050	1.219	0.048
1.016	0.040	0.508	0.020
0.457	0.018	0.406	0.016

The US Government preferred system of measurement is the metric S1 system. However, this item was originally designed using inch-pound units of measurements. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline.

Case Y

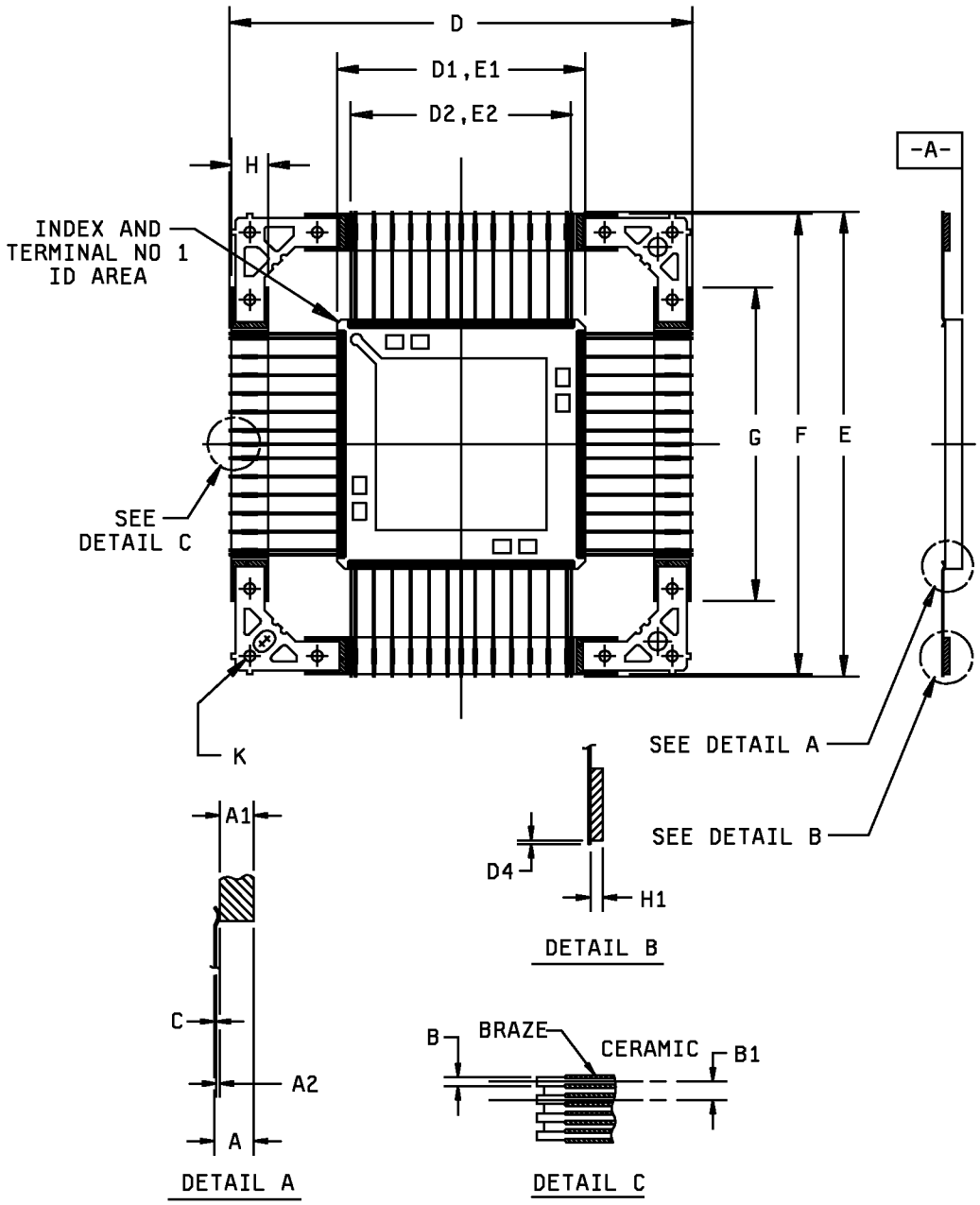


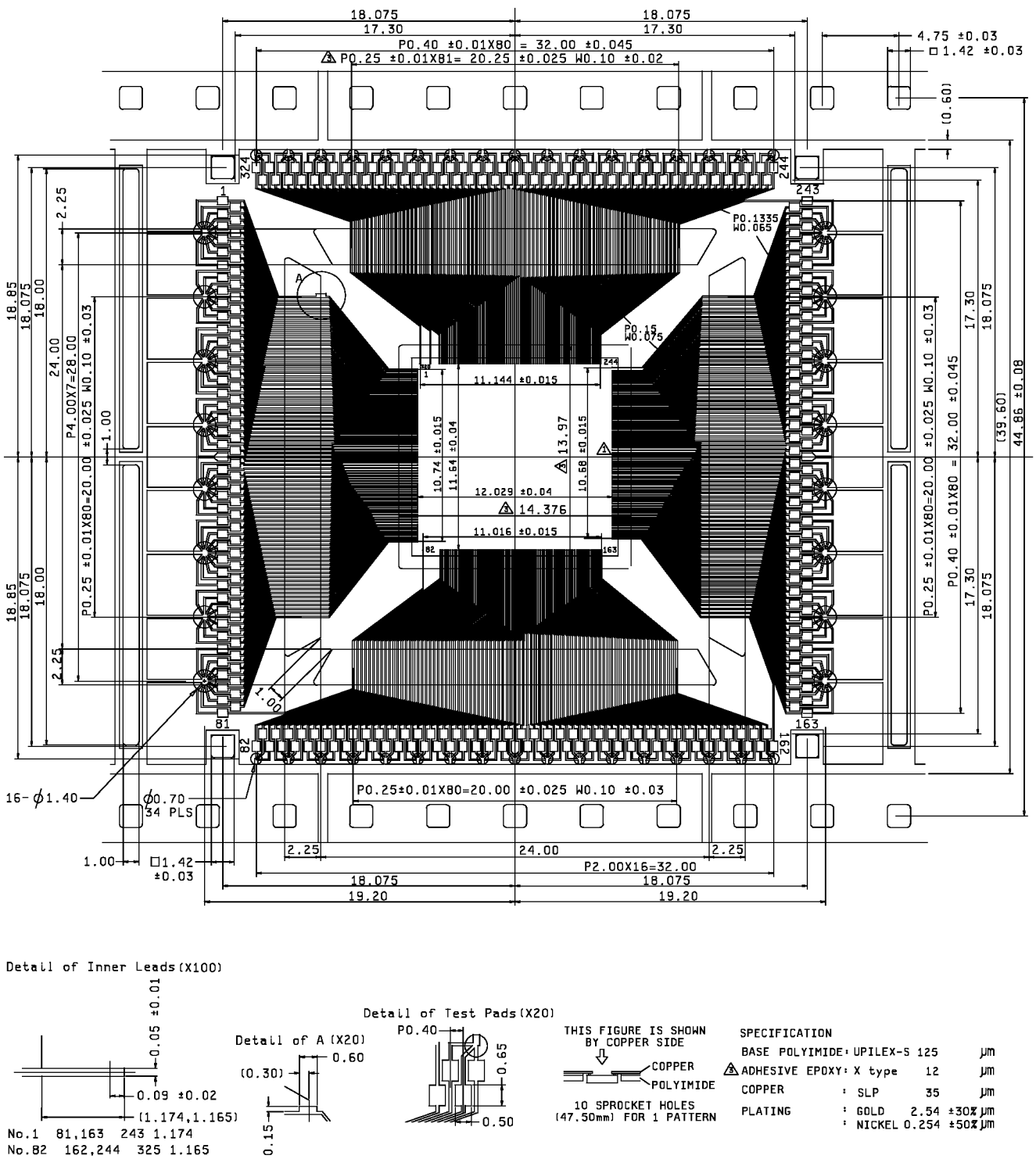
FIGURE 1. Case outline - Continued.

Case Y

Dimensions			
Ltr	Millimeters		Notes
	Min	Max	
A		4.55	
A1		4.00	
A2	0.050	0.350	
B	0.180	0.250	
B1	0.500 BSC		
C	0.10	0.20	
D,E	74.85	76.40	
D1,E1	47.52	48.48	
D2,E2	43.5 BSC		
D4		0.50	
F	74.60	75.40	Tie bar dimension
G	55.60	57.00	Tie bar dimension
H	4.5	5.5	Tie bar dimension
H1	0.75	1.05	Tie bar dimension
K	1.45	1.55	4 PLACES

FIGURE 1. Case outline - Continued

Case Z, U



Detail of Inner Leads (X100)

Detail of A (X20)

Detail of Test Pads (X20)

SPECIFICATION			
BASE POLYIMIDE	: UPILEX-S 125		µm
⚠5 ADHESIVE EPOXY	: X type 12		µm
COPPER	: SLP	35	µm
PLATING	: GOLD	2.54 ±30%	µm
	: NICKEL	0.254 ±50%	µm

FIGURE 1. Case Outline - Continued

Case Y

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
01	D31	41	D0	81	$\overline{\text{CSTRB}}5$	121	$DV_{DD}2/$	161	C1D7
02	D30	42	$\overline{\text{CE}}1$	82	$\overline{\text{CACK}}5$	122	$IV_{SS}1/$	162	C1D6
03	D29	43	$\overline{\text{RDY}}1$	83	$\overline{\text{CREQ}}5$	123	$IV_{SS}1/$	163	C1D5
04	D28	44	$DV_{SS}3/$	84	$\overline{\text{CRDY}}4$	124	C2D7	164	C1D4
05	D27	45	$DV_{SS}3/$	85	$\overline{\text{CSTRB}}4$	125	C2D6	165	C1D3
06	D26	46	$CV_{SS}1/$	86	$\overline{\text{CACK}}4$	126	C2D5	166	C1D2
07	$GDDV_{DD}2/$	47	$CV_{SS}1/$	87	$\overline{\text{CREQ}}4$	127	C2D4	167	C1D1
08	D25	48	$\overline{\text{LOCK}}$	88	$CV_{SS}1/$	128	C2D3	168	C1D0
09	D24	49	$V_{DDL}4/$	89	$DV_{SS}3/$	129	C2D2	169	$DV_{DD}2/$
10	D23	50	$V_{SSL}5/$	90	$DV_{SS}3/$	130	C2D1	170	C0D7
11	D22	51	$\overline{\text{CE}}0$	91	$DV_{DD}2/$	131	C2D0	171	C0D6
12	D21	52	$\overline{\text{RDY}}0$	92	C5D7	132	$CV_{SS}1/$	172	C0D5
13	D20	53	$\overline{\text{DE}}$	93	C5D6	133	$DV_{SS}3/$	173	C0D4
14	D19	54	TCK	94	C5D5	134	$DV_{SS}3/$	174	C0D3
15	D18	55	TDO	95	C5D4	135	$DV_{DD}2/$	175	C0D2
16	D17	56	TDI	96	C5D3	136	$\overline{\text{CRDY}}3$	176	C0D1
17	D16	57	TMS	97	C5D2	137	$\overline{\text{CSTRB}}3$	177	C0D0
18	$CV_{SS}1/$	58	$\overline{\text{TRST}}$	98	C5D1	138	$\overline{\text{CACK}}3$	178	$CV_{SS}1/$
19	$CV_{SS}1/$	59	EMU0	99	C5D0	139	$\overline{\text{CREQ}}3$	179	$DV_{DD}2/$
20	$IV_{SS}1/$	60	EMU1	100	$DV_{DD}2/$	140	$V_{DDL}4/$	180	ROMEN
21	$GDDV_{DD}2/$	61	$DV_{SS}3/$	101	C4D7	141	$V_{SSL}5/$	181	IIOF0
22	$GDDV_{DD}2/$	62	$DV_{SS}3/$	102	C4D6	142	$\overline{\text{CRDY}}2$	182	$DV_{SS}3/$
23	$DV_{SS}3/$	63	$DV_{DD}2/$	103	C4D5	143	$\overline{\text{CSTRB}}2$	183	$DV_{SS}3/$
24	$DV_{SS}3/$	64	PAGE1	104	C4D4	144	$\overline{\text{CACK}}2$	184	IIOF1
25	D15	65	R/$\overline{\text{W}}$1	105	C4D3	145	$\overline{\text{CREQ}}2$	185	IIOF2
26	D14	66	$\overline{\text{STRB}}1$	106	C4D2	146	$DV_{DD}2/$	186	IIOF3
27	D13	67	STAT0	107	C4D1	147	$\overline{\text{CRDY}}1$	187	$\overline{\text{NMI}}$
28	D12	68	STAT1	108	C4D0	148	$\overline{\text{CSTRB}}1$	188	$\overline{\text{LSTRB}}0$
29	D11	69	$IV_{SS}1/$	109	$CV_{SS}1/$	149	$\overline{\text{CACK}}1$	189	LR/$\overline{\text{W}}$0
30	D10	70	STAT2	110	$DV_{SS}3/$	150	$\overline{\text{CREQ}}1$	190	LPAGE0
31	D9	71	STAT3	111	$DV_{SS}3/$	151	$\overline{\text{CRDY}}0$	191	$\overline{\text{LRDY}}0$
32	D8	72	PAGE0	112	$DV_{DD}2/$	152	$\overline{\text{CSTRB}}0$	192	$\overline{\text{LCE}}0$
33	D7	73	R/$\overline{\text{W}}$0	113	C3D7	153	$\overline{\text{CACK}}0$	193	$\overline{\text{LSTRB}}1$
34	D6	74	$\overline{\text{STRB}}0$	114	C3D6	154	$\overline{\text{CREQ}}0$	194	LR/$\overline{\text{W}}$1
35	D5	75	$\overline{\text{AE}}$	115	C3D5	155	$CV_{SS}1/$	195	$DV_{DD}2/$
36	$GDDV_{DD}2/$	76	RESETLOC1	116	C3D4	156	$CV_{SS}1/$	196	$CV_{SS}1/$
37	D4	77	$DV_{DD}2/$	117	C3D3	157	$DV_{SS}3/$	197	LPAGE1
38	D3	78	RESETLOC0	118	C3D2	158	$DV_{SS}3/$	198	$\overline{\text{LRDY}}1$
39	D2	79	$\overline{\text{RESET}}$	119	C3D1	159	$1V_{SS}1/$	199	$\overline{\text{LCE}}1$
40	D1	80	$\overline{\text{CRDY}}5$	120	C3D0	160	$DV_{DD}2/$	200	$\overline{\text{LDE}}$

FIGURE 2. Terminal connections.

CASE Y - Continued.

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
201	TCLK0	239	$LADV_{DD}2$/	277	LD19	315	A26
202	TCLK1	240	$CV_{SS}1$/	278	LD18	316	A25
203	H3	241	$CV_{SS}1$/	279	LD17	317	A24
204	H1	242	$DV_{SS}3$/	280	$LDDV_{DD}2$/	318	A23
205	LAE	243	$DV_{SS}3$/	281	$LDDV_{DD}2$/	319	A22
206	$IV_{SS}1$/	244	LA15	282	$CV_{SS}1$/	320	A21
207	LLOCK	245	LA14	283	$DV_{SS}3$/	321	A20
208	LSTAT0	246	LA13	284	$DV_{SS}3$/	322	A19
209	LSTAT1	247	LA12	285	$IV_{SS}1$/	323	A18
210	LSTAT2	248	LA11	286	LD16	324	A17
211	LSTAT3	249	LA10	287	LD15	325	$GADV_{DD}2$/
212	LACK	250	LA9	288	LD14	326	$GADV_{DD}2$/
213	$V_{DDL}4$/	251	LA8	289	LD13	327	$CV_{SS}1$/
214	$V_{SSL}5$/	252	LA7	290	LD12	328	$CV_{SS}1$/
215	X1	253	LA6	291	LD11	329	$DV_{SS}3$/
216	X2/CLKIN	254	LA5	292	LD10	330	$DV_{SS}3$/
217	$CV_{SS}1$/	255	LA4	293	LD9	331	A16
218	$CV_{SS}1$/	256	$LADV_{DD}2$/	294	LD8	332	A15
219	$DV_{DD}2$/	257	LA3	295	LD7	333	A14
220	$DV_{SS}3$/	258	LA2	296	LD6	334	A13
221	$DV_{SS}3$/	259	LA1	297	LD5	335	A12
222	LA30	260	LA0	298	$LDDV_{DD}2$/	336	A11
223	LA29	261	$DV_{SS}3$/	299	LD4	337	A10
224	LA28	262	$DV_{SS}3$/	300	LD3	338	A9
225	LA27	263	$CV_{SS}1$/	301	LD2	339	A8
226	$LADV_{DD}2$/	264	LD31	302	LD1	340	A7
227	LA26	265	LD30	303	LD0	341	A6
228	LA25	266	LD29	304	$V_{DDL}4$/	342	A5
229	LA24	267	LD28	305	$V_{SSL}5$/	343	A4
230	LA23	268	$LDDV_{DD}2$/	306	$CV_{SS}1$/	344	$GADV_{DD}2$/
231	LA22	269	LD27	307	$CV_{SS}1$/	345	A3
232	LA21	270	LD26	308	$DV_{SS}3$/	346	A2
233	LA20	271	LD25	309	$DV_{SS}3$/	347	A1
234	LA19	272	LD24	310	A30	348	A0
235	LA18	273	LD23	311	A29	349	$CV_{SS}1$/
236	LA17	274	LD22	312	A28	350	$DV_{SS}3$/
237	LA16	275	LD21	313	$GADV_{DD}2$/	351	$DV_{SS}3$/
238	$LADV_{DD}2$/	276	LD20	314	A27	352	SUBS

1/ CV_{SS} and IV_{SS} pins are connected internally.
2/ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
3/ DV_{SS} pins are connected internally.
4/ V_{DDL} pins are connected internally.
5/ V_{SSL} pins are connected internally.

FIGURE 2. Terminal connections - Continued.

Case X

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
A0	$GDDV_{DD}$	AD30	$\overline{STRB0}$	AK24	C4D2	AM30	C5D4
A3	V_{SSL}	AD32	STAT0	AK26	C4D5	AM32	C5D6
A5	IV_{SS}	AD34	EMU1	AK28	C5D2	AM34	$\overline{CSTRB4}$
A7	DV_{DD}	AE1	CV_{SS}	AK32	$\overline{CACK4}$	AN1	V_{DDL}
A9	CV_{SS}	AE3	TCLK0	AK34	$\overline{CSTRB5}$	AN3	IIOF0
A11	DV_{SS}	AE5	$\overline{LRDY1}$	AL1	CV_{SS}	AN5	C0D2
A13	DV_{DD}	AE31	STAT3	AL3	IIOF1	AN7	C0D6
A15	DV_{SS}	AE33	STAT1	AL5	C0D1	AN9	C1D5
A17	DV_{DD}	AE35	$\overline{TRST}$	AL7	C1D0	AN11	$\overline{CACK0}$
A19	CV_{SS}	AF2	$\overline{LCE1}$	AL9	C1D6	AN13	$\overline{CACK1}$
A21	DV_{SS}	AF4	LR/$\overline{W}$1	AL11	$\overline{CSTRB0}$	AN15	$\overline{CREQ2}$
A23	DV_{DD}	AF6	$\overline{LRDY0}$	AL13	$\overline{CSTRB1}$	AN17	$\overline{CREQ3}$
A25	DV_{SS}	AF30	RESETLOC0	AL15	$\overline{CRDY2}$	AN19	C2D1
A27	CV_{SS}	AF32	R/$\overline{W}$0	AL17	$\overline{CRDY3}$	AN21	C2D5
A29	DV_{DD}	AF34	STAT2	AL19	C2D2	AN23	C3D1
A31	IV_{SS}	AG1	DV_{SS}	AL21	C2D6	AN25	C3D5
A33	$V_{SS}L$	AG3	LPAGE1	AL23	C3D2	AN27	C4D0
A35	$GDDV_{DD}$	AG5	$\overline{LCE0}$	AL25	C3D6	AN29	C4D6
AA1	X2/CLKIN	AG31	$\overline{AE}$	AL27	C4D3	AN31	C5D3
AA3	LSTAT0	AG33	PAGE0	AL29	C5D0	AN33	$\overline{CREQ4}$
AA5	$\overline{LLOCK}$	AG35	IV_{SS}	AL31	C5D7	AN35	V_{DDL}
AA31	$\overline{DE}$	AH2	LPAGE0	AL33	$\overline{CREQ5}$	AP2	$LDDV_{DD}$
AA33	$\overline{CE0}$	AH4	LR/$\overline{W}$0	AL35	CV_{SS}	AP4	C0D0
AA35	EMU0	AH6	II0F2	AM2	DV_{SS}	AP6	C0D4
AB2	$LADV_{DD}$	AH30	$\overline{CRDY4}$	AM4	C0D3	AP8	C1D1
AB4	$\overline{LAE}$	AH32	$\overline{CRDY5}$	AM6	C0D5	AP10	C1D7
AB32	PAGE1	AH34	RESETLOC1	AM8	C1D2	AP12	$\overline{CRDY0}$
AB34	TDO	AJ1	DV_{DD}	AM10	$\overline{CREQ0}$	AP14	$\overline{CRDY1}$
AC1	DV_{DD}	AJ3	$\overline{LSTRB0}$	AM12	$\overline{CREQ1}$	AP16	$\overline{CSTRB2}$
AC3	H1	AJ5	$\overline{NMI}$	AM14	$\overline{CACK2}$	AP18	$\overline{CSTRB3}$
AC5	H3	AJ31	$\overline{CACK5}$	AM16	$\overline{CACK3}$	AP20	C2D3
AC31	R/$\overline{W}$/1	AJ33	$\overline{RESET}$	AM18	C2D0	AP22	C2D7
AC33	$\overline{STRB1}$	AJ35	DV_{SS}	AM20	C2D4	AP24	C3D3
AC35	TDI	AK2	IIOF3	AM22	C3D0	AP26	C3D7
AD2	TCLK1	AK4	ROMEN	AM24	C3D4	AP28	C4D4
AD4	$\overline{LDE}$	AK8	C0D7	AM26	C4D1	AP30	C5D1
AD6	$\overline{LSTRB1}$	AK10	C1D4	AM28	C4D7	AP32	C5D5
		AK12	C1D3			AP34	$LADV_{DD}$

FIGURE 2. Terminal connections - Continued.

CASE X

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
AR1	$GADV_{DD}$	C1	V_{DDL}	E1	CV_{SS}	H2	LA9	P2	LA22
AR3	V_{SSL}	C3	LD29	E3	LA2	H4	LA8	P4	LA23
AR5	IV_{SS}	C5	LD24	E5	LD30	H6	LA4	P32	D10
AR7	CV_{SS}	C7	LD20	E7	LD25	H30	D29	P34	D5
AR9	DV_{SS}	C9	LD14	E9	LD19	H32	D24	R1	DV_{SS}
AR11	DV_{DD}	C11	LD10	E11	LD15	H34	D19	R3	LA24
AR13	CV_{SS}	C13	LD6	E13	LD11	J1	IV_{SS}	R5	LA25
AR15	DV_{SS}	C15	LD1	E15	LD7	J3	LA13	R31	D8
AR17	DV_{DD}	C17	A28	E17	LD4	J5	LA12	R33	D4
AR19	CV_{SS}	C19	A23	E19	LD0	J31	D20	R35	CV_{SS}
AR21	DV_{SS}	C21	A19	E21	A26	J33	D15	T2	LA26
AR23	DV_{DD}	C23	A16	E23	A22	J35	CV_{SS}	T4	LA28
AR25	CV_{SS}	C25	A12	E25	A18	K2	LA15	T32	D6
AR27	DV_{SS}	C27	A8	E27	A13	K4	LA14	T34	D2
AR29	DV_{DD}	C29	A3	E29	A7	K6	LA10	U1	$LDDV_{DD}$
AR31	IV_{SS}	C31	SUBS	E31	D30	K30	D22	U3	LA27
AR33	V_{SSL}	C33	D28	E33	D25	K32	D18	U5	LA30
AR35	$LDDV_{DD}$	C35	V_{DDL}	E35	CV_{SS}	K34	D13	U31	D3
B2	$GADV_{DD}$	D2	LA0	F2	LA5	L1	DV_{DD}	U33	D0
B4	LD26	D4	LA1	F4	LA3	L3	LA16	U35	$GADV_{DD}$
B6	LD22	D6	LD28	F6	LD31	L5	LA17	V2	$GDDV_{DD}$
B8	LD18	D8	LD23	F8	LD27	L31	D16	V4	LA29
B10	LD12	D10	LD17	F10	LD21	L33	D11	V32	D1
B12	LD8	D12	LD13	F12	LD16	L35	DV_{DD}	V34	$\overline{CE1}$
B14	LD3	D14	LD9	F24	A6	M2	LA18	W1	X1
B16	A30	D16	LD5	F26	A11	M4	LA19	W3	$\overline{IACK}$
B18	A27	D18	LD2	F28	A5	M6	LA11	W5	LSTAT3
B20	A25	D20	A29	F32	D31	M30	D17	W31	$\overline{RDY1}$
B22	A21	D22	A24	F34	D23	M32	D14	W33	$\overline{LOCK}$
B24	A17	D24	A20	G1	DV_{SS}	M34	D9	W35	TMS
B26	A14	D26	A15	G3	LA7	N1	CV_{SS}	Y2	LSTAT2
B28	A10	D28	A9	G5	LA6	N3	LA20	Y4	LSTAT1
B30	A4	D30	A2	G31	D27	N5	LA21	Y32	$\overline{RDY0}$
B32	A1	D32	A0	G33	D21	N31	D12	Y34	TCK
B34	$LADV_{DD}$	D34	D26	G35	DV_{SS}	N33	D7		
						N35	DV_{SS}		
Terminals located on top of package									
CP1	V_{SSL}	CP3	DV_{DD}	CP5	DV_{DD}	CP7	CV_{SS}, IV_{SS}		
CP2	V_{DDL}	CP4	CV_{SS}, IV_{SS}	CP6	DV_{SS}	CP8	DV_{DD}		

FIGURE 2. Terminal connections - Continued.

CASE Z and U

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
01	D31	41	RDY1	81	CREQ4	121	C2D1	161	C0D4
02	D30	42	$DV_{SS}3/$	82	$CV_{SS}1/$	122	C2D0	162	C0D3
03	D29	43	$CV_{SS}1/$	83	$DV_{SS}3/$	123	$CV_{SS}1/$	163	C0D2
04	D28	44	$V_{DDL}4/$	84	$DV_{DD}2/$	124	$DV_{SS}3/$	164	C0D1
05	D27	45	$V_{SSL}5/$	85	C5D7	125	$DV_{DD}2/$	165	COD0
06	D26	46	CEO	86	C5D6	126	CRDY3	166	$CV_{SS}1/$
07	$GDDV_{DD}2/$	47	RDY0	87	C5D5	127	CSTRB3	167	$DV_{DD}2/$
08	D25	48	DE	88	C5D4	128	CACK3	168	ROMEN
09	D24	49	TCK	89	C5D3	129	CREQ3	169	IIOF0
10	D23	50	TDO	90	C5D2	130	$V_{DDL}4/$	170	DV_{SS}
11	D22	51	TDI	91	C5D1	131	$V_{SSL}5/$	171	IIOF1
12	D21	52	TMS	92	C5D0	132	CRDY2	172	IIOF2
13	D20	53	TRST	93	$DV_{DD}2/$	133	CSTRB2	173	IIOF3
14	D19	54	EMU0	94	C4D7	134	CACK2	174	NMI
15	D18	55	EMU1	95	C4D6	135	CREQ2	175	LSTRB0
16	D17	56	$DV_{SS}3/$	96	C4D5	136	$DV_{DD}2/$	176	LR/W0
17	D16	57	$DV_{DD}2/$	97	C4D4	137	CRDY1	177	LPAGE0
18	$CV_{SS}1/$	58	PAGE1	98	C4D3	138	CSTRB1	178	LRDY0
19	$IV_{SS}1/$	59	R/W1	99	C4D2	139	CACK1	179	LCE0
20	$G_{DD}V_{DD}2/$	60	STRB1	100	C4D1	140	CREQ1	180	LSTRB1
21	$DV_{SS}3/$	61	STATO	101	C4D0	141	CRDY0	181	LR/W1
22	D15	62	STAT1	102	$CV_{SS}1/$	142	CSTRB0	182	$DV_{DD}2/$
23	D14	63	$IV_{SS}1/$	103	$DV_{SS}3/$	143	CACK0	183	$CV_{SS}1/$
24	D13	64	STAT2	104	$DV_{DD}2/$	144	CREQ0	184	LPAGE1
25	D12	65	STAT3	105	C3D7	145	$CV_{SS}1/$	185	LRDY
26	D11	66	PAGE0	106	C3D6	146	$DV_{SS}3/$	186	LCE1
27	D10	67	R/W0	107	C3D5	147	$IV_{SS}1/$	187	LDE
28	D9	68	STRB0	108	C3D4	148	$DV_{DD}2/$	188	TCLK0
29	D8	69	AE	109	C3D3	149	C1D7	189	TCLK1
30	D7	70	RESETLO	110	C3D2	150	C1D6	190	H3
31	D6	71	DV_{DD}	111	C3D1	151	C1D5	191	H1
32	D5	72	RESETLO	112	C3D0	152	C1D4	192	LAE
33	$G_{DD}V_{DD}2/$	73	REST	113	$DV_{DD}2/$	153	C1D3	193	$IV_{SS}1/$
34	D4	74	CRDY5	114	$IV_{SS}1/$	154	C1D2	194	LLOCK
35	D3	75	CSTRB5	115	C2D7	155	C1D1	195	LSTAT0
36	D2	76	CACK5	116	C2D6	156	C1D0	196	LSTAT1
37	D1	77	CREQ5	117	C2D5	157	DV_{DD}	197	LSTAT2
38	D0	78	CRDT4	118	C2D4	158	C0D7	198	LSTAT3
39	CE1	79	CSTRB4	119	C2D3	159	C0D6	199	IACK
40	RDY1	80	CACK4	120	C2D2	160	C0D5	200	$V_{DDL}4/$

FIGURE 2. Terminal connections.

CASE Z and U - Continued.

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
201	V_{SSL}5/	238	$LADV_{DD}$2/	275	LD6	312	A9
202	X1	239	LA3	276	LD5	313	A8
203	X2/CLK1	240	LA2	277	$LDDV_{DD}$2/	314	A7
204	CV_{SS}1/	241	LA1	278	LD4	315	A6
205	DV_{DD}2/	242	LA0	279	LD3	316	A5
206	DV_{SS}3/	243	DV_{SS}3/	280	LD2	317	A4
207	LA30	244	CV_{SS}1/	281	LD1	318	$GADV_{DD}$2/
208	LA29	245	LD31	282	LD0	319	A3
209	LA28	246	LD30	283	V_{DDL}4/	320	A2
210	LA27	247	LD29	284	V_{SSL}5/	321	A1
211	$LADV_{DD}$2/	248	LD28	285	CV_{SS}1/	322	A0
212	LA26	249	$LDDV_{DD}$2/	286	DV_{SS}3/	323	CV_{SS}1/
213	LA25	250	LD27	287	A30	324	DV_{SS}3/
214	LA24	251	LD26	288	A29	325	SUBS
215	LA23	252	LD25	289	A28		
216	LA22	253	LD24	290	$GADV_{DD}$2/		
217	LA21	254	LD23	291	A27		
218	LA20	255	LD22	292	A26		
219	LA19	256	LD21	293	A25		
220	LA18	257	LD20	294	A24		
221	LA17	258	LD19	295	A23		
222	LA16	259	LD18	296	A22		
223	$LADV_{DD}$2/	260	LD17	297	A21		
224	CV_{SS}1/	261	$LDDV_{DD}$2/	298	A20		
225	DV_{SS}3/	262	CV_{SS}1/	299	A19		
226	LA15	263	DV_{SS}3/	300	A18		
227	LA14	264	IV_{SS}1/	301	A17		
228	LA13	265	LD16	302	$GADV_{DD}$2/		
229	LA12	266	LD15	303	CV_{SS}1/		
230	LA11	267	LD14	304	DV_{SS}3/		
231	LA10	268	LD13	305	A16		
232	LA9	269	LD12	306	A15		
233	LA8	270	LD11	307	A14		
234	LA7	271	LD10	308	A13		
235	LA6	272	LD9	309	A12		
236	LA5	273	LD8	310	A11		
237	LA4	274	LD7	311	A10		

1/ CV_{SS} and IV_{SS} pins are connected internally.
2/ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
3/ DV_{SS} pins are connected internally.
4/ V_{DDL} pins are connected internally.
5/ V_{SSL} pins are connected internally.

FIGURE 2. Terminal connections - Continued.

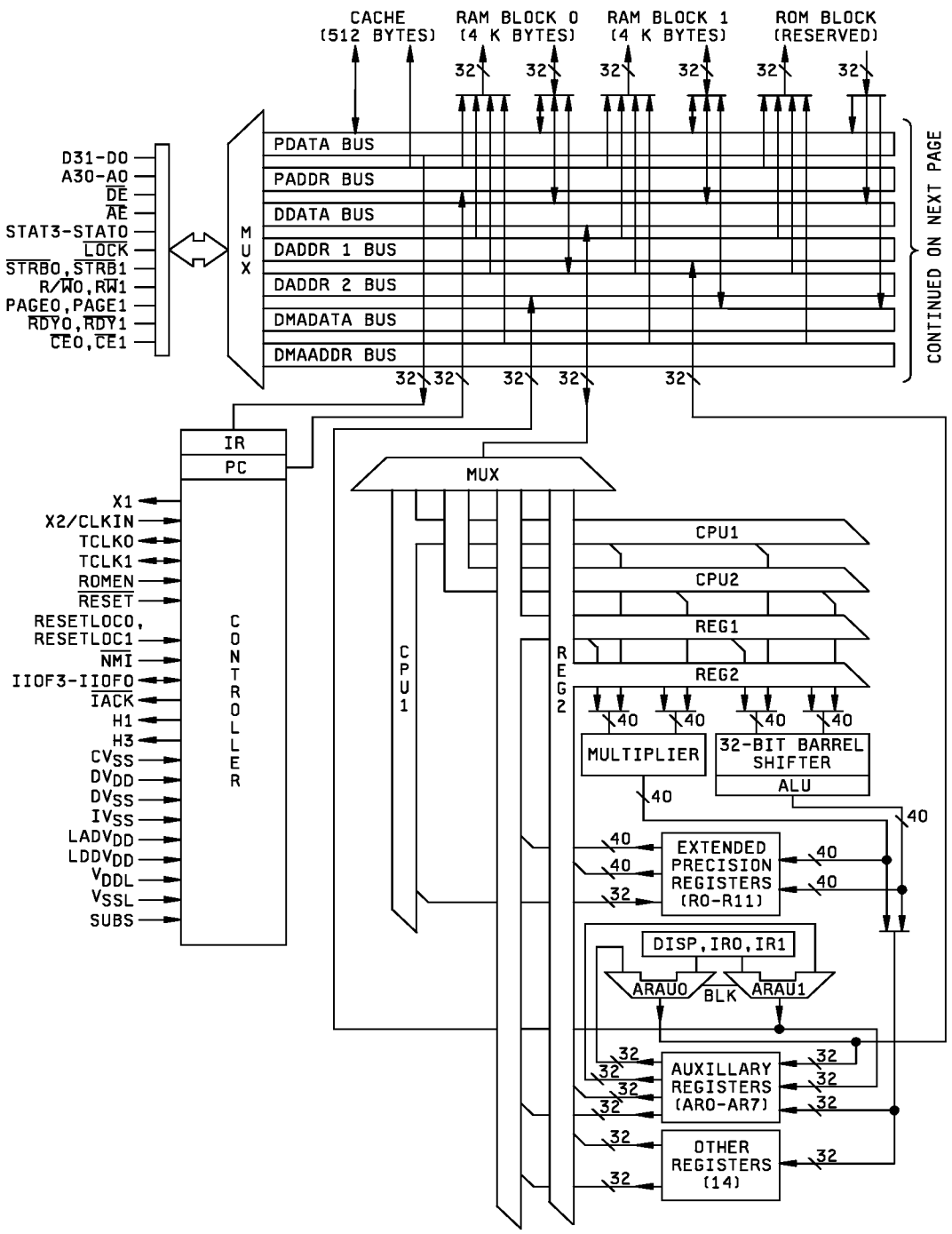


FIGURE 3. Block diagram.

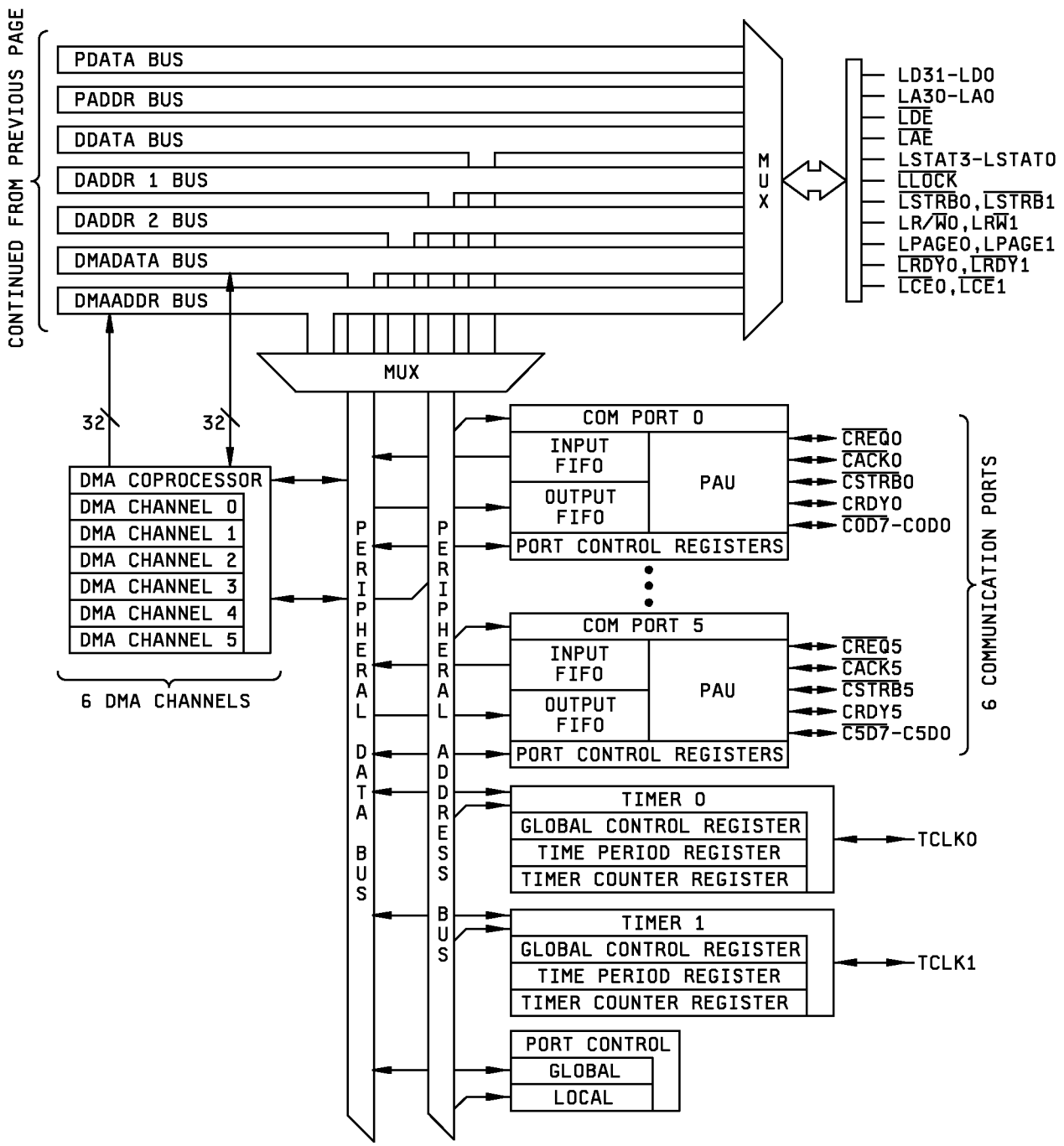
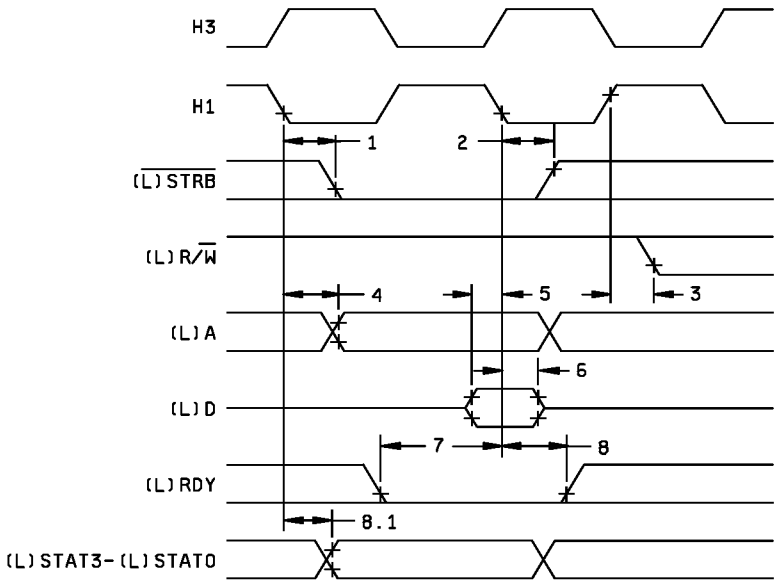


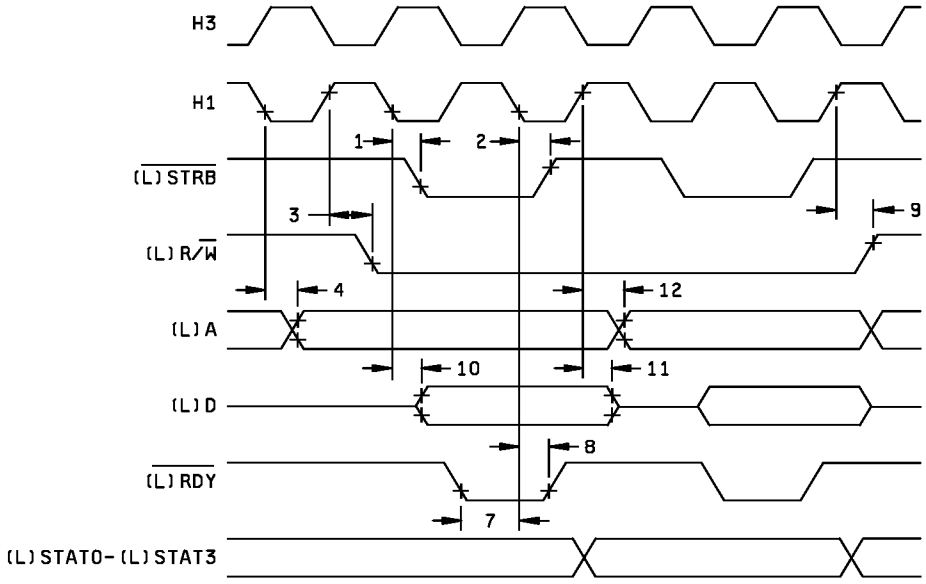
FIGURE 3. Block diagram - Continued.

Instruction code	Instruction name
00000000	EXTEST
11111111	BYPASS
00000010	SAMPLE
00000110	HIGHZ
00000011	PRIVATE1
00100000	PRIVATE2
00100001	PRIVATE3
00100010	PRIVATE4
00100011	PRIVATE5
00100100	PRIVATE6
00100101	PRIVATE7
00100110	PRIVATE8
00100111	PRIVATE9
00101000	PRIVATE10
00101001	PRIVATE11

FIGURE 4. Boundry scan instruction codes.



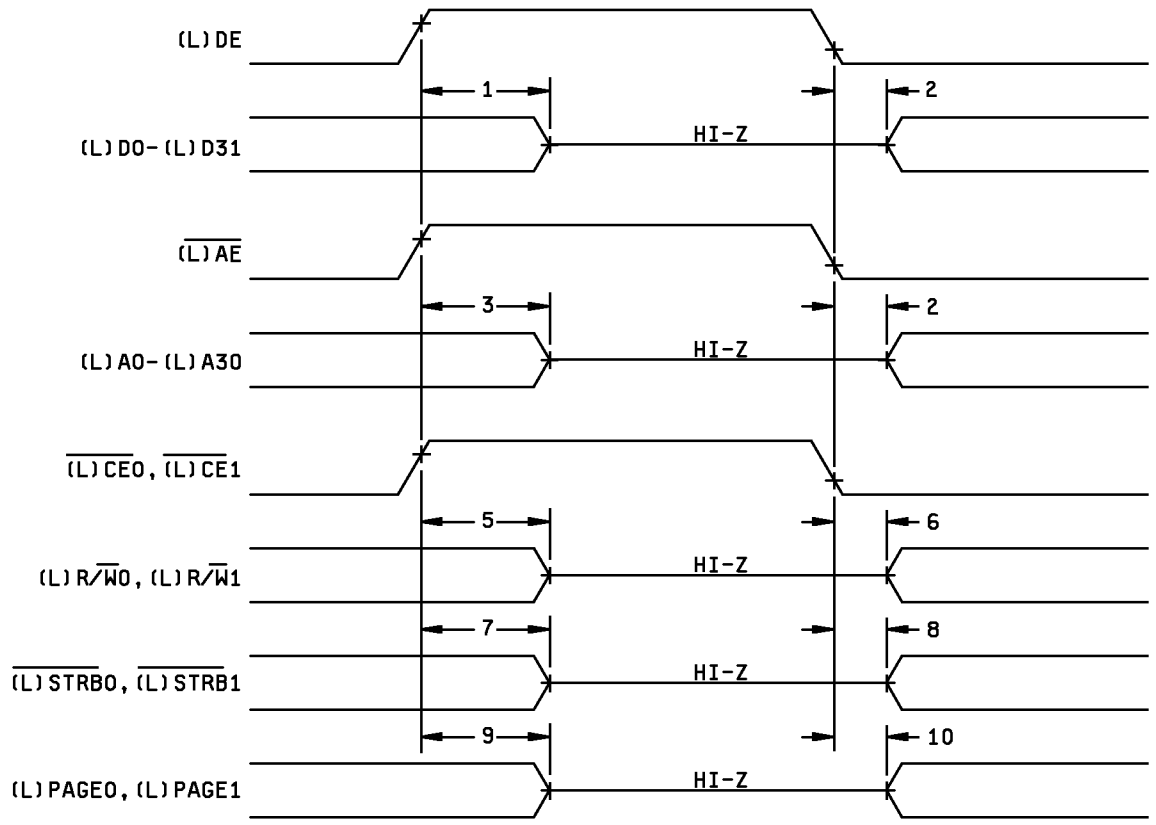
MEMORY READ CYCLE TIMING ((L) STRB = 0)



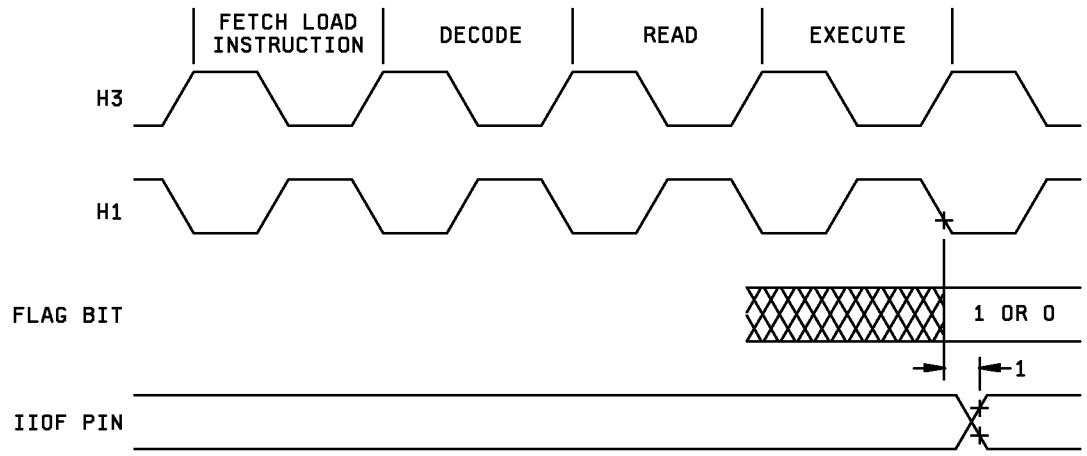
MEMORY WRITE CYCLE TIMING ((L) STRB = 0)

NOTE: Timing measurements, excluding t_r, t_f, and $t_{disable}$ (output going to high impedance or an I/O output becoming an input), are referenced from an input trip point of 1.5 V to an output trip point of 2.0 V. Timing measurements from H1 and H3 are referenced from 2.0 V on the rising or falling edges. t_r and t_f times are referenced from 20 percent below V_{OH} Min to 20 percent above V_{OL} Max. $t_{disabled}$ times are referenced from an input trip point of 1.5 V to 0.1 V below V_{OH} (t_{PHZ}) or above V_{OL} (t_{PLZ}). The I_{OL} and I_{OH} load current may be increased to reduce the RC time constant during t_{PHZ} and t_{PLZ} testing.

FIGURE 5. Timing waveforms.



DE, AE, AND CE ENABLE TIMING



TIMING FOR LOADING IIF REGISTER (IIOF PINS)
WHEN CONFIGURED AS AN OUTPUT PIN

FIGURE 5. Timing waveforms - Continued.

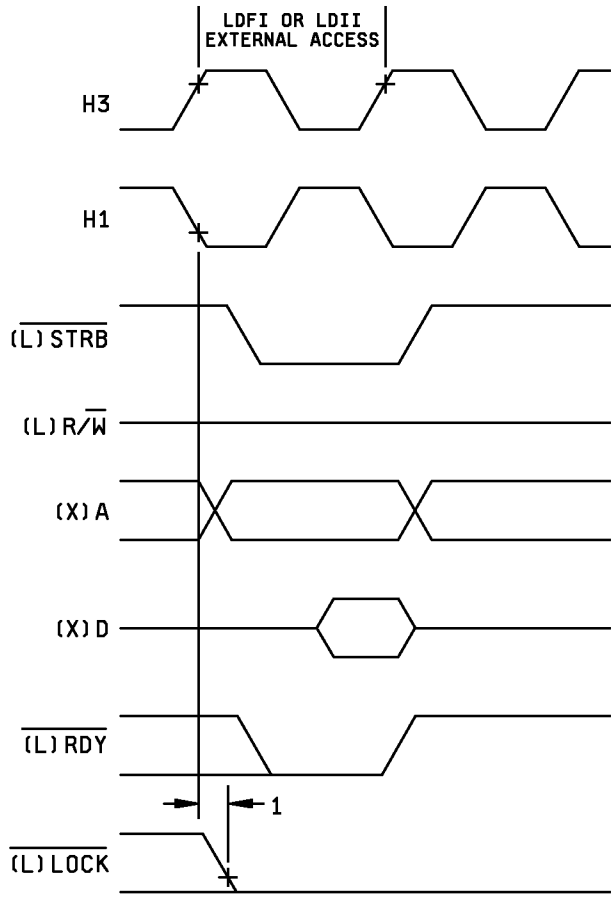
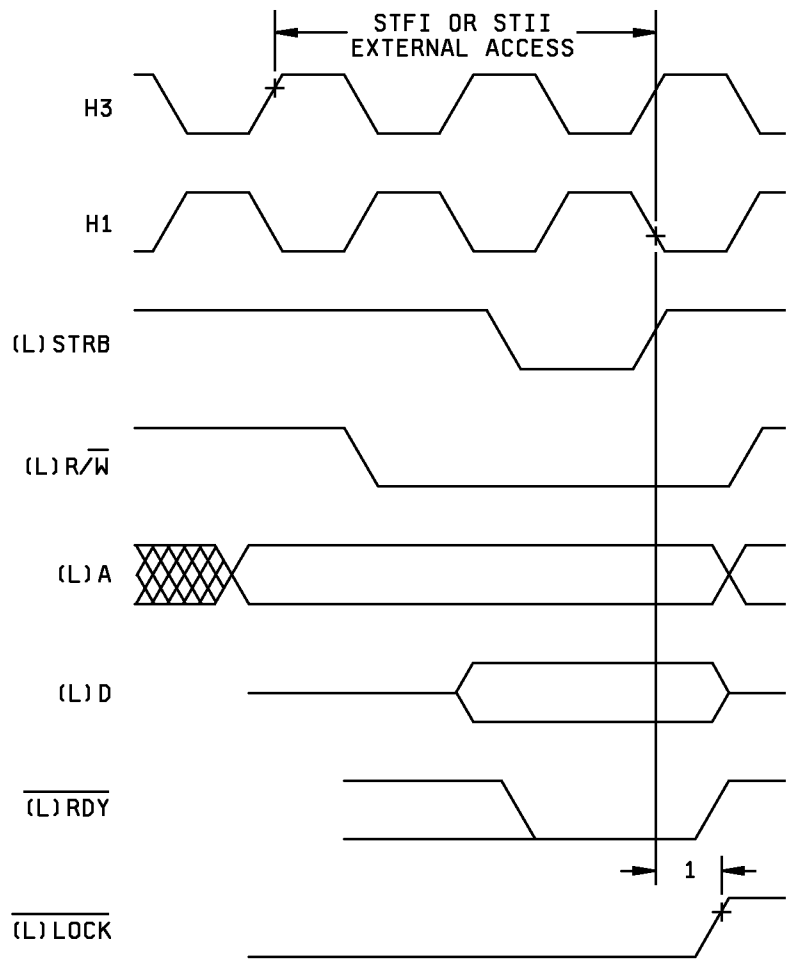
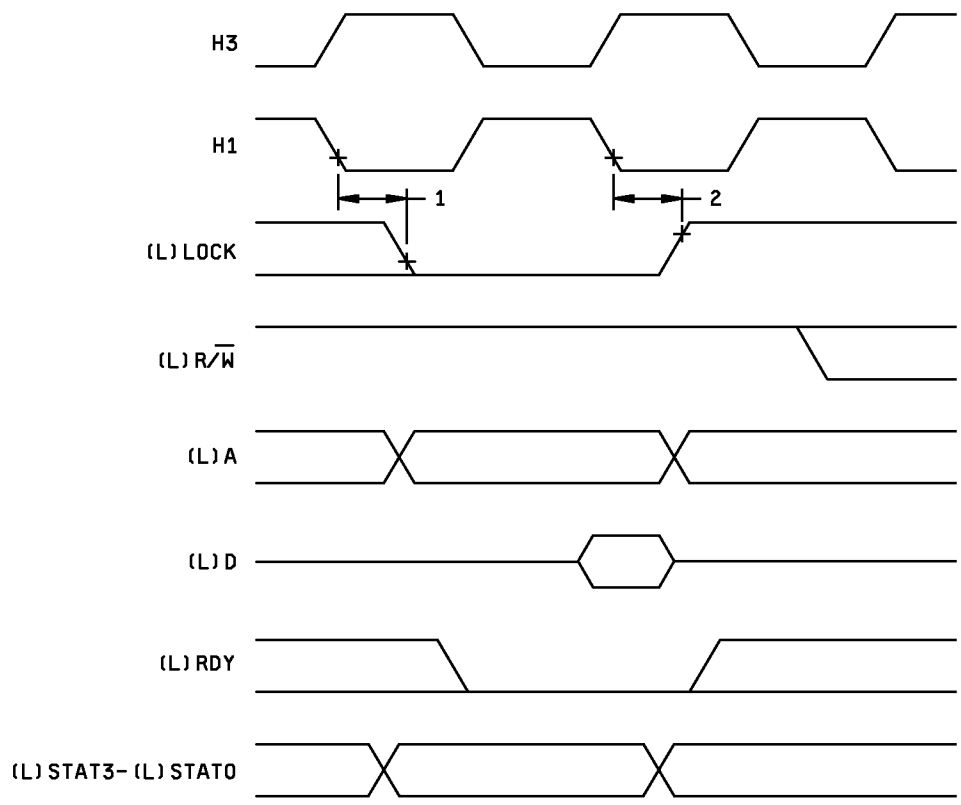


FIGURE 5. Timing waveforms - Continued.

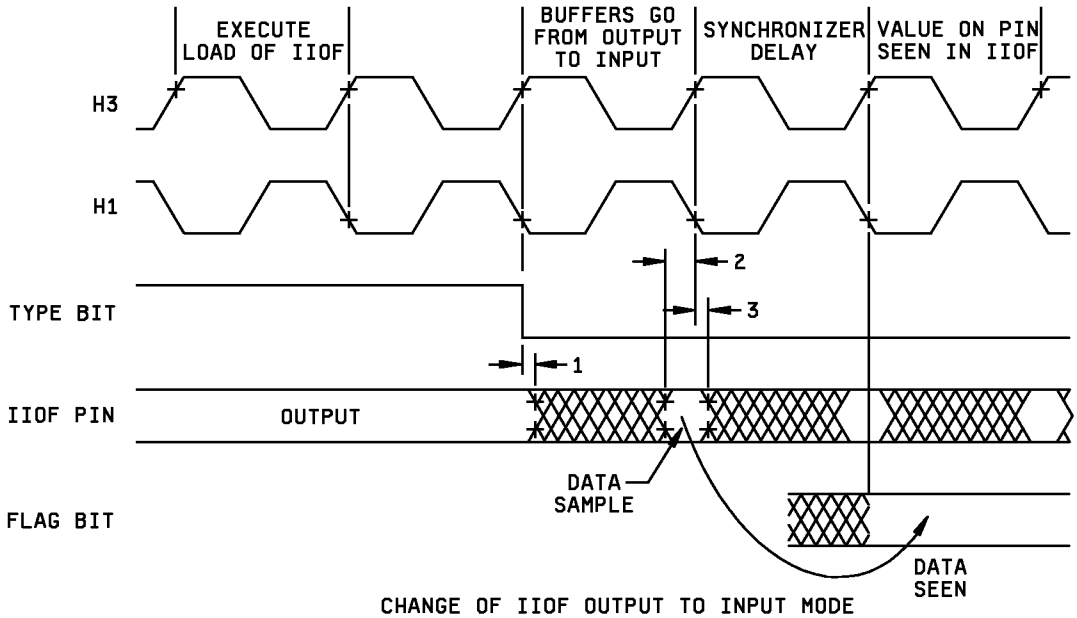


TIMING FOR (L) LOCK WHEN EXECUTING A STFI OR STII

FIGURE 5. Timing waveforms - Continued.



TIMING FOR $\overline{\text{(L) LOCK}}$ WHEN EXECUTING SIGI



CHANGE OF IIOF OUTPUT TO INPUT MODE

FIGURE 5. Timing waveforms - Continued.

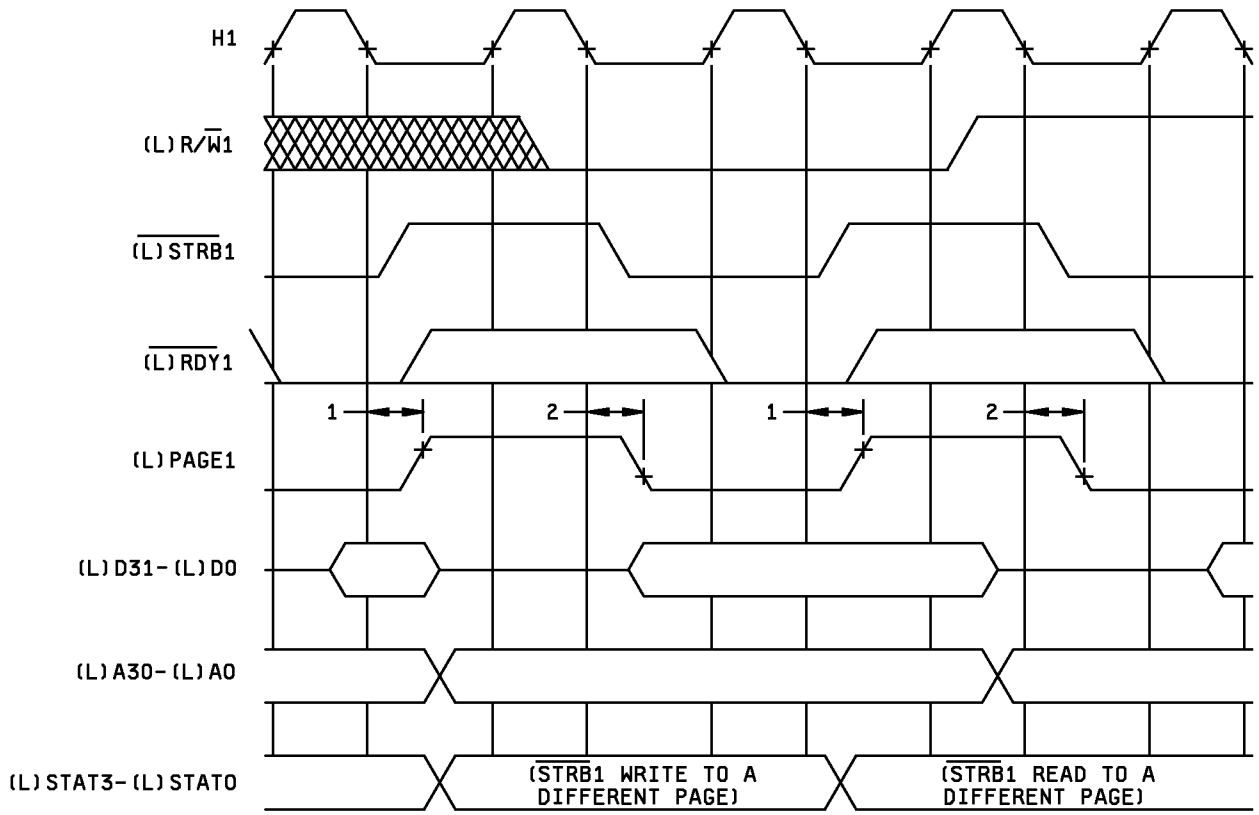
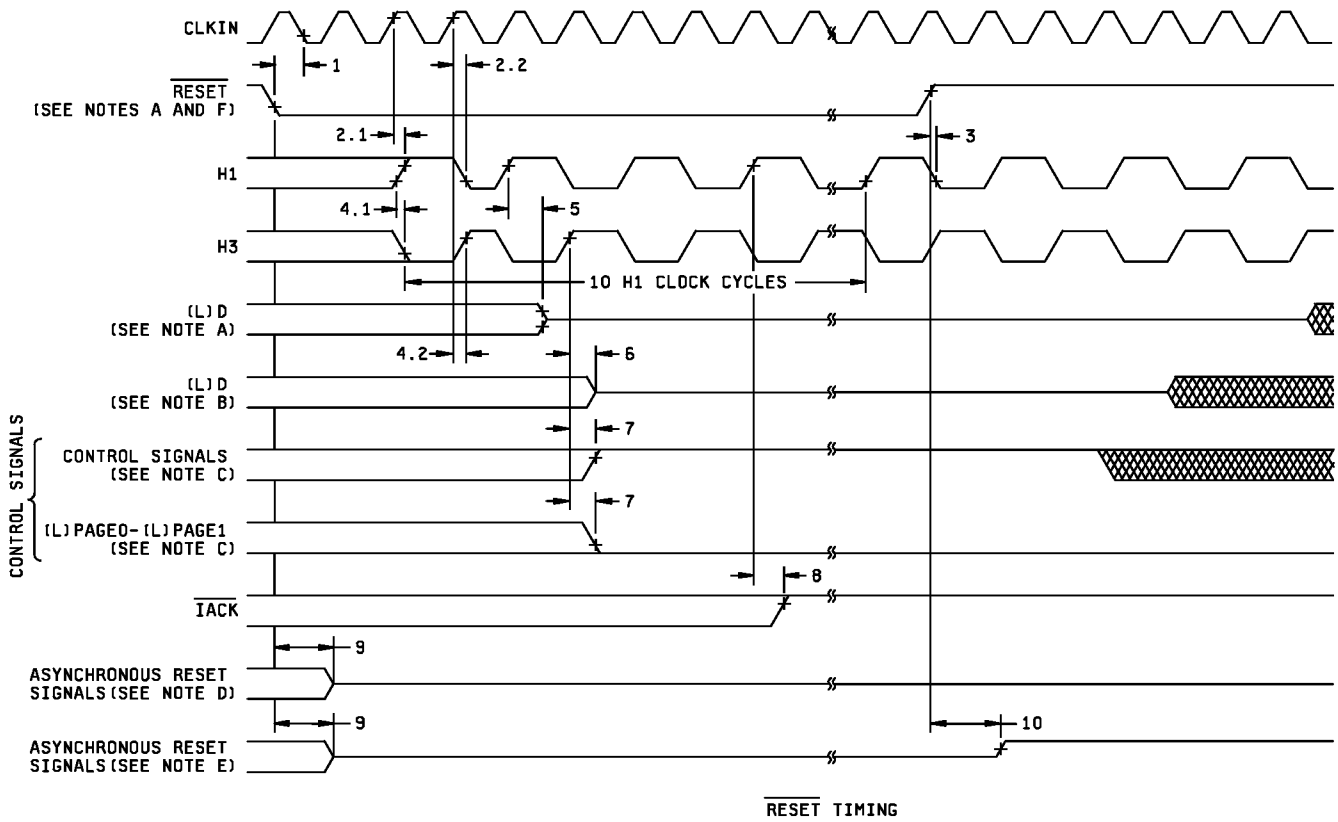


FIGURE 5. Timing waveforms - Continued.



NOTES:

A. (L)D includes D31-D0, LD31-D0, AND CxD7-CxD0.

B. L(A) includes A30-A0.

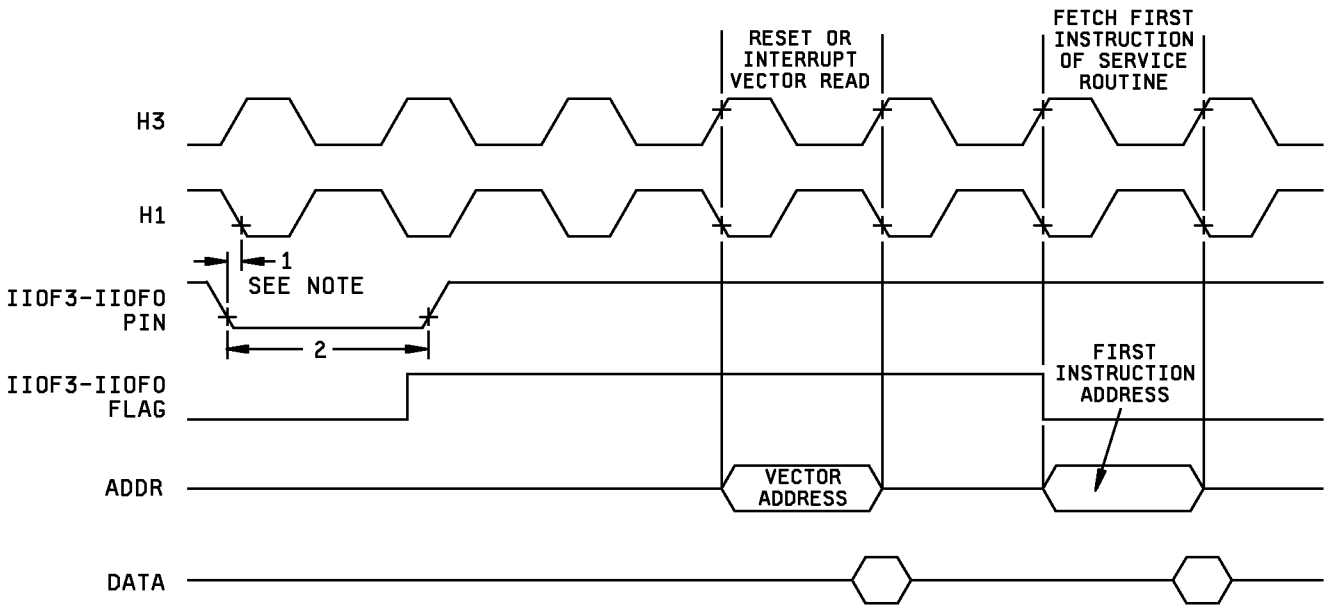
C. Control signals $\overline{\text{LSTRB0}}$, $\overline{\text{LSTRB1}}$, $\overline{\text{STRB0}}$, $\overline{\text{STRB1}}$, (L)STAT3-(L)STAT0, $\overline{\text{(L)LOCK}}$, (L)R/$\overline{\text{W}}$0, and (L)R/$\overline{\text{W}}$1 go high while (L)PAGE0, and (L)PAGE1 go low.

D. Asynchronously reset signals that go into high impedance after $\overline{\text{RESET}}$ goes low include TCLK0, TCLK1 IIOF3-IIOF0, and the communication port control signals $\overline{\text{CREQ}}$x, $\overline{\text{CACK}}$y, $\overline{\text{CSTRB}}$y, and $\overline{\text{CRDY}}$x (where X = 0, 1, or 2, and y = 3, 4, or 5). At reset, ports 0, 1, and 2 become outputs, and ports 3, 4, and 5 become inputs.)

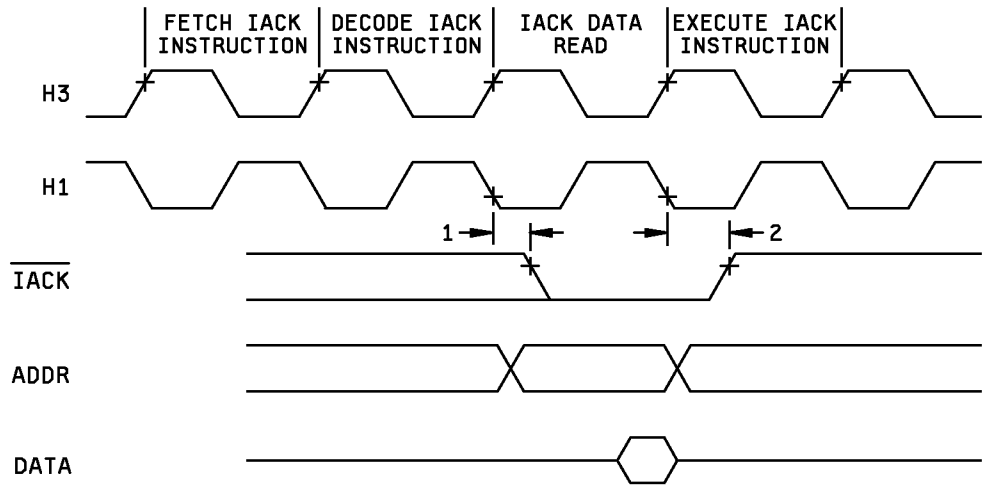
E. Asynchronously reset signals that go to a high logic level after $\overline{\text{RESET}}$ goes low include, $\overline{\text{CACK}}$x, $\overline{\text{CSTRB}}$x, and $\overline{\text{CRDY}}$y (where x = 0, 1, or 2, and y = 3, 4, or 5).

F. $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise an additional delay of one clock cycle may occur.

FIGURE 5. Timing waveforms - Continued.



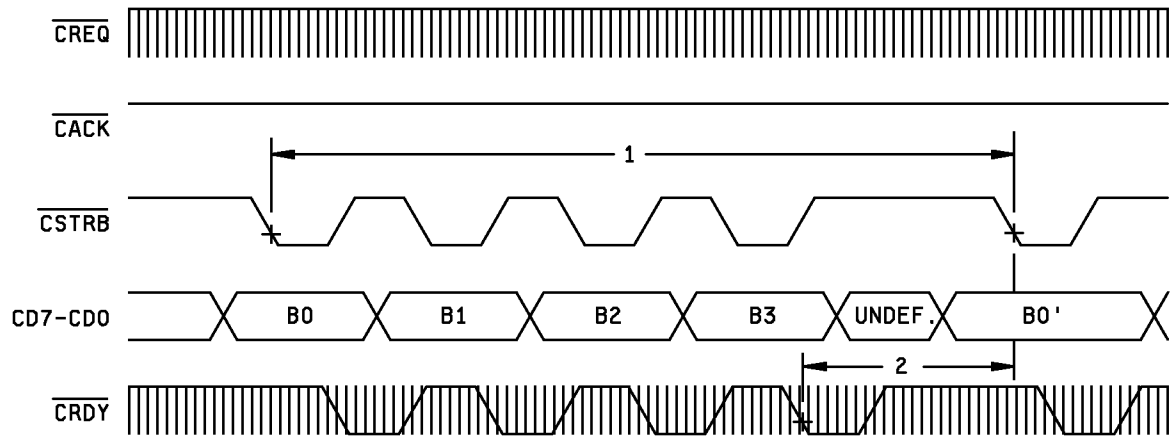
IIOF3-IIOFO INTERRUPT RESPONSE TIMING



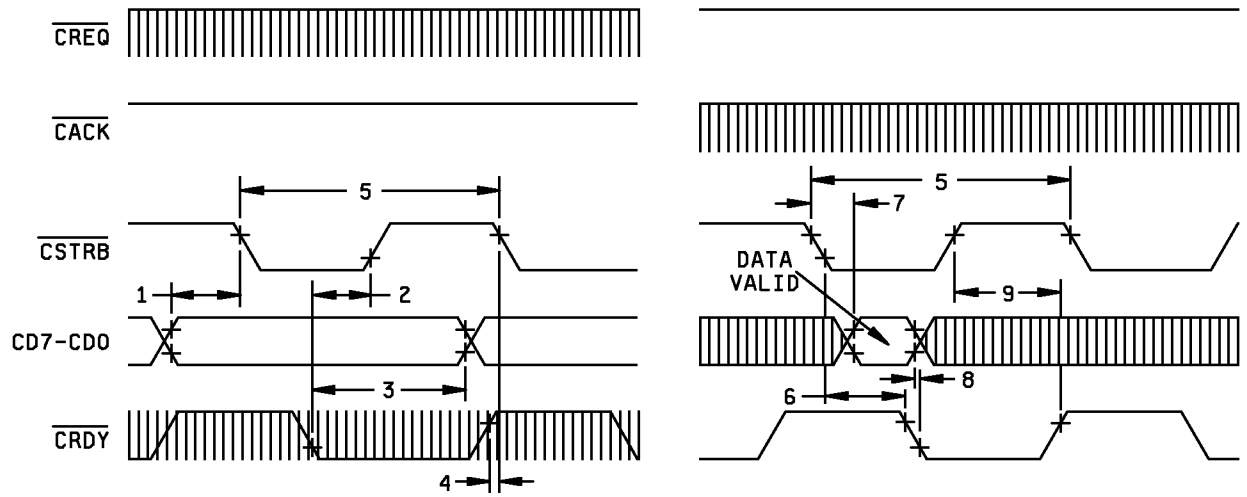
$\overline{\text{IACK}}$ TIMING

NOTES: The device can accept an interrupt from the same source every two H1 clock cycles.

FIGURE 5. Timing waveforms - Continued.



COMMUNICATION-PORT WORD-TRANSFER CYCLE TIMING



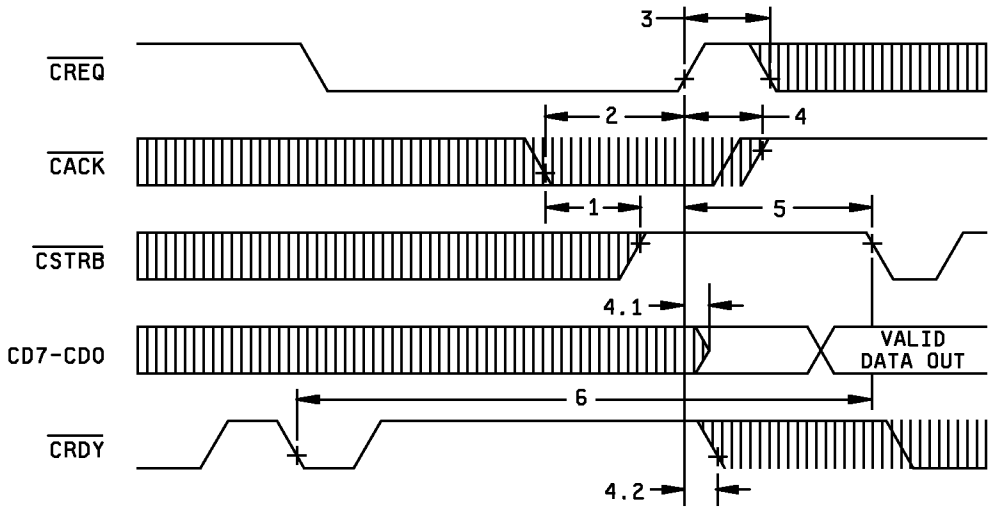
(a) WRITE TIMING (b) READ TIMING

COMMUNICATION-PORT BYTE TIMING (WRITE AND READ)

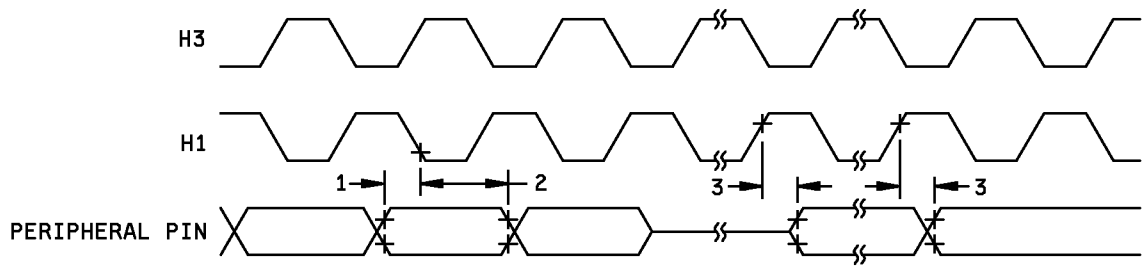
= WHEN SIGNAL IS AN INPUT (CLEAR = WHEN SIGNAL IS AN OUTPUT)

NOTES: For correct operation during token exchange, the two communicating devices must have CLKIN frequencies within a factor of 2 of each other (in other words, at most, one of the devices can be twice as fast as the other.

FIGURE 5. Timing waveforms - Continued.



COMMUNICATION TOKEN TRANSFER SEQUENCE, INPUT TO AN OUTPUT PORT

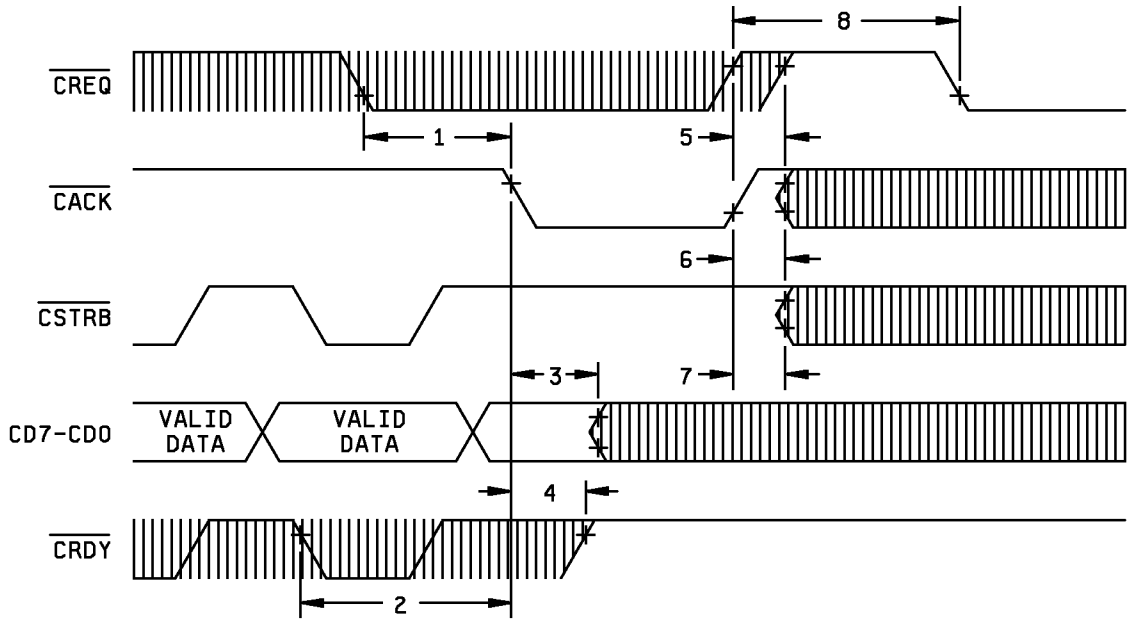


TIMER PIN TIMING CYCLE

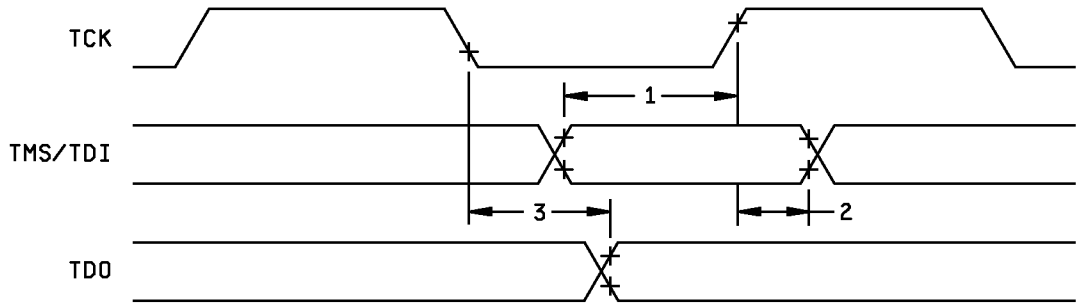
= WHEN SIGNAL IS AN INPUT (CLEAR = WHEN SIGNAL IS AN OUTPUT)

NOTE: Before the token exchange, $\overline{\text{CREQ}}$ and $\overline{\text{CRDY}}$ are output signals asserted by the device that is receiving data, $\overline{\text{CACK}}$, $\overline{\text{CSTRB}}$ and CD7-CD0 are input signals asserted by the device sending data to the device; these are asynchronous with respect to the H1 clock of the receiving device. After exchange, $\overline{\text{CACK}}$, $\overline{\text{CSTRB}}$, and CD7-CD0 become output signals and $\overline{\text{CREQ}}$ and $\overline{\text{CRDY}}$ become inputs.

FIGURE 5. Timing waveforms - Continued.



COMMUNICATION TOKEN TRANSFER SEQUENCE, OUTPUT TO AN INPUT PORT



JTAG EMULATION TIMINGS

= WHEN SIGNAL IS AN INPUT(CLEAR = WHEN SIGNAL IS AN OUTPUT).

NOTE: Before the token exchange, $\overline{\text{CACK}}$, $\overline{\text{CSTRB}}$, and CD7-CD0 are asserted by the device sending data. $\overline{\text{CREQ}}$ and $\overline{\text{CRDY}}$ are input signals asserted by the device receiving data and are asynchronous with respect to the H1 clock of the sending device. After token exchange, $\overline{\text{CREQ}}$ and $\overline{\text{CRDY}}$ become outputs, and $\overline{\text{CACK}}$, $\overline{\text{CSTRB}}$, and CD7-CD0 become inputs.

FIGURE 5. Timing waveforms - Continued

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and Appendix F of MIL-PRF-38535 and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 and Appendix F of MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and Appendix F of MIL-PRF-38535 and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT} and C_X measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B Inspection.

a. Attachability is not a requirement of case outlines Z and U .

b. For case outlines Z and U bond strength (method 2011) shall not be less than 30 g.

c. For case outlines Z and U constant acceleration in accordance with Method 2001 test condition E, Y1 direction, is required. 4 devices are to be tested with zero failures.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

TABLE III. Pin descriptions.

Signal	Pins	Type 1/	Description
Global bus external interface (80 pins)			
D31-D0	32	I/O/Z	32-bit data port of the global external interface
$\overline{DE}$	1	I	Data bus enable signal for the global external interface
A30-A0	31	O/Z	31-bit address port of the global external interface
$\overline{AE}$	1	I	Address bus enable signal for the global bus interface
STAT3-STAT0	4	O	Status signals for the global bus interface
$\overline{LOCK}$	1	O	Lock signal for the global bus interface
$\overline{STRB0}$ 2/	1	O/Z	Access strobe 0 for the global bus interface
R/$\overline{W0}$ 2/	1	O/Z	Read/write signal for $\overline{STRB0}$ accesses
PAGE0 2/	1	O/Z	Page signal for $\overline{STRB0}$ accesses
$\overline{RDY0}$ 2/	1	I	Ready signal for $\overline{STRB0}$ accesses
$\overline{CE0}$ 2/	1	I	Control enable for the $\overline{STRB0}$, PAGE0, and R/$\overline{W0}$ signals
$\overline{STRB1}$ 2/	1	O/Z	Access strobe 1 for the global bus interface
R/$\overline{W1}$ 2/	1	O/Z	Read/write signal for $\overline{STRB1}$ accesses
PAGE1 2/	1	O/Z	Page signal for $\overline{STRB1}$ accesses
$\overline{RDY1}$ 2/	1	I	Ready signal for $\overline{STRB1}$ accesses
$\overline{CE1}$ 2/	1	I	Control enable for the $\overline{STRB1}$, PAGE1, and R/$\overline{W1}$ signals
Local bus external interface (80 pins)			
LD31-LD0	32	I/O/Z	32-bit data port of the local external interface
$\overline{LDE}$	1	I	Data bus enable signal for the local external interface
LA30-LA0	31	O/Z	31-bit address port of the local external interface
$\overline{LAE}$	1	I	Address bus enable signal for the local bus interface
LSTAT3-LSTAT0	4	O	Status signals for the local bus interface
$\overline{LLOCK}$	1	O	Lock signal for the local bus interface

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
$\overline{\text{LSTRB0}}$ 2/	1	O/Z	Access strobe 0 for the local bus interface
LR/$\overline{\text{W0}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB0}}$ accesses
LPAGE0	1	O/Z	Page signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LRDY0}}$	1	I	Ready signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LCE0}}$	1	I	Control enable for the $\overline{\text{LSTRB0}}$, LPAGE0, and LR/$\overline{\text{W0}}$ signals
$\overline{\text{LSTRB1}}$ 2/	1	O/Z	Access strobe 1 for the local bus interface
LR/$\overline{\text{W1}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB1}}$ accesses
LPAGE1	1	O/Z	Page signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LRDY1}}$	1	I	Ready signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LCE1}}$	1	I	Control enable for the $\overline{\text{LSTRB1}}$, LPAGE1, and LR/$\overline{\text{W1}}$ signals
Communication port 0 interface (12 pins)			
C0D7-C0D0	8	I/O	Communication port 0 data bus
$\overline{\text{CREQ0}}$	1	I/O	Communication port 0 token request signal
$\overline{\text{CACK0}}$	1	I/O	Communication port 0 token request acknowledge signal
$\overline{\text{CSTRB0}}$	1	I/O	Communication port 0 data strobe signal
$\overline{\text{CRDY0}}$	1	I/O	Communication port 0 data ready signal
Communication port 1 interface (12 Pins)			
C1D7-C1D0	8	I/O	Communication port 1 data bus
$\overline{\text{CREQ1}}$	1	I/O	Communication port 1 token request signal
$\overline{\text{CACK1}}$	1	I/O	Communication port 1 token request acknowledge signal
$\overline{\text{CSTRB1}}$	1	I/O	Communication port 1 data strobe signal
$\overline{\text{CRDY1}}$	1	I/O	Communication port 1 data ready signal

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Communication port 2 interface (12 Pins)			
C2D7-C2D0	8	I/O	Communication port 2 data bus
$\overline{\text{CREQ2}}$	1	I/O	Communication port 2 token request signal
$\overline{\text{CACK2}}$	1	I/O	Communication port 2 token request acknowledge signal
$\overline{\text{CSTRB2}}$	1	I/O	Communication port 2 data strobe signal
$\overline{\text{CRDY2}}$	1	I/O	Communication port 2 data ready signal
Communication port 3 interface (12 pins)			
C3D7-C3D0	8	I/O	Communication port 3 data bus
$\overline{\text{CREQ3}}$	1	I/O	Communication port 3 token request signal
$\overline{\text{CACK3}}$	1	I/O	Communication port 3 token request acknowledge signal
$\overline{\text{CSTRB3}}$	1	I/O	Communication port 3 data strobe signal
$\overline{\text{CRDY3}}$	1	I/O	Communication port 3 data ready signal
Communication port 4 interface (12 Pins)			
C4D7-C4D0	8	I/O	Communication port 4 data bus
$\overline{\text{CREQ4}}$	1	I/O	Communication port 4 token request signal
$\overline{\text{CACK4}}$	1	I/O	Communication port 4 token request acknowledge signal
$\overline{\text{CSTRB4}}$	1	I/O	Communication port 4 data strobe signal
$\overline{\text{CRDY4}}$	1	I/O	Communication port 4 data ready signal
Communication port 5 interface (12 Pins)			
C5D7-C5D0	8	I/O	Communication port 5 data bus
$\overline{\text{CREQ5}}$	1	I/O	Communication port 5 token request signal
$\overline{\text{CACK5}}$	1	I/O	Communication port 5 token request acknowledge signal
$\overline{\text{CSTRB5}}$	1	I/O	Communication port 5 data strobe signal
$\overline{\text{CRDY5}}$	1	I/O	Communication port 5 data ready signal

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Interrupts, I/O flags, RESET, timer (12 pins)			
IIOF3-IIOF0	4	I/O	Interrupt and I/O flags
$\overline{\text{NMI}}$	1	I	Non-maskable interrupt. It is sensitive to a low-going edge.
$\overline{\text{IACK}}$	1	O	Interrupt acknowledge
$\overline{\text{RESET}}$	1	I	Reset signal
RESETLOC1- RESETLOC0	2	I	Reset-vector location pins
ROMEN	1	I	On-chip ROM enable (0 = disable, 1 = enable)
TCLK0	1	I/O	Timer 0 pin
TCLK1	1	I/O	Timer 1 pin
CLOCK (4 Pins)			
X1	1	O	Crystal pin
X2/CLKIN	1	I	Crystal/oscillator pin
H1	1	O	H1 clock
H3	1	O	H3 clock
Terminal connections located on top of the package 3/			
CP1	1	N/C	VSSL
CP2	1	N/C	VDDL
CP3	1	N/C	DVDD
CP4	1	N/C	CVSS, IVSS
CP5	1	N/C	DVDD
CP6	1	N/C	DVSS
CP7	1	N/C	CVSS, IVSS
CP8	1	N/C	DVDD

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Power (70 pins) 4/			
CV_{SS}	15	I	Ground pins
DV_{SS}	15	I	Ground pins
IV_{SS}	6	I	Ground pins
DV_{DD}	13	I	+ 5-V_{DC} supply pins
$GADV_{DD}$	3	I	+ 5-V_{DC} supply pins
$GDDV_{DD}$	3	I	+ 5-V_{DC} supply pins
$LADV_{DD}$	3	I	+ 5-V_{DC} supply pins
$LDDV_{DD}$	3	I	+ 5-V_{DC} supply pins
SUBS	1	I	Substrate pin (tie to ground)
V_{DDL}	4	I	+ 5-V_{DC} supply pins
V_{SSL}	4	I	Ground pins
Emulation (7 pins)			
TCK	1	I	JTAG test port clock
TDO	1	O/Z	JTAG test port data out
TDI	1	I	JTAG test port data in
TMS	1	I	JTAG test port mode select
TRST	1	I	JTAG test port reset
EMU0	1	I/O	Emulation pin 0
EMU1	1	I/O	Emulation pin 1

1/ I = input, O = output, Z = high impedance.
2/ $\overline{STRB0}$ and $\overline{STRB1}$ and associated signals (R/$\overline{W}$1, R/$\overline{W}$0, PAGE0, PAGE1, etc.) are effective over the address ranges defined by the STRB ACTIVE bits.
3/ These terminals are located on the top of Case X. Pins need not be connected for device to operate properly.
4/ Case Y has additional power and ground pins to reduce noise.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

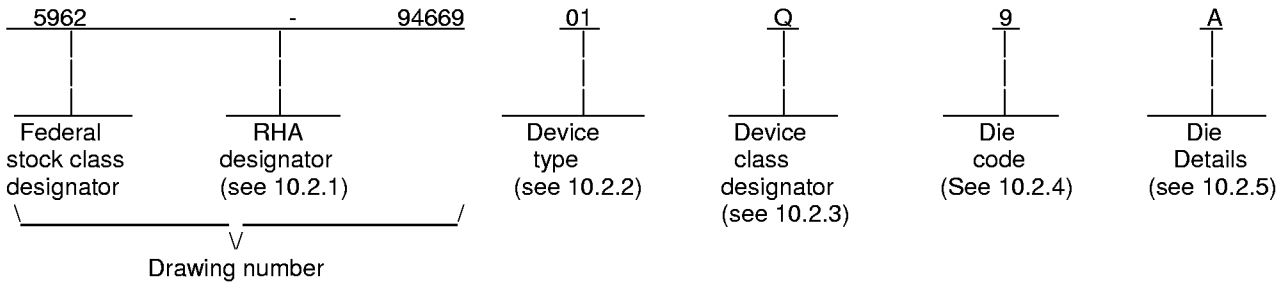
6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

Appendix A

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	320C40-33	Digital signal processor, 33 MHz
02	320C40-40	Digital signal processor, 40 MHz
03	320C40-50	Digital signal processor, 50 MHz
04	320C40-60	Digital signal processor, 60 MHz

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outlines.

10.2.5 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Die type	Figure number
02 - 04	A-1

10.2.5.2 Die bonding pad locations and electrical functions.

Die type	Figure number
02 - 04	A-1

1/ Device type 01 is available only as a packaged device. Devices 02, 03 and 04 are available as QML Die.

10.2.5.3 Interface materials.

Die type	Figure number
02 - 04	A-1

10.2.5.4 Assembly related information.

Die type	Figure number
02 - 04	A-1

10.3 Absolute maximum ratings.

See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.

See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.5.1 and on figures A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figures A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figures A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figures A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein.

Appendix A

50. Die carrier

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

6.0 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 489 mils x 474 mils.
Die thickness: 15 mils.

Interface materials.
Top metallization: TiW/ALCu2% 2KA/6KA
Backside metallization: Polysilicon

Glassivation.
Type: SiN3
Thickness: 3 kA OX/ 9 kA CN

Substrate: Silicon.

Assembly related information.
Substrate potential: Biased to Ground
Special assembly instructions: None

PAD	XCENTER	YCENTER	PAD NAME	PAD	XCENTER	YCENTER	PAD NAME
1	-429.48	11368.44	D31	41	-429.48	6377.44	RDY1
2	-429.48	11242.44	D30	42	-429.48	6099.44	DVSS
3	-429.48	11116.44	D29	43	-429.48	5973.44	CVSS
4	-429.48	10990.44	D28	44	-429.48	5847.44	VDDL
5	-429.48	10864.44	D27	45	-429.48	5721.12	VSSL
6	-429.48	10738.44	D26	46	-429.48	5564.70	CEO
7	-429.48	10612.44	GDDVDD	47	-429.48	5391.90	RDY0
8	-429.48	10486.44	D25	48	-429.48	5219.10	DE
9	-429.48	10360.44	D24	49	-429.48	5046.20	TCK
10	-429.48	10234.44	D23	50	-429.48	4894.20	TDO
11	-429.48	10108.44	D22	51	-429.48	4737.78	TDI
12	-429.48	9982.44	D21	52	-429.48	4564.98	TMS
13	-429.48	9856.44	D20	53	-429.48	4392.18	TRST
14	-429.48	9730.44	D19	54	-429.48	4240.08	EMU0
15	-429.48	9604.44	D18	55	-429.48	4114.08	EMU1
16	-429.48	9478.44	D17	56	-429.48	3988.08	DVSS
17	-429.48	9352.44	D16	57	-429.48	3862.08	DVDD
18	-429.48	9226.44	CVSS	58	-429.48	3736.08	PAGE1
19	-429.48	9100.44	IVSS	59	-429.48	3610.08	R/W1
20	-429.48	8974.44	GDDVDD	60	-429.48	3484.08	STRB1
21	-429.48	8848.44	DVSS	61	-429.48	3358.08	STAT0
22	-429.48	8722.44	D15	62	-429.48	3232.08	STAT1
23	-429.48	8596.44	D14	63	-429.48	3106.08	IVSS
24	-429.48	8470.44	D13	64	-429.48	2980.08	STAT2
25	-429.48	8344.44	D12	65	-429.48	2854.08	STAT3
26	-429.48	8218.44	D11	66	-429.48	2726.64	PAGE0
27	-429.48	8092.44	D10	67	-429.48	2600.64	R/W0
28	-429.48	7966.44	D9	68	-429.48	2474.64	STRB0
29	-429.48	7840.44	D8	69	-429.48	2318.22	AE
30	-429.48	7714.44	D7	70	-429.48	2143.98	RESETLO
31	-429.48	7588.44	D6	71	-429.48	1991.88	DVDD
32	-429.48	7462.44	D5	72	-429.48	1835.46	RESETLO
33	-429.48	7336.44	GDDVDD	73	-429.48	1662.66	RESET
34	-429.48	7210.44	D4	74	-429.48	1510.56	CRDY5
35	-429.48	7084.44	D3	75	-429.48	1384.56	CSTRB5
36	-429.48	6958.44	D2	76	-429.48	1258.56	CACK5
37	-429.48	6832.44	D1	77	-429.48	1132.56	CREQ5
38	-429.48	6706.44	D0	78	-429.48	1006.56	CRDT4
39	-429.48	6550.44	CE1	79	-429.48	880.56	CSTRB4
40	-429.48	6377.44	RDY1	80	-429.48	754.56	CACK4

FIGURE A-1 Die bonding pad locations and electrical functions.

PAD	XCENTER	YCENTER	PAD NAME	PAD	XCENTER	YCENTER	PAD NAME
81	-429.48	628.56	CREQ4	121	5850.00	0.00	C2D1
82	0.00	0.00	CVSS	122	5976.00	0.00	C2D0
83	1062.00	0.00	DVSS	123	6102.00	0.00	CVSS
84	1188.00	0.00	DVDD	124	6228.00	0.00	DVSS
85	1314.00	0.00	C5D7	125	6354.00	0.00	DVDD
86	1440.00	0.00	C5D6	126	6480.00	0.00	CRDY3
87	1566.00	0.00	C5D5	127	6606.00	0.00	CSTRB3
88	1692.00	0.00	C5D4	128	6732.00	0.00	CACK3
89	1818.00	0.00	C5D3	129	6858.00	0.00	CREQ3
90	1944.00	0.00	C5D2	130	6984.00	0.00	VDDL
91	2070.00	0.00	C5D1	131	7110.00	0.00	VSSL
92	2196.00	0.00	C5D0	132	7236.00	0.00	CRDY2
93	2322.00	0.00	DVDD	133	7362.00	0.00	CSTRB2
94	2448.00	0.00	C4D7	134	7488.00	0.00	CACK2
95	2574.00	0.00	C4D6	135	7614.00	0.00	CREQ2
96	2700.00	0.00	C4D5	136	7740.00	0.00	DVDD
97	2826.00	0.00	C4D4	137	7866.00	0.00	CRDY1
98	2952.00	0.00	C4D3	138	7992.00	0.00	CSTRB1
99	3078.00	0.00	C4D2	139	8118.00	0.00	CACK1
100	3204.00	0.00	C4D1	140	8244.00	0.00	CREQ1
101	3330.00	0.00	C4D0	141	8370.00	0.00	CRDY0
102	3456.00	0.00	CVSS	142	8496.00	0.00	CSTRB0
103	3582.00	0.00	DVSS	143	8622.00	0.00	CACK0
104	3708.00	0.00	DVDD	144	8748.00	0.00	CREQ0
105	3834.00	0.00	C3D7	145	8874.00	0.00	CVSS
106	3960.00	0.00	C3D6	146	9000.00	0.00	DVSS
107	4086.00	0.00	C3D5	147	9126.00	0.00	IVSS
108	4212.00	0.00	C3D4	148	9252.00	0.00	DVDD
109	4338.00	0.00	C3D3	149	9378.00	0.00	C1D7
110	4464.00	0.00	C3D2	150	9504.00	0.00	C1D6
111	4590.00	0.00	C3D1	151	9630.00	0.00	C1D5
112	4716.00	0.00	C3D0	152	9756.00	0.00	C1D4
113	4842.00	0.00	DVDD	153	9882.00	0.00	C1D3
114	4968.00	0.00	IVSS	154	10008.00	0.00	C1D2
115	5094.00	0.00	C2D7	155	10134.00	0.00	C1D1
116	5220.00	0.00	C2D6	156	10260.00	0.00	C1D0
117	5346.00	0.00	C2D5	157	10386.00	0.00	DVDD
118	5472.00	0.00	C2D4	158	10512.00	0.00	C0D7
119	5598.00	0.00	C2D3	159	10638.00	0.00	C0D6
120	5724.00	0.00	C2D2	160	10764.00	0.00	C0D5

FIGURE A-1 Die bonding pad locations and electrical functions - Continued

PAD	XCENTER	YCENTER	PAD NAME	PAD	XCENTER	YCENTER	PAD NAME
161	10894.00	0.00	C0D4	201	11779.74	6022.80	VSSL
162	11016.00	0.00	C0D3	202	11779.74	6154.74	X1
163	11779.74	810.00	C0D2	203	11779.74	6326.28	X2/CLK1
164	11779.74	936.00	C0D1	204	11779.74	6494.40	CVSS
165	11779.74	1062.00	COD0	205	11779.74	6620.40	DVDD
166	11779.74	1188.00	CVSS	206	11779.74	6746.40	DVSS
167	11779.74	1314.00	DVDD	207	11779.74	6873.84	LA30
168	11779.74	1470.42	ROMEN	208	11779.74	6999.84	LA29
169	11779.74	1622.88	IIOF0	209	11779.74	7125.84	LA28
170	11779.74	1748.88	DVSS	210	11779.74	7251.84	LA27
171	11779.74	1874.88	IIOF1	211	11779.74	7377.84	LADVDD
172	11779.74	2000.88	IIOF2	212	11779.74	7503.84	LA26
173	11779.74	2126.88	IIOF3	213	11779.74	7629.84	LA25
174	11779.74	2283.30	NMI	214	11779.74	7755.84	LA24
175	11779.74	2435.40	LSTRB0	215	11779.74	7881.84	LA23
176	11779.74	2561.40	LR/W0	216	11779.74	8007.84	LA22
177	11779.74	2687.40	LPAGE0	217	11779.74	8133.84	LA21
178	11779.74	2843.82	LRDY0	218	11779.74	8259.84	LA20
179	11779.74	3016.62	LCE0	219	11779.74	8385.84	LA19
180	11779.74	3168.72	LSTRB1	220	11779.74	8511.84	LA18
181	11779.74	3294.72	LR/W1	221	11779.74	8637.84	LA17
182	11779.74	3420.72	DVDD	222	11779.74	8763.84	LA16
183	11779.74	3546.72	CVSS	223	11779.74	8889.84	LADVDD
184	11779.74	3672.72	LPAGE1	224	11779.74	9015.84	CVSS
185	11779.74	3829.14	LRDY	225	11779.74	9141.84	DVSS
186	11779.74	4001.94	LCE1	226	11779.74	9267.84	LA15
187	11779.74	4174.74	LDE	227	11779.74	9393.84	LA14
188	11779.74	4326.84	TCLK0	228	11779.74	9519.84	LA13
189	11779.74	4452.84	TCLK1	229	11779.74	9645.84	LA12
190	11779.74	4578.84	H3	230	11779.74	9771.84	LA11
191	11779.74	4704.84	H1	231	11779.74	9897.84	LA10
192	11779.74	4861.26	LAE	232	11779.74	10023.84	LA9
193	11779.74	5013.36	IVSS	233	11779.74	10149.84	LA8
194	11779.74	5139.36	LLOCK	234	11779.74	10275.84	LA7
195	11779.74	5265.36	LSTAT0	235	11779.74	10401.84	LA6
196	11779.74	5391.36	LSTAT1	236	11779.74	10527.84	LA5
197	11779.74	5517.36	LSTAT2	237	11779.74	10653.84	LA4
198	11779.74	5643.36	LSTAT3	238	11779.74	10779.84	LADVDD
199	11779.74	5770.80	IACK	239	11779.74	10905.84	LA3
200	11779.74	5896.80	VDDL	240	11779.74	11031.84	LA2

FIGURE A-1 Die bonding pad locations and electrical functions - Continued.

PAD	XCENTER	YCENTER	PAD NAME	PAD	XCENTER	YCENTER	PAD NAME
241	11779.74	11157.84	LA1	281	6291.72	11819.88	LD1
242	11779.74	11283.84	LA0	282	6165.72	11819.88	LD0
243	11779.74	11489.76	DVSS	283	6038.10	11819.88	VDDL
244	10953.72	11819.88	CVSS	284	5912.10	11819.88	VSSL
245	10827.72	11819.88	LD31	285	5786.10	11819.88	CVSS
246	10701.72	11819.88	LD30	286	5660.10	11819.88	DVSS
247	10575.72	11819.88	LD29	287	5534.10	11819.88	A30
248	10449.72	11819.88	LD28	288	5408.10	11819.88	A29
249	10323.72	11819.88	LDDVDD	289	5282.10	11819.88	A28
250	10197.72	11819.88	LD27	290	5156.10	11819.88	GADVDD
251	10071.72	11819.88	LD26	291	5030.10	11819.88	A27
252	9945.72	11819.88	LD25	292	4904.10	11819.88	A26
253	9819.72	11819.88	LD24	293	4778.10	11819.88	A25
254	9693.72	11819.88	LD23	294	4652.10	11819.88	A24
255	9567.72	11819.88	LD22	295	4526.10	11819.88	A23
256	9441.72	11819.88	LD21	296	4400.10	11819.88	A22
257	9315.72	11819.88	LD20	297	4274.10	11819.88	A21
258	9189.72	11819.88	LD19	298	4148.10	11819.88	A20
259	9063.72	11819.88	LD18	299	4022.10	11819.88	A19
260	8937.72	11819.88	LD17	300	3896.10	11819.88	A18
261	8811.72	11819.88	LDDVDD	301	3770.10	11819.88	A17
262	8685.72	11819.88	CVSS	302	3644.10	11819.88	GADVDD
263	8559.72	11819.88	DVSS	303	3518.10	11819.88	CVSS
264	8433.72	11819.88	IVSS	304	3392.10	11819.88	DVSS
265	8307.72	11819.88	LD16	305	3266.10	11819.88	A16
266	8181.72	11819.88	LD15	306	3140.10	11819.88	A15
267	8055.72	11819.88	LD14	307	3014.10	11819.88	A14
268	7929.72	11819.88	LD13	308	2888.10	11819.88	A13
269	7803.72	11819.88	LD12	309	2762.10	11819.88	A12
270	7677.72	11819.88	LD11	310	2636.10	11819.88	A11
271	7551.72	11819.88	LD10	311	2510.10	11819.88	A10
272	7425.72	11819.88	LD9	312	2384.10	11819.88	A9
273	7299.72	11819.88	LD8	313	2258.10	11819.88	A8
274	7173.72	11819.88	LD7	314	2132.10	11819.88	A7
275	7047.72	11819.88	LD6	315	2006.10	11819.88	A6
276	6921.72	11819.88	LD5	316	1880.10	11819.88	A5
277	6795.72	11819.88	LDDVDD	317	1754.10	11819.88	A4
278	6669.72	11819.88	LD4	318	1628.10	11819.88	GADVDD
279	6543.72	11819.88	LD3	319	1502.10	11819.88	A3
280	6291.72	11819.88	LD2	320	1376.10	11819.88	A2

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

PAD	XCENTER	YCENTER	PAD NAME	PAD	XCENTER	YCENTER	PAD NAME
321	1250.10	11819.88	A1	324	440.10	11819.88	DVSS
322	1124.10	11819.88	A0	325	-74.70	11819.88	SUBS
323	988.10	11819.88	CVSS				

FIGURE A-1. Die bonding pad locations and electrical functions - Continued

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-11-10

Approved sources of supply for SMD 5962-94669 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE Number	Vendor Similar PIN 2/
5962-9466901QXA	3/	
5962-9466901QYC	3/	
5962-9466902QXA	01295	SMJ320C40GFM40
5962-9466902QXC	01295	SMJ320C40GFM40
5962-9466902QYC	01295	SMJ320C40HFHM40
5962-9466902QZA	01295	SMJ320C40TBBM40/10
5962-9466902QUA	01295	SMJ320C40TABM40/10
5962-9466902Q9A	01295	SMJ320C40KGDM40C
5962-9466903QXA	01295	SMJ320C40GFM50
5962-9466903QYC	01295	SMJ320C40HFHM50
5962-9466903QZA	01295	SMJ320C40TBBM50/10
5962-9466903QUA	01295	SMJ320C40TABM50/10
5962-9466903Q9A	01295	SMJ320C40KGDM50C
5962-9466904QXA	01295	SMJ320C40GFS60
5962-9466904QYC	01295	SMJ320C40HFHS60
5962-9466904QZA	01295	SMJ320C40TBBS60/10
5962-9466904QUA	01295	SMJ320C40TABS60/10
5962-9466904Q9A	01295	SMJ320C40KGDS60C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493