Ethernet-10 Core

Technical Manual

February 1997

Order Number R14006

This document is preliminary. As such, it contains data derived from functional simulations and performance estimates. LSI Logic has not verified either the functional descriptions, or the electrical and mechanical specifications using production parts.

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This document describes revision A of LSI Logic Corporation's Ethernet-10 (E-10) Core and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

To receive product literature, call us at 1.800.574.4286 (U.S. and Canada); +32.11.300.531 (Europe); 408.433.7700 (outside U.S., Canada, and Europe) and ask for Department JDS; or visit us at http://www.lsilogic.com.

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Preface

This book is the primary reference and Technical Manual for the Ethernet-10 Core. It contains a complete functional description for the E-10 core and includes complete physical and electrical specifications.

Audience

This document assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this manual are:

- Engineers and managers who are evaluating the E-10 core for possible use in value-added local area network (LAN) applications, such as network hubs, routers, and adapter cards
- Engineers with motherboard designs requiring system integration of an Ethernet core function

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, describes the general characteristics and capabilities of the E-10 core.
- Chapter 2, **Signal Description**s, describes each of the input and output signals of the E-10 core.
- Chapter 3, **E-10 Functional Description**, provides information on the architecture and functional blocks of the E-10 core.
- Chapter 4, **Functional Timing**, provides a detailed description of the E-10 Media Access Control (MAC) timing and the E-10 clock timing.
- Chapter 5, **Specifications**, contains the complete electrical and mechanical specifications of the E-10 core.

- Appendix A, **Glossary**, gives a list of terms applicable to the E-10 core.
- Appendix B, **Customer Feedback**, includes a form that you may use to fax us your comments about this document.

Related Publications

IEEE Standard 802.3 10 Mbits/s Ethernet Specification

CoreWare® Mixed Signal 10 Mbits/s Ethernet Transceiver for 10BASE-T and AUI Datasheet, Order Number R15003

Conventions Used in This Manual

The first time a word or phrase is used in this manual, it is *italicized.* See the glossary at the end of this manual for definitions of italicized words.

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

The following signal naming conventions are used throughout this manual:

- A signal whose name ends with a P (positive) is true or valid when the signal is HIGH.
- A signal whose name ends in an N (negative) is true or valid when the signal is LOW.
- If a signal can be either active-HIGH or active-LOW and is an input, the signal name ends in I (input).
- If a signal can be either active-HIGH or active-LOW and is an output, the signal name ends in O (output).

The following register bit conventions are used throughout this manual:

- A register bit that is *set* has a binary value of one.
- A register bit that is *cleared* has a binary value of zero.

Hexadecimal numbers are indicated by the prefix “0x” before the number—for example, 0x32CF. Binary numbers are indicated by the prefix “0b” before the number—for example, 0b0011.0010.1100.1111.

Chapter 1
Introduction

LSI Logic's CoreWare® library consists of leading-edge microprocessors, floating-point processors, digital signal processing (DSP) functions, and peripheral functions. Designers can combine CoreWare building blocks with other LSI Logic library elements to implement highly integrated systems in silicon for a wide variety of applications. This document describes the function, operation, and features of the Ethernet-10 (E-10) building block that is part of the CoreWare library.

This chapter provides an overview of LSI Logic's CoreWare program and the CoreWare building blocks, introduces some networking concepts, describes in general terms the E-10 core, and then provides a summary of the core's features.

The chapter contains the following sections:

- Section 1.1, "CoreWare Program"
- Section 1.2, "Local Area Networks Overview"
- Section 1.3, "General Description"
- Section 1.4, "Features"

1.1 CoreWare Program

An LSI Logic core is a fully defined, optimized, and reusable block of logic. It supports industry-standard functions and has predefined timing and layout. The core is also an encrypted RTL simulation model for a wide range of VHDL and verilog simulators.

The CoreWare library contains an extensive set of complex cores for the communications, consumer, and computer markets. The library consists of high-speed interconnect functions such as the GigaBlaze G10™-p core, MIPS embedded microprocessors, MPEG-2 decoders, a PCI core, and many more.

The library also includes megafunctions or building blocks, which provide useful functions for developing a system on a chip. Through the CoreWare program, you can create a system on a chip uniquely suited to your applications.

Each core has an associated set of deliverables, including:

- RTL simulation models for the Verilog and HDL environments
- A System Verification Environment (SVE) for RTL-based simulation
- Synthesis and timing shells
- Netlists for full timing simulation
- Complete documentation
- LSI Logic ToolKit support

LSI Logic's ToolKit provides seamless connectivity between products from leading electronic design automation (EDA) vendors and LSI Logic's manufacturing environment. Standard interfaces for formats and languages such as VHDL, Verilog, Waveform Generation Language (WGL), Physical Design Exchange Format (PDEF), and Standard Delay Format (SDF) allow a wide range of tools to interoperate within the LSI Logic ToolKit environment. In addition to design capabilities, full scan Automatic Test Pattern Generation (ATPG) tools and LSI Logic's specialized test solutions can be combined to provide high-fault coverage test programs that assure a fully functional design.

Because your design requirements are unique, LSI Logic is flexible in working with you to develop your system-on-a-chip CoreWare design. Three different work relationships are available:

- You provide LSI Logic with a detailed specification and LSI Logic does all of the design
- You design some functions while LSI Logic provides you with the cores and megafunctions, and LSI Logic completes the integration
- You perform the entire design and integration, and LSI Logic provides the core and associated deliverables

Whatever the working relationship, LSI Logic’s advanced CoreWare methodology and ASIC process technologies consistantly produce Right-First-Time™ silicon.

1.2 Local Area Networks Overview

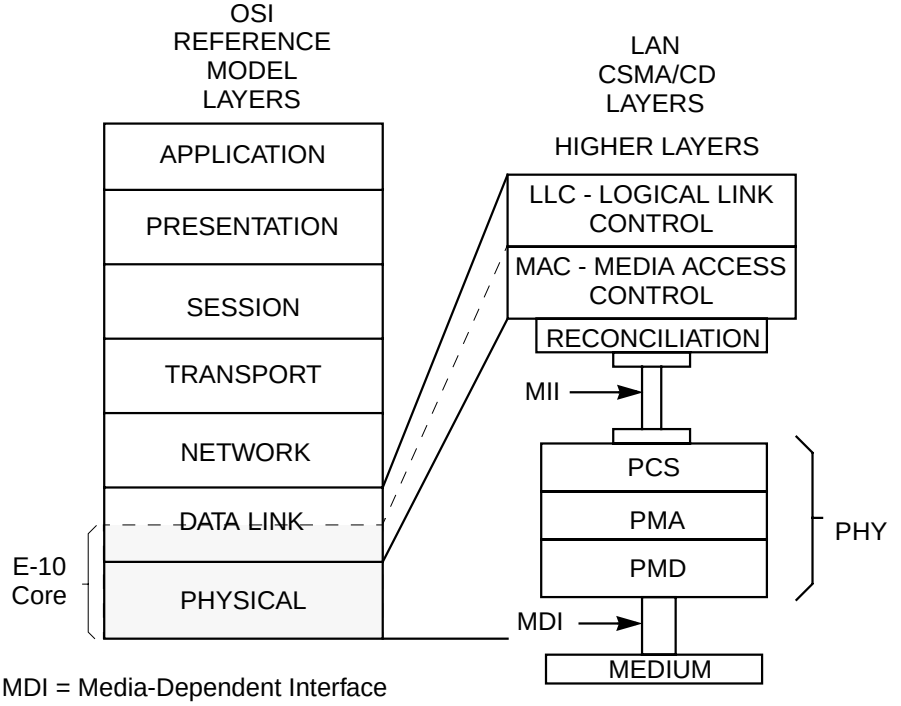
If you are already familiar with networking and local area networks, you may skip this section and proceed directly to Section 1.3 on page 1-4.

1.2.1 Ethernet Standards

Standards organizations govern the development of specifications for *Ethernet LAN* technology. The standard having the greatest influence over LAN design and specifications is the ANSI/IEEE *802.3* Ethernet standard, which is available from the IEEE in published form.

Each major LAN system technology has gained acceptance by the IEEE 802 Standards Committee. The IEEE 802 standards are compatible with the International Standards Organization's (ISO) Open System Interconnect (OSI) reference model, shown in Figure 1.1.

Figure 1.1 Ethernet-10 MAC Relationship to the OSI Model



MDI = Media-Dependent Interface
MII = Media-Independent Interface
PCS = Physical Coding Sublayer
PMA = Physical Medium Attachment
PHY = Physical Layer Device
PMD = Physical Medium Dependent

The E-10 core complies with the *Media Access Control (MAC)* sublevel within the Data Link layer of the OSI reference model and also contains a *Manchester Encoder/Decoder (ENDEC)* and *transceivers* for 10BASE-T or AUI interfaces. The ENDEC and transceivers are part of the Physical layer of the OSI model.

1.3 General Description

The *IEEE 802.3* E-10 core provides the designer flexibility in integrating an Ethernet port into an LSI Logic application-specific design. An Ethernet port includes the following:

- Media Access Control (MAC)
- Manchester Encoder/Decoder (ENDEC)
- Network Transceivers

The E-10 core is part of the LSI Logic CoreWare Library. The CoreWare program provides the critical building blocks, CAD tools, and applications support necessary to achieve high levels of system integration and product differentiation using LSI Logic's Right-First-Time ASIC design methodology.

As a CoreWare product, the E-10 core provides a highly-integrated Ethernet core implementation using submicron CMOS process technology. This optimization of size and functionality enables designers to easily integrate multiple Ethernet cores onto a single chip.

The E-10 core is fully synchronous, therefore providing predictable and reliable operation.

The E-10 core processes data at 10 Mbit/s at half-duplex and 10 Mbit/s simultaneously in each direction in full-duplex mode, provides a comprehensive solution for *10BASE-T* based systems, and is designed for easy interface to *10BASE-2, 10BASE-5*, or *10BASE-F* (fiber) media through an *Attachment Unit Interface (AUI)*. The E-10 core engine gives the designer a very effective systems integration building block for developing next-generation networking products for switched *hub* or *router* applications. The E-10 core also enables the highest form of system integration for workstation or high-end PCs by converting all the I/O and system logic into a single-chip motherboard solution.

The functional blocks within the E-10 core are:

- Media Access Control (MAC). The Media Access Control function provides simple and independent *frame* transmission and reception control by means of parallel eight-bit data interfaces.
- Manchester Encoder/Decoder (ENDEC). The E-10 core contains an integrated ENDEC function that performs Manchester encoding and decoding and utilizes a digital *phase-locked loop* for decoding data at 10 Mbit/s.
- Network Transceivers. LSI Logic provides two methods for integrating AUI/TP transceivers:
  - LSI library cells (best for single-port applications)
  - Mixed signal cells (best for multiport applications)

LSI Logic provides the following mixed signal cores for interfacing to a network:

– 10BASE-T/AUI driver

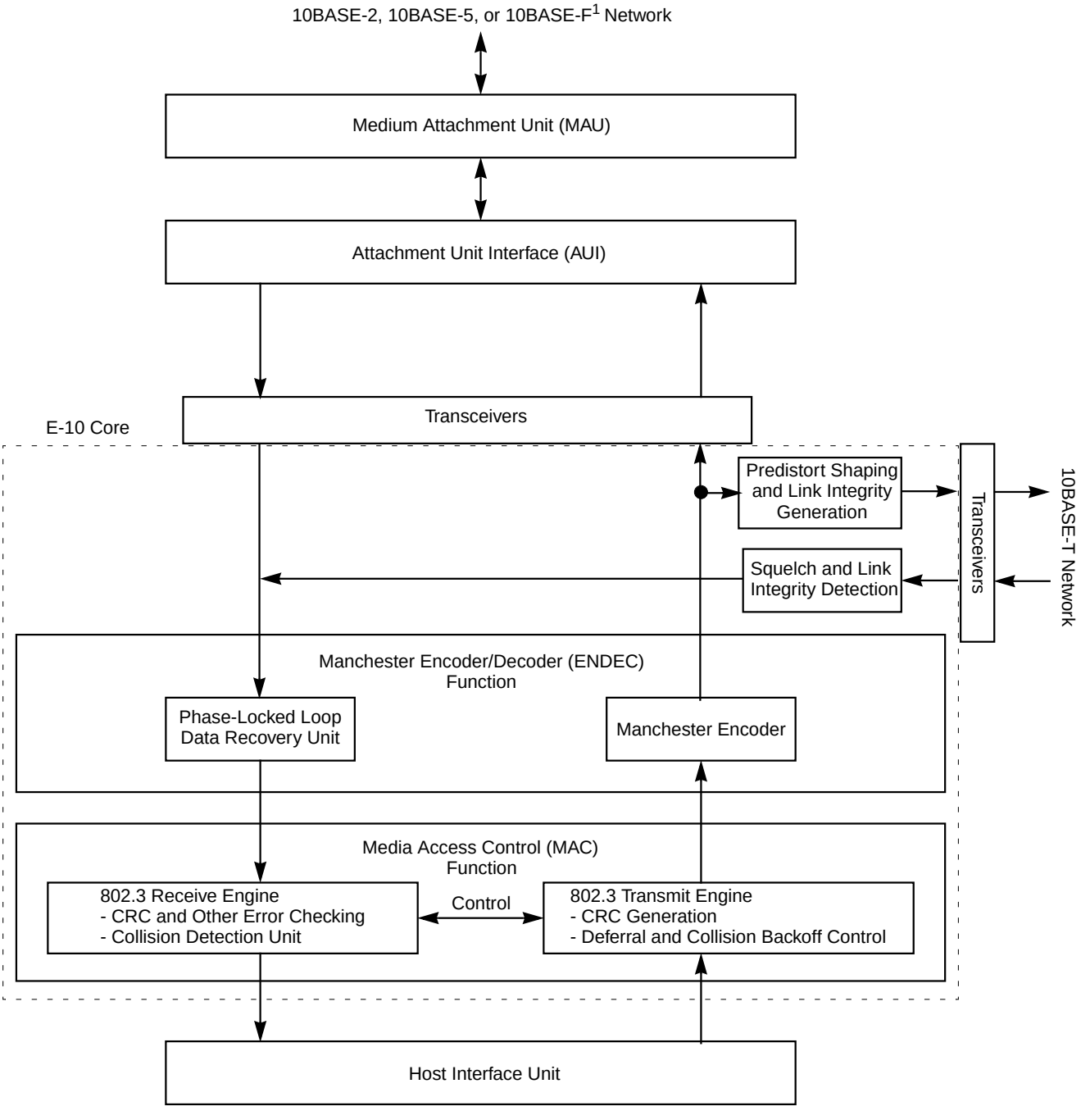
– 10BASE-T/AUI receiver

– Bias generator.

These cores perform all the analog interface functions for a 10BASE-T four-wire *twisted pair* or AUI six-wire connection, reduce requirements for external components, and reduce emissions, which is especially useful for multiport devices. The E-10 core provides inputs and outputs that are easily connected to the mixed signal cores, which are compatible with IEEE 802.3 networks. The core has pins that can be connected to an 8-wire twisted-pair interface or a 9-wire AUI interface using transmit drivers and differential receivers.

Figure 1.2 is a block diagram of the E-10 core.

Figure 1.2 E-10 Block Diagram



1. With the proper transceiver implementation, the E-10 can be compatible with 10BASE-F, 10BASE-FL and 10BASE-FX.

1.4 Features

This section summarizes the key features of the E-10 core.

1.4.1 General Features and Benefits

The E-10 core contains the following general features and associated benefits:

- Certification to IEEE 802.3 Ethernet requirements by a recognized Ethernet Interoperability Lab. Compliance with other Ethernet products at the MAC and PHY layers of the OSI Model is assured.
- Deep submicron CMOS process technology. Submicron technology allows optimized core size and functionality, which enables integration of multiple cores.
- System Verification Environment (SVE) for E-10 simulation. Verilog SVE allows designers to rapidly simulate with the E-10 core, and includes an Ethernet emulator, packet analyzer, and host interface bus emulator for performing system analysis.
- VHDL and Verilog HDL simulation model support.
- LSI Logic-created core test vectors. The core test vectors are guaranteed to provide a minimum 95% fault coverage.
- CoreWare engineering support for applications, development, and test needs. Expert engineering assistance is available for integrating the E-10 core into an ASIC design.

1.4.2 Media Access Control (MAC) Features

The MAC contains the following features:

- IEEE 802.3 Ethernet standards compliance
- Functionality at the MAC sublevel of OSI layer 2
- Support for an external *Multicast Hash filter*
- Automatic internal *Frame Check Sequence (FCS)* generator and checker

- Programmable source address insertion
- Programmable pad insertion
- Separate, parallel eight-bit host interfaces for transmit and receive data

1.4.3 Encoder/Decoder (ENDEC) Features

The ENDEC contains the following features:

- Manchester encoding/decoding
  - 10 Mbit/s receive or transmit (half-duplex)
  - 10 Mbit/s receive and transmit (full-duplex—twisted-pair mode only)
- Frame decoding up to 4,500 bytes
- Digital phase-locked loop with synchronous *data recovery*
- Manchester data decoding of incoming signals containing up to ± 18 ns of *jitter*
- PLL with fast *lock time* (seven bit times)—one bit at 10 Mbit/s equals 100 ns
- Randomized collision *backoff* algorithm

1.4.4 Twisted-Pair Transceiver Interface Features

The E-10 twisted-pair transceiver interface has the following features:

- Integrated transceiver, which provide:
  - Transmitter and receiver (four-wire or eight-wire interface) for 10BASE-T
  - *Collision detection*
  - *Link integrity* test
- Internal *loopback* test capability
- *Link polarity* detection and correction
- *Smart receive squelch* for receive data

1.4.5 Attachment Unit Interface Features

The E-10 AUI interface contains the following features:

- Signal Quality Error test (*Heartbeat*)
- Smart receive squelch for receive data
- Smart *SQE* squelch for collision detection
- 10BASE-2, 10BASE-5, or 10BASE-F interface

1.5 Other Key E-10 Features

Following are some additional key features of the E-10 core:

- Three *Address Filtering* Modes:
  - Individual address filtering (matches 48-bit destination address to 48-bit host-supplied address)
  - Multicast address filtering (provides nine-bit polynomial output for matching by an external multicast hashing table)
  - Promiscuous address filtering (matches to any individual address)
- Status Pins
  - Frame size checking/*runt* frame detection
  - *Dribble bit* error
  - Frame check sequence error
  - Phase-locked loop error

Chapter 2
Signal Descriptions

This chapter provides detailed descriptions of the E-10 signals. These descriptions are useful for designers who are interfacing the E-10 core with other core logic or logic external to the core. This chapter contains the following sections:

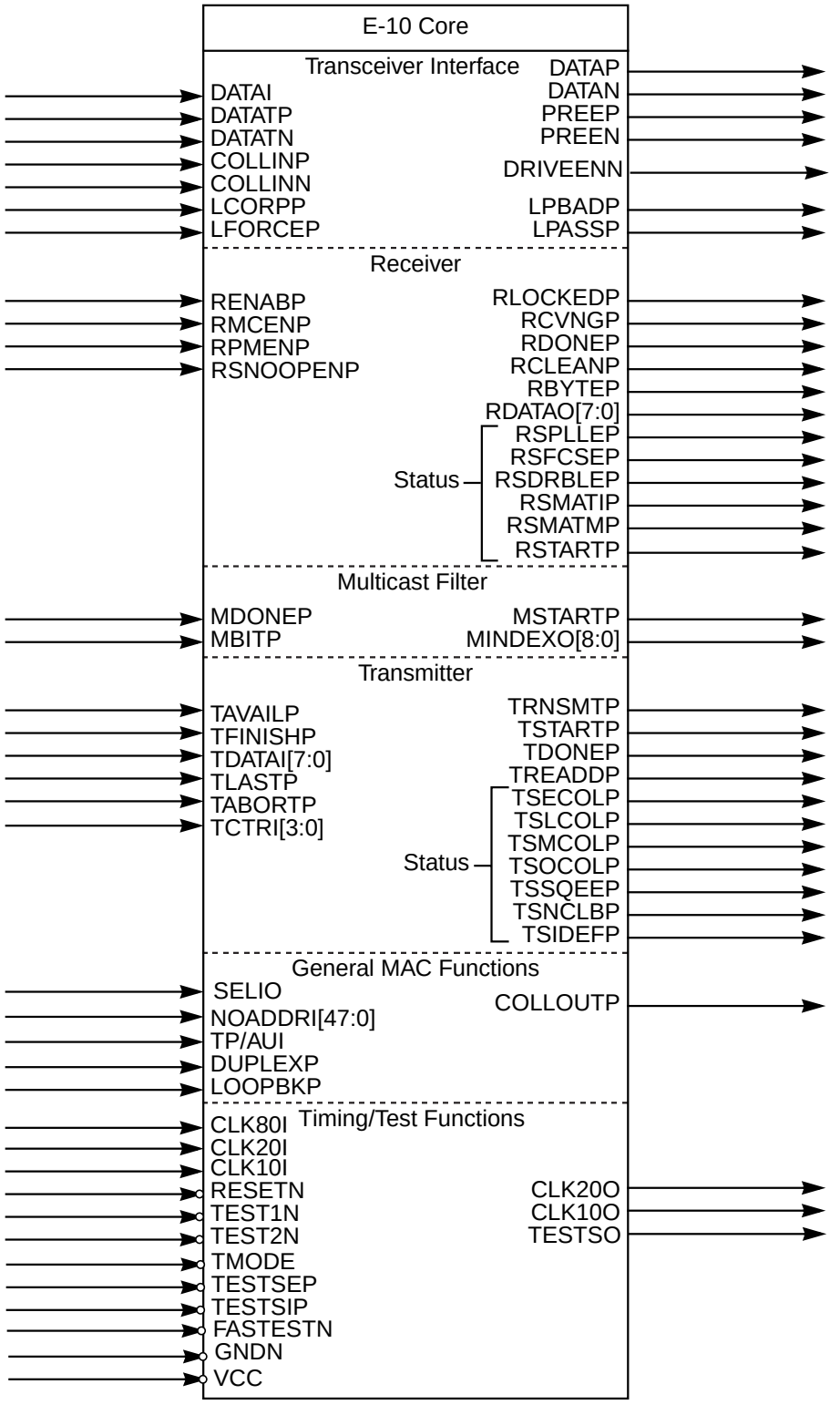
- Section 2.1, “Logic Symbol”
- Section 2.2, “Transceiver Interface Signals”
- Section 2.3, “Receiver Signals”
- Section 2.4, “Receiver Status Signals”
- Section 2.5, “Multicast Filter Signals”
- Section 2.6, “Transmitter Signals”
- Section 2.7, “Transmitter Status Signals”
- Section 2.8, “General MAC Signals”
- Section 2.9, “Timing and Test Signals”

Please see the subsection entitled “Conventions Used in This Manual,” in the preface of this manual for a description of how signals are named.

2.1 Logic Symbol

The logic diagram for the E-10 core is shown in Figure 2.1.

Figure 2.1 E-10 Logic Symbol



2.2 Transceiver Interface Signals

The E-10 transceiver interface signals connect to Ethernet transceivers or transceiver control lines that are external to the E-10 core. The descriptions of each individual signal are given below.

COLLINN **Negative Collision Threshold** **Input**
COLLINN is one of two pins (the other is COLLINP) used to detect *collisions*. It is used for the AUI mode only and must be connected to the negative threshold output of the off-core collision differential receiver.

COLLINP **Positive Collision Threshold** **Input**
COLLINP is one of two pins (the other pin is COLLINN) used to detect collisions. It is used for the AUI mode only and must be connected to the positive threshold output of the off-core collision differential receiver.

DATAI **Data In** **Input**
This input pin receives the serial data from the network and is used by the E-10 ENDEC PLL logic for data recovery. It should be connected to the zero offset output of the off-core differential input data receiver.

DATAP **Data Positive** **Output**
The E-10 core ENDEC transmits positive Manchester-encoded data on the DATAP pin. DATAP is used in conjunction with the PREEP signal and operates in both AUI and TP modes. DATAP must be connected to the data input of the off-core transmit driver.

DATAN **Data Negative** **Output**
The E-10 core ENDEC transmits negative Manchester-encoded data on the DATAN pin. DATAN is used in test mode and is not needed for interfacing to the mixed signal transmit driver.

DATATN **Data Threshold Negative** **Input**
DATATN is used in conjunction with DATATP to control the E-10 core ENDEC squelch function and link integrity pulse detection. It should be connected to the negative threshold output of the off-core differential input data receiver.

DATATP **Data Threshold Positive** **Input**

DATATP is one of two pins (the other pin is DATATN) that control the E-10 core ENDEC squelch function and link integrity pulse detection. It should be connected to the positive threshold output of the off-core differential input data receiver.

DRIVEENN **Drive Enable** **Output**

DRIVEENN is the enable output signal needed for enabling the mixed signal drivers in a four-wire solution when frame data or link pulses are to be transmitted from the E-10 core. DRIVEEN is an active-LOW signal and must be connected to the enable input of the driver.

LCORPP **Link Correct Polarity** **Input**

LCORPP is used in the Twisted-Pair mode only. When this input is HIGH in Twisted-Pair mode and the polarity of the link integrity pulses is inverted, the received data is inverted to correct for inverted wiring. The E-10 core ENDEC monitors Link Integrity pulses, which may be sent on a regular basis from any other device on the network when the channel is idle. The Link Integrity pulses received by the core normally must be positive-going pulses spaced from 6 to 96 milliseconds apart. If the E-10 core ENDEC detects eight consecutive pulses of the wrong polarity and the LCORPP pin is HIGH, the E-10 core ENDEC inverts the received data. When LCORPP is LOW, the E-10 core ENDEC does not correct for inverted wiring.

LFORCEP **Link Control Force** **Input**

LFORCEP is used in the Twisted-Pair mode only. When LFORCEP is asserted HIGH, the E-10 core ENDEC allows a transmission even in a link integrity fail situation (occurs when link pulses are not present due to a broken or missing wire).

LPASSP **Link State Pass** **Output**

LPASSP is used in the Twisted-Pair mode only to indicate the link status. LPASSP is HIGH when the link is active (data or link integrity pulses received). LPASSP is LOW when there is a *link failure* (no data or link integrity pulses received for more than 96 milliseconds). When in the link fail state (LPASSP is LOW), the transmit function within the E-10 core ENDEC is disabled. The disabling of the

receive operation has to be done in the MAC logic, using this output. The collision output is invalid during the link fail state.

LPBADP **Link Polarity Bad** **Output**

LPBADP is used in the Twisted-Pair mode only to indicate the link polarity status. LPBADP is HIGH when eight consecutive link integrity pulses of inverted polarity are received. If LCORPP is HIGH, the E-10 core ENDEC automatically inverts the data coming from the link to compensate for inverted wiring.

PREEP **Positive Data Pre-Emphasis** **Output**

This pin is used in Twisted-Pair mode only and is the positive *pre-emphasis* output from the core. The purpose of PREEP is to increase the amplitude of the higher frequencies in the output signal. Data pre-emphasis guarantees that Twisted-Pair mode can drive signals properly at 10 Mbit/s on cable up to 100 meters long. PREEP is used in conjunction with DATAP and must be connected to the pre-emphasis input of the off-core mixed signal transmit driver. The mixed signal cell uses DATAP with PREEP to generate the proper transmit signals.

PREEN **Negative Data Pre-Emphasis** **Output**

This pin is used in Twisted-Pair mode only and is the negative pre-emphasis output from the core. The purpose of PREEN is to increase the amplitude of the higher frequencies in the output signal. It is used in test mode and is not needed for interfacing to the mixed signal transmit driver.

2.3 Receiver Signals

The receiver signals connect to the parallel interface and the control circuitry of the system. The description of each signal follows.

RLOCKEDP **Receiver Locked** **Output**

The E-10 core ENDEC asserts this output HIGH when the receiver phase-locked loop is locked onto an input signal and is receiving frame bits. It takes a minimum of six bits and a maximum of eight bits for lock to occur. At least three bits are required for the smart squelch operation and the remaining bits are required for the PLL to operate.

RBYTEP **Received Byte** **Output**

A 100-ns positive pulse on this pin indicates that a new receive data byte is valid and available on the RDATAO[7:0] pins. RBYTEP pulses for 100 ns every 800 ns (a byte time) as long as the E-10 core is receiving data.

RCLEANP **Receiver Cleanup** **Output**

The E-10 core drives RCLEANP with a 100-ns positive pulse when the end of an invalid frame is encountered. An invalid frame is a frame that failed the address filter or was shorter than a minimum length frame. RCLEANP indicates to the host that the bytes received and stored by the host since the last RSTARTP pulse can be discarded.

RCVNGP **Receiving** **Output**

The E-10 core asserts RCVNGP HIGH when the receiver is receiving valid Manchester-encoded input data. Every valid Manchester-encoded bit contains a transition (either HIGH-to-LOW or LOW-to-HIGH) in the middle of the 100-ns bit time. The E-10 core asserts RCVNGP HIGH directly following the *start of frame delimiter* and deasserts it LOW when a bit cell is received without a transition in the center of the bit time.

RDATAO[7:0] **Received Data** **Output**

The E-10 core drives the RDATAO[7:0] receive data bus with a new data byte when the RBYTEP pin is pulsed HIGH. The data on these pins is valid and stable for 800 ns until the next RBYTEP pulse is received.

RDONEP **Receiver Done** **Output**

The E-10 core drives RDONEP with a 100-ns positive pulse after the reception of a complete frame. The RDONEP pulse indicates that all data bytes have been written and all receive status bits are valid.

RENABP **Receive Enable** **Input**

When RENABP is HIGH, the receive engine is enabled, frames are able to be received, and address checking is performed.

RMCENP **Receive Multicast Enable** **Input**

When RMCENP is HIGH and the multicast filter logic external to the E-10 receiver is enabled, the E-10 core continues to receive the frame. Multicast addressing is used when it is necessary to transmit to a selected group of destinations with a single individual address. The first bit of a multicast address is always a one. However, even if RMCENP is HIGH, an individual address (first address bit is a zero) can still be recognized.

The external multicast filter logic supplied by the host uses the nine-bit polynomial supplied on the MINDEXO[8:0] E-10 pins to create an index into a hash table. The nine bits are the nine MSBs of the E-10 linear feedback shift register (LFSR), which generates the 32-bit FCS. The host hash table result (MBITP, MDONEP) determines whether or not the E-10 core should continue to receive the frame.

RPMENP **Receive Promiscuous Mode Enable** **Input**

When this input is HIGH, the E-10 core disables individual address checking. All frames with an individual address are accepted. The least-significant bit of the most-significant byte of an individual address is always a zero.

RSNOOPENP

Receiver Lookback Enable **Input**

When RSNOOPENP is HIGH, all transmitted frames are routed back through the receiver. Operation is similar to that of loopback except that the phase-locked loop is bypassed. A lookback frame is indicated when both the RSMATIP and RSMATMP receiver output pins are asserted HIGH.

2.4 Receiver Status Signals

The E-10 receiver status signals may be used by the host to monitor various conditions regarding the reception of a data frame.

RSDRBLEP **Receive Status Dribble Bits** **Output**
When RSDRBLEP is HIGH, the number of bits in the received frame was not a multiple of eight, or contained dribble bits.

RSFCSEP **Receive Status Frame Check Sequence Error Output**
When this signal is HIGH, the frame check sequence (FCS), which consists of the last four bytes of the received frame, did not correspond with the expected value. The FCS is also known as a *Cyclic Redundancy Check (CRC)*. The E-10 core preloads a 32-bit LFSR with all ones. It then uses the incoming source address, destination address, length, data, pad, and FCS fields to update the 32-bit LFSR. If the contents of the 32-bit LFSR are incorrect after all bits are received, the E-10 core asserts RSFCSEP HIGH.

RSMATIP **Receive Status Match Individual Address** **Output**
When this signal is HIGH, all 48 destination address bits of the received frame matched the 48 bits of the node or individual address. In promiscuous mode, RSMATIP goes HIGH only if the address received matches the individual address. RSMATIP is not asserted for multicast addresses.

RSMATMP **Receive Status Match Multicast Address** **Output**
When this signal is HIGH, the frame was received because the external multicast filter logic accepted the frame. RSMATMP is not asserted for individual or promiscuous address modes.

RSPLLEP **Receive Status Phase-Locked Loop (PLL) Error** **Output**
When this pin is HIGH, the phase-locked loop encountered a clock rate error during the reception of the frame. The state of RSPLLEP is a “don’t care” prior to the time that the PLL acquires phase-lock.

A phase-locked loop error signals that the data recovery circuit ran out of *elasticity* during the reception of the frame. Elasticity is a measure of the tolerance of the phase-locked loop to the cumulative bit shift due to small differences in the free-running clock oscillator frequencies of the transmitting source and receiving destination. If the oscillator frequencies are not exactly the same, it is possible that the centers of the bits during lengthy frames will drift apart so much that the phase-locked loop cannot properly recover the data. The PLL runs out of elasticity after a bit shift between the transmitter and receiver of exactly six bit times or a clock period difference of ± .05%. For more information on elasticity, see the subsection entitled “PLL Characteristics” on page 3-13.

RSTARTP **Receiver Start** **Output**
The E-10 core drives this pin with a 100-ns positive pulse immediately following the start of frame delimiter. The pulse may be used to prepare the external logic for the reception of data.

2.5 Multicast Filter Signals

The multicast filter signals connect to the parallel interface and the control circuitry of the system. The description of each signal follows.

MBITP **Multicast Hash Table Bit** **Input**
While the MDONEP pulse is asserted HIGH, the MAC samples MBITP. When MBITP is HIGH, it indicates that the external logic has determined that the destination multicast address is valid.

MDONEP **Multicast Filter Done** **Input**
External host logic must examine the E-10 MINDEXO[8:0] lines to determine if a destination multicast address is valid. The host may use MINDEXO[8:0] as an index into a multicast hash lookup table. When the external logic decides to accept or reject the multicast message based on the hash table results, the logic indicates it to the E-10 receive engine by asserting the MBITP pin HIGH (if the multicast address is accepted) or by deasserting the MBITP pin LOW (if the multicast address is rejected) and asserting a 100-ns positive pulse on the MDONEP pin.

MINDEXO[8:0] Multicast Hash Function **Output**

These nine output pins contain the nine-bit hash function computed from the destination address. The E-10 core uses the nine MSBs of the 32-bit LFSR that is used to generate the FCS to create the nine-bit hash function. The nine-bit hash function is generated after the final destination address bit is received.

MSTARTP **Multicast Filter Start** **Output**

When multicast is enabled (RMCENP is HIGH) and a frame is received with a destination multicast address, the E-10 core places a 100-ns pulse on MSTARTP to indicate to the external logic that a new nine-bit hash function has been computed from the destination address.

2.6 Transmitter Signals

The MAC transmitter signals connect to the parallel interface and the control circuitry of the system. The description of each signal follows.

TABORTP **Transmit Abort** **Input**

The host asserts TABORTP to indicate that an underflow condition exists, which signifies that the host is not supplying transmit data fast enough to the core. The host is responsible for detecting the underflow condition. Assertion of TABORTP forces an invalid end to the frame. The host may assert TABORTP for any reason in order to stop transmission of data. As soon as TABORTP is received, the E-10 core transmits 32 bits of alternating ones and zeros, starting with a one, before stopping transmission.

TAVAILP **Transmit Packet Available** **Input**

TAVAILP should be asserted HIGH when the host has one or more data *packets* available to be transmitted. This signal is sampled only once per frame, so it can be deasserted LOW by the host after the E-10 core asserts the TRNSMTP and TSTARTP output pins. The E-10 core continues to attempt to transmit the frame until it is transmitted successfully, an error occurs, or the transmission is aborted.

After the TAVAILP signal is first sampled, it is not sampled again until a minimum of 800 ns after the TDONEP pulse, to give external logic time to do buffer housekeeping, and to determine whether or not another buffer is ready to be transmitted.

TCTRI[3:0] **Transmit Control** **Input**

The bits in this four-bit control bus are described in the following table.

Bit	Description
0	Insert Source Address Enable
1	Insert FCS Field Enable
2	Automatic Frame Padding Enable
3	SQE Test Enable

The TCTRI[3:0] signals come from the host. They are normally static signals that the E-10 core uses to determine transmission operation.

TCTRI[0] is the Insert Source Address Enable signal. When TCTRI[0] is HIGH, the E-10 core inserts the source address into a transmitted frame from the 48-bit NOADDRI[47:0] bus supplied at the E-10 input pins by the host. If TCTRI[0] is LOW, the host itself must place the source address in the transmitted frame.

TCTRI[1] is the Insert FCS Field Enable signal. When TCTRI[1] is HIGH, the E-10 core computes a four-byte FCS and appends it to the end of a transmitted frame. When TCTRI[1] is LOW, the host must generate and append the FCS field to the frame.

TCTRI[2] is the Automatic Frame Padding Enable signal. When TCTRI[2] is HIGH, the E-10 core examines the data field supplied by the host. If the data field contains less than 46 bytes (46 bytes is the minimum amount of data required for a minimum frame length), the E-10 core supplies enough bytes filled with zeroes to make a 46-byte data field. If TCTRI[2] is LOW, the E-10 core does not automatically append any bytes to the data field.

TCTRI[3] is the SQE Test Enable signal. When TCTRI[3] is HIGH, the E-10 core expects to receive a “heartbeat” on the COLLINP and COLLINN signal inputs after each frame is transmitted. The heartbeat is a 10-MHz burst

and starts six to 16 bit times (0.6 µs to 1.6 µs) after the last transition of the transmitted signal and lasts for a duration of five to 15 bit times. If TCTRI[3] is LOW, the E-10 core expects no such signalling. The SQE Test Enable signal is not applicable to Twisted-Pair mode.

TDATAI[7:0] **Transmit Data** **Input**

The data on this eight-bit transmit data bus is sampled on the LOW-to-HIGH transition of CLK10I when TREADDP is asserted. After TREADDP is asserted HIGH, the external logic has up to 800 ns to place the next data byte onto the TDATAI[7:0] bus.

TDONEP **Transmit Done** **Output**

The E-10 core puts a 100-ns positive pulse on the TDONEP pin to indicate either the end of a transmission, the frame was transmitted successfully, excessive collisions are detected, or the signals TFINISHP or TABORTP are asserted. When this signal is asserted, the transmit status pins are valid. Section 2.7, “Transmitter Status Signals,” defines the transmit status pins.

TFINISHP **Transmit Finish** **Input**

When TFINISHP is asserted HIGH during a transmission, the current transmission attempt is completed, no retry is attempted, and a TDONEP pulse generated even if the transmission attempt is not successful.

TLASTP **Transmit Last Byte** **Input**

The host asserts TLASTP HIGH to indicate that TDATAI[7:0] contains the last byte of data in the frame.

TREADDP **Transmitter Read Data** **Output**

A HIGH pulse on this output pin indicates that the data byte previously placed on the TDATAI[7:0] lines by the host is going to be read into the E-10 core on the next LOW-to-HIGH transition of CLK10I. After the data is read, the host can remove the data from the TDATAI[7:0] pins. The host should put the next data byte on the TDATAI[7:0] pins within 800 ns.

TRNSMTP **Transmitting** **Output**
A HIGH on TRNSMTP indicates to external logic for both the AUI and TP modes that the MAC is in transmit mode and is putting Manchester-encoded data on the E-10 pins that drive the off-core transceivers.

TSTARTP **Transmit Start** **Output**
The E-10 core asserts a 100-ns positive pulse on the TSTARTP pin to indicate the start of a transmission (or retransmission). The host should supply data on the TDATAI[7:0] pins within 6.4 µs of the TSTARTP pulse. External logic may use this signal to reset the data pointer to the beginning of the transmit data buffer.

2.7 Transmitter Status Signals

The E-10 transmitter status signals may be used by the host to monitor various conditions regarding the transmission of a data frame.

TSECOLP **Transmit Status Excessive Collisions** **Output**
This signal is asserted HIGH when the frame could not be transmitted after 16 attempts. The transmission will then be aborted with no further retry attempts.

TSIDEFP **Transmit Status Initially Deferred** **Output**
This signal is asserted HIGH when the first transmission attempt of a frame is deferred because of activity on the network and the frame was transmitted without a collision. The core keeps the TSIDEFP signal asserted during any subsequent transmission attempt and does not deassert the TSIDEFP signal until after the end of the transmission.

TSLCOLP **Transmit Status Late Collision** **Output**
This signal is asserted HIGH when a collision is detected more than 512 bits into the frame. The transmit engine continues to retry. The time period corresponding to 512 bits is a “slot” time (51.2 µs), and is considered to be the maximum time necessary to transmit data on an Ethernet channel so that all nodes detect activity. If a late collision (after 512 bit times) occurs, it indicates that the Ethernet connection is out of specification and corrective action should be taken.

When the E-10 core detects a collision less than 512 bits into the frame, the TSECOLP, TSMCOLP, or TSOCOLP signals are asserted HIGH, depending on the circumstances surrounding the collision (see the individual signal descriptions for more details).

TSMCOLP **Transmit Status Multiple Collisions** **Output**
This signal is asserted HIGH when more than one transmission attempt resulted in a collision during the transmission of the frame. This signal is also asserted when the transmission is terminated due to the assertion of TABORTP.

TSNCLBP **Transmit Status No Carrier Loopback** **Output**
In AUI mode, TSNCLBP is asserted HIGH when a transmission results in a *transmit carrier loopback* or *transmit carrier dropout error*. If the E-10 core does not detect a signal within 512 bit times from the time it was transmitted, the error condition exists. A transmit dropout condition could result from a broken or missing *coaxial* cable.

In Twisted-Pair mode TSNCLBP is asserted HIGH if a frame is transmitted while the transceiver is in the link-fail state. Link pulses are 100-ns in duration and are transmitted every 16.384 ms in the absence of transmit data. A link fail state could result from a broken or missing receive wire pair.

TSOCOLP **Transmit Status One Collision** **Output**
This signal is asserted HIGH when the frame was transmitted after exactly one collision. This signal is also asserted when the transmission was terminated due to the assertion of TABORTP.

TSSQEEP **Transmit Status SQE Error** **Output**
A HIGH on this output pin indicates a SQE test error.

2.8 General MAC Signals

The general MAC signals connect to the parallel interface and the control system circuitry. The description of each signal follows.

COLLOUTP **Transmit Collision** **Output**

COLLOUTP is asserted (HIGH) when a collision is encountered during a transmission. COLLOUTP is valid for AUI mode and Twisted-Pair half duplex mode. COLLOUTP is not valid for Twisted-Pair full duplex mode. In AUI mode, the collision signal coming from the external *Media Attachment Unit (MAU)* at the collision input pins causes the COLLOUTP signal to be asserted. In Twisted-Pair mode, when simultaneous transmit and receive activity takes place, the E-10 core asserts COLLOUTP. The host must take the operational mode into account when interpreting this signal.

DUPLEXP **Full Duplex Select** **Input**

When this input is asserted, the MAC is in full duplex mode. Full duplex mode is applicable only in the Twisted-Pair mode of operation.

In Twisted-Pair full duplex mode, collision detection is not valid. The host must take the operating mode into account when interpreting the collision output signal (COLLOUTP).

LOOPBKP **Diagnostic Loopback Enable** **Input**

When LOOPBKP is HIGH, the E-10 core ENDEC is in the diagnostic loopback mode and the transmitter output is fed back to the receiver input inside the core. Loopback mode allows testing the E-10 transmitter and receiver up to but not including the off-core transceivers under program control without the need of an external loopback connector. This diagnostic loopback capability is applicable to both the AUI and Twisted-Pair modes. It does not represent the standard loopback function in Twisted-Pair mode (as the core presents an internal on-chip MAU for Twisted-Pair mode)

NOADDRI[47:0]

Node Address **Input**

This 48-bit node address bus is driven with the individual address of the station. It is up to the host to provide the appropriate levels on NOADDRI[47:0] to configure the address.

SELIO **4-Wire and 8-Wire Mixed Signal Cell Select** **Input**

SELIO must be asserted for four-wire Twisted-Pair mode and deasserted for eight-wire Twisted-Pair mode. When SELIO is asserted, the core does not use the PREEP, PREEN, or DATAN signals. For more information on the four-wire and eight-wire modes, see Section 3.3, “Twisted-Pair Interface” on page 3-14.

TP/AUI **Twisted-Pair/AUI Select** **Input**

When TP/AUI is deasserted (LOW), the MAC core is in AUI mode. When the signal is asserted (HIGH), Twisted-Pair mode is selected. Below are listed the principal differences in the way the E-10 core operates in these two modes:

Feature	TP Mode	AUI Mode
SQE Test	No	Yes
Link Pulse Detection	Yes	No
Link Pulse Polarity Detection and Correction	Yes	No
Link Integrity Pulses Generated	Yes	No
Collision Pair Pins (COLLINP, COLLINN) are used	No	Yes
Cause of Loopback Transmit Carrier Error	Link Fail	No Carrier Loopback

It makes no difference to the core if the AUI interface is 6-wire or 9-wire. The transceivers and external circuitry used in either 6-wire or 9-wire AUI operation present the same signals to the MAC core.

For more information on the AUI mode of operation, see Section 3.4, “Attachment Unit Interface (AUI)” on page 3-20. For more information on the twisted-pair mode of operation, see Section 3.3, “Twisted-Pair Interface” on page 3-14.

2.9 Timing and Test Signals

The timing and test signals connect to the parallel interface and the control circuitry of the system. In multiple-core environments, only one core may be the clock master. All other cores must be slaves. For clock duty cycles and tolerances, see Section 4.2, “E-10 Clock Timing,” on page 4-10. The description of each signal follows.

CLK10I **10-MHz Clock In** **Input**
The E-10 core ENDEC uses CLK10I for MAC and bus interface timing. CLK10I should be driven by the CLK10O output pin through a buffer external to the E-10 core.

CLK10O **10-MHz Clock Out** **Output**
This 10-MHz output is derived from the 80-MHz input signal, CLK80I.

CLK20I **20-MHz Clock In** **Input**
The E-10 core uses CLK20I for timing and for the Manchester encoder clocking. CLK20I should be driven by the CLK20O output pin through a buffer external to the E-10 core.

CLK20O **20-MHz Clock Out** **Output**
This 20-MHz output is derived from the 80-MHz input signal, CLK80I.

CLK80I **80-MHz Clock In** **Input**
CLK80I is the master clock source provided to the E-10 core ENDEC. It is the only external timing signal used by the E-10 core ENDEC. CLK80I may be provided as an external oscillator or it may be provided with a PLL circuit as part of some chip logic surrounding the E-10 core.

FASTESTN **Fast Test** **Input**
FASTESTN is used for chip testing purposes only (fast test) and must be left HIGH during normal operation.

GNDN **Ground** **Input**
The GND signal must be asserted (LOW) during normal core operation. It is used for testing the core.

RESETN **Core Reset** **Input**
After power is applied to the chip, RESETN should be asserted LOW for a minimum of 200 ns (at least 100 ns after TEST1N goes HIGH) to force initialization.

TESTSEP **Scan Enable** **Input**
TESTSEP is the scan enable pin for testing the module in the ENDEC. The ENDEC has a full-scan test chain built into it.

TESTSIP **Scan Input** **Input**
TESTSIP is the scan input pin for full scan testing.

TESTSOP **Scan Output** **Output**
TESTSOP is the scan output pin for full scan testing.

TEST1N **Test 1** **Input**
TEST1N is for chip testing purposes only (fast test) and must be left HIGH in normal operation.

TEST2N **Test 2** **Input**
TEST2N must be left HIGH in normal operation. It must be asserted LOW for 100 ns to initialize the ENDEC core logic. The CLK10O AND CLK20O outputs become operational only after the TES2N signal is deasserted (HIGH) during initialization RESETN is then asserted (LOW) for an additional 100 ns to initialize the rest of the ENDEC logic. In test mode, TEST2N is used for testing the ENDEC core.

TMODE **Test Mode** **Input**
TMODE must be left deasserted (LOW) during normal operation and asserted (HIGH) in test mode. TMODE is used during scan testing.

VCC **Positive Voltage** **Input**
The VCC pin should be asserted (HIGH) during normal operation. It is used for core testing.

Chapter 3
E-10 Functional Description

This chapter provides a functional description of the E-10 core and contains the following sections:

- Section 3.1, “Media Access Control (MAC)”
- Section 3.2, “Encoder/Decoder (ENDEC)”
- Section 3.3, “Twisted-Pair Interface”
- Section 3.4, “Attachment Unit Interface (AUI)”

3.1 Media Access Control (MAC)

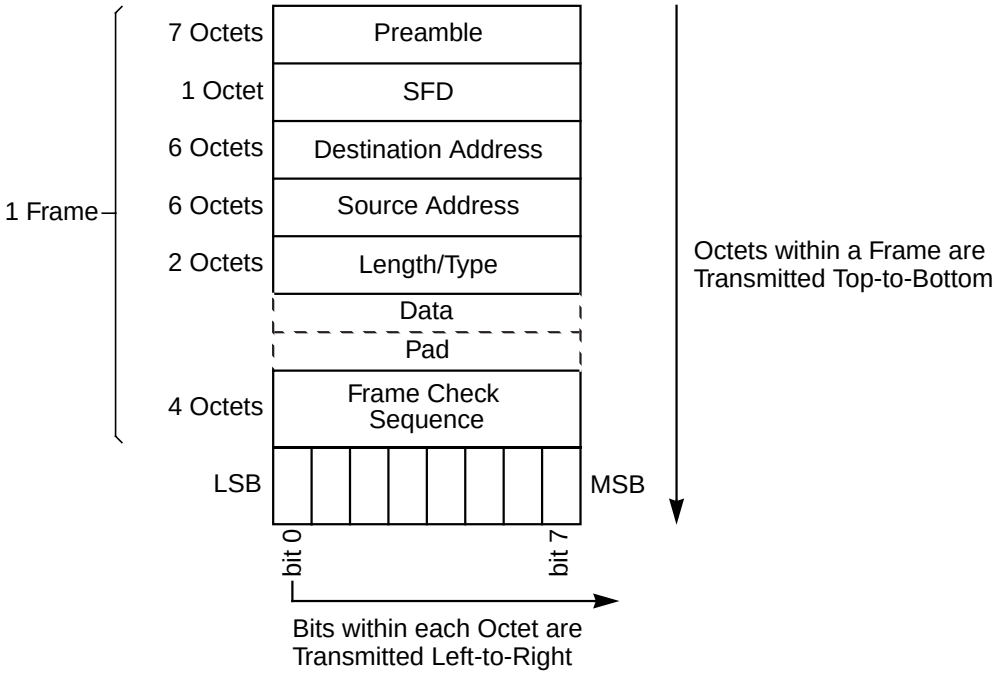
The MAC is the portion of the E-10 core that handles the Carrier Sense Multiple Access with Collision Detection (*CSMA/CD*) protocol for transmission and reception of frames. The MAC performs the following functions:

- Frame Data Encapsulation and Decapsulation
- Frame Transmission
- Frame Reception

3.1.1 Frame Data Encapsulation and Decapsulation

The format of the frame generated by the ANSI/IEEE Ethernet 802.3 protocol consists of several fields, as explained in the following subsections. Figure 3.1 shows the overall structure and order of transmission of bits and octets of a frame.

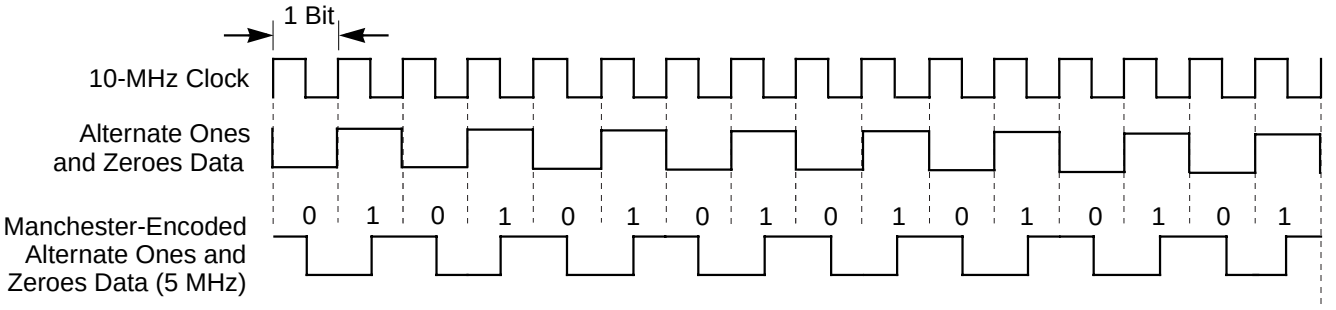
Figure 3.1 MAC Frame Format



3.1.1.1 Preamble Field

The preamble field is a 7-octet (56-bit) alternating one-zero pattern (starting with a one), which is Manchester-encoded before being transmitted onto the media. The alternating one-zero pattern ensures that there are no transitions between bits in the Manchester-encoded signal, which results in a 5-MHz signal (see Figure 3.2). Because the twisted-pair Ethernet cable attenuates higher frequencies, the 5-MHz signal creates a perfect signal for acquisition by the digital Phase-Locked Loop (PLL). Any pattern other than an alternating one-zero pattern would create a higher-frequency signal and make acquisition more difficult. In addition, an alternating one-zero data pattern, when Manchester-encoded, has data transitions at the same clock edge, which makes it easier for the PLL to achieve lock.

Figure 3.2 Alternate One-Zero Manchester Encoding



3.1.1.2 Start Frame Delimiter (SFD) Field

The eight-bit start of frame delimiter field contains the 10101011_2 bit pattern. This bit pattern allows alignment of the data received in the rest of the frame.

3.1.1.3 Address Fields

The frame has two 48-bit address fields. The first field contains the destination address and specifies the address(es) for which the frame is intended. If the first bit of the destination address is a zero, the address is an individual address. A one in the first bit indicates a multicast or group address. The second address is the source address and should contain the individual address of the station from which the message originated.

3.1.1.4 Length/Type Field

The two-byte length field indicates the number of data bytes in the data field. The MAC does not interpret the data in the length field and does not treat it any differently than the data field.

3.1.1.5 Data and Pad Field

The data field contains a sequence of fully transparent data bytes; that is, the data bytes are not analyzed or interpreted in any way by the MAC. The size of the data field may be between zero and 1,500 bytes, but can be extended up to 4,500 bytes or more, depending on the clock accuracy of the transmitting and receiving stations.

The function of the pad field is to ensure minimum frame size. If the supplied data field contains less than 46 bytes of data, the MAC can add a pad field to make the sum of bytes in the data and pad field equal to 46. Appended pad data consists of bytes filled with zeroes.

3.1.1.6 Frame Check Sequence (FCS) Field

The transmit and receive algorithm uses the standard 802.3 four-byte frame check sequence (FCS) field to ensure data integrity. The E-10 core uses a linear feedback shift register to compute the value in the FCS field. The FCS is a function of the content of the source address, destination address, length, data, and pad fields. The generating polynomial shown in Equation 3.1 defines the encoding. The nine MSBs of the FCS may be used by an external hashing table function to perform multicast address filtering.

Equation 3.1 FCS Encoding

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^3 + x^2 + x + 1$$

3.1.2 Frame Transmission

Frame transmission is enabled with the TAVAILP signal. TAVAILP indicates that at least one frame is ready to be transmitted. All transmissions start by complying with the rules of deference; that is, they monitor the physical medium for activity. If no activity exists, the transmit cycle starts.

During the start of a transmission, the transmitter asserts a 100-ns positive start of transmission pulse (TSTARTP). The start pulse resets the transmit pointer to the beginning of the transmit buffer. When the TREADDP signal is pulsed (HIGH), it indicates to the external control logic that data is read on the LOW-to-HIGH transition of the CLK10I input. If a collision is detected during a transmission, the collision enforcement rules are followed, and the transmission is aborted. If the signals TABORTP and TFINISHP are not asserted, and the frame was not retried 15 times, backoff and deference rules are followed and the frame transmission is retried.

The external control logic asserts the TLASTP signal to indicate that the last byte of data to be transmitted is present at the TDATAI[7:0] pins. When a frame is transmitted successfully, or when a serious error is

detected during the transmission, the transmitter asserts the transmitter done (TDONEP) pulse. The TDONEP pulse indicates to the external logic that either the transmission is complete, or the TABORTP or TFINISHP signals were asserted before the end of the transmission, or that the transmitter exhausted its ability to transmit the frame successfully. External logic has a minimum of 800 ns to deassert or assert TAVAILP indicating whether or not a new frame is ready for transmission.

3.1.2.1 Carrier Deference Rules

Even when it has nothing to transmit, the transmit portion of the MAC monitors the traffic on the physical medium. When there is no traffic (a carrier is not detected by the MAC and the MAC is not transmitting) the MAC starts a 9.6 µs interframe timer. The interframe timer is reset if the MAC senses a carrier during the first 5.6 µs of the interframe gap after a reception. During the time from 5.6 µs to 9.6 µs, the interframe timer is not reset, to ensure fair access to the medium.

If, at the end of the interframe gap, a frame is waiting to be transmitted, transmission is started regardless of the presence of a carrier. If a carrier is present, a collision occurs so that a node constantly transmitting is forced to back off. If, at the end of the interframe gap, there is no frame waiting to be transmitted, the MAC starts monitoring for a carrier again, and resets the interframe timer as soon as it detects a carrier.

3.1.2.2 Interframe Spacing

The carrier deference method described above ensures that the E-10 provides an interframe gap of 9.6 µs. The interframe gap ensures fair arbitration among all sources trying to transmit and prevents one transmitter from dominating the transmission channel.

3.1.2.3 Collision Enforcement Rules

When a collision is detected during a frame transmission (for the definition of a frame, see the subsection entitled “Frame Data Encapsulation and Decapsulation” on page 3-1), the transmission is not terminated immediately. The preamble and start of frame delimiter (SFD) are transmitted unmodified regardless of the collision state. If a collision is detected before the preamble and SFD have finished transmitting, a 32-bit *jam* pattern of alternating ones and zeros is transmitted immediately after the SFD and then the transmission ends. If the collision is detected after

the preamble and SFD, while data is being transmitted, the data transmitted changes to a jam pattern of alternating ones and zeros for 32 bits before the transmission is terminated.

3.1.2.4 Transmission Backoff Algorithm

When a transmission attempt has terminated due to a collision, the transmission is retried until either it is successful or 15 retries (16 attempts total) have been terminated due to collisions. A controlled randomization process called “truncated binary exponential backoff” schedules the retransmission. At the end of enforcing a collision (jamming), the transmit engine delays before attempting to retransmit the frame. The delay is in 51.2 µs increments, or *slot times*. The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer r in the range:

$-1 < r < 2^k$, where $k = \min(n, 10)$

Note that min (n, 10) signifies that the value is the minimum of n or 10, whichever is less.

A 25-bit Linear Feedback Shift Register (LFSR) generates a pseudo-random number. Because of potential synchronization problems between multiple stations on the network using the same pseudo-random number generator, the number is further randomized every transmission attempt with the station’s individual address.

3.1.2.5 Source Address Insertion

The hardware can insert the source address during transmission from the individual address input pins. In this mode, the host is responsible for supplying the first six bytes (destination address). The six address bytes are transmitted from the host on the E-10 transmit data input pins (TDATAI[7:0]). The next six bytes transmitted are read from the individual address registers (source address). After these two addresses are sent, the transmitter returns to the transmit data pins and continues transmitting subsequent data bytes from there. The byte counter in the transmit data buffer must not include the six source address bytes in this mode, but must include the six destination address bytes. The transmitter is in source address insertion mode when the TCTRI[0] pin is HIGH.

3.1.2.6 Automatic Pad Insertion

During transmission, a pad field can be inserted by the hardware. In this mode enough bytes are added just before the FCS field to increase the total data field length to the IEEE 802.3 minimum of 46 bytes. The data inserted in the pad field is all zeroes. The transmitter is in automatic pad insertion mode when the TCTRI[2] pin is HIGH.

3.1.2.7 Frame Check Sequence (FCS) Insertion

During transmission the E-10 hardware can compute and transmit the FCS field automatically. In this mode, a 32-bit polynomial is computed from the source address, destination address, length, data, and pad fields and transmitted immediately following the data or pad field. The transmitter is in FCS insertion mode when the TCTRI[1] pin is HIGH.

If the host instead is going to supply the FCS field and the E-10 core is going to insert the source address, the host must ensure that the FCS is computed based on the 48-bit source address being supplied to the E-10 core on the NOADDRI[47:0] pins.

3.1.2.8 Transmit Status Indications

The six E-10 pins listed below indicate the status of Ethernet transmission with regard to collisions and errors:

- Late Collision (TSLCOLP). The bit durations for transmit and receive data are each 100 ns. When a collision onset is detected after the allowed window of 512 bit times (51.2 μs), the E-10 core asserts the late collision error bit (TSLCOLP) HIGH. A late collision is treated just like a normal collision, following the collision enforcement rules, and the transmission is retried.
- Excessive Collisions (TSECOLP). When the transmission engine has attempted to transmit a frame 16 consecutive times, and all attempted transmissions have terminated due to a collision, the E-10 core asserts the excessive collision error pin (TSECOLP) HIGH, and no more transmit retries are performed.

- Transmit Carrier Loopback Error (TSNCLBP). In AUI mode, when an error is detected in the receive carrier signal that is required to be fed back during the transmission of a frame, the E-10 core asserts the transmit carrier loopback error pin (TSNCLBP) HIGH. Two different conditions can cause the transmit carrier loopback error pin to be asserted in AUI mode:
  - During transmission, no carrier is received during the first 512 bit times (51.2 µs) of the transmission.
  - During transmission, carrier was received but was interrupted before transmission stopped.

The transmit carrier loopback error has no effect on the transmission/retransmission process, but no SQE test is performed.

In Twisted-Pair mode, the E-10 core asserts the transmit carrier loopback pin HIGH to indicate a link failure during the transmission of the frame. A link failure can be caused by a twisted-pair transceiver failure or by a broken twisted-pair cable. In the link fail state, the E-10 core does not route the Manchester-encoded data to the transmitter pins, but it still transmits link integrity pulses.

- SQE Error (TSSQEEP). The E-10 core asserts the signal quality error pin (TSSQEEP) HIGH when the MAC detects all the following conditions:
  - The E-10 core is in AUI mode
  - The E-10 core is in half-duplex mode
  - SQE testing is enabled (TCTRI[3] pin is HIGH)
  - The late collision status pin (TSLCOLP) is not HIGH
  - The excessive collisions status pin (TSECOLP) is not HIGH
  - The transmit carrier loopback error status pin (TSNCLBP) is not HIGH
  - No SQE signal was received in the first 5.6 µs of the interframe gap
- One Collision (TSOCOLP). The E-10 core asserts the one collision status pin (TSOCOLP) HIGH when the frame is transmitted after exactly one collision. If more than one collision occurred before the frame was transmitted, the TSMCOLP pin is asserted (HIGH) and the TSOCOLP pin is deasserted (LOW). Assertion of the TSOCOLP pin is not an error indication, but is intended only for information, and

can be used to update network statistics counters. When the transmission of a frame is terminated with the signal TABORTP, the E-10 core asserts the TSOCOLP signal (together with TSMCOLP) to indicate this fact to external logic. Section 2.6, “Transmitter Signals,” contains a description of the TABORTP signal. TSOCOLP is valid when the TDONE pin pulses.

- Multiple Collisions (TSMCOLP). The E-10 core asserts the multiple collision status pin (TSMCOLP) HIGH when the frame is transmitted after more than one collision. This pin is not an error indication, but is intended only for information, and can be used to update network statistical counters. When the transmission of a frame was terminated with the signal TABORTP, the E-10 core asserts the TSMCOLP signal (together with TSOCOLP) to indicate this fact to external logic. TSMCOLP is valid when the TDONEP pin pulses.

3.1.3 Frame Reception

Frame reception is allowed after the receiver enable signal (RENABP) is asserted. After the transceiver squelch circuitry detects a valid signal, and the receiver PLL locks onto the incoming signal as indicated by assertion of the RLOCKEDP signal, the receiver starts searching for a valid start of frame delimiter. The PLL takes a minimum of six and a maximum of eight bit times (600 to 800 ns) to achieve lock.

A valid start of frame delimiter is defined as 0b10101011. When the start of frame delimiter is detected, the receiver pulses the RSTARTP pin. A pulse on the RSTARTP pin informs the external logic to make available a new receive buffer, because received data will start arriving in 800 ns. Every time a new byte of received data is available on the RDATAO[7:0] bus, the E-10 receiver pulses the RBYTEP pin.

The first 48 bits of the frame contain the destination address. The MAC receiver portion of the E-10 core compares the destination address bits with the data on the 48-bit node address bus (NOADDRI[47:0]), and when the bits are equal, allows the continued reception of the frame. When the receiver promiscuous mode pin (RPMENP) is asserted, any individual destination address validates the frame, and allows the reception process to continue. When the destination address is a multicast address, including the broadcast address (the address contains all ones), the receiver computes a nine-bit hash function from the destination address, and leaves the decision to accept or reject the frame to external logic.

When an *end-of-frame delimiter* is detected, the receiver accepts the frame and generates a 100-ns pulse on the RDONEP pin when all the following conditions are true:

- At least one address filter passed
- The frame was at least 64 bytes in length
- The receiver is still enabled

When the end-of-frame delimiter does not generate an RDONEP pulse, the receiver instead pulses the RCLEANP pin, which indicates to the external logic that it must ignore the data received. It is then up to the host logic to manage the receive buffer space properly (either give up the buffer space so it can be used for other transmit or receive data or allocate another buffer).

3.1.3.1 Address Filtering

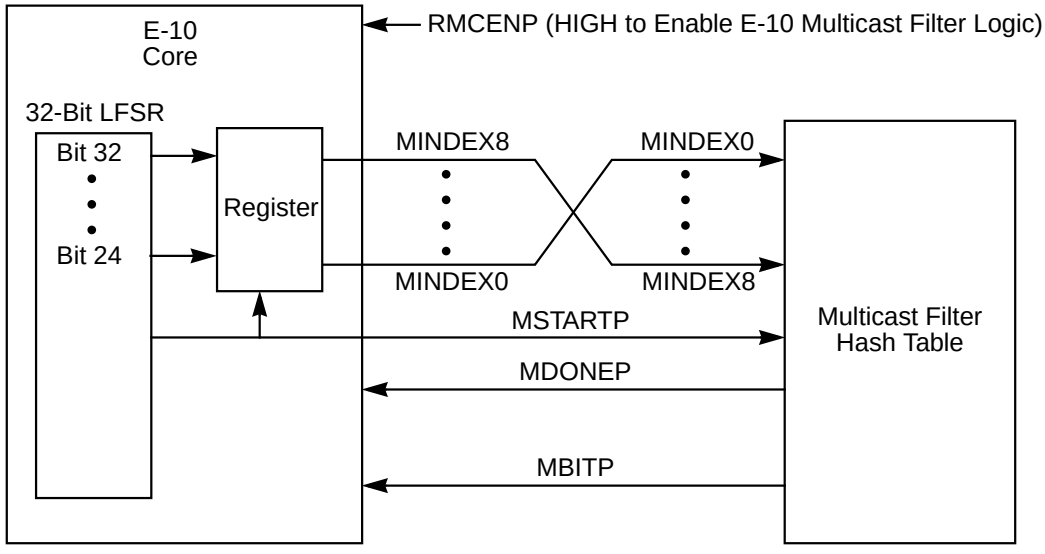
Three address filter mechanisms are present in the receiver, two for individual addresses, and one for multicast addresses. At least one of these address filters must pass to accept the received frame. The address filters are listed below:

- *Individual Address Filter*. The first bit of an individual address is a zero. The incoming destination address is compared with the data from the individual address pins. When all 48 bits match and the receiver is enabled (RENABP pin asserted HIGH), the address filter passes.
- *Individual Address Promiscuous Mode*. When the external logic asserts the individual address promiscuous mode enable pin (RPMEN) HIGH and the destination address is an individual address, the address filter always passes, and the incoming frame is received.
- *Multicast Address Filter*. The first bit of an multicast address is a one. When the destination address bits that are received in the frame contain a multicast address, the E-10 core uses its built-in FCS generator to compute a nine-bit polynomial (the nine MSBs of the 32-bit FCS generator) from the incoming address. The value of this polynomial can be used as an index into an external multicast filter hash table. External logic can decide to either accept or reject the incoming frame. The external logic asserts the RMCENP pin (HIGH) to enable the multicast address filter. Figure 3.3 shows the general

host implementation of a multicast filter. Section 2.5, “Multicast Filter Signals,” in Chapter 2, “Signal Descriptions,” explains the functions of the individual signals shown in the figure.

When the destination address is all ones, it indicates a broadcast address. When the E-10 core detects a broadcast address, it receives the incoming frame.

Figure 3.3 Host Multicast Filter Implementation



3.1.3.2 FCS Checking

During reception, the FCS value is checked against the value computed by the receive CRC checker. If the two values do not match, the frame is received and the E-10 core asserts the FCS error pin (RSFCSEP) HIGH to indicate data corruption in the frame. The decision to accept or reject the frame is left to external logic.

3.1.3.3 Frame Size Checking

Frame size checking is performed on every received frame. If a frame is less then 64 bytes in length, the receiver cleanup pulse (RCLEANP) discards the received data (collision fragment). IEEE 802.3 specifies a maximum frame size of 1,518 bytes, but the MAC does not do any maximum length checking, and much larger frames (for instance 4,500 bytes) can be received, as long as care is taken not to exceed PLL elasticity. The application is responsible for checking the maximum frame size and reporting any errors.

3.1.3.4 Start of Frame Delimiter Checking

The start of frame delimiter, a bit sequence of 0b10101011 that occurs following the preamble, starts the reception of bytes.

3.1.3.5 Receive Status Indications

The five E-10 pins listed below indicate the status of Ethernet reception with regard to collisions and errors.

- Frame Check Error (RSFCSEP). The E-10 core asserts the frame check error pin (RSFCSEP) HIGH when bits of the incoming frame do not generate a CRC identical to the one in the received FCS field, indicating data corruption has occurred in the received frame.
- Dribble Bit Error (RSDRBLEP). The E-10 core asserts the dribble bit error pin (RSDRBLEP) HIGH at the end of a frame when less than a complete byte has been received, indicating the reception of from one to seven “dribble” bits. The E-10 core asserts the RSDRBLEP pin HIGH independently of the frame check error bit. RSDRBLEP can be ignored if the RSFCSEP pin is not set.

  The reason RSDRBLEP can be ignored is that the FCS is updated every eight bits. If there are less than eight dribble bits (from one to seven bits) at the end of the frame and the current FCS is correct, any extra dribble bits (less than eight) do not matter. However, if there are eight or more dribble bits, the FCS will be updated and will most likely be wrong due to the dribble bits. In this case, RSDRBEL should not be ignored.
- Phase-Locked Loop Error (RSPLLEP). The E-10 core asserts the phase-locked loop error pin (RSPLLEP) when, during reception of a frame, the digital phase-locked data recovery circuit elasticity is exhausted. The elasticity becomes exhausted due to drift between the 10-MHz clock frequency of the device sending the data and the ENDEC 10-MHz clock frequency. See the subsection entitled “PLL Characteristics” on page 3-13 for an explanation of elasticity. RSPLLEP is asserted when a frame is received with a transmit clock error sufficiently larger than the IEEE 802.3 requirement of 0.01% that the PLL elasticity is exhausted within a normal frame, or when a frame length sufficiently larger than that specified in IEEE 802.3 has caused the elasticity to be exhausted even when the clock is within tolerance.

- Match Individual Address (RSMATIP). The E-10 core asserts the match individual address pin (RSMATIP) HIGH when the destination address matches the node address.
- Match Multicast Address (RSMATMP). The E-10 core asserts the match multicast address pin (RSMATMP) HIGH or deasserts it LOW as a result of the decision of the external multicast filter logic to accept or reject the multicast address.

3.2 Encoder/Decoder (ENDEC)

The ENDEC consists of the Manchester encoder, Manchester decoder, and the digital phase-locked loop.

3.2.1 PLL Characteristics

The digital phase-locked loop used for data recovery has the following characteristics:

- Sampling
  - Sampling Frequency: 160 MHz
  - Sampling Interval: 6.25 ns

  With the above sampling parameters, each bit of 100 ns is sampled 16 times.
- Jitter Tolerance: ± 18.00 ns

  This parameter indicates that the incoming data bits may have a jitter up to ±18.00 ns and the digital PLL will still work acceptably.
- Tracking speed
  - Initial (first 4.8 µs): 0.39%
  - Steady-state (after 4.8 µs): 0.098%

  When first attempting to lock on to an oncoming data stream (during the first 4.8 µs), the PLL looks every 16 bits to see if a bit transition is occurring in the center of the sampling window. Dividing the sampling interval of 6.25 ns by the 16-bit interval (1600 ns) yields 0.0039 or 0.39%.

After the first 4.8 µs, the PLL maintains a window of 64 bits for finding a transition. Dividing the sampling interval of 6.25 ns by the 64-bit interval (6400 ns) yields 0.00098 or 0.098%.

- Elasticity
  - Maximum clock drift time 600 ns (6 bit times)
  - Maximum clock error @ 1518 byte frame: 0.05%
  - Maximum clock error @ 4500 byte frame: 0.016%

  Elasticity indicates the tolerance of the PLL to slightly different clock rates between a transmitter and a receiver. The E-10 core allocates a buffer of 13 bits to accommodate clock drift. The 13-bit buffer allows a clock drift of six bits (600 ns) from center in either direction during a frame transfer.

  For a 1518-byte frame, consisting of six bytes of destination address, six bytes of source address, two bytes of length, 1500 bytes of data, and four bytes of FCS (6 + 6 + 2 + 1500 + 4 = 1518), the maximum clock drift allowed is 0.05% (0.05% x 1518 bytes x 8 bits/byte = 6 bits).

  For a 4500 byte frame, the maximum clock drift allowable during frame transfer is 0.016% (0.016% x 4500 bytes x 8 bits/byte = 6 bits).

3.3 Twisted-Pair Interface

The E-10 core supports two twisted-pair configurations:

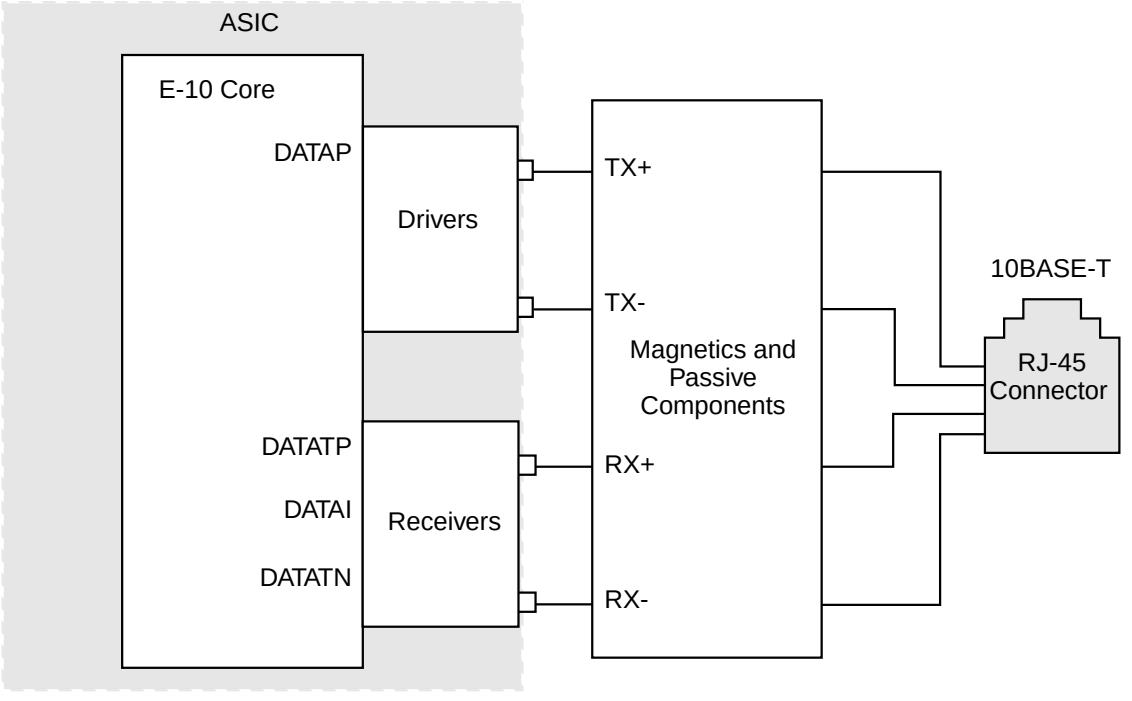
- Four-wire
- Eight-wire

3.3.1 4-Wire Twisted-Pair Interface

The four-wire E-10 twisted-pair interface is shown in Figure 3.4. The four-wire interface implements CoreWare mixed signal transmitter and receiver cores to prepare the E-10 core's I/O signals for connection to the network. An ASIC implementation of an Ethernet port using the E-10 core and mixed signal I/O cores provides a simple interface to the network.

A four-wire interface is usually best for multiport applications. The mixed signal I/O cores reduce the number of ASIC device pins and external passive components.

Figure 3.4 4-Wire Twisted-Pair Interface Using Mixed Signal Cores



3.3.1.1 4-Wire Twisted-Pair Transmit Interface

With the four-wire twisted-pair interface, the E-10 core outputs a single Manchester-encoded transmit signal, DATAP, to a mixed signal differential driver core. The driver produces low common-mode noise differential outputs, which provide the desired output swing to the magnetics (transformer). The mixed signal driver reduces the generation of high-frequency signal components, thereby minimizing external filtering requirements and reducing external component costs.

3.3.1.2 4-Wire Twisted-Pair Receive Interface

The four-wire receiver interface complies with the receiver specifications of the IEEE 802.3 10BASE-T standard, including noise immunity, propagation delays, jitter requirements, and received signal rejection criteria (Smart Squelch).

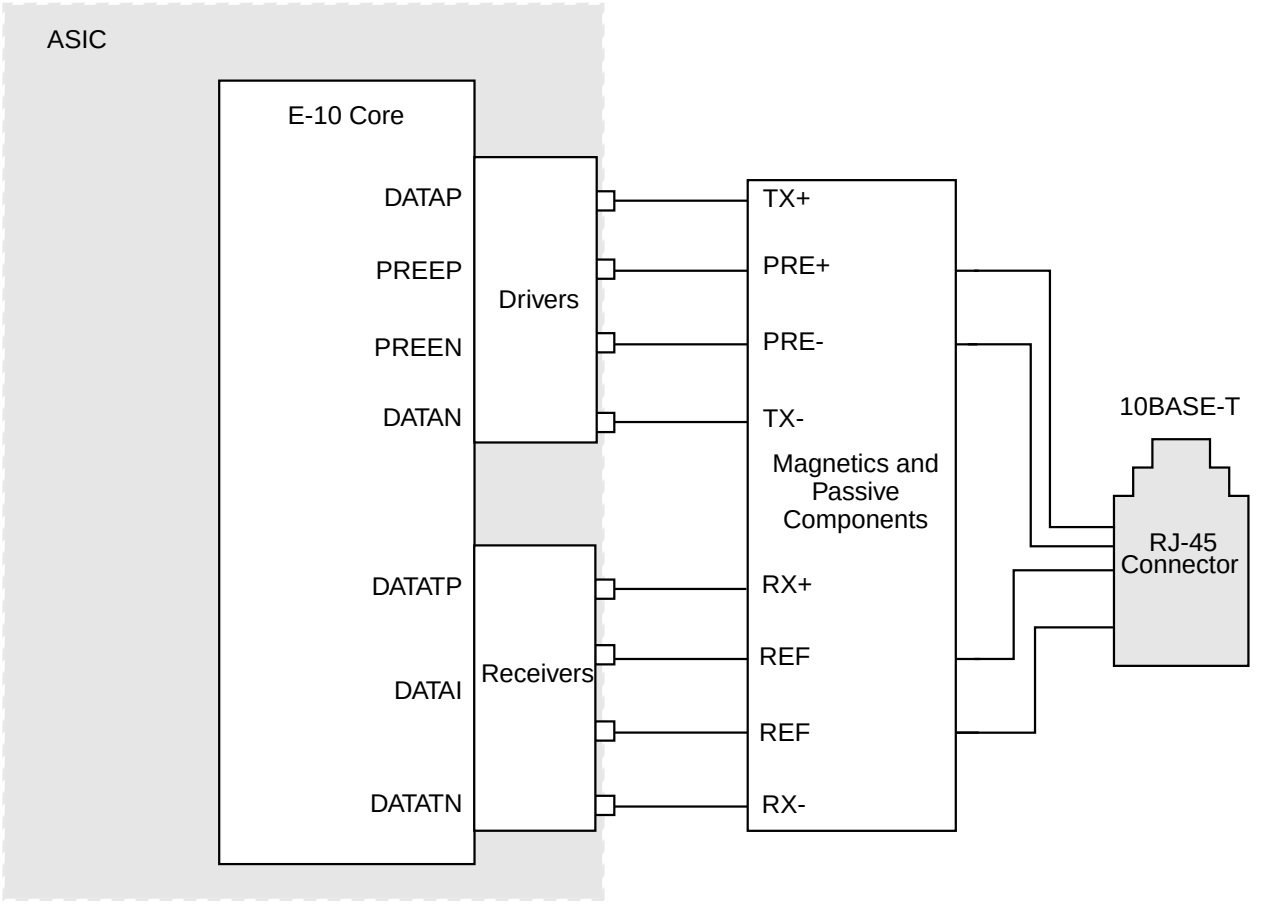
The four-wire twisted pair receive interface has three signals at the E-10 core interface: DATATP, DATATN, and DATAI. The three signals are inputs to the E-10 core and come from a two-input differential mixed signal receiver.

The receiver converts the two differential analog data signals from the network to DATATP, DATATN, and DATAI, which are CMOS-level single-ended digital outputs. The three signals switch in such a way that the E-10 core can properly perform data detection, reverse polarity detection, and smart squelch.

3.3.2 8-Wire Twisted-Pair Interface

The eight-wire E-10 twisted-pair interface is shown in Figure 3.5. This interface uses data pre-emphasis on data transmitted from the core and threshold detection circuitry on the data being received by the core.

Figure 3.5 8-Wire Twisted-Pair Interface



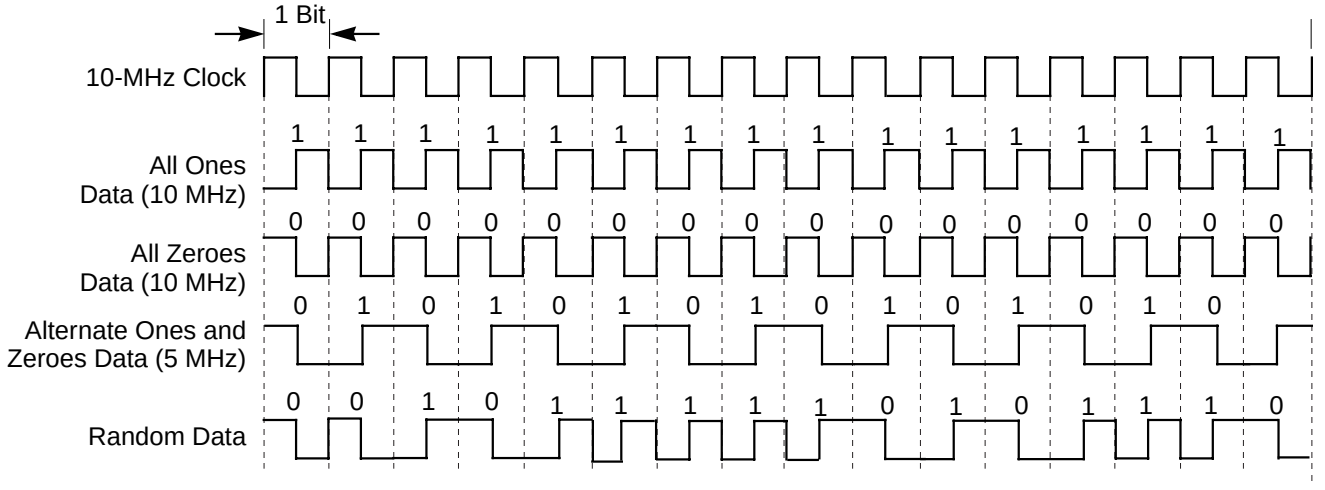
3.3.2.1 8-Wire Twisted-Pair Transmit Interface

With the eight-wire twisted-pair interface, the core outputs four transmit signals, the true and complemented (differential) Manchester-encoded data (DATAP and DATAN) and those signals delayed by 50 ns (PREEP and PREEN). These four signals are sent through four individual transmit buffers and resistively combined (DATAP with PREEP and DATAN with PREEN). The technique of resistively combining the signals is known as digital pre-emphasis and provides the necessary electrical driving capability and predistortion control for transmitting signals over a maximum length twisted-pair cable, as specified by the IEEE 802.3 10BASE-T standard. Digital pre-emphasis compensates for the twisted-pair cable, which acts like a low-pass filter and causes greater attenuation to the 10-MHz (50-ns) pulses of the Manchester encoded waveform than the 5-MHz (100-ns) pulses. When a data stream of all ones or all zeroes is present, Manchester encoding causes a transition

every bit time, which creates a 10-MHz bitstream. With a data stream of alternate ones and zeroes, Manchester encoding causes a transition every other bit time, which creates a 5-MHz bitstream. Figure 3.6 shows how different data patterns are Manchester encoded.

The differential Manchester-encoded signal is passed to an external transmit filter. The transmit function meets the propagation delays and jitter specified by the standard.

Figure 3.6 Manchester Encoding



3.3.2.2 8-Wire Twisted-Pair Receive Interface

The eight-wire receiver interface complies with the receiver specifications of the IEEE 802.3 10BASE-T standard, including noise immunity, propagation delays, jitter requirements, and received signal rejection criteria (Smart Squelch).

With the eight-wire twisted-pair receive interface, there are three input signals at the E-10 core interface: DATATP, DATATN, and DATAI. These input signals are the outputs from three distinct differential receivers.

In a similar fashion to the four-wire interface, the three input signals switch in such a way that the E-10 core can properly perform data detection, reverse polarity detection, and smart squelch.

Following is a functional description of the twisted-pair interface. It includes these sections:

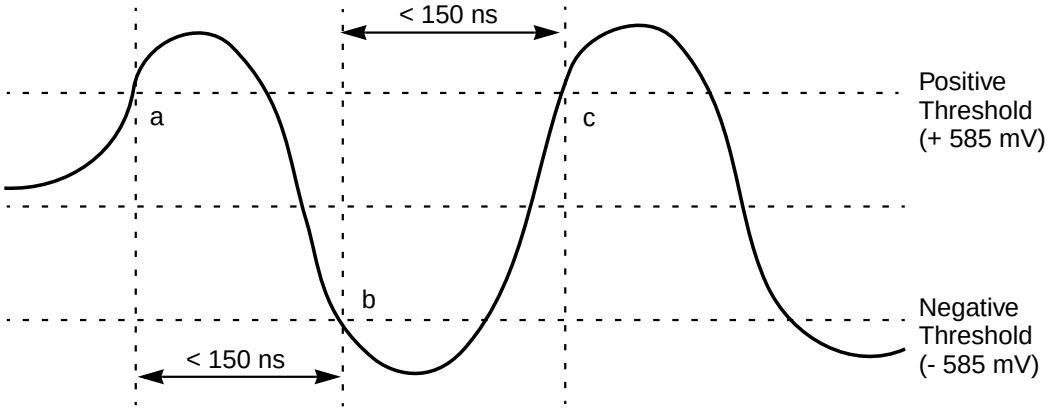
- Squelch
- Link Test Function
- Polarity Detection and Correction

3.3.3 Squelch

An intelligent (smart) receive squelch is implemented on the receiver differential inputs to ensure that impulse noise on the receiver inputs is not mistaken for a valid signal. The smart squelch logic uses a combination of amplitude and timing measurements to determine the validity of data on the twisted-pair inputs.

The squelch circuitry operation is illustrated in Figure 3.7. Squelching determination starts when the input signal crosses the positive or negative threshold (a). To continue a valid signal sequence, the signal then has to cross the other threshold (b) within 150 ns. To complete the valid signal process, the input signal has to cross the original threshold (c) again within 150 ns. If the signal proves to be valid, the smart squelch logic does not suppress the signal. However, if not all of the conditions just outlined are met, the signal is suppressed.

Figure 3.7 Squelch Signal



3.3.4 Link Test Function

The link test function is implemented as specified by the IEEE 802.3 10BASE-T standard. During periods of transmit pair inactivity, Link Test pulses are periodically sent from any transmitting device over the twisted-pair medium to allow constant monitoring of medium integrity. Link pulses, which are 100 ns wide, are transmitted from the E-10 core every 16.384 ms in the absence of transmit data. The core expects to receive a link pulse every 96 ms.

The absence of serial Link Integrity pulses on the receiver inputs causes a Link Fail State to occur. In the Link Fail State, data transmission, data reception, and the collision detection functions are disabled and remain disabled until valid data or eight consecutive Link Test pulses appear on the receiver inputs.

When the E-10 core identifies the link as functional, the E-10 core asserts the LPASSP pin HIGH to indicate that the link status is good.

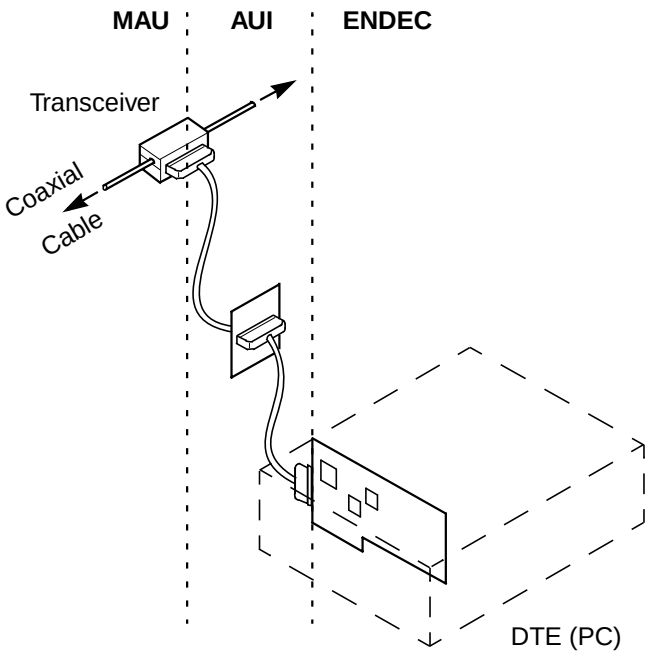
3.3.5 Polarity Detection And Correction

The receive function includes the ability to invert the polarity of the signals appearing at the receiver pair if the polarity of the received signal is reversed, as in the case of a wiring error. This feature allows frames received from a reversed twisted-pair interface to be corrected prior to transfer to the E-10 core. The function uses link pulses to determine polarity of the received signal. A reversed polarity condition is detected when seven consecutive opposite-polarity receive link pulses are detected without receipt of a link pulse of the expected polarity.

3.4 Attachment Unit Interface (AUI)

An AUI provides the link from a 10BASE-T network to a 10BASE-5, 10BASE-2, or 10BASE-F network. As shown in Figure 3.8, an AUI provides the appropriate interface to a Medium Attachment Unit (MAU) so that the MAU can interface to a variety of physical media.

Figure 3.8 10BASE-5 AUI Connection



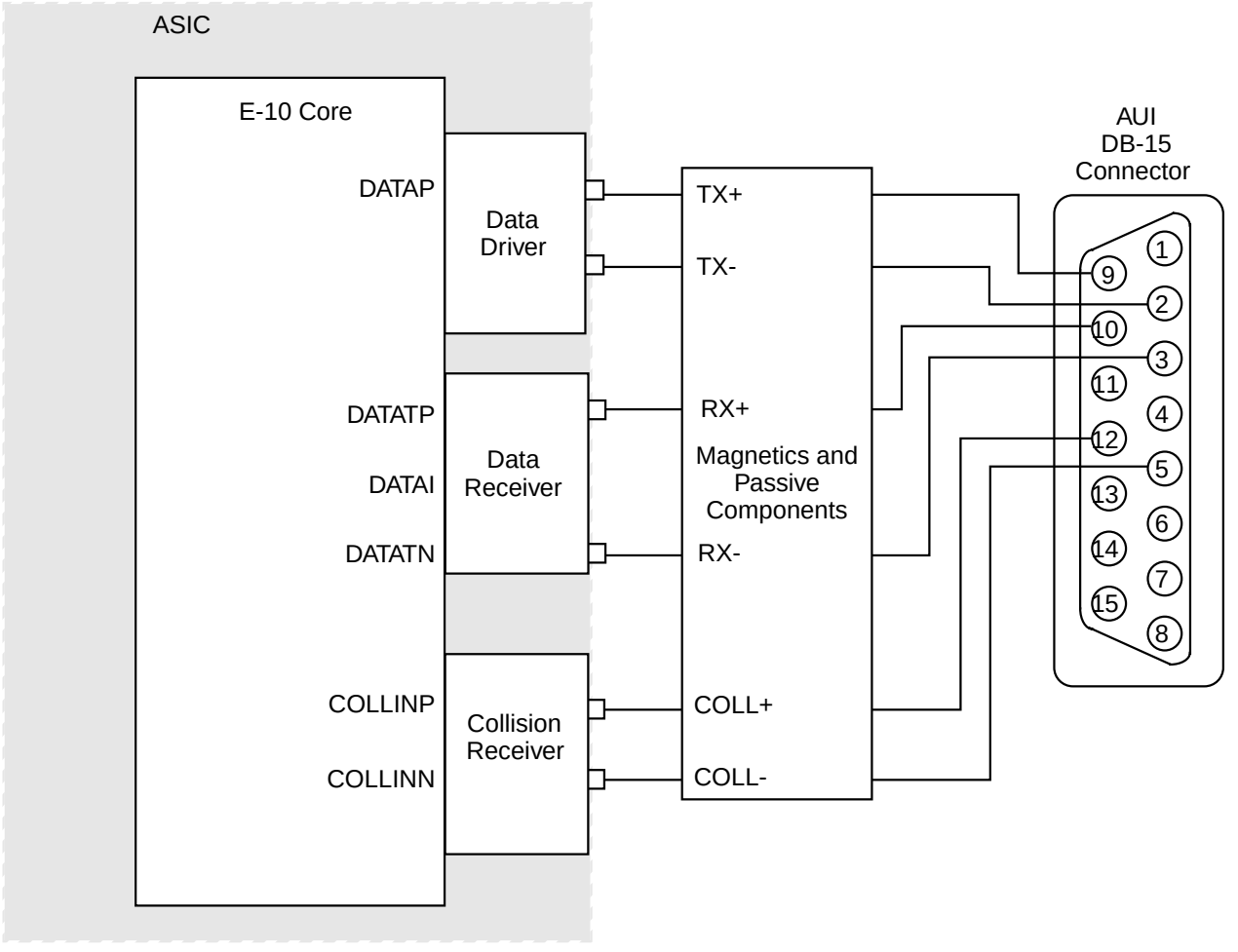
AUIs provide transmit, receive, and collision control functions. The E-10 core supports two different Attachment Unit Interface (AUI) configurations:

- Six-wire
- Nine-wire

3.4.1 6-Wire AUI Interface

The six-wire E-10 AUI interface shown in Figure 3.9 implements CoreWare mixed signal transmitter and receiver cores to prepare the E-10 core's I/O signals for connection to the network. An ASIC implementation of an Ethernet port using the E-10 core and mixed signal cores, along with a few discrete components provide impedance matching, isolation, filtering and electromagnetic interference (EMI) suppression.

Figure 3.9 AUI 6-Wire Interface



Without the integrated mixed signal I/O cores, multiple-port interfaces produce high common-mode coherent noise, which requires the use of expensive filtering to meet FCC requirements.

3.4.1.1 6-Wire AUI Transmit Interface

With the six-wire AUI interface, the E-10 core outputs a single Manchester-encoded signal, DATAP, to a mixed signal differential driver core. The driver produces low common-mode noise differential outputs. Using controlled impedance voltage, the driver produces the desired output swing to the magnetics (transformer).

Using mixed signal drivers reduces the generation of high-frequency signal components, which propagate easily and cause interference. High-frequency components must otherwise be eliminated with external filtering. Using mixed signal drivers minimizes external filtering requirements and thereby reduces the associated external component costs.

3.4.1.2 6-Wire AUI Receive Interface

The six-wire twisted pair receive interface provides a receiver for data and a receiver for collision control.

The data receiver has three signals at the E-10 core interface: DATATP, DATATN, and DATAI. The three signals are inputs to the E-10 core and come from a two-input differential mixed signal receiver.

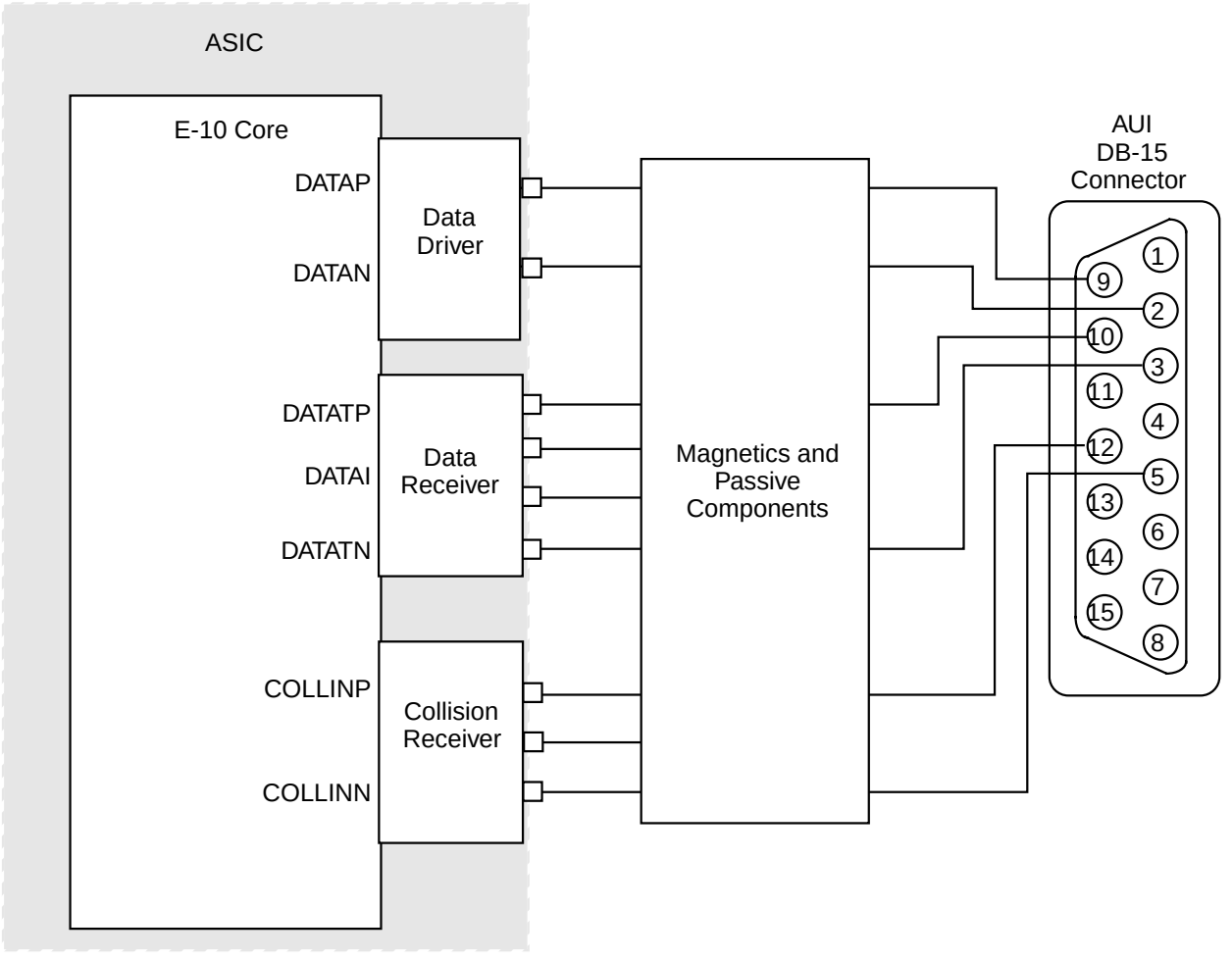
The data receiver converts the two differential analog data signals from the network to DATATP, DATATN, and DATAI. The three signals switch in such a way that the E-10 core can properly perform data detection, reverse polarity detection, and smart squelch.

The collision receiver has two signals at the E-10 core interface: COLLINP and COLLINN. These two signals are inputs to the core and come from a two-input differential mixed signal receiver

3.4.2 9-Wire AUI Interface

The nine-wire E-10 AUI interface is shown in Figure 3.10.

Figure 3.10 AUI 9-Wire Interface



3.4.2.1 9-Wire AUI Transmit Interface

With the nine-wire AUI interface, the E-10 core outputs two transmit signals, the true and complemented (differential) Manchester-encoded data signals DATAP and DATAN. The transmit circuitry sends these differential signals to the AUI cable through a transformer.

A transformer isolates the transmit pins from the transceiver cable, achieving system isolation.

3.4.2.2 9-Wire AUI Receive Interface

The nine-wire twisted pair receive interface provides a receiver for data and a receiver for collision control.

The data receiver has three signals at the E-10 core interface: DATATP, DATATN, and DATAI.

The data receiver converts the two differential analog data signals from the network to DATATP, DATATN, and DATAI. The three signals switch in such a way that the E-10 core can properly perform data detection, reverse polarity detection, and smart squelch.

The collision receiver has two signals at the E-10 core interface: COLLINP and COLLINN.

3.4.3 Signal Quality Error (SQE) Function (Heartbeat)

The Signal Quality Error (SQE) diagnostic feature has been specified for the MAU in the IEEE 802.3 standard. The feature is supported by the E-10 core when it operates in the AUI mode with an external MAU (see Figure 3.8).

The SQE test is a self-test feature supported in the MAU that is invoked after the end of each transmission by the DTE, where the E-10 core is located. When enabled, the SQE test consists of a 10-MHz burst sent from the MAU over the collision pair and starts six to 16 bit times (0.6 µs to 1.6 µs) after the last transition of the transmitted signal and lasts for a duration of five to 15 bit times. This test is an indication to the E-10 core that the MAU has recognized the end of the transmission and the MAU collision circuitry is intact and operational.

Chapter 4
Functional Timing

This chapter describes the Media Access Controller (MAC) and E-10 clock timing and contains the following sections:

- Section 4.1, “MAC Transmission and Reception Timing”
- Section 4.2, “E-10 Clock Timing”
- Section 4.3, “Multiple Core Clocking”

4.1 MAC Transmission and Reception Timing

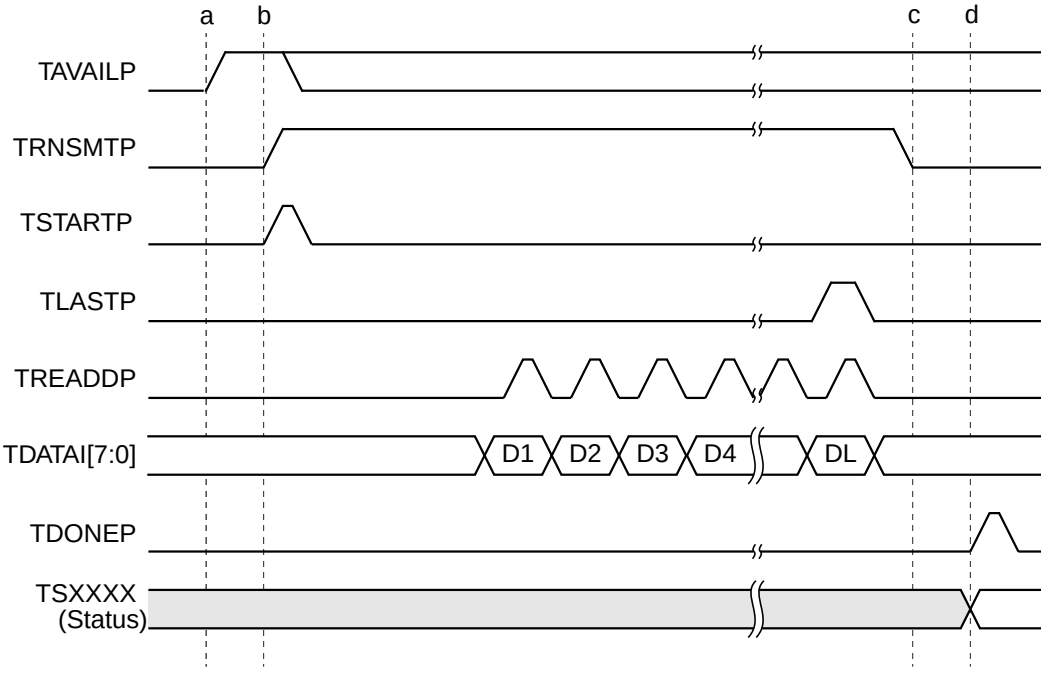
This section explains MAC transmission and reception timing, and Manchester encoder-decoder (ENDEC) timing.

4.1.1 MAC Transmission Timing

Figure 4.1 shows the MAC transmission timing. The transmission process starts with external logic asserting TAVAILP to indicate that a complete frame is ready to be transmitted (a). The transmitter starts transmitting (the E-10 core asserts TRNSMTP HIGH) as soon as it is finished deferring, and then waits an additional 9.6 µs for the interframe gap (b). At this time, the E-10 core pulses the TSTARTP pin to indicate that transmit data is needed within 6.4 µs on the transmit data bus (TDATAI[7:0]). At this point, the E-10 core pulses the TREADDP pin every 800 ns for every byte of transmit data read from the transmit data bus. There are gaps in the stream of TREADDP pulses when the transmitter does an automatic insertion of the source address, pad field, or frame check sequence. External logic asserts the TLASTP signal, accompanied by the last byte of transmit data.

The E-10 core stops transmission after the optional autoinsertion of the pad and FCS fields and after all data has been transmitted to the network (c). As soon as all transmit status bits are valid, the E-10 core pulses the TDONEP pin to indicate that transmission of the frame is complete (d). The TAVAILP signal is not sampled again until a minimum of 800 ns after the TDONEP pulse, to give external logic time to do buffer housekeeping, and to determine whether or not another buffer is ready to be transmitted.

Figure 4.1 Successful Transmission

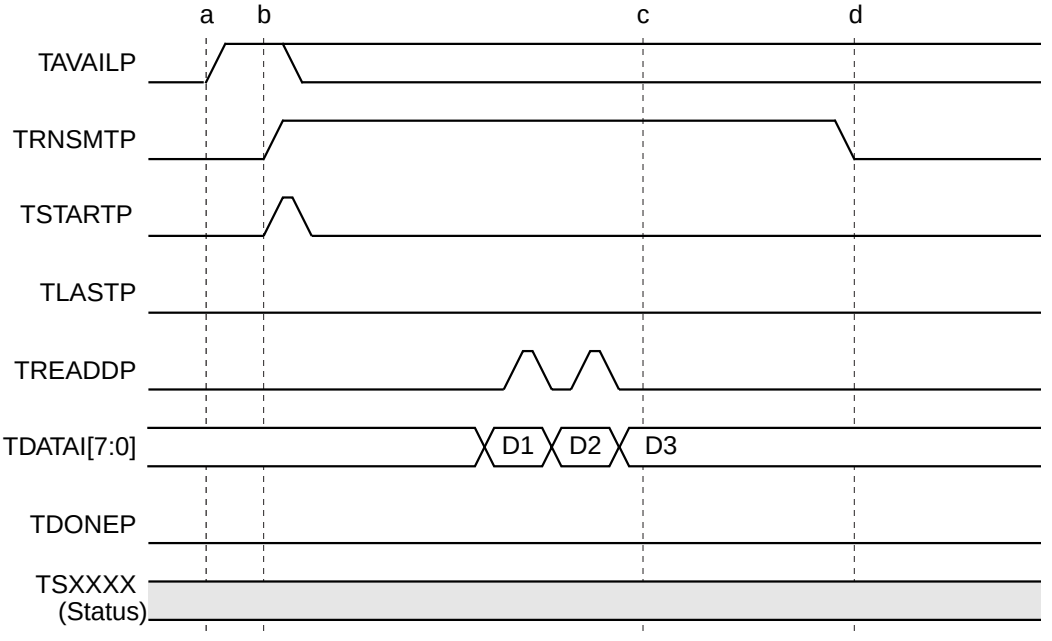


Note: TSXXXX consists of the following Transmit Status signals:
TSECOLP, TSIDEFP, TSLCOLP, TSMCOLP, TSNCLBP, TSOCOLP, and TSSQEEP

4.1.1.1 Transmission Aborted by a Collision

A collision can abort a transmission. The timing for this condition is shown in Figure 4.2. The transmission starts normally as shown in (a) and (b). The transmitter transmits the complete preamble and start of frame delimiter while it latches any collision. As soon as the transmitter detects the presence of a collision after the SFD is transmitted (c), it stops requesting additional transmit data bytes, transmits four bytes of alternating ones and zeros and then terminates the transmission without asserting a TDONEP pulse (d). After the transmission is terminated, the transmitter starts the backoff algorithm, and then, after deferring, starts a frame retransmission.

Figure 4.2 Transmission Aborted by a Collision



Note: TSXXXX consists of the following Transmit Status signals:
TSECOLP, TSIDEFP, TSLCOLP, TSMCOLP, TSNCLBP, TSOCOLP, and TSSQEEP

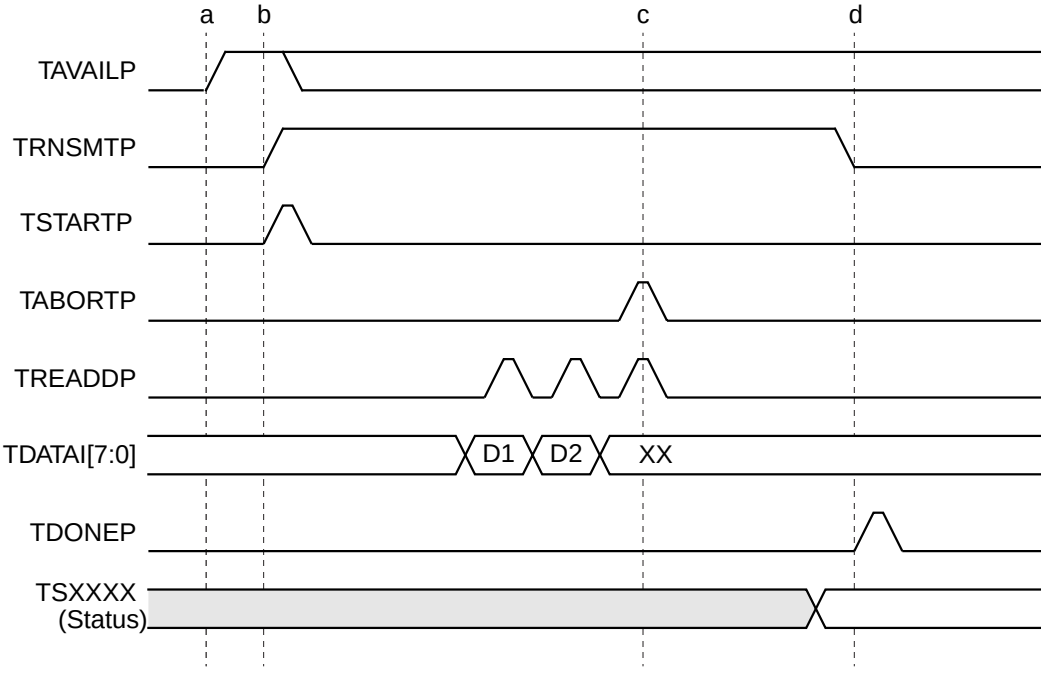
4.1.1.2 Retransmission

The host asserts AVAILP to the E-10 core when the host has one or more frames available to be transmitted. A transmission that was aborted by a collision initiates a retransmission. After the backoff algorithm and deferral, the E-10 core starts the retransmission. The E-10 core does not sample the TAVAILP signal during a retransmission, but the rest of the timing is identical to any normal transmission. The host asserts the TLASTP signal to indicate to the core that the TDATA[7:0] signals from the host contain the last byte of data in the frame.

4.1.1.3 Transmission Aborted by TABORTP

When external logic decides it wants to terminate a transmission (for example, after a transmission data underrun), it can assert the signal TABORTP instead of sending a new transmit data byte. The timing for this condition is shown in Figure 4.3. The transmission starts normally as shown in (a) and (b). The transmitter terminates the transmission when it detects the assertion of TABORTP (c) after transmitting four bytes of alternating ones and zeros (d). This operation is identical to a transmission aborted by a collision.

Figure 4.3 Transmission Aborted by TABORTP



Note: TSXXXX consists of the following Transmit Status signals:
TSECOLP, TSIDEFP, TSLCOLP, TSMCOLP, TSNCLBP, TSOCOLP, and TSSQEEP

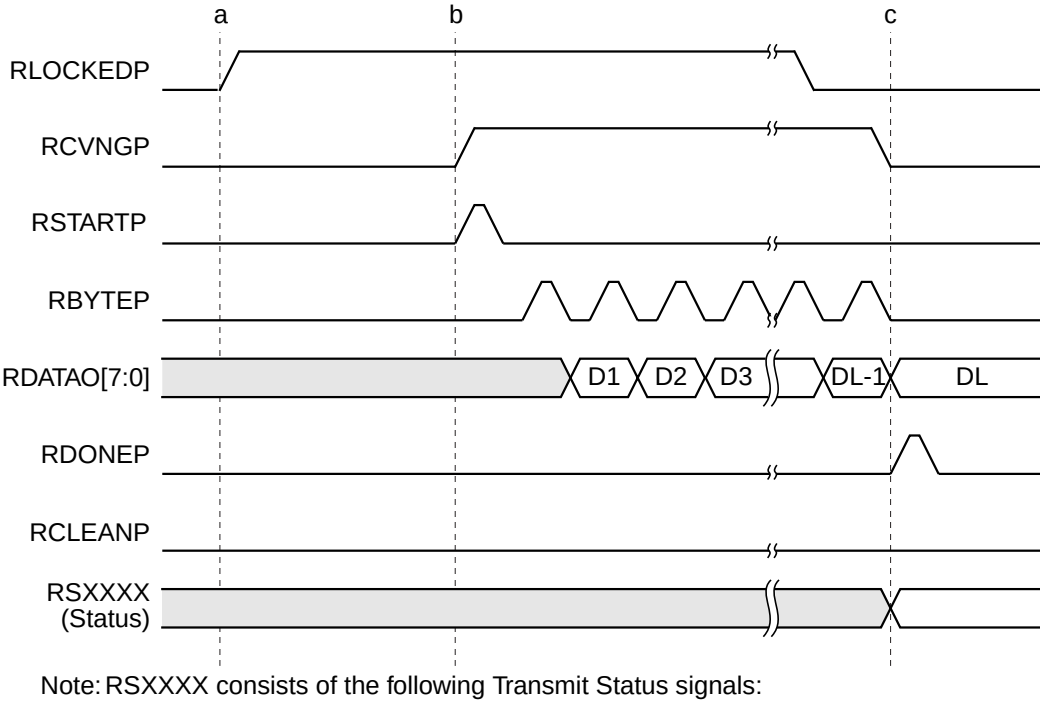
4.1.1.4 Transmission Terminated With TFINISHP

When the signal TFINISHP is asserted at the end of a transmission, the MAC terminates the transmission with the assertion of TDONEP, independent of the detection of a collision. The frame is *not* retried, even if it normally would have been. Assertion of TFINISHP can prevent a frame from being retried independent of the normal default conditions. For example, the transmit status pin TSLCOLP can be connected to TFINISHP to prevent frames with a late collision from being retried.

4.1.2 MAC Reception Timing

MAC reception timing is shown in Figure 4.4. When the E-10 core receives a frame from the network, the data recovery digital PLL locks onto the transitions of the preamble. Phase-lock occurs within six to eight bit times (three bits for intelligent squelch operation and the remainder for the PLL to operate). When phase-lock occurs, the E-10 core asserts the RLOCKEDP pin (a). The receiver then goes into receiving mode and asserts RCVNGP (b) when the start of frame delimiter is detected (b). The beginning of a reception is marked with an RSTARTP pulse, which prepares the off-core logic for the arrival of new data. The off-core logic has 800 ns to make a new receive buffer available before new data bytes start arriving (indicated by RBYTEP pulses). Reception is stopped when the end of frame delimiter is detected and the receive status pins (RSxxxx) are valid. Section 2.4, “Receiver Status Signals,” lists the individual receive status pins. The RDONEP pulse indicates to external logic that the received frame is complete (c).

Figure 4.4 Successful Reception

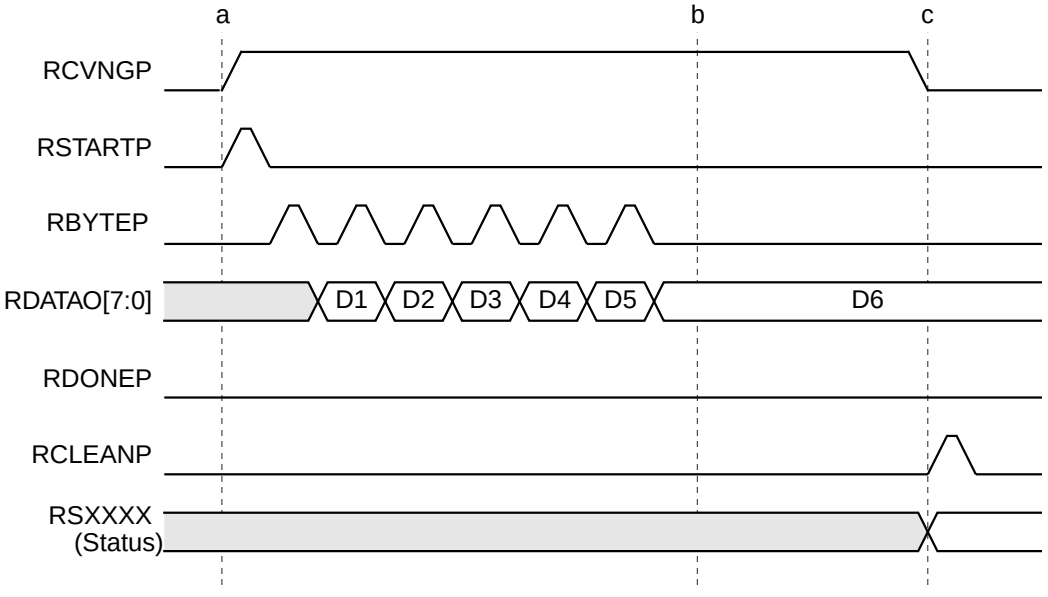


Note: RSXXXX consists of the following Transmit Status signals:
RSDRBLEP, RSFCSEP, RSMATIP, RSMATMP and RSPLLEP

4.1.2.1 Reception With No Individual Address Filter Match

Figure 4.5 shows the timing of the address filters during reception. Packet reception begins at (a). When all address filters do not match during a reception of a frame from the network (b), the receiver stops transferring received data to the host. When reception stops, the receiver terminates with the assertion of the RCLEANP pulse (c).

Figure 4.5 Reception With No Individual Address Filter Match

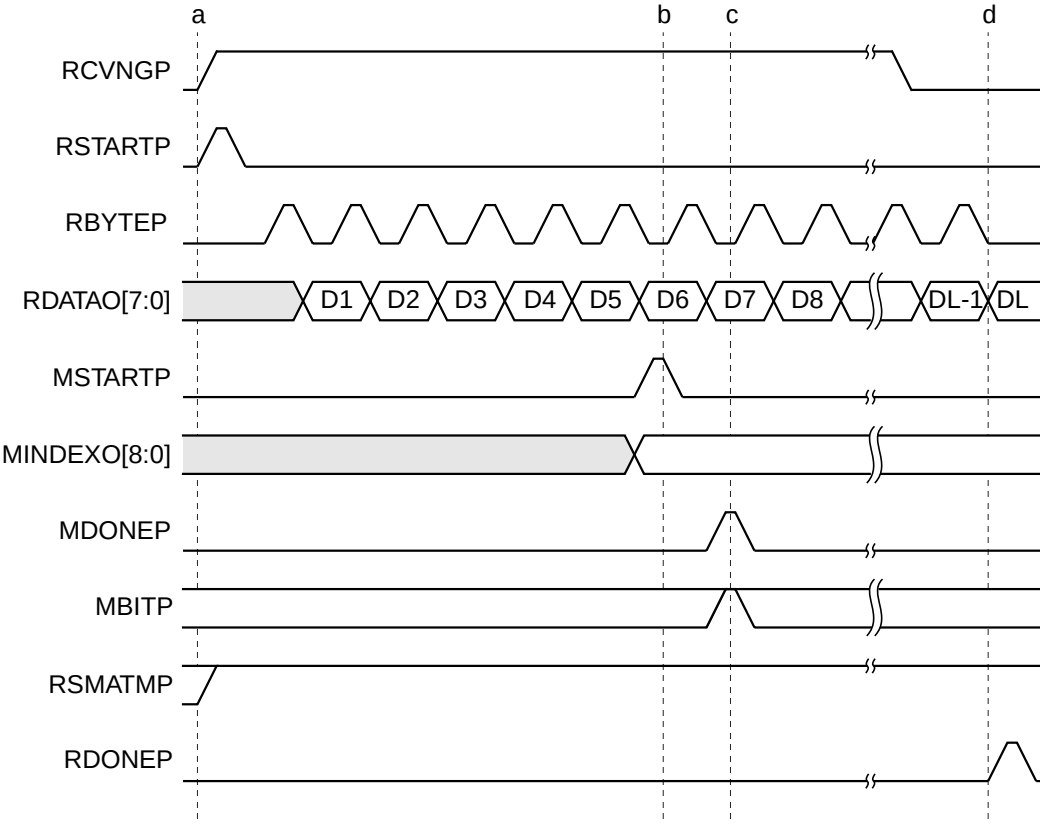


Note: RSXXXX consists of the following Transmit Status signals:
RSDRBLEP, RSFCSEP, RSMATIP, RSMATMP and RSPLLEP

4.1.2.2 Reception With External Multicast Filter Match

Figure 4.6 shows the external multicast filter match timing. Packet reception begins at (a). When multicast is enabled, and a multicast frame is received from the network, the receive engine calculates a nine-bit hash function (MINDEXO[8:0]) from the 48-bit multicast destination address. The receiver indicates to external logic to either accept or reject the message with the MSTARTP pulse (b). External logic has until the end of a minimum length frame (51.2 μs from the SFD) to make a decision. When the external logic decides to accept the frame, it asserts the MBITP signal and pulses the MDONEP input (c). The receiver now permanently asserts the RSMATMP signal and accepts the rest of the frame, and when the receiver is finished, it asserts the RDONEP pulse (d).

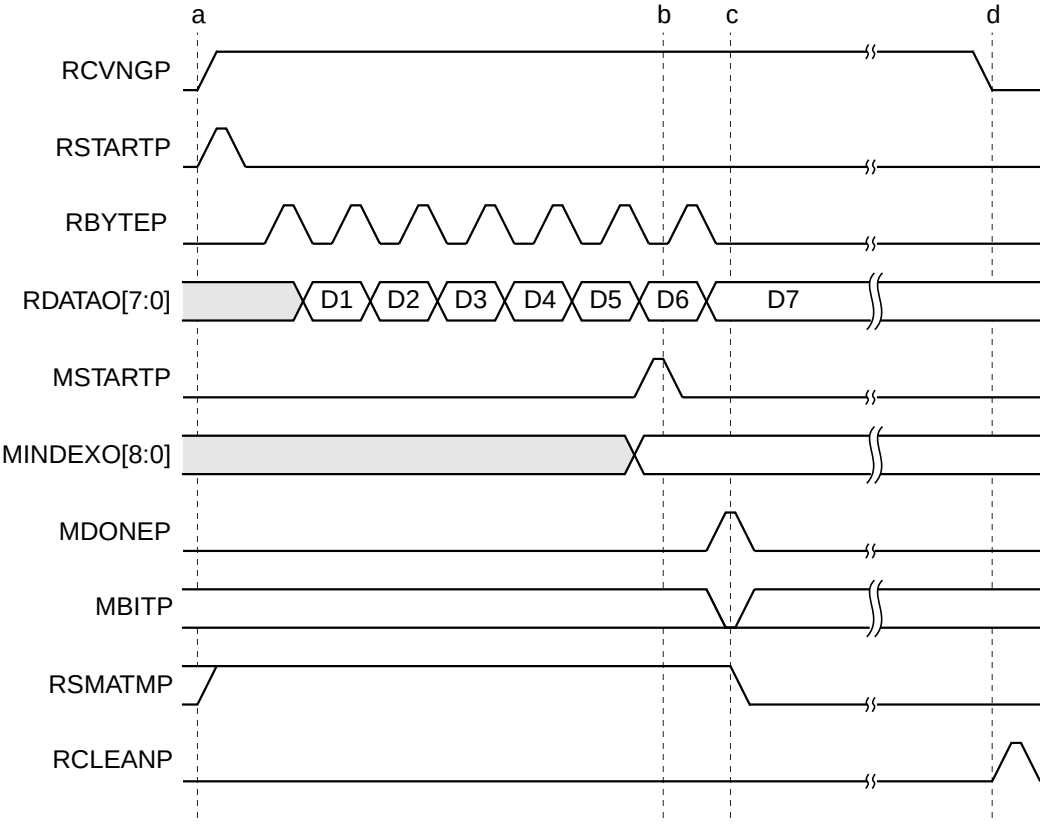
Figure 4.6 Reception With External Multicast Filter Match



4.1.2.3 Reception With No External Multicast Filter Match

Figure 4.7 shows the no external multicast filter match timing. Packet reception begins at (a). A pulse on MSTARTP (b) indicates to the external logic that a new nine-bit hash function has been computed from the destination address. When the external logic decides to reject the frame, it deasserts the MBITP signal and pulses the MDONEP input to indicate to the receiver that it has made the decision (c). The receiver now deasserts the RSMATMP signal and rejects the rest of the frame. When the receiver is finished, the E-10 core pulses the RCLEANP pin (d).

Figure 4.7 Reception With No External Multicast Filter Match



4.1.3 ENDEC Timing

Examples of ENDEC timing are shown in Figure 4.8 and Figure 4.9. The bit times shown in the diagrams are 100 ns in duration.

Figure 4.8 Twisted Pair Serial Output Data

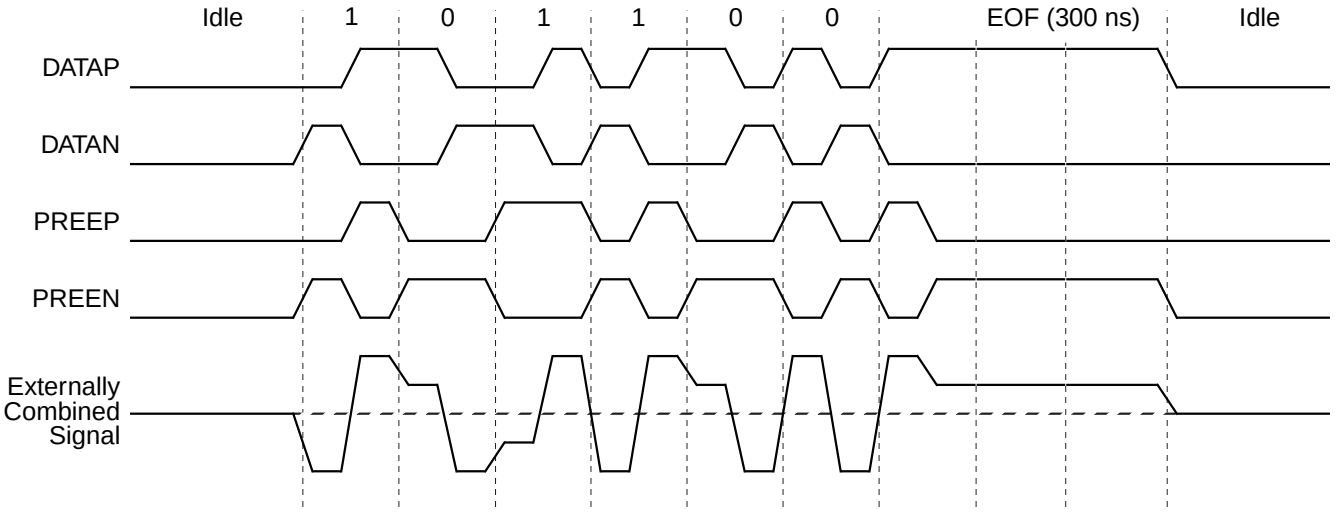
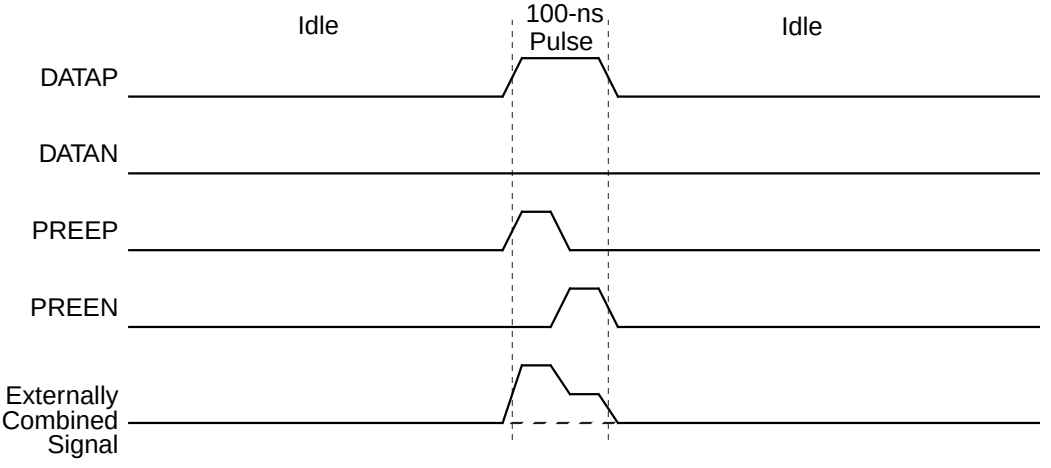


Figure 4.9 Twisted Pair Link Integrity Pulses



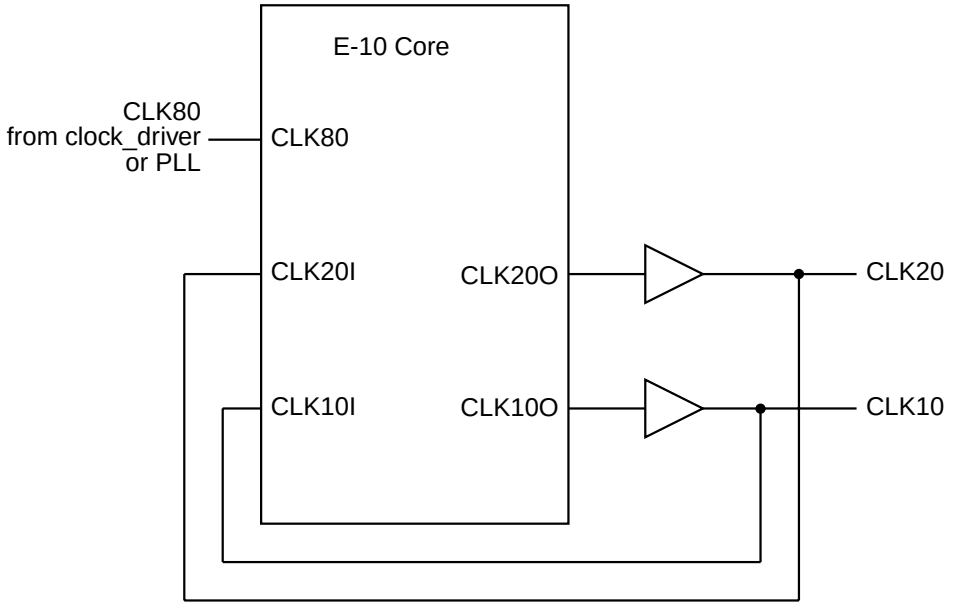
4.2 E-10 Clock Timing

This section explains the E-10 clock, receiver, and transmitter timing.

The input clock to the E-10 core is 80 MHz. The duty cycle should have a nominal duty cycle of 50/50, with a worst-case duty cycle of 60/40 because both the LOW-to HIGH and the HIGH-to-LOW transitions of this signal are used in the digital phase-locked loop that samples the input data. The MAC timing logic divides the 80 MHz down to 20 MHz and 10 MHz. These derived frequencies are available on the E-10 output pins.

Noninverting buffers have to be put outside of the E-10 core. The outputs of these buffers have to be routed back to the E-10 input pins as shown in Figure 4.10. The E-10 core expects all input signals from the host to be synchronous with its own 10-MHz clock rate. This requirement for synchronism dictates that the external logic use the same synchronous 10-MHz clock driver that E-10 uses. If more than one E-10 core resides on the same chip, only the clock drivers from a *single* E-10 core can drive all clock inputs and the external logic.

Figure 4.10 E-10 Clock Buffers



Because the transmit clock is derived from the 80 MHz input clock, the maximum clock error has to comply with the IEEE 802.3 maximum error of ± 0.01% or 100 ppm.

4.3 Multiple Core Clocking

Multiple E-10 cores can be used in an ASIC. This section describes how multiple E-10 core clocking can best be accomplished.

4.3.1 Core Clocks

The E-10 core uses three different clocks:

- 80 MHz. This clock is used as the primary timing input, and is used in several places, as follows:
  - Clocking the data recovery digital PLL
  - Clocking the Ethernet signal squelch circuits
  - Generating the lower frequency clocks (20 and 10 MHz)
- 20 MHz. This clock is used for the Manchester encoding.
- 10 MHz. This main clock drives the MAC, ENDEC, and Transceiver state machines.

The E-10 core does *not* contain any clock drivers. The designer should add two clock buffers (see Figure 4.10) of sufficient strength to drive all E-10 cores in parallel. The 10- and 20-MHz clock buffers should be driven by the 10- and 20-MHz output pins of *only one* of the E-10 cores.

4.3.2 80-MHz Clock

The 80-MHz clock can be generated by a Phase-Locked Loop (PLL), which consists of a phase comparator, external loop filter, and voltage-controlled oscillator (see Figure 4.11). The reference input can be a 10- or 20-MHz clock or can be driven by an on chip 10- or 20-MHz crystal oscillator. Generating the 80-MHz clock on the chip reduces the higher frequencies on the printed circuit board and should allow for easier passing of the FCC emissions test.

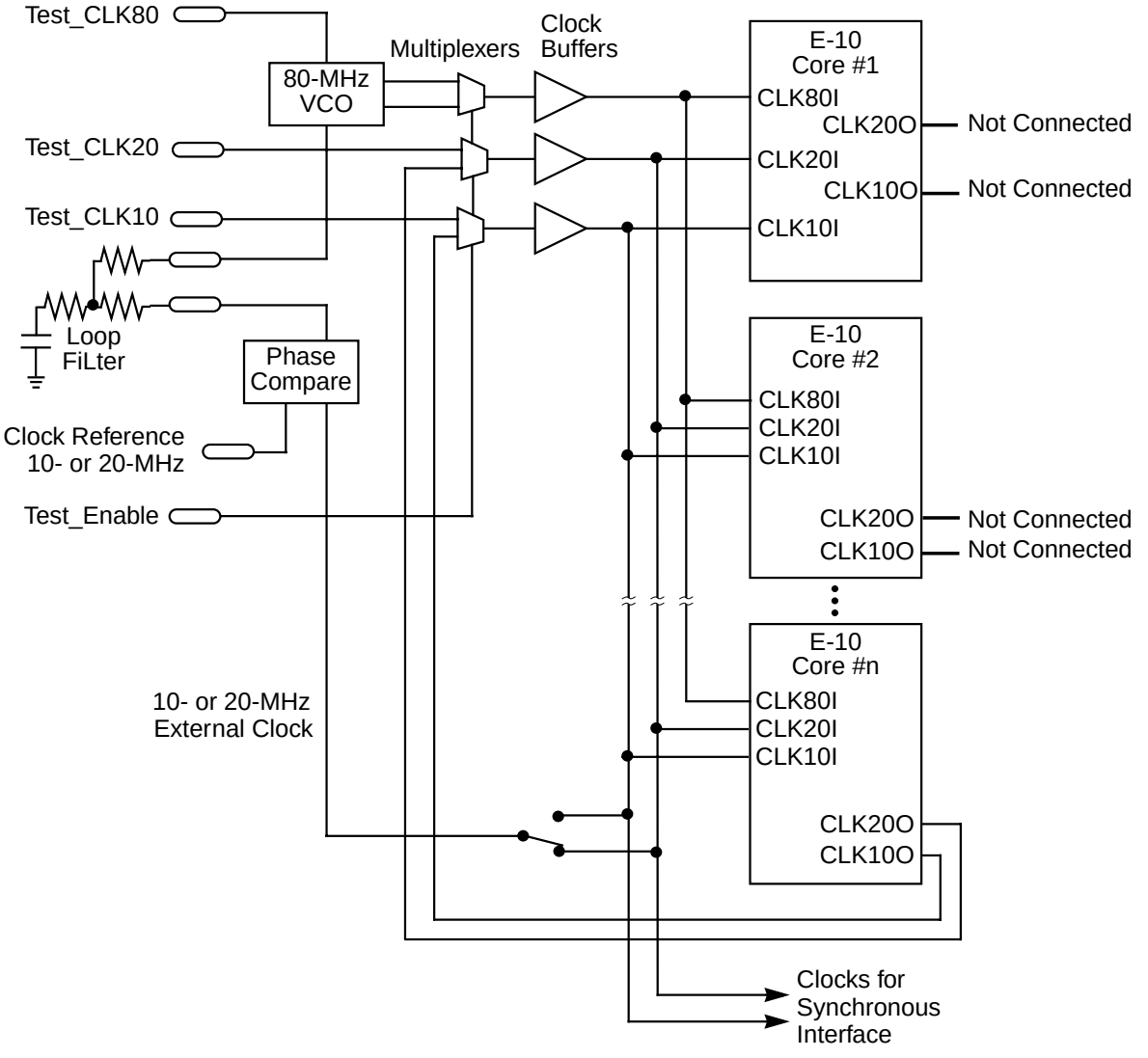
4.3.3 10- and 20-MHz Clocks

The 10- and 20-MHz inputs should be synchronized to the 80-MHz input clock. The E-10 core generates 20- and 10-MHz clocks and makes these three signals available on core output pins. The 20- and 10-MHz output pins of only one of the E-10 cores should be used to drive all E-10 cores on the chip. Most of the input signals of the E-10 core are synchronous and should be clocked with the same 10-MHz clock as is used by the cores. The 10- and 20-MHz clock buffers should be strong enough to allow for a delay of no more than 9 ns from CLK80 input to the CLK10 and CLK20 inputs.

4.3.4 E-10 Testing

To allow testing of the E-10 cores, the three clocks used by the cores should be multiplexed with three signals coming directly from the input pins. The E-10 test vectors need direct control over the three test inputs plus the multiplexer control input. The clock multiplexing scheme is shown in Figure 4.11.

Figure 4.11 Multiple-Core Clock Multiplexing



Chapter 5
Specifications

This chapter provides specifications for the E-10 core, including the AC timing as well as input and output loading, driver type, and power consumption.

This chapter has three sections:

- Section 5.1, “Derivation of AC Timing and Loading”
- Section 5.2, “AC Timing”
- Section 5.3, “Pin Summary”

5.1 Derivation of AC Timing and Loading

Every customer that buys a core from LSI Logic for incorporation into an ASIC also receives delay predictor software, which gives you an input loading report so you can plan for buffer strengths that drive core inputs.

When you integrate the core into the rest of your logic and run other simulation software, you get a ramptime violation report that indicates if a core output is too heavily loaded. You can then adjust buffering, wire length, and other parameters to eliminate the violation.

As a result, there are no specific numbers in this chapter for AC timing and loading, because the numbers depend on the technology you use and the design layout.

5.2 AC Timing

This section gives a list of the signals that must operate properly with respect to the CLK10I and CLK20O signals. The relationship between the signals is depicted in Figure 5.1 and Figure 5.2.

The numbers in Figure 5.1 and Figure 5.2 refer to the AC timing parameters listed in the first column of Table 5.1. The core has been verified under worst-case process voltage and ambient temperature.

Table 5.1 E-10 Core AC Timing Parameters

Parameter	Description
1.	TFINISHP setup to CLK10I
2.	TFINISHP hold from CLK10I
3.	TAVAILP setup to CLK10I
4.	TAVAILP hold from CLK10I
5.	TDATAI[7:0] setup to CLK10I
6.	TDATAI[7:0] hold from CLK10I
7.	TABORTP setup to CLK10I
8.	TABORTP hold from CLK10I
9.	TLASTP setup to CLK10I
10.	TLASTP hold from CLK10I
11.	RENABP setup to CLK10I
12.	RENABP hold from CLK10I
13.	MDONEP setup to CLK10I
14.	MDONEP hold from CLK10I
15.	MBITP setup to CLK10I
16.	MBITP hold from CLK10I
17.	TSTARTP delay from CLK10I
18.	TDONEP delay from CLK10I
19.	TREADDP delay from CLK10I
20.	TRNSMTP delay from CLK10I
21.	RSTARTP delay from CLK10I

Table 5.1 (Cont.) E-10 Core AC Timing Parameters

Parameter	Description
22.	RDONEP delay from CLK10I
23.	RCLEANP delay from CLK10I
24.	RBYTEP delay from CLK10I
25.	RDATAO[7:0] delay from CLK10I
26.	RCVNGP delay from CLK10I
27.	RLOCKEDP delay from CLK10I
28.	DATAP delay from CLK20O
29.	DATAN delay from CLK20O
30.	PREEP delay from CLK20O
31.	PREEN delay from CLK20O
32.	LPASSP delay from CLK10I
33.	LPBADP delay from CLK10I
34.	COLLOUTP delay from CLK10I
35.	MSTARTP delay from CLK10I
36.	MINDEXO[8:0] delay from CLK10I
37.	RESETN pulse width
38.	RESETN LOW before CLK10I rise
39.	RESETN HIGH before CLK10I rise

Figure 5.1 E-10 Core Setup and Hold Timing Diagram

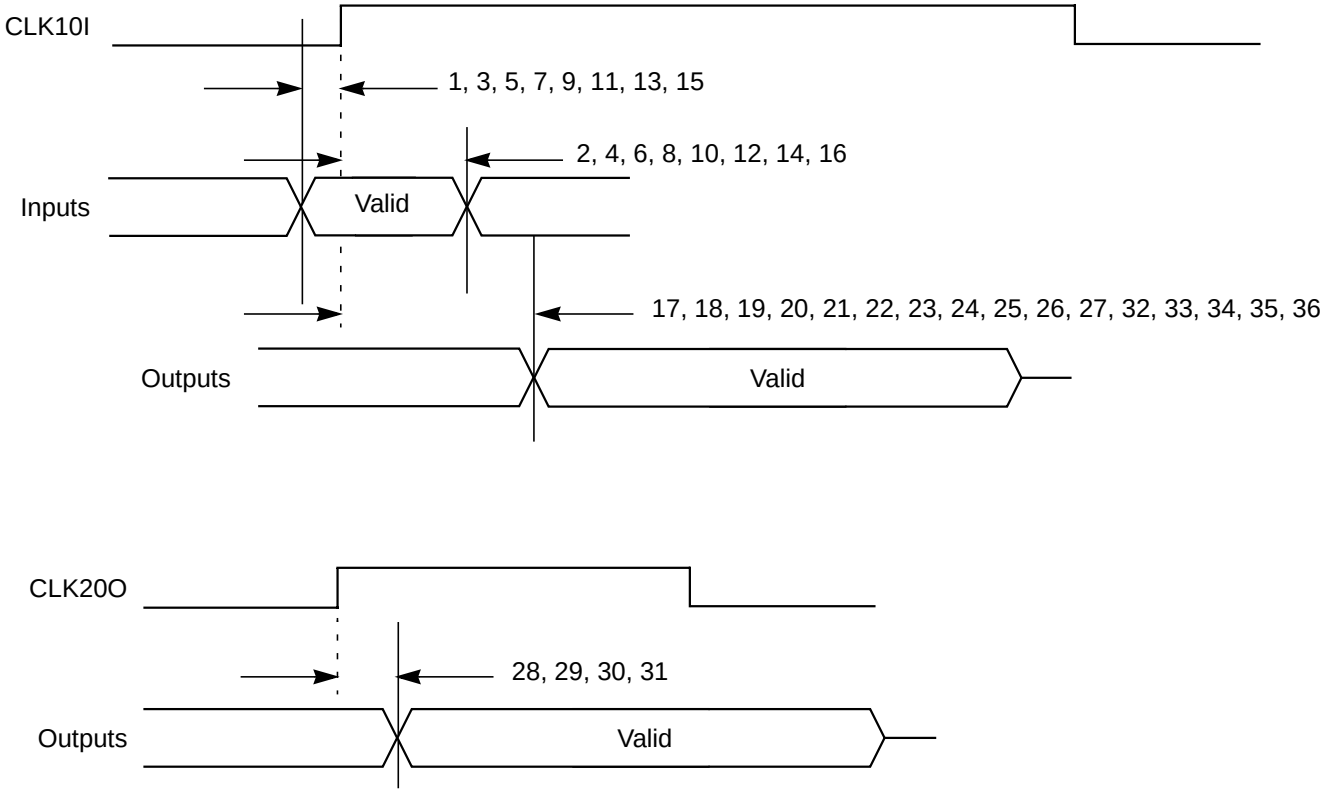
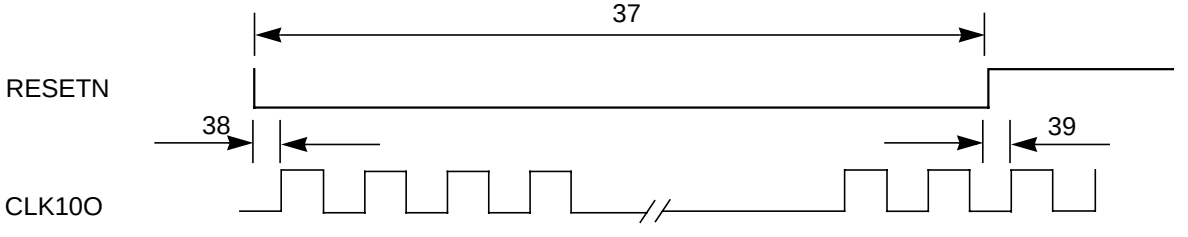


Figure 5.2 E-10 Core Reset Timing Diagram



5.3 Pin Summary

Table 5.2 summarizes the E-10 core input and output signals. The table provides the signal names and types for both outputs and inputs.

Table 5.2 E-10 Pin Summary

Mnemonic	Description	Type	Active
CLK80I	80-MHz Clock	Input	–
CLK10I	10-MHz Clock	Input	–
CLK20I	20-MHz Clock	Input	–
CLK10O	10-MHz Clock	Output	–
CLK20O	20-MHz Clock	Output	–
COLLINN	Negative Collision Threshold	Input	–
COLLINP	Positive Collision Threshold	Input	–
COLLOUTP	Transmit Collision	Output	HIGH
DATAI	Data Input from Network	Input	–
DATAP	Positive Data	Output	–
DATAN	Negative Data	Output	–
DATATP	Positive Data Threshold	Input	–
DATATN	Negative Data Threshold	Input	–
DRIVEENN	Drive Enable	Output	LOW
DUPLEXP	Full Duplex Select	Input	HIGH
FASTESTN	Fast Test	Input	LOW
LCORPP	Link Correct Polarity	Input	HIGH
LFORCEP	Force Link	Input	HIGH
LOOPBKP	Loopback Enable	Input	HIGH
LPASSP	Link Pass	Output	HIGH
LPBADP	Link Polarity Bad	Output	HIGH
MBITP	Multicast Hash Table Bit	Input	HIGH
MDONEP	Multicast Filter Done	Input	HIGH

(Sheet 1 of 3)

Table 5.2 (Cont.) E-10 Pin Summary

Mnemonic	Description	Type	Active
MINDEXO[8:0]	Multicast Hash Function	Output	–
MSTARTP	Multicast Filter Start	Output	HIGH
NOAD-DRI[47:0]	Node Address	Input	–
PREEP	Positive Data Pre-Emphasis	Output	–
PREEN	Negative Data Pre-Emphasis	Output	–
RBYTEP	Received Byte	Output	HIGH
RCLEANP	Receiver Cleanup	Output	HIGH
RCVNGP	Receiving	Output	HIGH
RDATAO[7:0]	Received Data	Output	–
RDONEP	Receiver Done	Output	HIGH
RENABP	Receive Enable	Input	HIGH
RESETN	Reset	Input	LOW
RLOCKEDP	Receiver Locked Output	Output	HIGH
RMCENP	Receive Multicast Enable	Input	HIGH
RPMENP	Receive Promiscuous Mode Enable	Input	HIGH
RSDRBLEP	Receive Status Dribble Bits	Output	HIGH
RSFCSEP	Receive Status Frame Check Sequence Error	Output	HIGH
RSMATIP	Receive Status Match Individual Address	Output	HIGH
RSMATMP	Receive Status Match Multicast Address	Output	HIGH
RSPLLEP	Receive Status Phase-Locked Loop Error	Output	HIGH
RSTARTP	Receiver Start	Output	HIGH
RSNOOPENP	Receiver Lookback Enable	Input	HIGH
SELIO	4-Wire/8-Wire Mixed Signal Cell Select	Input	–

(Sheet 2 of 3)

Table 5.2 (Cont.) E-10 Pin Summary

Mnemonic	Description	Type	Active
TABORTP	Transmit Abort	Input	HIGH
TAVAILP	Transmitter Packet Available	Input	HIGH
TCTRI[3:0]	Transmit Control	Input	–
TDATAI[7:0]	Transmit Data	Input	–
TDONEP	Transmit Done	Output	HIGH
TESTSE	Scan Enable	Input	HIGH
TESTSI	Scan Input	Input	–
TESTSO	Scan Output	Output	–
TEST1N	Fast Test	Input	LOW
TEST2N	Reset B	Input	LOW
TFINISHP	Transmit Finish	Input	HIGH
TLASTP	Transmit Last Byte	Input	HIGH
TMODE	Test Mode	Input	HIGH
TP/AUI	Twisted-Pair/AUI Select	Input	–
TREADDP	Transmitter Read Control	Output	HIGH
TRNSMTP	Transmitting	Output	HIGH
TSECOLP	Transmit Status Excessive Collisions	Output	HIGH
TSIDEFP	Transmit Status Initially Deferred	Output	HIGH
TSLCOLP	Transmit Status Late Collision	Output	HIGH
TSMCOLP	Transmit Status Multiple Collision	Output	HIGH
TSNCLBP	Transmit Status No Carrier Loopback	Output	HIGH
TSOCOLP	Transmit Status One Collision	Output	HIGH
TSSQEEP	Transmit Status SQE Error	Output	HIGH
TSTARTP	Transmit Start	Output	HIGH

(Sheet 3 of 3)

Appendix A
Glossary

Address Filtering (Individual, Multicast, Promiscuous) – Address filtering is the process the E-10 core performs to match a destination address within a received frame with an address derived at the receiving station. Three common types of address filtering are:

- Individual—the first bit of an individual address is a zero. The incoming destination address is compared with the data from the individual address pins. When all 48 bits match and the receiver is enabled, the address filter passes.
- Multicast—the first bit of an multicast address is a one. When the destination address bits that are received in the frame contain a multicast address, the E-10 core uses its built-in FCS generator to compute a nine-bit polynomial (the nine MSBs of the 32-bit FCS generator) from the incoming address. The value of this polynomial can be used as an index into an external multicast filter hash table. External logic can decide to either accept or reject the incoming frame. The external logic enables the multicast address filter.
- Promiscuous—when the external logic asserts the individual address promiscuous mode enable pin (RPMEN) HIGH and the destination address is an individual address, the address filter always passes, and the incoming frame is received.

Attachment Unit Interface (AUI) – The AUI is the interface between the Medium Attachment Unit (MAU) and the data terminal equipment (DTE) device or repeater. A typical AUI interface consists of a 15-pin “D” connector.

Backoff – In IEEE 802.3 networks, backoff occurs when two or more nodes attempt a transmission and collide. The function of stopping transmission, and waiting a specified random time before retrying the transmission is considered backoff. In IEEE 802.3 networks a “truncated binary exponential backoff” algorithm is employed.

Coaxial Cable – Coaxial cable is a transmission medium with a central copper-wire conductor surrounded by concentric layers of plastic/polyvinyl chloride, aluminum or aluminized mylar and a copper tube that acts as an insulator (ground) and source of shielding from electromagnetic and radio frequency interference (CMI/RFI). Two types of coaxial cable—known as “thick” and “thin” for their respective diameters—are used in Ethernet data transmissions.

Collision – When an Ethernet station is operating in the AUI mode, it can sense a change in the energy level of the communication channel and interpret the phenomenon as a collision. A collision is caused by two stations attempting to transmit at the same time.

Collision Detection – Collision detection is the ability of a transmitting node on an Ethernet LAN to sense a change in the energy level of the channel and to interpret the phenomenon as a collision

CRC (Cyclic Redundancy Check) – CRC is a basic error-checking mechanism for link-level data transmission; a characteristic link-level feature of (typically) bit-oriented data communications protocols. The data integrity of a received frame or packet is checked via a polynomial algorithm based on the content of the frame and then matched with the result that is performed by the sender and included in a (most often, 16-bit) field appended to the frame.

CSMA/CD (Carrier Sense Multiple Access with Collision Detection) – CSMA/CD is a LAN protocol access method where the nodes are attached to a cable. When a node transmits data onto the network and raises the carrier, the remaining nodes detect the carrier (Carrier Sense) and “listen” for the information to detect if it is intended for them. The nodes have network access (Multiple Access) and can send if no other transmission is taking place. If two nodes attempt to send simultaneously, a collision takes place (Collision Detection) and both nodes must retry at random intervals.

Data Recovery – The data sent over an Ethernet LAN is Manchester-encoded and must be recovered by the receiving station. In the E-10 core, a digital phase-locked loop recovers the data through a sampling process and has the necessary elasticity to allow for the bit drift that occurs over lengthy frame sizes.

Dribble Bit – A dribble bit is a bit that is “extra” and occurs when, at the end of a frame, less than a complete byte is received. It is possible to have from one to seven dribble bits at the end of a frame if a complete byte is not received.

Dropout Error – A dropout error occurs when the carrier on a transmission channel stops due to a broken or missing cable.

Elasticity – Elasticity is a measure of the tolerance of the phase-locked loop to the cumulative bit shift due to small differences in the free running clock oscillator frequencies of the transmitting source and receiving destination.

End-of-Frame Delimiter – An end-of-frame delimiter is a series of three bits of ones at the end of a frame that are not Manchester-encoded; that is, they are non-return-to-zero bits that do not contain a transition in the middle of the bit time. The purpose of the end-of-frame delimiter is to cause the PLL at the receiving station to lose lock so the host can be notified that the frame has ended.

When a receiving node detects a bit that is not Manchester-encoded, it considers the previous four bytes to be the FCS.

ENDEC – ENDEC is short for Encoder/Decoder and is a functional block within network adapters that performs two basic functions. First, this function encodes the data from the controller to be transmitted over the network. Second, it decodes the data on the network to a form suitable for the network controller chip. In the case of Ethernet, the ENDEC converts NRZ controller data to Manchester data (and back again).

Ethernet Local Area Network (LAN) – An Ethernet LAN is a branching broadcast communications system for carrying digital data packets among locally distributed computing stations. Ethernet is a 10 Mbit/s baseband, Local Area Network that has evolved into the IEEE 802.3 specification and is defined by a data-link protocol that specifies how data is placed on and retrieved from a common transmission medium. Ethernet is used as the underlying transport vehicle by several upper level protocols, including TCP/IP and Xerox Network System (XNS). See IEEE 802.3.

Frame – An Ethernet frame contains the following eight fields:

- Preamble
- Start-of-Frame Delimiter
- Destination Address
- Source Address
- Length
- Data
- Pad (if necessary)
- Frame Check Sequence

Frame Check Sequence (FCS) – The Ethernet transmit and receive algorithm uses the standard IEEE 802.3 four-byte frame check sequence (FCS) field to ensure data integrity. During data transmission, the E-10 core uses a 32-bit linear feedback shift register (LFSR) to compute the value that will be sent in the FCS field. The FCS value is a function of the content of the source address, destination address, length, data, and pad fields. On data reception, the E-10 core preloads the LFSR with all ones and updates this value with each byte received, including the received FCS. If the final value in the LFSR does not match a predetermined value after all bytes including the FCS are received, the E-10 core flags an FCS error.

Heartbeat – In IEEE 802.3 networks, a heartbeat is a short burst of collision signal that is transmitted from the MAU to the DTE after every packet. See Signal Quality Error (SQE) Test.

Hub – The E-10 core operating in 10BASE-T mode uses a hub to concentrate connections to multiple terminals. Hubs come in various sizes, with 4-port, 8-port, and 12-port being the most common. The number of ports indicates the number of terminals that can be connected to the hub. Most hubs have built-in transceivers and network management features. Hubs are mainly used in star topology LANs. The E-10 core is specifically designed for multiple-core integration, especially for “hub-on-a-chip” implementations.

IEEE 802.3 – IEEE 802.3 is a standard set by the IEEE for CSMA/CD network protocol, which is a Physical Layer definition including specifications for cabling in addition to transmitting data and controlling cable access. See Ethernet LAN.

Jam – In IEEE 802.3 networks, when a collision occurs the colliding nodes ensure that the collision is seen by the entire network by continuing to transmit for a minimum time during a collision. This occurrence is known as jamming.

Jitter – Jitter is the slight movement of a transmission signal in time or phase that can introduce errors and loss of synchronization in high-speed synchronous communications.

LAN (Local Area Network) – A LAN is a communications system linking computers together to form a network whose dimensions typically are less than five kilometers. Transmissions within a Local Area Network generally are digital, carrying data among stations at rates usually above one megabit per second. A LAN is an assembly of computing resources such as microcomputers (for example, PCs), printers, minicomputers and mainframes linked by a common transmission medium, including coaxial cable or twisted-pair wiring.

Link Failure – In the Twisted-Pair mode, a link failure can be caused by a twisted-pair transceiver failure or by a broken twisted-pair receive cable. A link failure occurs when there are eight consecutive missing link integrity pulses.

Link Integrity Pulses – The E-10 core monitors Link Integrity pulses, which may be sent on a regular basis from any other device on the network when the channel is idle. The purpose of the pulses is to ensure that the channel is functional even in the absence of active data. The Link Integrity pulses should be positive-going pulses spaced approximately 50 milliseconds apart.

Link Polarity Detection/Correction – Link Integrity pulses should be positive-going pulses. If they are not, it is an indication that the wiring is inverted. The E-10 core can optionally, under control of the host, invert the data on the receive pair when it detects that eight consecutive Link Integrity pulses have been received with inverted polarity.

Lock Time – Lock time is the amount of time it takes the receiver phase-locked loop to achieve phase lock with an input signal, which may be either data bits or preamble bits. It takes approximately six to eight bits for the E-10 digital phase-locked loop circuit to achieve lock. Three bits are required for the smart squelch operation and the remaining bits are required for the PLL to operate.

Loopback – When the E-10 core is in loopback mode, the transmitter output is fed back to the receiver input inside the chip. Loopback mode allows testing of the E-10 transmitter and receiver up to but not including the off-core transceivers under program control without the need of an external loopback connector. Loopback is applicable to both the AUI and Twisted-Pair modes.

Another loopback mode is known as “lookback.” When the E-10 core is in lookback mode, all transmitted frames are routed back through the receiver. Operation is similar to that of normal loopback described in the previous paragraph except that the phase-locked loop is bypassed.

MAC (Media Access Control) – The data link sublayer that is responsible for transferring data to and from the physical layer.

Manchester Encoding/Decoding – A Manchester-encoded bit contains a transition (either HIGH-to-LOW or LOW-to-HIGH) in the center of the bit time. Having a transition every bit time allows a phase-locked loop at a receiving station to maintain lock and extract both data and clock from the waveform.

With Manchester encoding, each bit is divided into two complementary halves. A LOW-to-HIGH voltage transition in the middle of the bit period designates a binary one, while a HIGH-to-LOW transition represents a binary zero.

MAU (Media Attachment Unit) – An MAU is the physical and electrical component that provides the means of attaching a terminal to a local area network medium.

Multicast Hash Function – See address filtering (multicast).

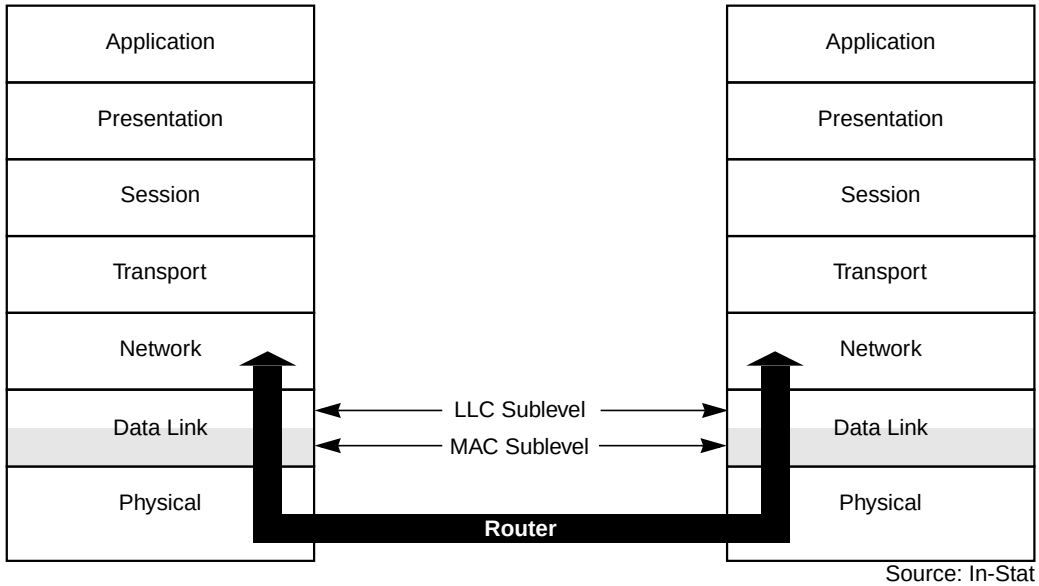
Packet – A packet is data sent in the data field of an Ethernet frame.

Phase-Locked Loop Circuit – A phase-locked loop circuit operates from a local free-running oscillator and is able to achieve and maintain phase and frequency with a signal received from a source that is operating on a different free-running oscillator. The purpose of a phase-locked loop is to provide a clock source that is synchronous with data that is derived from a different clock source. Such a circuit is used commonly in telecommunications systems where data is transmitted without an accompanying clock.

Pre-Emphasis – The purpose of pre-emphasis is to increase the amplitude of the higher frequencies in an output signal. Data pre-emphasis guarantees that an Ethernet system operating Twisted-Pair mode can drive signals properly at 10 Mbit/s on cable up to 100 meters long.

Router – A router is similar to a bridge but has the ability to connect networks at the OSI network level, as shown in Figure A.1.

Figure A.1 Router OSI Interconnect Level



Source: In-Stat

A router is an intelligent device that plans the most efficient route for data to move between networks. Routers generally have the ability to recover lost data packets. The end user must address the router to send data through it. Routers are slower in the transfer of data than bridges and are more expensive to purchase. For this reason, routers are not used to connect LANs (although it is possible) but are more commonly used to connect LANs to wide area networks.

Runt Packet – In IEEE 802.3 networks, a runt packet is a special case of a fragment packet where the length of the packet is less than 512 bit times.

Signal Quality Error (SQE) Test – The Signal Quality Error (SQE) test is a self-test feature supported in the MAU that is invoked after the end of each transmission by the station. When enabled, the SQE test consists of a 10-MHz burst and starts six to sixteen bit times (0.6 µs to 1.6 µs) after the last transition of the transmitted signal and lasts for a duration of five to 15 bit times. This test is an indication to the station that the MAU has recognized the end of the transmission and the MAU collision circuitry is intact and operational.

Slot Time – A slot time is 512 bit times (51.2 µs), and is the time it takes to "fill up" an Ethernet cable with data. In AUI mode, if the receive circuitry of a station does not detect a carrier within one slot time from the initiation of transmission (preamble start), it is an indication of trouble on the cable.

Smart Receive Squelch – An intelligent (smart) receive squelch is implemented on the receiver differential inputs to ensure that impulse noise on the receive inputs is not mistaken for a valid signal. The smart squelch logic uses a combination of amplitude and timing measurements to determine the validity of data.

SQE Burst (Heartbeat) – See Signal Quality Error (SQE) Test.

Start of Frame Delimiter (SFD) – The eight-bit start of frame delimiter field follows the seven-octet preamble at the beginning of a frame and contains the 10101011_2 bit pattern. This pattern allows synchronization of the data received in the rest of the frame.

Tracking Speed – Tracking speed refers to the speed with which a PLL responds to changes in the incoming signal. In the E-10 core, when first attempting to lock on to an oncoming data stream (during the first 4.8 µs), the PLL looks every 16 bits (1.6 µs) to see if a bit transition is occurring in the center of the sampling window. After the first 4.8 µs, the PLL maintains a window of 64 bits (6.4 µs) for finding a transition.

Transceiver – A transceiver is a combined transmitter and receiver and is an essential element of all LAN networks. When an Ethernet LAN operates in the 10BASE-2 or 10BASE-5 mode, the transceivers are generally located in the MAU and connect directly to the coaxial cable. In the Twisted-Pair mode, the transceivers are generally located in the data terminal equipment and connect directly to the twisted-pair cable.

Transmit Carrier Loopback – Transmit Carrier Loopback occurs in the AUI mode. When a station transmits onto the wire, it should detect its own activity on the line within 512 bit times (51.2 µs), which is the maximum amount of time to “fill the wire” under normal circumstances.

Transmit Carrier Loopback Error – Transmit Carrier Loopback Error occurs when a station does not detect its own activity on the line within 512 bit times (51.2 µs).

Transmit Carrier Dropout Error – A transmit carrier dropout error occurs when the carrier on a transmission channel stops due to a broken or missing cable, or bad transceivers.

Twisted-Pair Transmission System – In 10BASE-T terminology, this term refers to the twisted-pair wire link and its two attached MAUs.

Twisted-Pair Wire – Twisted-pair wire is a cable comprised of two 18 to 24 AWG (American Wire Gauge) solid copper strands twisted around each other. The twisting provides a measure of protection from electromagnetic and radio-frequency interference (EMI/RFI). Two types are available: shielded and unshielded. The former is wrapped inside a metallic sheath that provides protection from EMI/RFI. The latter, also known as telephone wire, is covered with plastic or PVC, which provides no protection from EMI/RFI.

10BASE-2 – 10BASE-2 is the IEEE 802.3 Physical Layer Standard for thin wire Ethernet (sometimes called cheapernet). This standard uses RG58 standard coaxial cable. 10BASE2 stands for: 10 = 10 Mbit/s data rate, BASE = Baseband, 2 = 185 meter segment length.

10BASE-5 – 10BASE-5 is the IEEE 802.3 Physical Layer Standard for thick cable Ethernet, utilizing thick double shielded coaxial cable. 10BASE-5 stands for: 10 = 10 Mbit/s data rate, BASE = Baseband, 5 = 500 meters segment length.

10BASE-F – 10BASE-F is the IEEE 802.3 Physical Layer Standard for fiber-based Ethernet. 10BASE-F stands for; 10 = 10 Mbit/s data rate, BASE = baseband, F= fiber.

10BASE-T – 10BASE-T is the IEEE 802.3 Physical Layer Standard for the new twisted-pair Ethernet in a star topology. 10BASE-T stands for; 10 = 10 Mbit/s data rate, BASE = baseband, T = Twisted-pair over 100 meters nominal segment length.

Customer Feedback

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