Design Idea DI-25
DPA-Switch® 30 W DC-DC Converter with Synchronous Rectification

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
DC-DC Converter	DPA425R	30 W	36-75 VDC	5 V	Forward

Design Highlights

- Extremely low component count
- High Efficiency – 90% using synchronous rectification
- Accurate UV/OV allows self-driven synchronous rectification
- No current sense resistor or current transformer required
- Output overload, open loop and thermal protection
- 300 kHz switching frequency – optimizes efficiency when simple self-driven synchronous rectification is used

Operation

DPA-Switch greatly simplifies the deisign compared to a discrete implementation. Resistor R1 programs the input under/over voltages to 33 V and 86 V, respectively, and linearly reduces the maximum duty cycle with input voltage to prevent core saturation during load transients. Tight tolerances of the UV/OV thresholds determine the secondary MOSFETs gate voltage range, allowing low cost, self-driven synchronous rectification. Resistor R3 programs the internal current limit of the DPA425R to 45% of nominal. The larger *DPA-Switch* selection reduces conduction losses, raising efficiency without design or overload penalty.

DRAIN voltage clamping and core reset is provided by VR1 and the gate capacitance of Q1. The bias supply for U1 is generated from an auxiliary winding on L2, providing higher efficiency than a winding on T1.

Capacitor C17 and R15 drive the gate of Q2, C17 providing DC isolation to prevent Q1 gate overstress during power down. Diode D4 resets the voltage on C17 before the next switching cycle. Resistor R17 filters voltage spikes at the gate of Q1 and D2 prevents the body diode of Q1 from conducting. MOSFETs Q1 and Q2 are connected as self-driven synchronous rectifiers.

Key Design Points

- For nominal undervoltage set point V_{UV}: R1 = (V_{UV}-2.35 V)/50 µA. V_{OV} = (R1×135 µA) + 2.5 V.
- Select time constant of R16 and C17 to be much longer than the period of one switching cycle.
- Zener VR1 safely limits the DRAIN voltage below BV_{DSS} and guarantees transformer reset.
- Opto U2 should have a CTR range of 100% to 200% for optimum loop stability.

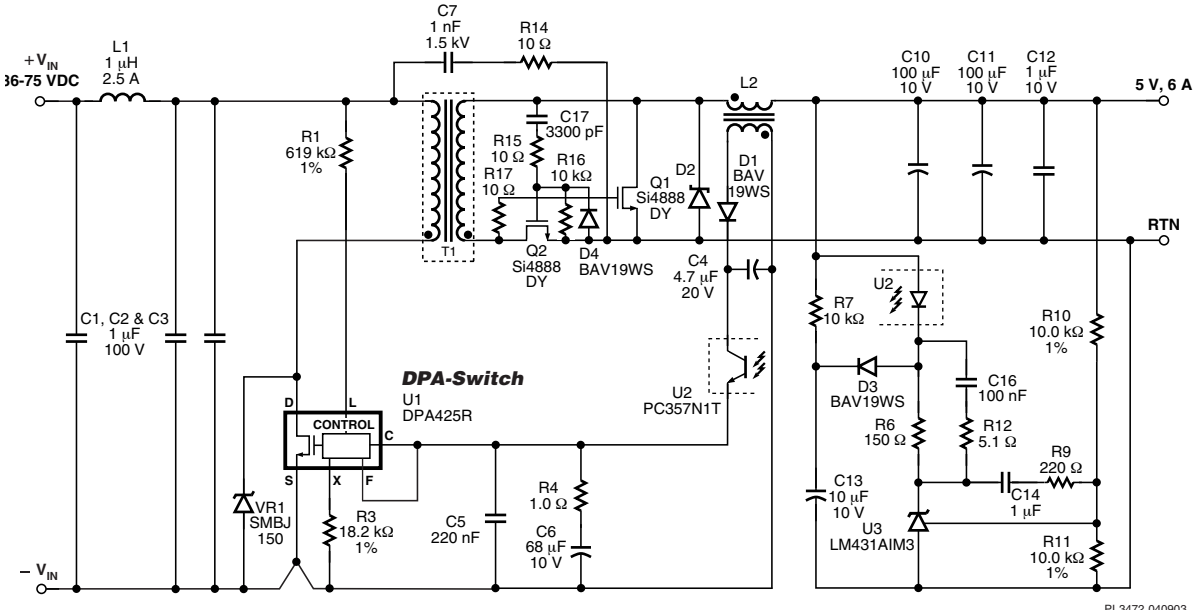

Figure 1. DPA-Switch 30 W, 5 V, 6 A DC-DC Converter.

- At zero load, maximum input voltage, the bias voltage across C4 should be ≥8 V (12 V to 15 V under nominal conditions).
- Good layout practices should be followed:
  - Locate C5, C6 and R4 close to U1 with grounds returned to the SOURCE pin.
  - Primary return should be connected to the *DPA-Switch* tab, not the SOURCE pin.
  - Minimize the primary and secondary loop areas to reduce parasitic leakage inductance.
- Consult AN-31 for additional design tips and information.
- Choose C17 to provide adequate gate charge to Q2 at low line (typically 5 V) and to limit Q2 gate to a safe voltage at high line (typically less than 20 V).

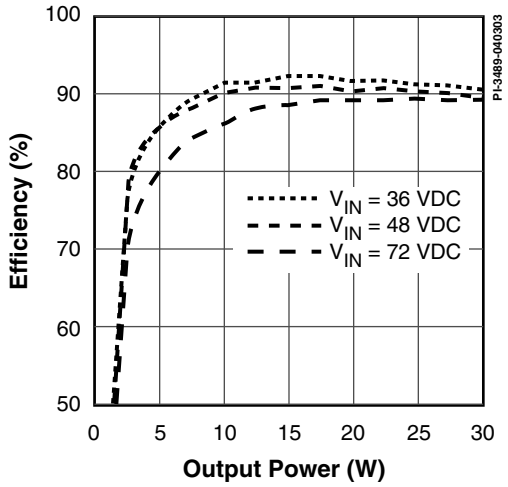

Figure 2. DPA-Switch 30 W, 5 V Synchronous Rectifier Efficiency vs. Output Power.

OUTPUT INDUCTOR PARAMETERS	
Core	RM6ILP Ferroxcube 3F3 material Gap for A_{LG} of 278 nH/T²
Winding Details	Main: 6T, 4x26 AWG Bias: 15T, 32 AWG
Bobbin	RM6ILP 8 pin (EPCOS B-65821-A6008-T1 or equivalent)
Winding Order (pin numbers)	Bias (1-2), tape, Main Winding (7,8-5,6), tape
Inductance	8 µH ±10%

Table 2. Output Inductor Construction Information.

TRANSFORMER PARAMETERS	
Core	EFD20 Ungapped Ferroxcube EFD20-3F3
Bobbin	EFD20 10 pin (B&B B-052 or equivalent)
Winding Detail	Primary: 8T + 8T, 25 AWG Secondary: 4T, 0.002" Cu Foil
Winding Order (pin numbers)	Primary (5-3), tape, Secondary (6,7-9,10), tape, Primary (3-1), tape
Inductance	Primary: 307 µH ±25%, Leakage: 1 µH (max.)
Primary Resonant Frequency	3 MHz (minimum)

Table 1. Transformer Construction Information.

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