Semiconductor Corporation

CS5412

12-Bit, 1MHz Self-Calibrating A/D Converter

Features

- Monolithic CMOS Sampling ADC
  - On-Chip Track and Hold Amplifier
  - Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  - Typical Nonlinearity: 3/4 LSB
  - No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 750mW

General Description

The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acqusition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

ORDERING INFORMATION: Page 3-228

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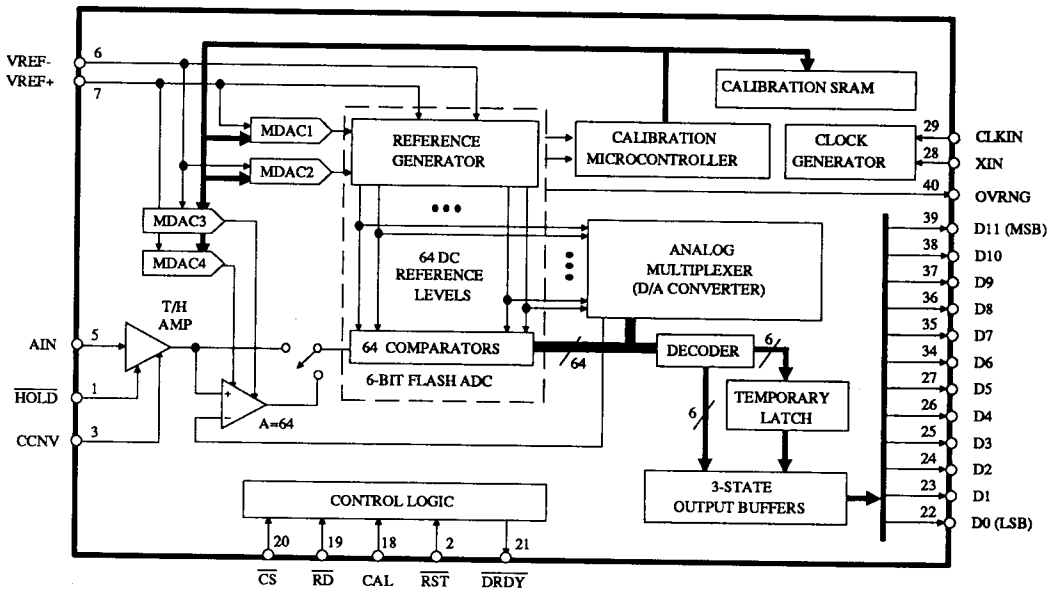

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ANALOG CHARACTERISTICS (T_A = 25°C (Note 1); All VA+ pins, VD+ = 5V; All VA- pins, VD- = -5V; VREF+ = +1.5V; VREF- = -1.5V; f_{CLK} = 8MHz for -1; 100 kHz Full Scale Input Sinewave; Continuous Convert Mode unless otherwise specified).

Parameter*	CS5412-J,K min	CS5412-J,K typ	CS5412-J,K max	CS5412-A,B min	CS5412-A,B typ	CS5412-A,B max	CS5412-S,T min	CS5412-S,T typ	CS5412-S,T max	Units
Resolution T_{min} to T_{max}	12			12			12			Bits
Specified Temperature Range		0 to 70			-40 to +85			-55 to +125		°C
Dynamic Performance										
Peak Harmonic or Spurious Noise (Note 1) T_{min} to T_{max} 100kHz Input	75	82		75	82		75	82		dB
490kHz Input		68			68			68		
Total Harmonic Distortion		0.0125			0.0125			0.0125		%
Signal-to-(Noise plus Distortion)(Note 1) 0dB Input (Full Scale) T_{min} to T_{max} -J,A,S	65	71		65	71		65	71		dB
-K,B,T	68	71		68	71		68	71		
-40dB Input		32			32			32		
dc Accuracy										
Linearity Error (Note 1,2) T_{min} to T_{max} -J,A,S		±3/4	±2.0		±3/4	±2.0		±1	±3.0	LSB
T_{min} to T_{max} -K,B,T		±3/4	±1.0		±3/4	±1.0		±3/4	±2.0	
Differential Linearity (Note 1) T_{min} to T_{max} -J,A,S		±1/2	NMC		±1/2	NMC		±1/2	NMC	LSB
T_{min} to T_{max} -K,B,T		±1/2	±0.9		±1/2	±0.9		±1/2	-0.9/+1.25	
Full Scale Error (Note 1) T_{min} to T_{max}		±2	±8		±2	±8		±3	±10	LSB
Offset Error (Note 1) T_{min} to T_{max}		±1.5	±3		±1.5	±3		±1.5	±4	LSB

NMC = No Missing Codes

Notes:
1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest. Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.
2. If the input voltage is static such that 128 consecutive conversions yield the same output code, then the transfer function may become non-monotonic.

* Refer to *Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter	CS5412-J,K min	CS5412-J,K typ	CS5412-J,K max	CS5412-A,B min	CS5412-A,B typ	CS5412-A,B max	CS5412-S,T min	CS5412-S,T typ	CS5412-S,T max	Units
Analog Input										
Aperture Time		35			35			35		ns
Aperture Jitter		50			50			50		ps, rms
Input Bandwidth										
Small Signal, -3dB (Note 3)		4			4			4		MHz
Full Power, -3dB		3.5			3.5			3.5		MHz
Analog Input Impedance at dc		10			10			10		Mohms
Input Capacitance VREF- pin		50			50			50		pF
AIN, VREF+ pins		10			10			10		pF
Conversion & Throughput										
Conversion Time (Notes 4, 5)	1.25		1.5	1.25		1.5	1.25		1.5	us
Throughput Rate		1			1			1		MHz
Acquisition Time (Note 6)		400			400			400		ns
Power Supplies										
Power Supply Current (Note 7)										
I_{A+}		70	90		70	90		70	90	mA
I_{A-}		-70	-90		-70	-90		-70	-90	mA
I_{D+}		5	10		5	10		5	10	mA
I_{D-}		-5	-10		-5	-10		-5	-10	mA
Power Consumption (Note 7)		750	1000		750	1000		750	1000	mW
Power Supply Rejection at dc										
Positive Supplies		50			50			50		dB
Negative Supplies		50			50			50		dB

Notes:
3. Input 40 dB below full scale.
4. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{DRDY}$.
5. Applies to conversions triggered externally. In Continuous Convert mode throughput proceeds at one-eighth the master clock frequency with a fixed 10 clock cycle conversion time.
6. The internal track-and-hold returns to the track mode on the fourth master clock cycle after the start of a conversion cycle. It is guaranteed to acquire a full-scale step to 12-bit accuracy while operating at full throughput.
7. All outputs unloaded. All inputs CMOS levels.

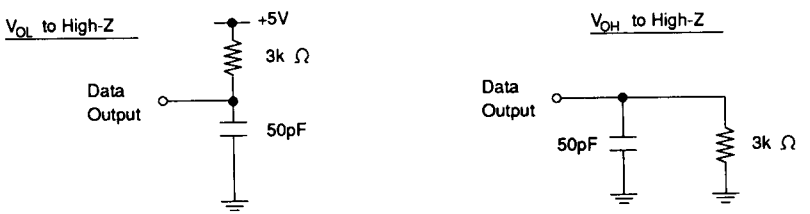
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF).

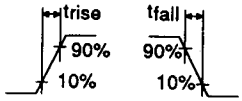
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:	f_{CLK}	3	-	8	MHz
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input (Note 8) Any Digital Output	t_{rise}	- -	- 20	1.0 -	us ns
Fall Times: Any Digital Input (Note 8) Any Digital Output	t_{fall}	- -	- 20	1.0 -	us ns
$\overline{HOLD}$/CLKIN Phase Relationship State 7 to $\overline{HOLD}$ Low $\overline{HOLD}$ Low to State 0 State 0 to $\overline{HOLD}$ High $\overline{HOLD}$ High to State 7	 t_{ha} t_{hb} t_{hc} t_{hd}	 62.5 0 75 30	 - - - -	 - - - -	 ns ns ns ns
Conversion Time (Note 9)	t_c	10	-	12	MCC*
$\overline{DRDY}$ Pulse Width	t_{dpw}	-	3	-	MCC*
Data Delay Time	t_{dd}	-	20	50	ns
Access Times: $\overline{CS}$ Low to Data Valid (Note 9) $\overline{RD}$ Low to Data Valid	t_{csa} t_{rda}	- -	55 55	110 110	ns ns
Output Float Delay: $\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	t_{fd}	-	40	110	ns
Cal Pulse Width: (Note 11) CAL high and $\overline{CS}$ Low	t_{csh}	2	-	-	MCC*
$\overline{RST}$ Pulse Width	t_{rpw}	2	-	-	MCC*

Notes: 8. $\overline{HOLD}$ and CLKIN should be driven with signals which have rise and fall times of 25 ns or faster.
9. Conversion time in the Continuous Convert mode is a fixed 10 clock cycles.
10. Data goes valid when both $\overline{CS}$ and $\overline{RD}$ are low simultaneously. Each access time assumes the other control input is already low or falls concurrently.
11. If CAL is brought low while $\overline{CS}$ is low, a calibration cycle will be initiated.

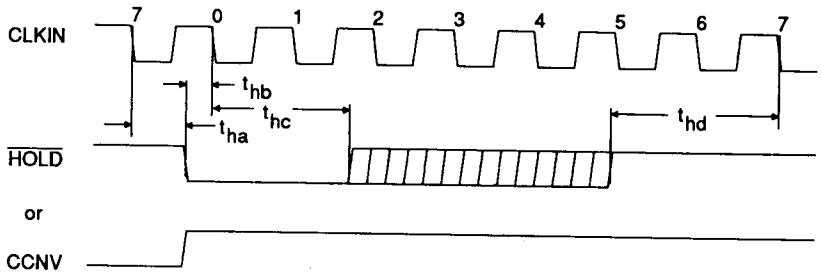
* MCC = Master Clock Cycles; 1 MCC = $1/f_{CLK}$

Float Delay Test Circuits

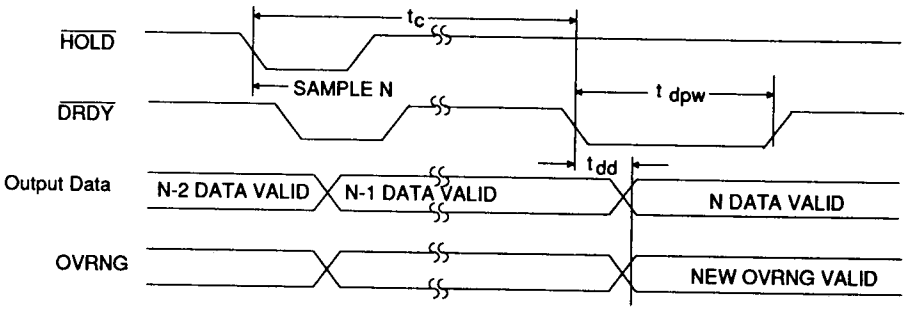




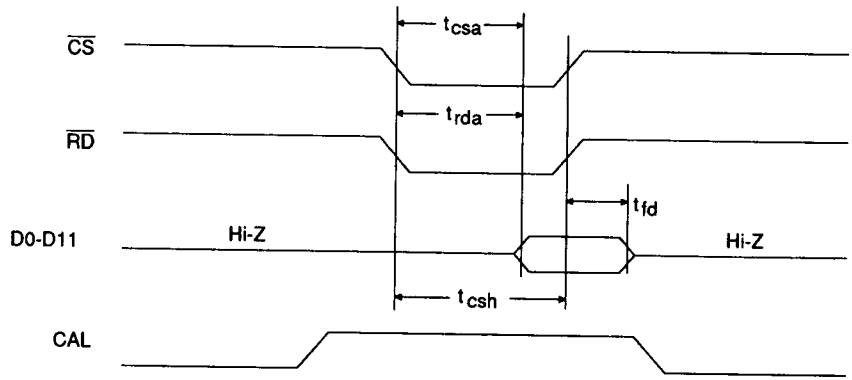
Rise and Fall Times



Hold/Master Clock Phase Relationship



Conversion Timing



Read and Calibration Control Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%) All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 12)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 12)	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 13)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-10	-	+10	uA
3-State Leakage Current	I_{OZ}	-10	-	+10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 12. All pins except $\overline{HOLD}$ and CLKIN which require inputs of V_{IL} = 0.5V and V_{IH} = VD+ - 0.5V.
13. I_{out} = -100µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 14).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.75	5.0	VA2+, VA5+	V
Negative Digital	VD-	−4.75	−5.0	−5.25	V
Positive Analog	VA1+ - VA5+	4.75	5.0	5.25	V
Negative Analog	VA1- - VA3-	−4.75	−5.0	−5.25	V
Analog Input Voltage	V_{AIN}	VREF-	-	VREF+	V
Analog Reference Voltages					
Unipolar Input Range	VREF+	2.0	-	3.0	V
	VREF-	-	AGND	-	V
Bipolar Input Range	VREF+	1.0	-	1.5	V
	VREF-	−1.0	-	−1.5	V

Notes: 14. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	VD+	−0.3	VA2+,VA5+ + 0.3	V
Negative Digital	VD-	0.3	−6.0	V
Positive Analog (Note 15)	VA1+ - VA5+	−0.3	6.0	V
Negative Analog	VA1- - VA3-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 16)	I_{in}	-	+10	mA
Analog Input Voltage (AIN and VREF pins)	V_{INA}	VA1- - VA3- - 0.3	VA2+,VA5+ + 0.3	V
Digital Input Voltage	V_{IND}	−0.3	VA2+,VA5+ + 0.3	V
Ambient Operating Temperature	T_A	−55	125	°C
Storage Temperature	T_{stg}	−65	150	°C
Junction Temperature	T_J	-	160	°C
Junction to Ambient Tempco for CLCC Package	Θ_{JA}	-	60	°C/W

Notes: 15. VA1+, VA3+, VA4+ must never exceed VA2+ and VA5+ by more than 0.3V.
16. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

To achieve high speed and high accuracy, the CS5412 implements a standard 2-step flash A/D conversion using a self-calibrating architecture. Throughput is further maximized using pipelined acquisition and settling times as well as overlapped conversion cycles.

2-Step Flash A/D Conversion

The fastest method of performing A/D conversion is the brute-force single-step flash approach, for which an N-bit conversion involves comparing the analog input to 2^N-1 graduated voltage levels. The outputs from the 2^N-1 comparators are then processed and encoded into the proper binary format. The major limitation to this technique is that the number (and accuracy requirements) of comparators doubles with each additional bit of resolution. Thus, single-step flash converters are impractical today at greater than 8 or 10 bits of resolution.

The 2-step technique that the CS5412 uses employs slightly more complex sub-circuit blocks to achieve high resolution and results in negligible speed degradation. As shown in Figure 1, the CS5412 consists of a track-and-hold amplifier (T/H_1), a 6-bit flash ADC, a 6-bit DAC, and a differential amplifier. When the convert command is issued, T/H_1 holds the analog input signal and the flash ADC converts the six MSB's (most-significant-bits) of the output word. The MSB's, once decoded, are latched. The flash converter's output is also loaded into the DAC. The DAC's output therefore represents the analog input less the quantization error of the first 6-bit flash conversion. This signal is then subtracted from the original analog input to yield the quantization error, which is then multiplied by 64 (2^6) and again applied to the flash ADC to yield the six LSB's (least-significant-bits). In effect, the first 6-bit flash forms the transfer function into 64 segments which are then filled in with 64 codes each by the second 6-bit flash. This yields a total of 4096 codes (64x64) for 12-bit resolution.

Calibration

The CS5412 uses several calibration techniques to insure 12-bit accuracy over time and temperature. A unique reference generating circuit provides the 64 graduated reference levels for the flash ADC and DAC. Critical to the CS5412's overall linearity, these references are continually adjusted to 12-bit accuracy during device operation. This background adjustment process is completely transparent to the user and results in less than ±1/2 LSB nonlinearity. Also, all comparators in the flash ADC are auto-zeroed to avoid differential linearity errors at the 64 segment boundaries due to noise and/or offsets in the comparators.

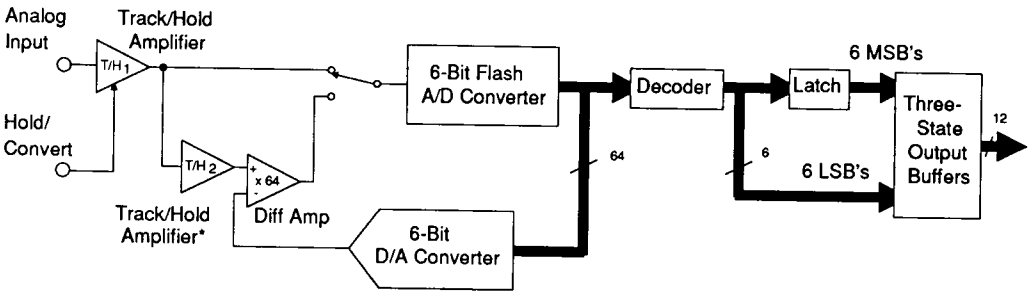


Figure 1. Block Diagram of 2-Step Flash A/D Converter

The CS5412 also uses digital correction schemes. An on-chip microcontroller manipulates dedicated MDAC's to set the gain and offset of the 6-bit flash ADC; this insures less than ±1/2 LSB overall full-scale and offset errors in the CS5412. Gain and offset are similarly calibrated in the differential amplifier to avoid linearity errors at the 64 segment boundaries.

Upon power-up, the CS5412 is reset in hardware or software to initially calibrate the device. Calibration can be similarly initiated at any later time throughout operating life to insure 12-bit accuracy independent of environmental conditions.

Pipelined Timing

To achieve throughput rates up to 1MHz, the CS5412 pipelines settling times in both the sampling and conversion processes. The CS5412 can actually begin a conversion cycle while still operating on the previous sample. As shown in Figure 2, the *Hold and Convert* command for Sample N+1 can be issued before data from Sample N is valid at the output. By definition, the throughput time of the CS5412 is shorter than the conversion time due to the overlapped conversion cycles. Compared to a non-pipelined 1MHz ADC, the CS5412 provides the same 1MHz throughput, only the output data is delayed slightly in time (1.25µs delay through the ADC rather than 1µs).

The CS5412 also uses a second track-and-hold amplifier (termed T/H_2 in Figure 3) to pipeline the converter's acquisition time. As shown in Figure 3, T/H_2 holds the output from T/H_1 valid for the second flash conversion, *Flash 2*. This allows T/H_1 to release and acquire the analog input signal during the second flash conversion, allowing another *Hold & Convert* command to be issued even before the completion of *Flash 2*.

DIGITAL CIRCUIT CONNECTIONS

In addition to master clock and sampling connections which set the converter's timing, the CS5412 offers an *Overrange* output, 3-state output buffers, and flexible control interface. The CS5412 can therefore connect directly to a microprocessor's data and control busses or can be operated in a stand-alone mode.

Master Clock

The CS5412 operates from a master clock reference which must be supplied in the form of either a crystal or external clock. A crystal can be tied across the CLKIN and XIN pins, or alternatively, the CS5412 can be synchronized to the external system by driving CLKIN with a CMOS-compatible clock (XIN left floating). If the master clock is shut off while the CS5412 is powered up, an internal oscillator will start-up to keep all in-

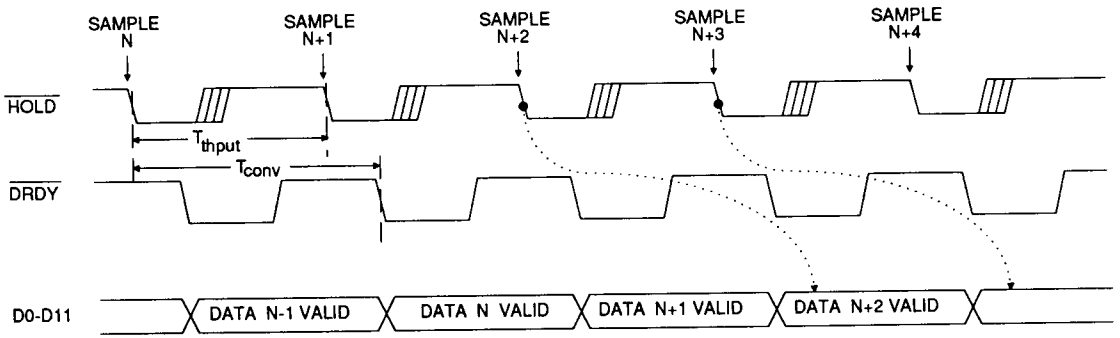


Figure 2. Pipelined Conversion Cycles

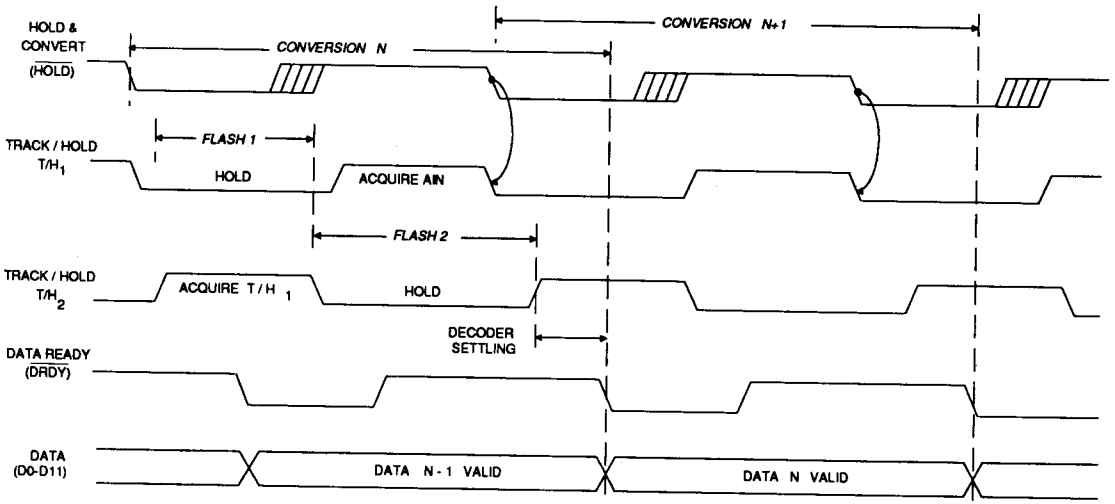


Figure 3. Pipelined Acquisition and Settling Times.

ternal dynamic logic refreshed. This internal oscillator should not be used for conversions. Clock cycles can be selectively skipped at any time, but the clock's average frequency should never drop below the device's minimum specification (see Switching Characteristics).

Sampling/Initiating Conversions

There are two methods of controlling the CS5412's sampling/conversion timing. First, the CS5412 has a $\overline{\text{HOLD}}$ input which, on a falling edge, places the input track-and-hold amplifier in the hold state and initiates a conversion cycle. The CS5412 also features a *Continuous Convert* mode (CCNV and $\overline{\text{HOLD}}$ high) in which hold commands are internally generated every eight master clock cycles. The sampling/throughput rate is therefore controlled by adjusting the master clock frequency and there is no need to generate a sampling clock.

When CCNV is brought high with the proper relationship to CLKIN (shown in the timing diagrams), the next falling clock edge defines state 0.

Lower sampling rates can be created in the *Continuous Convert* mode by running the CS5412 at full throughput and decimating the output, selectively reading only a fraction of the available samples. Variable sampling rates can be implemented in this manner using a programmable divider on the $\overline{\text{DRDY}}$ output. When operating in the *Continuous Convert* mode, attention should be paid to jitter on the master clock, since jitter will directly affect sampling purity.

If the phase of sampling must be precisely controlled, the $\overline{\text{HOLD}}$ input must be used since the hold signal is internally-generated in the *Continuous Convert* mode. A falling edge on $\overline{\text{HOLD}}$ places the internal track-and-hold amplifier in the hold state and signals a conversion cycle to begin on the next falling edge of the master clock. The $\overline{\text{HOLD}}$ input was designed for minimum aperture jitter and therefore requires CMOS-compatible logic levels (not TTL-compatible).

Due to the CS5412's refreshing the 64 reference levels in the background, $\overline{\text{HOLD}}$ commands must be synchronized to the master clock and can only occur at intervals of 8 master clock cycles. The first $\overline{\text{HOLD}}$ command after the start of a reset or

calibration cycle defines state 0 in the CS5412's timing circuitry (see Figure 4). The sampling signal applied to $\overline{HOLD}$ must adhere to frequencies of $f_{clk}/8N$ such that subsequent $\overline{HOLD}$ commands will always fall between state 7 and state 0. If the sampling clock changes phase and a $\overline{HOLD}$ command occurs before state 7 or after state 0 the CS5412 may be thrown out of calibration, and 4288 clock cycles must be allowed for the converter to complete two full background refresh cycles. Likewise, conversion data should be considered invalid for 4288 clock cycles following the first $\overline{HOLD}$ command after the end of calibration to insure specified accuracy. If a normal, periodic, $\overline{HOLD}$ signal is applied during the entire calibration period, the data will be valid immediately after calibration, i.e. when OVRNG goes low.

Most often the sampling signal applied to $\overline{HOLD}$ can be derived from the master clock. In these cases, the master clock is divided by 8, 16, 24, 32, etc. If sampling must be locked to some external clock source, a phase-locked loop can be used to generate a master clock signal for CLKIN from the sampling signal. In this instance jitter on the $\overline{HOLD}$ input will directly affect sampling purity; however, the CS5412 will tolerate significant jitter on the master clock without loss of accuracy (assuming the $\overline{HOLD}$/CLKIN phase specifications are met).

Conversion Time/Throughput

In the *Continuous Convert* mode, throughput will proceed at one-eighth the master clock frequency and the delay through the CS5412 will be ten master clock cycles. When hold commands are generated externally at the $\overline{HOLD}$ pin, the analog input is held immediately as the $\overline{HOLD}$ input falls and the conversion cycle begins on the next falling edge of the master clock. The CS5412's conversion time will range from 10 to 11 clock cycles depending on the phase relationship of the $\overline{HOLD}$ signal to the master clock (see Figure 4). Throughput can still proceed at $f_{clk}/8$ independent of the conversion time. The pipelined overlap between conversion cycles will range from to 2 to 3 clock cycles.

Reset

Upon power-up, the CS5412 must be reset to guarantee a consistent starting condition and initially calibrate the device. A falling edge on the $\overline{RST}$ pin clears internal logic and a rising edge initiates a calibration cycle which takes 6,052,445 master clock cycles to complete. The $\overline{RST}$ input must remain low for at least 2 master clock cycles to be considered valid. A simple power-up reset circuit can be constructed by tying a capacitor from $\overline{RST}$ to DGND and a resistor from $\overline{RST}$ to VD+.

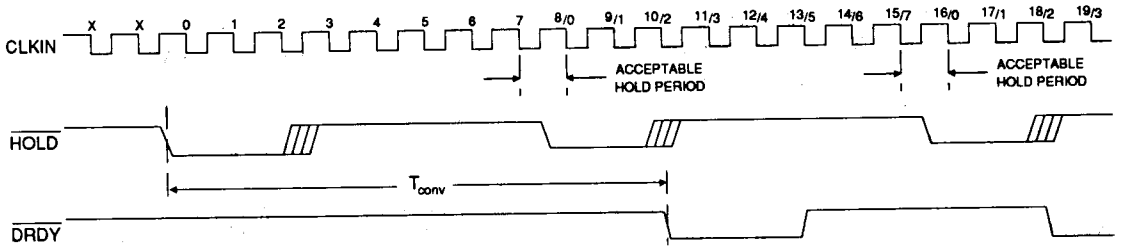


Figure 4. Hold / Conversion Timing.

Due to the CS5412's modest power dissipation and low temperature drift, no warm-up time is needed before reset to accommodate any self-heating effects. However, the voltage references (VREF+ and VREF-) should have stabilized to within their specified accuracies. The CS5412 can be reset later at any time during operation to initiate calibration. Reset overrides all other functions. If reset, the CS5412 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Overrange

The CS5412 will flag an overrange input at the OVRNG pin whenever *the sampled analog input* exceeds either the positive or negative reference voltage. If the sampled input exceeds VREF+, OVRNG will go high as DRDY falls, and all ones will be loaded into the output buffers. Similarly, if the analog input is below VREF-, OVRNG will go high as all zeroes are loaded into the output buffers. OVRNG should be latched on the rising edge of $\overline{DRDY}$. The internal reference voltages are not affected by excursions of AIN outside the external reference voltages up to the supply voltages.

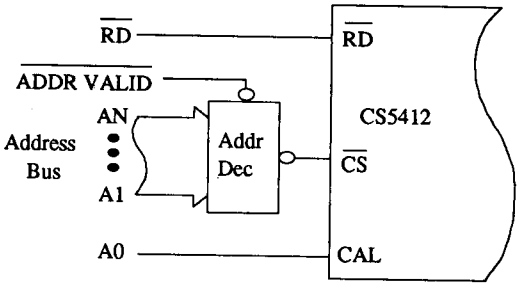


Figure 5. Microprocessor Controlled Operation.

Thirteen clock cycles after $\overline{RST}$ or CAL transitions, OVRNG goes high. The OVRNG output remains high throughout a reset/calibration sequence and will return low after its completion. It can therefore be used to generate an interrupt indicating the CS5412 has completed calibration and is ready for operation.

Microprocessor Controlled Operation

The CS5412 features 3-state output buffers and a control interface which allow the device to connect directly to a microprocessor's data and control busses. Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CS5412's 3-state output buffers with the converter's 12-bit output word. As shown in Figure 5, a decoded address is normally applied

$\overline{CS}$	$\overline{RD}$	CCNV	$\overline{HOLD}$	CAL	$\overline{RST}$	Function
0	0	X	X	0	1	Read Output Data
*	1	X	X	*	1	High Impedance Data Bus
1	X	X	X	X	1	High Impedance Data Bus
*	X	1	X	*	1	Continuous Convert Mode
*	X	0	↓	*	1	Hold and Start Convert
X	X	X	X	X	↓	Start Reset
0	X	X	X	↓	X	Start Reset

*** Not critical to the operation specified. However, $\overline{CS}$ should not be low with CAL transitioning low or a software reset will result.**

Table 1. CS5412 Truth Table.

to $\overline{CS}$, and the $\overline{RD}$ input is derived from read and strobe signals from the microprocessor's control bus. The Data Ready ($\overline{DRDY}$) output can be used to generate an interrupt or drive a DMA controller to dump the CS5412's output directly into memory after each conversion. The $\overline{DRDY}$ output falls as new data is being loaded into the output buffers. Data should be latched on the rising edge of $\overline{DRDY}$ which occurs three master clock cycles after it falls.

The CS5412 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. The CS5412 should be synchronized to the digital system via CLKIN to avoid potential errors due to enabling the 3-state output buffers while the part is converting. Using TTL loads also increases the potential for crosstalk between the digital and analog portions of the system. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the CS5412's digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

Initiating Calibration

In addition to the hardware reset, the CS5412 features a software calibration capability. Whenever CAL transitions low with $\overline{CS}$ low, or $\overline{CS}$ transitions high with CAL high, a calibration cycle will be initiated which is equivalent to the reset function. As shown in Figure 5, line A0 from the address bus can be connected to the CAL input when operating under microprocessor control. A read cycle from the CS5412's base address with A0 low will therefore retrieve output data while a read or write cycle with A0 high will initiate calibration. The CAL input is level sensitive, and like $\overline{RST}$, CAL overrides all other functions. Software-initiated calibrations can thus be used in lieu of a hardware reset at power-up.

Stand-Alone Operation

The CS5412 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low, permanently enabling the 3-state output buffers. A free-running condition is established when CAL is tied low, and $\overline{HOLD}$ is continually strobed low or CCNV is held high. The CS5412's $\overline{DRDY}$ output can be used to externally latch the output data if desired. The $\overline{DRDY}$ output will strobe low for three master clock cycles after each conversion. Data will typically be unstable for 40ns after $\overline{DRDY}$ falls, so it should be latched on the rising edge of $\overline{DRDY}$. This results in a total delay of 13 master clock cycles through the CS5412.

ANALOG CIRCUIT CONNECTIONS

Like most 2-step flash A/D converters with internal track-and-hold amplifiers, the CS5412 offers a trivial load at its analog input compared to successive-approximation and single-step flash A/D converters. The reference connections similarly present high impedance loads. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Analog Input and Reference Connections

The CS5412's analog input range is defined by the voltages applied to the VREF- and VREF+ pins. The analog input (AIN) is referenced only to these reference voltages and is completely independent of the analog ground pins. The first code transition ideally occurs 1 LSB above VREF- and the last transition occurs 1 LSB below VREF+. The CS5412 can operate with a full-scale reference as low as 2.0V p-p, but signal-to-noise performance is maximized by using the full specified range of 3V p-p. Unipolar input ranges are achieved by tying VREF- to the system's analog ground and applying the reference voltage to VREF+. Bipolar input ranges are

achieved by applying positive and negative voltages of equal magnitude to VREF+ and VREF- respectively. In this configuration, coding is in offset-binary format.

The CS5412's analog input (AIN) pin looks directly into the noninverting terminal of the track-and-hold amplifier resulting in over 10MΩ input impedance and less than 10pF input capacitance.

The reference voltages at the +VREF and -VREF inputs are dynamically sampled. This pulsed charge load requires each of the reference inputs to be decoupled with a 0.1µF ceramic capacitor in parallel with a 3.3µF tantalum capacitor. The tantalum capacitors should be chosen to maintain 3.3µF minimum capacitance over the operating temperature range. To maintain DC accuracy the reference(s) should have an output impedance of less than 5Ω at DC.

The CS3901 voltage reference provides +3V or ±1.5V for the CS5412 (see CS3901 data sheet).

Grounding and Power Supply Decoupling

The CS5412 uses the analog ground connections, AGND1 and AGND2, only as stable, low impedance sources. No dc power currents flow through these connections, and they are completely independent of AIN and DGND. Still, AGND1 and AGND2 should be tied to the system's analog ground. The CS5412's analog input is referenced only to VREF+ and VREF-. Therefore, the analog input and reference voltages should be referred to the same ground potential (not necessarily AGND) which should be used as the entire system's analog ground. The optimal grounding configuration for the CS5412 utilizes one ground plane under the CS5412. Peripheral analog and digital circuitry should be partitioned on the circuit board and separate ground planes may or may not be used.

The digital and analog supplies are isolated within the CS5412 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. The analog supplies also have multiple connections which minimize lead inductances and power separate portions of the converter's analog circuitry. The decoupling scheme shown in the *System Connection Diagram* in Figure 9 provides optimal decoupling between the CS5412's digital circuitry and the various analog sections of the chip. Ceramic capacitors are acceptable for all decoupling, and they should be placed as close to the supply pins as possible. If significant low-frequency noise is present on the supplies, 10µF tantalum capacitors are recommended in parallel with 0.1µF ceramic capacitors on the ±5V rails.

The positive digital power supply (VD+) should never exceed the positive analog supplies (VA2+ or VA5+) or the CS5412 could experience permanent damage. If the two supplies are derived from separate sources, care should be taken that the analog supply comes up first at power-up. The *System Connection Diagram* in Figure 8 shows a decoupling scheme which allows the CS5412 to be powered from a single set of ±5V rails. The positive digital supply is derived from the analog supplies though a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is used, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of the digital supplies to drop below their minimum specification of 4.75V.

As with any high-speed, high-precision A/D converter, the CS5412 requires careful attention to grounding and layout arrangements. The CDB5412 evaluation board is available for the CS5412, which eliminates the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5412 and can be quickly reconfigured to simulate any combination of sampling, calibration, and master clock conditions.

Performance

Two types of performance test results are presented here. With FFT based tests, a pure sine wave is input to the CS5412, and an FFT analysis is performed on the output data. Figure 6 shows the resulting plot with a 100 kHz input sine. Notice the absence of any harmonic distortion and the overall Signal to (Noise + Distortion) value of 70.3 dB.

Figure 7 shows the FFT plot when two sine waves are simultaneously applied to the input. Notice the lack of sum and difference products, indicating very good linearity.

A second test looks for variation in the code width of the CS5412, as the input moves from -Full Scale to +Full Scale. This is called the Differential Non Linearity (DNL) and is expressed as a deviation from the ideal (in LSB), with 0 being perfect. Figure 8 shows the CS5412's excellent DNL performance with most codes being within ± 0.1 LSB of perfect.

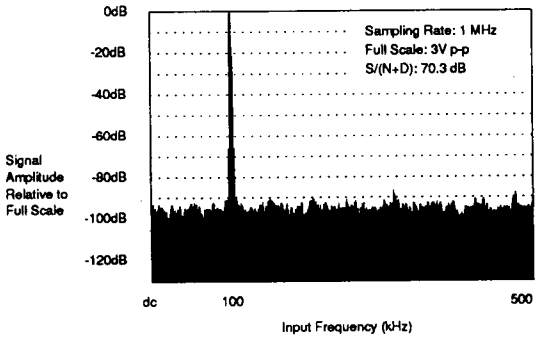


Figure 6. Typical CS5412 FFT Performance

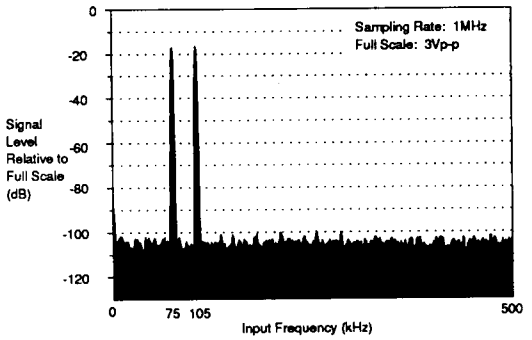


Figure 7. Intermodulation Distortion Performance

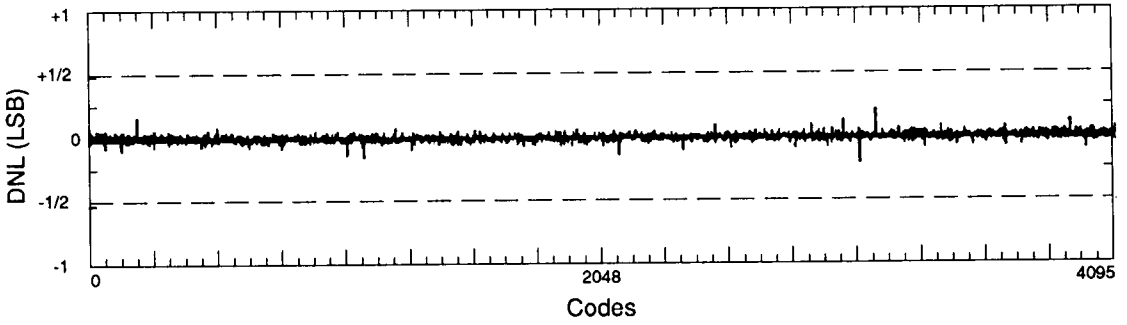
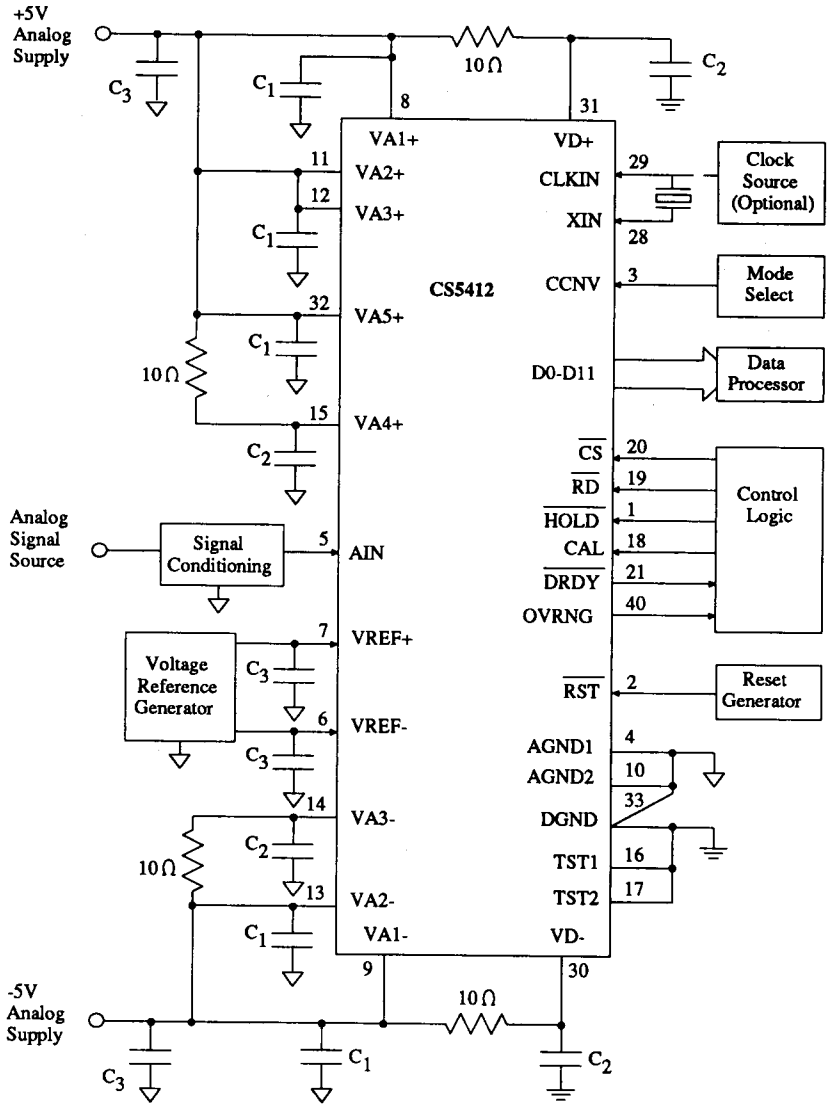


Figure 8. Typical CS5412 Differential Non-Linearity Plot

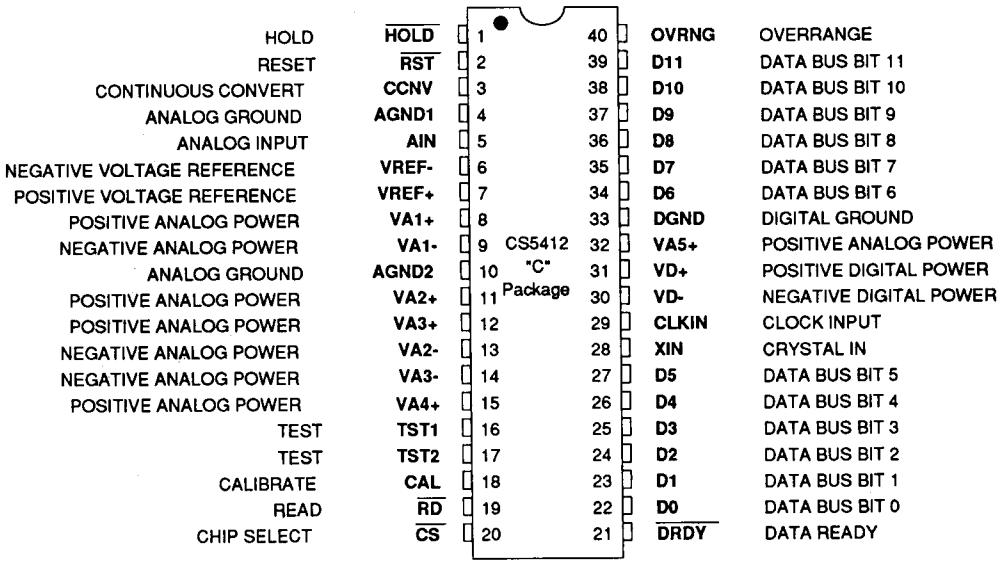


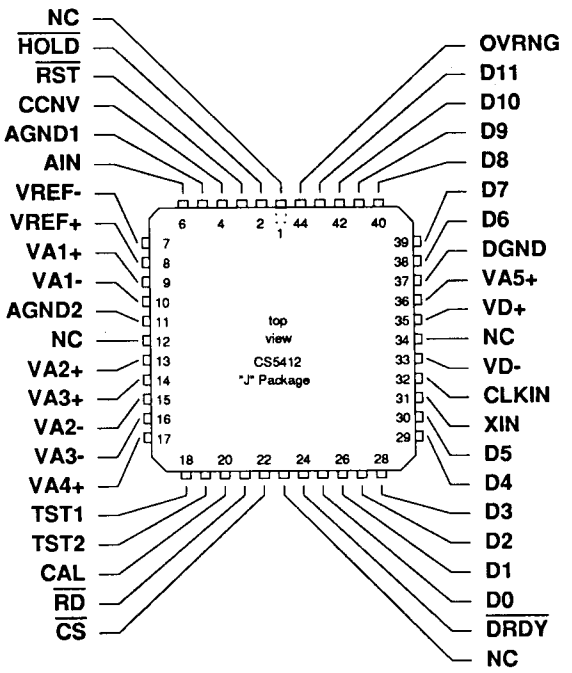
*VA2+ and VA5+ must be externally connected.

C1 - 0.01µF ceramic
C2 - 0.01µF in parallel with 0.1µF ceramic
C3 - 0.1µF ceramic in parallel with 3.3 µF tantalum

Figure 9. System Connection Diagram.

PIN DESCRIPTIONS





Power Supply Connections

VD+ - Positive Digital Power, PIN 31.
Positive digital supply voltage. Nominally +5 volts.

VD- - Negative Digital Power, PIN 30.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 33.
Digital ground reference.

VA+ - Positive Analog Power, PINS 8, 11, 12, 15, 32.
Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, PINS 9, 13, 14.
Negative analog supply voltage. Nominally -5 volts.

AGND - Analog Ground, PIN 4, 10.
Analog ground reference.

Oscillator

CLKIN; XIN - Clock In, PIN 29; Crystal In, PIN 28.
Used to generate the internal master clock. A crystal can be tied across the two pins or an external CMOS-compatible clock can be driven into CLKIN if XIN is left floating.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold Input, PIN 1.
A negative transition on $\overline{\text{HOLD}}$ puts the track-and-hold amplifier into the hold state and initiates the conversion sequence. Conversions must be synchronized with the master clock at $f_{CLK}/8N$ where N = 1,2,3. The $\overline{\text{HOLD}}$ input is CMOS-compatible.

CCNV - Continuous Convert, PIN 3.
When held high throughput will proceed at $1/8^{th}$ the master clock frequency. The $\overline{\text{HOLD}}$ pin can be high or low but must not transition.

$\overline{\text{CS}}$ - Chip Select, PIN 20.
Activates the $\overline{\text{RD}}$ and CAL inputs. When $\overline{\text{CS}}$ is high, these inputs have no effect and the data bus (D0 through D11) is held in a high impedance state.

$\overline{\text{RD}}$ - Read, PIN 19.
When held low with $\overline{\text{CS}}$ also low, enables D0-D11.

Note: Pin numbers are for the DIP package.

$\overline{RST}$ - Reset, PIN 2.

When $\overline{RST}$ transitions from low to high a full calibration is started 13 master clock cycles later indicated by OVRNG going high. OVRNG will return low when calibration is finished. Calibration takes 6,052,445 master clock cycles.

CAL - Calibrate, PIN 18.

Same as $\overline{RST}$ except it it logically inverted and enabled by $\overline{CS}$ going low .

Analog Inputs

VREF+ - Positive Voltage Reference, PIN 7.

Represents positive full scale voltage. Typically +1.5V with respect to AGND (bipolar system) or +3V with respect to AGND and VREF- (unipolar system).

VREF- - Negative Voltage Reference, PIN 6.

Represents negative full scale voltage. Typically -1.5V with respect to AGND (bipolar system) or tied to AGND (unipolar system).

AIN - Analog Input, PIN 5.

Analog input to the track-and-hold amplifier.

Digital Outputs

OVRNG - Overrange, PIN 40.

Goes high if the sampled analog input voltage exceeds VREF+ or VREF-. OVRNG also goes high during calibration cycles and can therefore be used to indicate end of calibration.

$\overline{DRDY}$ - Data Ready, PIN 21.

Falls when new data is becoming available at the outputs. Returns high three master clock cycles later. Data should be retrieved on the rising edge of $\overline{DRDY}$.

Digital Input/Outputs

D0 through D11 - Data Bus, PINS 22 thru 27, 34 thru 39.

Three-state data bus where D11 is the MSB and D0 is the LSB. The output coding is binary for unipolar and offset binary for bipolar.

Miscellaneous Pins

TST1 - Test, PIN 16.

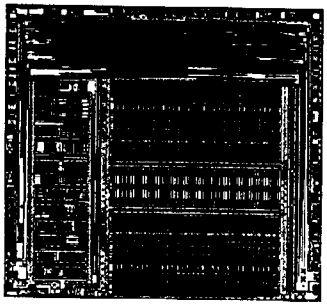
Reserved for factory use. Must be tied to DGND for proper device operation.

TST2 - Test, PIN 17.

Reserved for factory use. Must be tied to DGND for proper device operation.

Note: Pin numbers are for the DIP package.

DIE INFORMATION



CS5412-YU

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.374" by 0.348" (± 0.002").

2. The die is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

3. Die thickness shall be 0.0175" ± 0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 9.

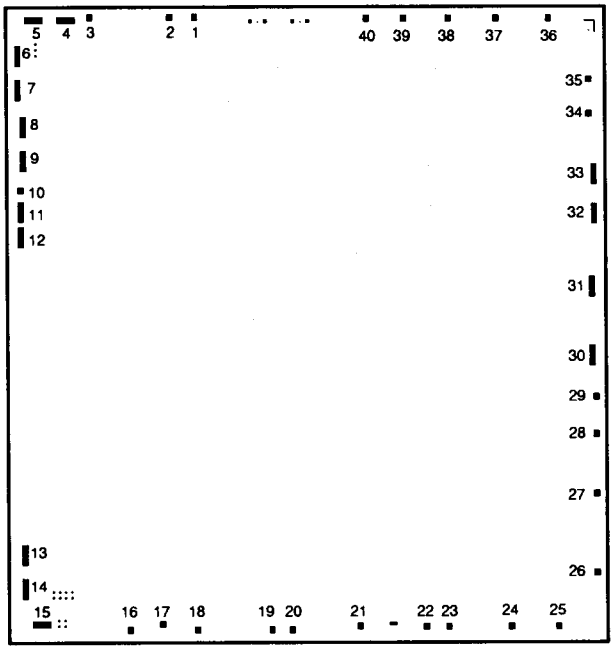
5. The cavity dimensions for each die within the waffle pack are 0.425" by 0.425". Exterior waffle pack dimensions are 2.0" by 2.0"

6. The die requires no particular bonding sequence.

7. Each pin on the CS5412 has both ESD and latch-up protection circuitry. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.

8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

CS5412-YU Bonding Diagram



1	-	$\overline{\text{HOLD}}$	21	-	$\overline{\text{DRDY}}$
2	-	$\overline{\text{RST}}$	22	-	D0
3	-	CCNV	23	-	D1
4	-	AGND1	24	-	D2
5	-	AIN	25	-	D3
6	-	VREF-	26	-	D4
7	-	VREF+	27	-	D5
8	-	VAl+	28	-	XIN
9	-	VAl-	29	-	CLKIN
10	-	ANGD2	30	-	VD-
11	-	VA2+	31	-	VD+
12	-	VA3+	32	-	VA5+
13	-	VA2-	33	-	DGND
14	-	VA3-	34	-	D6
15	-	VA4+	35	-	D7
16	-	TST1	36	-	D8
17	-	TST2	37	-	D9
18	-	$\overline{\text{CAL}}$	38	-	D10
19	-	$\overline{\text{RD}}$	39	-	D11
20	-	$\overline{\text{CS}}$	40	-	OVRNG

DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - Ratio of the rms sum of all harmonics to the rms value of of the signal. Units in percent.

Signal-to-(Noise plus Distortion) - Ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc). Expressed in decibels.

Linearity Error - The deviation of the worst code width center, out of all 4096 codes, from a straight line. The straight line is determined by using a least squares fit algorithm from the measured points. Units in LSB's.

Differential Nonlinearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full Scale Error - The deviation of the last code transition from the ideal (VREF+ - 1 LSB). Units in LSB's.

Offset Error - The deviation of the first code transition from the ideal (VREF- + 1 LSB). Units in LSB's.

Aperture Time - The time required after the hold command is issued for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuracy. Units in picoseconds.

Ordering Guide

Model	Throughput	Signal to (Noise plus Distortion)	Linearity Error	Temp Range	Package
CS5412-JC1	1 MHz	65 dB	± 2.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-JJ1	1 MHz	65 dB	± 2.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-KC1	1 MHz	68 dB	± 1.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-KJ1	1 MHz	68 dB	± 1.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-AC1	1 MHz	65 dB	± 2.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-BC1	1 MHz	68 dB	± 1.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-SC1	1 MHz	65 dB	± 3.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
CS5412-TC1	1 MHz	68 dB	± 2.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
CS5412-SJ1	1 MHz	65 dB	± 3.0 LSB	-55 to +125 °C	44-Pin J Lead CLCC
CS5412-TJ1	1 MHz	68 dB	± 2.0 LSB	-55 to +125 °C	44-Pin J Lead CLCC
CS5412-YU	1 MHz				Unpackaged Die

MIL-STD-883C Rev.B Versions

SMD Number: 5962-90957

Refer to SMD for accuracy and package suffixes.