#### CMOS 4-Bit Microcontroller

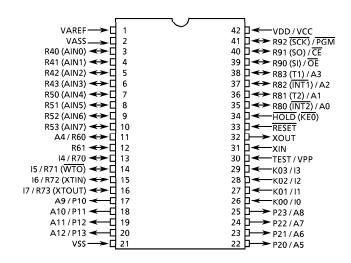
# **TMP47P840VN** TMP47P840VF

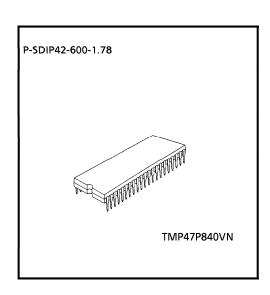
The 47P840V is the OTP microcontroller with 64Kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764AD type) and adapter socket. The function of this device is exactly same as the 47C640/840.

Part No.	ROM	RAM	Package	Adapter Socket
TMP47P840VN	ОТР	F124 bit	P-SDIP42-600-1.78	BM1171
TMP47P840VF	8192 × 8-bit	512 × 4-bit	P-QFP44-1414-0.80D	BM1172

### Pin Assignment (Top View)

P-SDIP42-600-1.78





980901EBP1

For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter

For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.
 TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
 The products described in this document are subject to foreign exchange and foreign trade laws.
 The information contained herein is presented only as a quide for the applications of our products. No responsibility

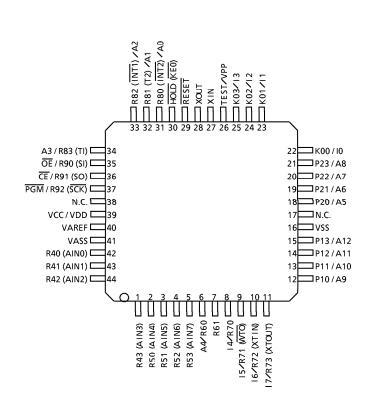
The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

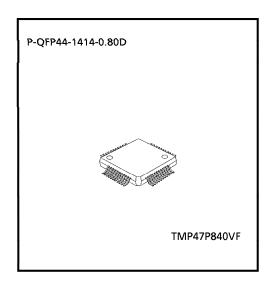
The information contained herein is subject to change without notice.

4-40-17 1999-09-01

# Pin Assignment (Top View)

P-QFP44-1414-0.80D





# **Pin Function**

The 47P840V has MCU mode and PROM mode.

# (1) MCU mode

The 47C640/840 and the 47P840V are pin compatible (TEST pin for out-going test. Be fixed to low level.).

# (2) PROM mode

Pin Name	Input / Output	Functions	Pin Name (MCU mode)
A12 to A9			P13 to P10
A8 to A5	Input	Address inputs	P23 to P20
A4	mput	Address inputs	R60
A3 to A0			R83 to R80
17 to 14	I/O	Data outputs (Inputs)	R73 to R70
13 to 10	1/0	Data outputs (inputs)	K03 to K00
PGM		Program control input	R92
CE	Input	Chip Enable input	R91
ŌĒ		Output Enable input	R90
VPP		+ 12.5 V / 5 V (Program supply voltage)	TEST
vcc	Power supply	+5V	VDD
VSS		0 V	VSS
R43 to R40			
R53 to R50	I/O	Be fixed to low level	
R61			
RESET	Input	PROM and a serious in the final day level and	
HOLD	Input	PROM mode setting pin. Be fixed to low level.	
XIN	Input	Barrata and the side	
XOUT	Output	Resonator connecting pin	
VAREF	D	De fined to book and	
VASS	Power supply	Be fixed to low level	

#### **Operational Description**

The following is an explanation of hardware configuration and operation in relation to the 47P840V. The 47P840V is the same as the 47C640/840 except that an EPROM or OTP is used instead of a built-in mask ROM.

#### 1. Operation mode

The 47P840V has an MCU mode and a PROM mode.

#### 1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C640/840, except that the TEST / VPP pin does not have built in pull-down resistor and cannot be used open.

#### 1.1.1 Program Memory

The program storage area is the same as for the 47C840. Data conversion tables must be set in two locations when using the 47P840V to check 47C640 operation.

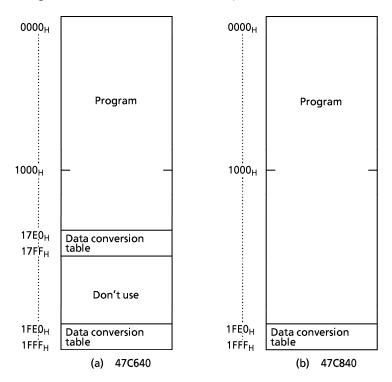


Figure 1-1. Program area

### 1.1.2 Data Memory

The 47P840V has  $512 \times 4$ -bit data memory bank (RAM).

When using the 47P840V as a 47C640 evaluator, do not write data to address  $80_H$  and following, even though the bank 1 addresses are 00 to  $FF_H$ . There is no necessity to take into consideration a special common function area because one is built in bank 0.

# 1.1.3 Input/Output Circuitry

# (1) Control pins

This is the same as for the 47C640/840 except that there is no built-in pull-down resistance for the TEST pin.

#### (2) I/O Ports

The input/output circuit of the 47P840V is the same as I/O code IA of the 47C640/840. External resistance, for example, is required when using as evaluator of other I/O codes (IB, IC), (Refer to Figure 1.2)



Figure 1-2. I/O code and external circuitry

#### 1.2 PROM mode

The PROM mode is set by setting the RESET and HOLD pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification. (A high-speed program mode is used set the ROM type the same as for the TMM 2764AD.)

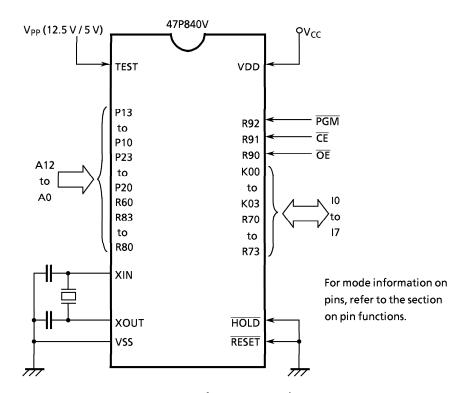


Figure 1-3. Setting for PROM mode

An adapter socket is available for connecting a PROM writer.

BM1171: TMP47P840VNBM1172: TMP47P840VF

# 1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5 V) is applied to the Vpp terminal with Vcc = 6 V and  $\overline{PGM} = V_{IH4}$ . The programming is achieved by applying a Single TTL low level 1 ms, pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

Start

Address = Start Address  $V_{CC} = 6 V$  $V_{pp} = 12.5 \text{ V}$ Yes Data = FF? N = 0Program 1 ms Pulse N = N + 1Yes N = 25? NG Verify? OK ) Over Program 3X Pulses of 1 ms or One Pulse of 3X ms Duration Verify? Address = Address + 1 ОК No Last Address? Yes  $V_{CC} = 5 V$  $V_{pp} = 5 V$ Read NG Fail All Byte? OK **Pass** Figure 1-4. Flow Chart

### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	$V_{DD}$		– 0.3 to 6.5	V
Program Voltage	$V_{PP}$	TEST / VPP pin	– 0.3 to 13.0	٧
Input Voltage	$V_{IN}$		$-0.3$ to $V_{DD} + 0.3$	٧
Output Voltage	V <sub>OUT</sub>		– 0.3 to V <sub>DD</sub> + 0.3	V
Output Current (per 1 pin)	I <sub>OUT1</sub>	Ports P1, P2	30	A
	I <sub>OUT2</sub>	Ports R4 to R9	3.2	mA
Output Currnent (Total)	Σ l <sub>OUT</sub>	Ports P1, P2	120	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating Conditions

$$(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$$

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
			fc = 6 MHz	4.5		
Consultable	.,		fc = 4.2 MHz	2.7		,,
Supply Voltage	$V_{DD}$		In the SLOW mode	2.7	5.5	V
			In the HOLD mode			
	V <sub>IH1</sub>	Except Hysteresis Input	V > 4 E V	$V_{DD} \times 0.7$		
	$V_{IH2}$	Hysteresis Input	$V_{DD} \ge 4.5 V$	$V_{DD} \times 0.75$	V <sub>DD</sub>	V
	V <sub>IH3</sub>		$V_{DD}$ < 4.5 V	$V_{DD} \times 0.9$		
	V <sub>IL1</sub>	Except Hysteresis Input	V > 4.5.V		$V_{DD} \times 0.3$	
Input Low Voltage	$V_{IL2}$	Hysteresis Input	$V_{DD} \ge 4.5 V$	0	$V_{DD} \times 0.25$	V
V <sub>IL3</sub>			$V_{DD}$ < 4.5 V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30	34	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage  $V_{IH3}$ ,  $V_{IL3}$ : In the SLOW or HOLD mode.

D.C. Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis Input		_	0.7	_	٧
lament Command	I <sub>IN1</sub>	KO, TEST, RESET, HOLD	V <sub>DD</sub> = 5.5 V,			± 2	
Input Current	I <sub>IN2</sub>	ports R (open drain)	V <sub>IN</sub> = 5.5 V / 0 V			= 2	μA
Input Resistance	R <sub>IN</sub>	RESET		100	220	450	kΩ
Output Leakage Current	I <sub>LO</sub>	sink open drain	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}$	_	_	2	μA
Output Level Low Voltage	V <sub>OL</sub>	Except Xout, ports P	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	_	0.4	V
Output Level Low Voltage	I <sub>OL</sub>	Ports P1, P2	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	_	20	_	mA
Supply Current (in the Normal mode)	I <sub>DD</sub>		V <sub>DD</sub> = 5.5 V, fc = 4 MHz	_	3	6	mA
Supply Current (in the SLOW mode)	I <sub>DDS</sub>		V <sub>DD</sub> = 3.0 V, fs = 32.768 kHz	_	30	60	μΑ
Supply Current (in the HOLD mode)	I <sub>DDH</sub>		V <sub>DD</sub> = 5.5 V	_	0.5	10	μΑ

Note 1: Typ. values show those at Topr = 25°C,  $V_{DD}$  = 5 V.

Note 2: Input Current  $I_{IN1}$ ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Supply Current  $I_{DD}$ ,  $I_{DDH}$ ;  $V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$ 

The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

Supply Current  $I_{DDS}$ ;  $V_{IN} = 2.8 \text{ V} / 0.2 \text{ V}$ 

Low frequency clock is only osillated (connecting XTIN, XTOUT).

A/D Conversion Characteristics

 $(Topr = -40 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Analog Reference Voltage	V <sub>AREF</sub>		V <sub>DD</sub> _ 1.5	_	V <sub>DD</sub>	
Analog Reference Voltage	V <sub>ASS</sub>		V <sub>SS</sub>	_	1.5	\ \
Analog Reference Voltage Range	$_{\Delta}V_{AREF}$	V <sub>AREF</sub> -V <sub>ASS</sub>	2.5	_	_	V
Analog Input Voltage	V <sub>AIN</sub>		V <sub>ASS</sub>	_	V <sub>AREF</sub>	V
Analog Supply Current	I <sub>REF</sub>		_	0.5	1.0	mA
Nonlinearity Error			_	_	± 1	
Zero Point Error		$V_{DD} = 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 1	l cp
Full Scale Error		$V_{AREF} = V_{DD} \pm 0.001 V$	_	_	± 1	LSB
Total Error		V <sub>ASS</sub> = 0.000 V	_	_	± 2	

A.C. Characteristics

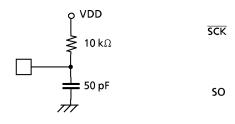
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, T_{opr} = -40 \text{ to } 70^{\circ}\text{C})$ 

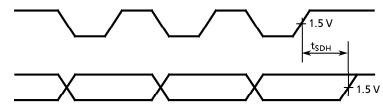
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Instruction Cycle Time	tau	In the Normal mode	1.33	_	20	
Instruction Cycle Time	tcy	In the SLOW mode	235	_	267	μS
High Level Clock pulse Width	t <sub>WCH</sub>	Fotom of the demands	00			
Low Level Clock pulse Width	t <sub>WCL</sub>	External clock mode	80	_	_	ns
A/D Sampling Time	t <sub>AIN</sub>	fc = 4 MHz	_	4	_	μs
Shift Data Hold Time	t <sub>SDH</sub>		0.5 tcy – 300	_	_	ns

Note: Shift data Hold time:

External circuit for SCK pin and SO pin

Serial port (completion of transmission)





**Recommended Oscillating Conditions** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, Topr = -40 \text{ to } 70^{\circ}\text{C})$ 

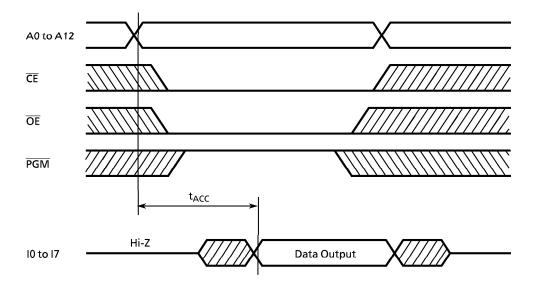
Recommended oscillating conditions of the 47P840V are equal to the 47C840's.

D.C./A.C. Characteristics

 $(V_{SS} = 0 V)$ 

# (1) Read Operation

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Output Level High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	_	V <sub>CC</sub>	\
Output Level Low Voltage	V <sub>IL4</sub>		0	_	V <sub>CC</sub> × 0.3	>
Supply Voltage	V <sub>CC</sub>		4.75		6.0	V
Programming Voltage	V <sub>PP</sub>		4.75	_	6.0	v
Address Access Time	t <sub>ACC</sub>	V <sub>CC</sub> = 5.0 ± 0.25 V	0	-	350	ns



# (2) High Speed Programming Operation

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Input High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	-	V <sub>CC</sub>	٧
Input Low Voltage	V <sub>IL4</sub>		0	_	V <sub>CC</sub> × 0.3	٧
Supply Voltage	V <sub>CC</sub>		4.75	_	6.0	٧
V <sub>PP</sub> Power Supply Voltage	V <sub>PP</sub>		12.25	12.50	12.75	٧
Programming Pulse Width	t <sub>PW</sub>	V <sub>CC</sub> = 6.0 ± 0.25 V	0.95	1.0	1.05	ms

