Z8001/Z8002 CPU

LH8001/LH8002

Central Processing Unit

Features

- Regular, easy-to-use architecture.
- Instruction set more powerful than many minicomputers.
- Directly addresses 8M bytes.
- Eight user-selectable addressing modes.
- Seven data types that range from bits to 32-bit long words and word strings.
- System and normal operating modes; separate code, data and stack spaces.
- Sophisticated interrupt structure.
- Resource-sharing capabilities for multiprocessing systems.
- Multi-programming and compiler support.
- Memory management and protection provided by Z8010 Memory Management Unit.
- 32-bit operations, including signed multiply and divide.
- Z-Bus compatible.

Description

The Z8000 is an advanced high-end 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing systems. Essentially a monolithic minicomputer central processing unit, the Z8000 CPU is characterized by an instruction set more powerful than many minicomputers; resources abundant in registers, data types, addressing modes and addressing range; and a regular architecture that enhances throughput by avoiding critical bottlenecks such as implied or dedicated registers.

CPU resources include sixteen 16-bit general-purpose registers, seven data types that range from bits to 32-bit long words and word strings, and eight user-selectable addressing modes. The 110 distinct instruction types can be combined with the various data types and addressing modes to form a powerful set of 414 instructions. Moreover, the instruction set exhibits a high degree of regularity: most instructions can use any of the five main addressing modes and can operate on byte, word and long-word data types.

The CPU can operate in either system or normal modes. The distinction between these two modes permits privileged operations, thereby improving operating system organization and implementation. Multiprogramming is supported by the "atomic" Test and Set instruction; multiprocessing by a combination of instruction and hardware features; and compilers by multiple stacks, special instructions and addressing modes.

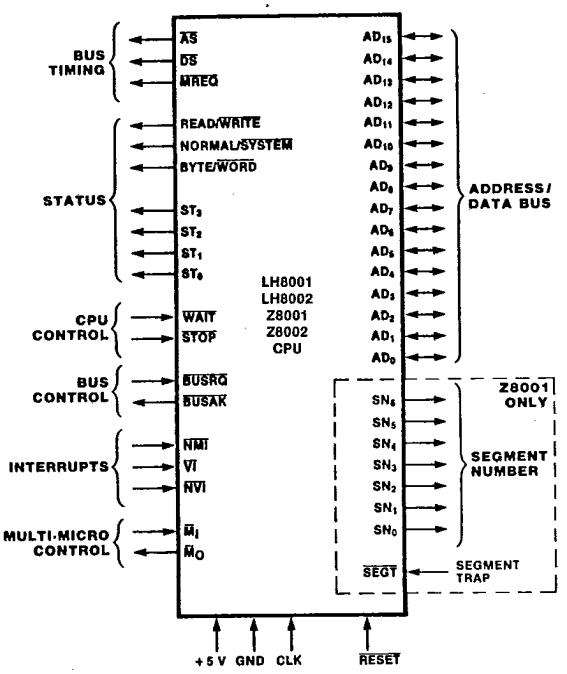

Figure 1. Pin Functions

Description (Continued)

The Z8000 CPU is offered in two versions: the Z8001 48-pin segmented CPU and the Z8002 40-pin non-segmented CPU. The main difference between the two is in addressing range. The Z8001 can directly address 8M bytes of memory; the Z8002 directly addresses 64K bytes. The two operating modes—system and normal—and the distinction between code, data and stack spaces within each mode allows memory extension up to 48M bytes for the Z8001 and 384K bytes for the Z8002.

To meet the requirements of complex, memory-intensive applications, a companion memory-management device is offered for the Z8001. The Z8010 Memory Management Unit manages the large address space by providing features such as segment relocation and memory protection. The Z8001 can be used with or without the Z8010. If used by itself, the Z8001 still provides an 8M byte direct addressing range, extendable to 48M bytes.

Register Organization. The Z8000 CPU is a register-oriented machine that has sixteen 16-bit general-purpose registers. The Z8002 CPU has one stack pointer register, and the Z8001 has two.

Stacks. The Z8001 and Z8002 can use stacks located anywhere in memory. Two implied stack pointers are available: the system stack pointer and the normal stack pointer.

Refresh. The Z8000 CPU contains a counter that can be used to refresh dynamic memory automatically.

Program Status Registers. This group of status registers contains the program counter, flags, and control bits. These are automatically saved when an interrupt or trap occurs, and a new status group is loaded.

Interrupt and Trap Structure. The CPU supports three types of interrupts: vectored and nonvectored maskable, and nonmaskable. There are four traps: system call, unimplemented instruction, privileged instruction, and segmentation trap.

Data Types. Z8000 instructions can operate on bits, BCD digits (4 bits), bytes (8 bits), words (16 bits), long words (32 bits), byte strings and word strings up to 64K bytes long.

Segmentation and Memory Management. The Z8001 can directly access 8M bytes of address space, using a segmented addressing scheme, implemented via the Z8010 MMU Memory Management Unit. The 8M bytes of Z8001 address space is divided into 128 relocatable segments of up to 64K bytes each. The addresses entered into instructions and output by the CPU in executing them are *logical* addresses. The MMU translates these logical addresses into addresses in physical memory. This process—relocation—is transparent to the user software.

Addressing Modes. Eight addressing modes are provided in the instruction set: Register (R), Immediate (IM), Indirect Register (IR), Direct Address (DA), Indexed (X), Relative Address (RA), Base Address (BA), and Base Indexed (BX).

Input/Output. A set of I/O instructions performs 8-bit or 16-bit transfers between CPU and I/O devices.

Multimicroprocessor Support. A pair of CPU pins is used in conjunction with certain instructions to coordinate multiple microprocessors.

Instruction Set. The Z8000 has in its repertoire the nine categories of instructions following:

- Load and exchange
- Arithmetic
- Logic
- Program control
- Bit manipulation
- Rotate and shift
- Block transfer and string manipulation
- Input/output
- CPU control

Status Lines. Seven pins of the Z8000 are dedicated to the issuance of status information. Three are the function select lines Read/Write, Normal/System, and Byte/Word. The other four lines (ST_0-ST_3) issue codes denoting type of operation (program or I/O reference, data or stack memory request, or internal operation), acknowledging external requests (segment trap or interrupt), and initiating memory refresh cycles.

Pin Description

AD_0-AD_{15}. *Address/Data* (inputs/outputs, active High, 3-state). These multiplexed address and data lines are used both for I/O and to address memory.

$\overline{AS}$. *Address Strobe* (output, active Low, 3-state). The rising edge of $\overline{AS}$ indicates addresses are valid.

$\overline{BUSACK}$. *Bus Acknowledge* (output, active Low). A Low on this line indicates the CPU has relinquished control of the bus.

$\overline{BUSREQ}$. *Bus Request* (input, active Low). This line must be driven Low to request the bus from the CPU.

$\overline{DS}$. *Data Strobe* (output, active Low, 3-state). This line times the data in and out of the CPU.

$\overline{MREQ}$. *Memory Request* (output, active Low, 3-state). A Low on this line indicates that the address/data bus holds a memory address.

$\overline{M}_I$, $\overline{M}_O$. *Multi-Micro In, Multi-Micro Out* (input and output, active Low). These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource.

$\overline{NMI}$. *Non-Maskable Interrupt* (edge triggered, input, active Low). A high-to-low transition on $\overline{NMI}$ requests a non-maskable interrupt. The NMI interrupt has the highest priority of the three types of interrupts.

$\overline{NVI}$. *Non-Vectored Interrupt* (input, active Low). A Low on this line requests a non-vectored interrupt.

CLK. *System Clock* (input). CLK is a 5V single-phase time-base input.

$\overline{RESET}$. *Reset* (input, active Low). A Low on this line resets the CPU.

R/$\overline{W}$. *Read/Write* (output, Low = Write, 3-state). R/$\overline{W}$ indicates that the CPU is reading from or writing to memory or I/O.

SN_0-SN_6. *Segment Number* (outputs, active High, 3-state). These lines provide the 7-bit segment number used to address one of 128 segments by the Z8010 Memory Management Unit. Output by the Z8001 only.

$\overline{SEGT}$. *Segment Trap* (input, active Low). The Memory Management Unit interrupts the CPU with a Low on this line when the MMU detects a segmentation trap.

ST_0-ST_3. *Status* (outputs, active High, 3-state). These lines specify the CPU status (see table).

$\overline{STOP}$. *Stop* (input, active Low). This input can be used to single-step instruction execution.

$\overline{VI}$. *Vectored Interrupt* (input, active Low). A Low on this line requests a vectored interrupt.

$\overline{WAIT}$. *Wait* (input, active Low). This line indicates to the CPU that the memory or I/O device is not ready for data transfer.

B/$\overline{W}$. *Byte/Word* (output, Low = Word, 3-state). This signal defines the type of memory reference on the 16-bit address/data bus.

N/$\overline{S}$. *Normal/System Mode* (output, Low = System Mode, 3-state). N/$\overline{S}$ indicates the CPU is in the normal or system mode.

Reserved. Do not connect.

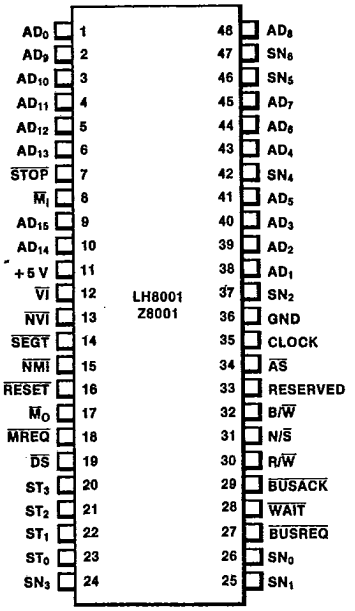

Figure 2. Z8001 Pin Assignments

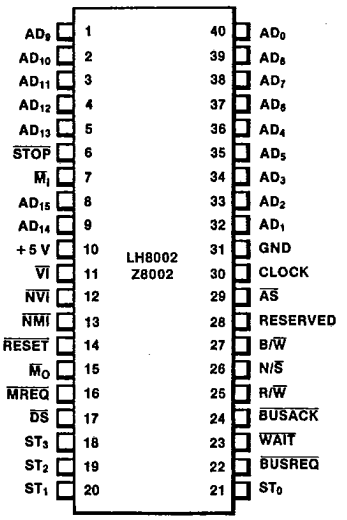

Figure 3. Z8002 Pin Assenments