*Multi*GEN™ GF9101 High Performance Multirate Digital Filter

DATA SHEET

GF9101

FEATURES

- **highly optimized & flexible architecture for multirate FIR filtering applications**
- **implements dual 12 tap filters operating at 40 MHz or single 23 or 24 tap filter operating at 20 MHz maximum data rate**
- **stores up to 108 fully-programmable 12 tap filters with 12 bit coefficients at each tap, dynamically addressable in each clock cycle**
- **3 flexible memory loading modes**
- **20 bit pipeline for cascading up to 3 devices**
- **20 bit output accumulator**
- **filter output negate and zero controls**
- **supports both symmetrical and asymmetrical FIR filters**
- **40 MHz maximum computation and input/output data rates**

APPLICATIONS

Video rate conversion; High performance FIR filters; Adaptive digital filters; Video encoding; Digital modulation

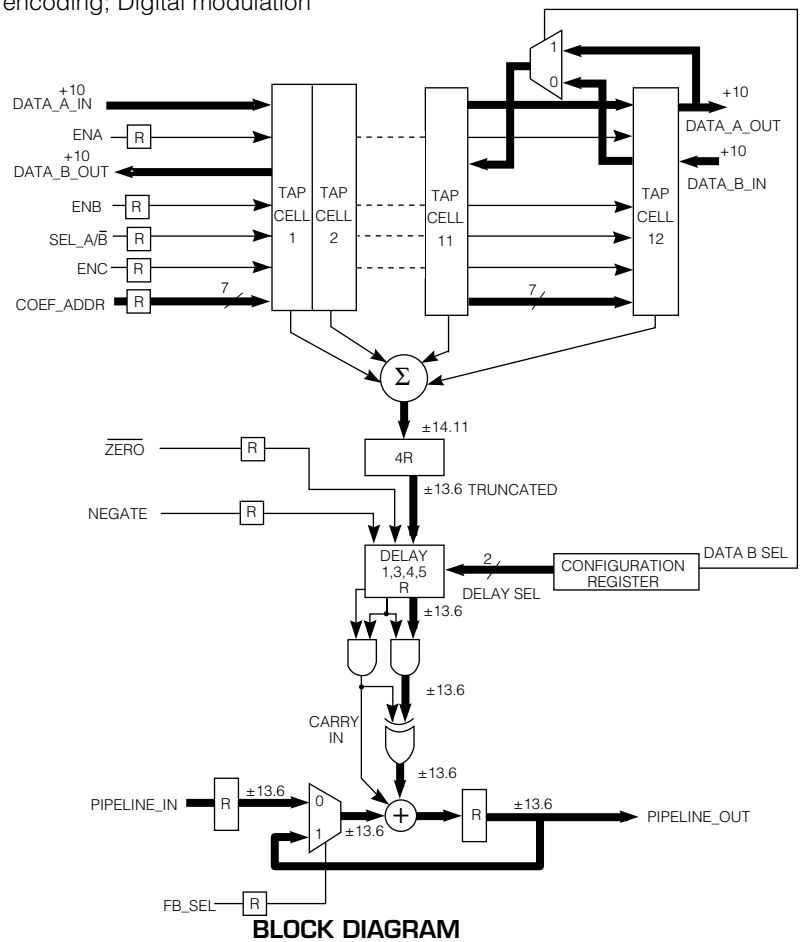
DESCRIPTION

The GF9101 is a high performance multirate digital filter which can be programmed to implement a wide range of signal processing functions using both symmetrical and asymmetrical filter structures. It is composed of a 12-tap FIR filter with internal RAM to hold up to 108 individual filters. An externally controlled address bus selects one of the 108 filters in each clock cycle. Pipelined architecture allows cascading of up to three devices with no additional hardware.

Two 10-bit input shift registers are provided for multiplexed filtering applications. The 12-bit coefficients can be programmed in serial, high speed parallel or microprocessor modes. In the high speed parallel mode, any one of the 108 filters can be reprogrammed in 18 clock cycles.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GF9101 - CMQ	160 pin Metal Quad	0° to 70°C



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
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I/O DESCRIPTION

SYMBOL	PIN NO.	TYPE	DESCRIPTION
V_{DD}	1, 10, 20, 29, 40, 41, 59, 69, 80, 81, 90, 99, 109, 120, 121, 129, 140, 150, 160		+5 V power supply pins. 0.1μF capacitors between the V_{CC} and GND pins are recommended.
GND	3, 6, 8, 19, 33, 36, 39, 46, 49, 60, 73, 76, 79, 83, 86, 88, 100, 113, 116, 119, 122, 125, 139, 153, 155, 159		Device ground.
CLK_IN	138	I	System clock. All inputs except for CONFIGURE, and all internal registers are clocked on the rising edge of CLK_IN.
DATA_A_IN (9-0)	127, 128, 130-137	I	Input data to registers A0 - A11. 9 bit signed or 10 bit unsigned data.
DATA_B_IN (9-0)	141-149, 151	I	Input data to registers B11 - B0. 9 bit signed or 10 bit unsigned data.
ENA	23	I	Shift enable for A0 - A11. Enables shifting of A registers when high.
ENB	24	I	Shift enable for B0 - B11. Enables shifting of B registers when high.
ENC	25	I	Enable for C0-C11. Enables C registers when high. The C registers transfer data from either the A or B registers depending on the state of SEL_A/$\overline{B}$.
SEL_A/$\overline{B}$	22	I	Selects A or B registers. Selects registers A when high or registers B when low to be transferred to the C registers.
COEF_DATA (7-0)	96-98, 101-105	I	Data bus for coefficients and configuration register: a) Parallel and microprocessor loading modes : COEF_DATA (7-0) is used to load 8 bit data into internal RAM. b) Serial Loading mode: COEF_DATA (7) is used to serially load the internal RAM. c) Configuration mode: COEF_DATA (6-0) are inputs to the CONFIGURATION register.
COEF_ADDR (9-0)	78, 77, 75, 74, 72, 47, 45-42	I	Address bus for internal RAM (address 0 —> 107): a) Run mode: COEF_ADDR (6-0) selects one of the 108 sets of 12 coefficients in the internal RAM. b) Parallel and micro-processor loading modes: Selects the internal RAM address for the 8-bit data loading COEF_DATA (7-0).
$\overline{\text{COEF\_WR}}$	17	I	Enable for COEF_DATA (7-0). $\overline{\text{LOAD\_EN}}$ must be enabled for $\overline{\text{COEF\_WR}}$ to work: a) Parallel and micro-processor loading modes : Enables COEF_DATA (7-0) registers or loading 8 bit data in internal RAM. b) Serial Loading mode: On a high to low transition, a one bit data gets clocked in to the internal RAM through COEF_DATA bit 7.
$\overline{\text{LOAD\_EN}}$	18	I	Used during loading mode. This signal selects a particular GF9101 device when 2 or more share the same bus for loading. The particular GF9101 device is selected when set low. $\overline{\text{LOAD\_EN}}$ must be enabled for $\overline{\text{COEF\_WR}}$. For a single GF9101 using the serial loading, this pin can be set low.
NEGATE	126	I	This signal negates the filter sum before it enters the pipelined output section when high.
$\overline{\text{ZERO}}$	123	I	Zeros filter sum before it enters the pipelined output section when low.
FB_SEL	124	I	Feedback select. Selects data in PIPELINE_IN when low or filter sum in PIPELINE_OUT when high to the input of the output accumulator.

I/O DESCRIPTION

SYMBOL	PIN NO.	TYPE	DESCRIPTION
CONFIGURE	21	I	GF9101 reset/configure. Resets the GF9101 when high for at least one clock period. Loads COEF_DATA (6-0) into the CONFIGURATION register on a high to low transition. This bit is set low in run mode. When CONFIGURE is high, the GF9101 is reset but the values in the internal RAM and registers in the run mode sections are not altered. This means that the GF9101 may be reconfigured after the internal RAM has been loaded.
PIPELINE_IN (19-0)	38,37, 35, 34, 32-30, 28-26, 15-11, 9, 7, 5, 4, 2	I	Pipeline input. Input to the output accumulator when FB_SEL is low.
DATA_A_OUT (9-0)	71, 70, 68-61	O	Output data from register A11.
DATA_B_OUT (9-0)	58-50, 48	O	Output data from register B0.
PIPELINE_OUT (19-0)	82, 84, 85, 87, 89, 91-95, 106-108, 110-112, 114, 115, 117, 118	O	Pipeline output. Output of the accumulator or PIPELINE_IN depending on FB_SEL.
S_LOAD_CMP	16	O	Serial loading complete. a) Serial loading mode: When high, indicates that all the internal RAM has been loaded.
SCAN_IN, SCAN_EN	157, 156		Set low.
TEST	158		Set high.
POUT, SCANOUT	152, 154		No Connect.

Note: All unused inputs of the GF9101 should be connected to GND

GF9101 OPERATION

The GF9101 has two operating modes: the load mode and the run mode. In the load mode, the coefficients for the filters are written to the internal RAM. In the run mode, the GF9101 is used to filter signals.

Before the GF9101 can filter signals, two steps must be performed:

1. CONFIGURATION - is accomplished by writing one 7 bit word into the CONFIGURATION REGISTER. This register holds static operating parameters that affect both the load mode and the run mode.
2. MEMORY LOADING - is done after configuration. The internal RAM must be loaded with at least one of the 108 filter coefficient sets before signals can be processed.

CONFIGURATION

The GF9101 is reset by holding CONFIGURE high for at least one clock cycle. Configuration occurs upon a high to low transition on the CONFIGURE pin. This transition registers COEF_DATA (6-0) into the CONFIGURATION REGISTER. Table 1 shows the meaning of each bit in the CONFIGURATION REGISTER.

When CONFIGURE is high, the GF9101 is reset but the values in the internal RAM and registers in the run mode sections are not altered. This means that the GF9101 may be reconfigured after the internal RAM has been loaded.

MEMORY LOADING

The GF9101 contains 12 tap cells with 108 12-bit memory locations for each tap. When loading the memory, the tap cells must be viewed as 6 memory banks with 108 24-bit memory locations in each bank. Each memory bank is assigned to a pair of tap cells as shown in Table 2.

During configuration, either the parallel, microprocessor, or serial loading is selected. When in the load mode, the memory outputs are undefined. Please refer to the GF9101 block diagram and notice that, even though the memory outputs are undefined, several valid outputs may be in the processing section below the multipliers and can exit the GF9101 correctly. This would be useful for adaptive filtering where the tap memories can be changed while the GF9101 outputs are still valid. During power up, the internal RAM of the GF9101 is in a random state, and is not intialized to zero.

TABLE 1: Configuration Register Format

CONFIGURATION REGISTER BIT COEF_DATA(6-0)	MEANING	
0	MODE A (1 if A input signed, 0 if unsigned)	
1	MODE B (1 if B input signed, 0 if unsigned)	
3, 2	DELAY_SEL selects delay for pipelining:	
	Bits 3, 2	Delay in CLK_IN cycles
	0, 0	1
	0, 1	3
	1, 0	4
	1, 1	5
4	DATA_B_SEL 0 selects B12 for two 12 tap filters or one 24 tap filter by externally connecting DATA_A_OUT to DATA_B_IN. DATA_B_SEL 1 selects A12 for a 23 tap filter.	
6,5	LOAD MODE SELECT (see below)	
	Bits 6, 5	Loading mode
	0, 0	Serial
	0, 1	Parallel
	1, 0	Microprocessor
	1, 1	Reserved

TABLE 2: Memory Locations for Internal RAM

MEMORY BANKS (BITS)	TAPS (BITS)
0 (23-12)	0 (11-0)
0 (11-0)	2 (11-0)
1 (23-12)	3 (11-0)
1 (11-0)	4 (11-0)
2 (23-12)	5 (11-0
2 (11-0)	6 (11-0)
3 (23-12)	7 (11-0)
3 (11-0)	8 (11-0)
4 (23-12)	9 (11-0)
4 (11-0)	10 (11-0)
5 (23-12)	11 (11-0)
5 (11-0)	12 (11-0)

PARALLEL LOADING

If parallel loading is selected, both the $\overline{\text{COEF\_WR}}$ pin and the $\overline{\text{LOAD\_EN}}$ pin determine whether the GF9101 is in the load mode. When $\overline{\text{COEF\_WR}}$ and $\overline{\text{LOAD\_EN}}$ are both low, the load mode is selected, the run mode is disabled, and writes to memory can occur. Parallel loading is random access and synchronous.

Data is written through COEF_DATA (7-0) and its destination is determined by COEF_ADDR (9-0). Coefficient memory is loaded by writing 8 bits at a time, first to two temporary registers (bits 15 -0) and finally to the desired memory bank (bits 23-0). Each memory bank word is loaded in three clock cycles. COEF_ADDR (9-7) defines the address location for temporary registers (TEMP_REG_A and TEMP_REG_B) and memory banks. COEF_ADDR (6-0) determines the filter coefficient address (0 -107) in the internal RAM. COEF_ADDR (6-0) must be less than 108. In Table 3, COEF_ADDR (9-7) determines the following:

TABLE 3: Temporary Loading Registers and Memory Banks

COEF_ADDR(9-7) (binary)	DESTINATION	NUMBER OF BITS
111	TEMP_REG_B	8 (15-8)
110	TEMP_REG_A	8 (7-0)
101	MB5[1]	24 (23-0)
100	MB4	24 (23-0)
011	MB3	24 (23-0)
010	MB2	24 (23-0)
001	MB1	24 (23-0)
000	MB0	24 (23-0)

NOTE 1: Memory Bank No. 5

TEMP_REG_A and TEMP_REG_B temporarily hold memory bits, (7-0) and (15-8) respectively. Three 8 bit writes are necessary to write one 24-bit memory as follows:

1. Load COEF_DATA (7-0) into TEMP_REG_A
2. Load COEF_DATA (7-0) into TEMP_REG_B
3. Load COEF_DATA (7-0), TEMP_REG_B (7-0), and TEMP_REG_A (7-0) into the selected memory bank, MB0-MB5 (23-0).

While COEF_ADDR (9-7) selects MB0-MB5 for writing, COEF_ADDR (6-0) selects the memory bank location that the 24-bit word is written into. Parallel loading is synchronous with CLK_IN. When $\overline{\text{COEF\_WR}}$ and $\overline{\text{LOAD\_EN}}$ are both low, 8-bit words will be written on the rising edge of CLK_IN. Consecutive writes may be done indefinitely by keeping $\overline{\text{COEF\_WR}}$ and $\overline{\text{LOAD\_EN}}$ low. A parallel loading timing diagram is shown in Figure 1.

The timing diagram shown in Figure 1 loads the memories shown in Table 4:

TABLE 4: Memory Loaded into Internal RAM in Parallel Load Mode

TAP (location)	12-bit WORD IN HEX.	MEMORY BANK
1 (0)	FB2	MB0
2 (0)	EF4	MB0
11 (107)	CCC	MB5
12 (107)	DDD	MB5

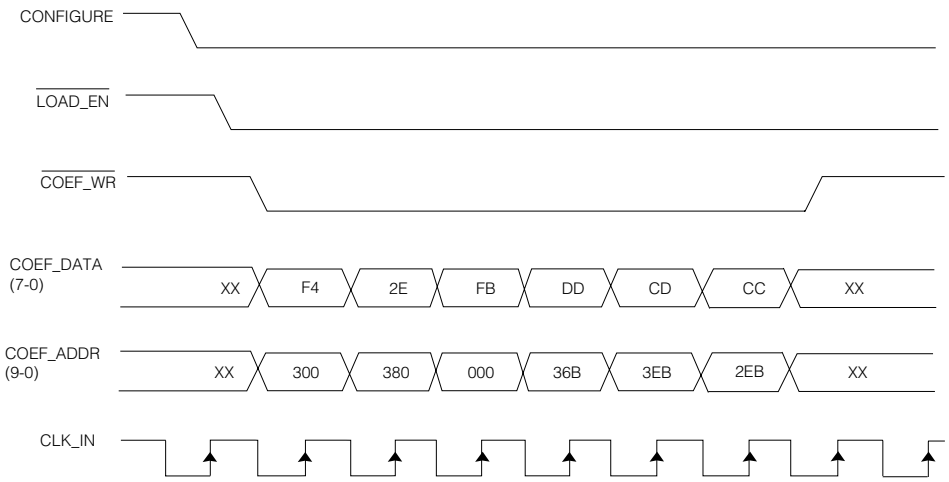


Fig. 1 Parallel Loading Timing Diagram

The address generated is shown in Table 5.

Timing for the parallel loading signals is the same as that for other synchronous inputs.

TABLE 5: Address Generation for Parallel Loading Example

DESTINATION	COEF_ADDR (9-7) IN BINARY	COEF_ADDR (6-0) IN HEX	COEF_ADDR (9-0) IN HEX
TEMP_REG_A	110	X	300
TEMP_REG_B	111	X	380
MB0	000	0	000
TEMP_REG_A	110	X	36B or 300
TEMP_REG_B	111	X	3EB or 380
MB5	101	6B	2EB

MICROPROCESSOR LOADING

If microprocessor loading is selected, the $\overline{\text{LOAD\_EN}}$ pin alone determines the run mode or the load mode. When $\overline{\text{LOAD\_EN}}$ is low, the load mode is selected, the run mode is disabled, but a write will not occur until $\overline{\text{COEF\_WR}}$ is low.

Microprocessor loading is random access and asynchronous. Like parallel loading, microprocessor loading uses COEF_DATA (7-0) and COEF_ADDR (9-0) to write three 8-bit words for each 24-bit memory written. Addressing is the same as for parallel loading. In microprocessor mode, at least one set of filter coefficients

need to be loaded into the internal RAM. If location 0 is used for filtering, MB0 > MB5 must be loaded for this location. The example shown in Figure 2 loads the value BB_H into TEMP_REG_A.

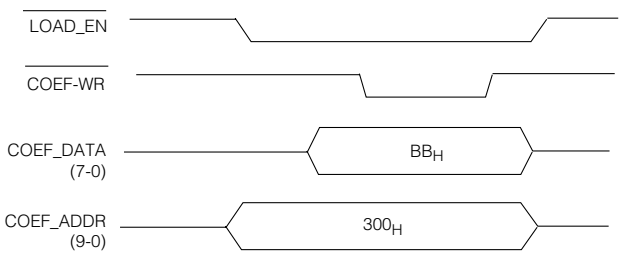


Fig. 2 Microprocessor Loading Timing Diagram

SERIAL LOADING

Serial loading is sequential and synchronous. If serial loading is selected the GF9101 will not enter the run mode until the entire serial load sequence is completed at which time the S_LOAD_CMP signal will go high. A bit will be written each time $\overline{\text{LOAD\_EN}}$ is low and $\overline{\text{COEF\_WR}}$ makes a high to low transition. Once the GF9101 is configured for serial loading, 24 x 108 x 6 =15552 bits must be written before the run mode is entered automatically. The 15552 bits must be entered in the order defined in Table 6. MB0 is loaded first from RAM location 0 starting to fill the first 12 bits of tap 2. MB5 RAM location 107, tap 11 is loaded last.

When the serial load sequence is completed, S_LOAD_CMP will go high and the run mode will be active. Below is a serial loading timing diagram. This example shows the serial loading start-up sequence. Notice that the falling edge of $\overline{\text{COEF\_WR}}$ is used to register the serial data. The frequency of $\overline{\text{COEF\_WR}}$ should be ≤1/4 CLK_IN frequency.

TABLE 6: Serial Mode Loading Order

Memory Bank 0		Memory Bank 1		.....	Memory Bank 5		Ram Location
TAP 2	TAP 1	TAP4	TAP 3	.....	TAP12	TAP 11	
1,2,3 12	13 24	2593 2617			5185 5208		
0,1,2 11	0 11	0 11	0 11		0 11	0 11	0
25 48		2618 2642			5209 5233		
0 11	0 11	0 11	0 11	.....	0 11	0 11	1
⋮	⋮	⋮	⋮		⋮	⋮	⋮
2568 2592		5160 5184			15528 15552		
0,1,2 11	0 11	0 11	0 11	.....	0 11	0 11	107

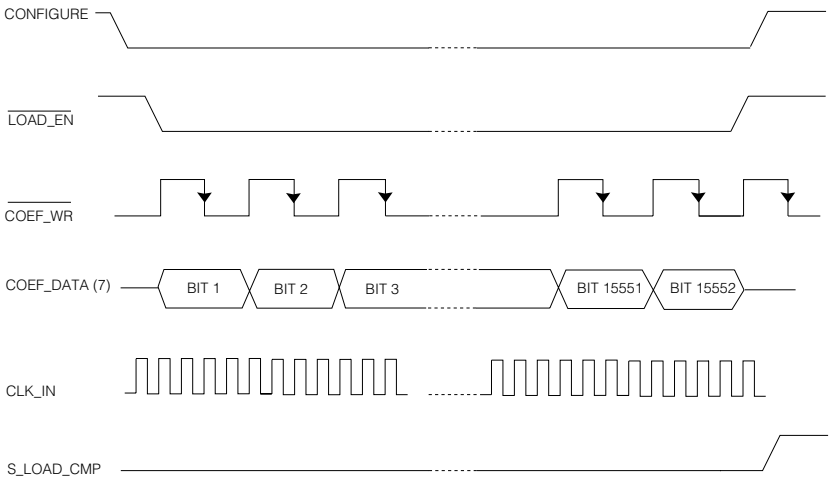


Fig. 3 Serial Mode Timing Diagram

FILTER ARCHITECTURE

For the following discussion on filter architecture, refer to the GF9101 Block Diagram and Figure 4.

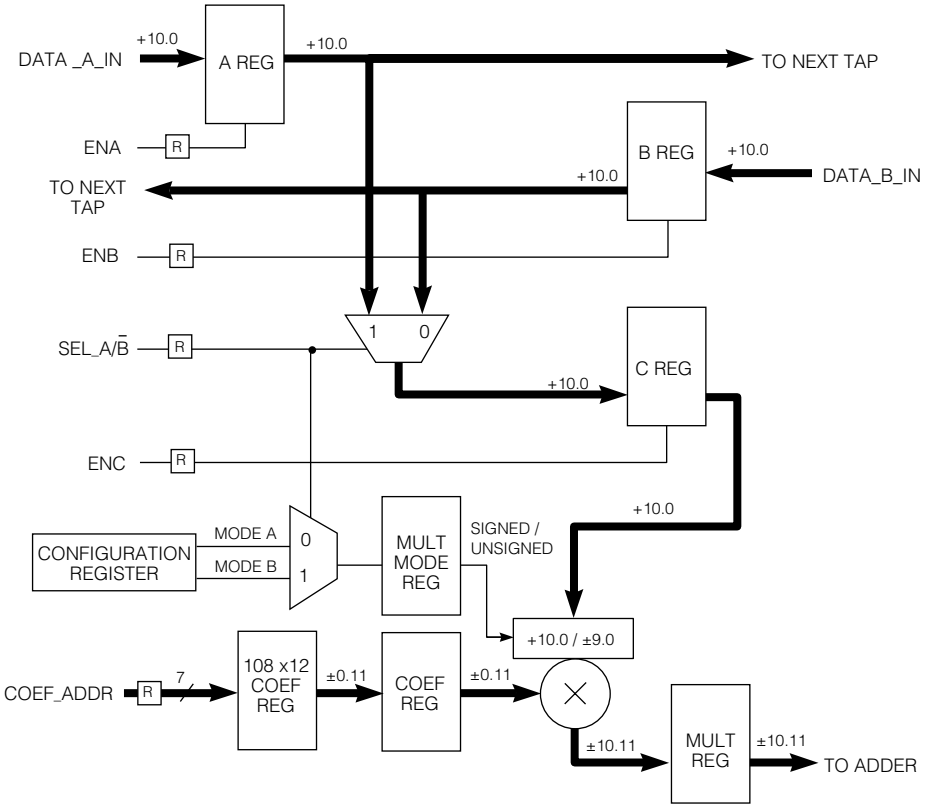


Fig. 4 Tap Cell (1-12)

COEFFICIENT MULTIPLICATION AND ADDITION STAGE

Two shift registers, A and B, are used to shift input data through the GF9101. Notice that if DATA_B_SEL was set low during configuration, data applied at DATA_A_IN enters at tap 1 and exits from tap 12, while data applied at DATA_B_IN enters at tap 12 and exits from tap 1. This gives two 12 tap filters. If DATA_B_SEL was set high during configuration, data applied at DATA_A_IN enters at tap 1, reverses direction at tap 12 (bypasses REG_12B) and exits from tap 1 on DATA_B_OUT, while DATA_B_IN is disabled. This gives a 23 tap filter. ENA and ENB control the shifting of the input data. The C register holds the next set of 12 input values to be applied to the multipliers.

If ENC is high, SEL_A/$\overline{B}$, determines whether the A or B shift register data enters the C register. SEL_A/$\overline{B}$, also determines whether the MODE A or MODE B control signal enters the MULT_MODE register. The value in the MULT_MODE register determineswhether theinputdatato themultiplierisrecognized as signed or unsigned. MODE A and MODE B are separate, static control signals which determine signed/unsigned for A or B input data respectively. They are common to all taps. When using the GF9101 as a 23 or 24 tap filter (combiningREG_A and REG_B to get a single filter output), MODE A and MODE B should be in the same state. If not, a signed/unsigned mismatch will occur. One needs to be cautious while using the GF9101 as two separate filters with MODE A and MODE B not in the same state (data entering REG_A is signed/ unsigned while in REG_B it is the opposite of REG_A) . If ENC is low and SEL_A/$\overline{B}$, changes state, a signed/unsigned mismatch will occur. To avoid an error under these circumstances, always make ENC high after a SEL_A/$\overline{B}$, state change.

The input values in the C register are multiplied by the coefficient values in the COEF register and the result enters an adder tree . The coefficients that enter the COEF register are stored in the internal RAM and are selected by the externally controlled COEF_ADDR (6-0) bus, which is common to all taps. At the output of the adder tree is the untruncated sum of taps 1 through 12.

This sum is then truncated as shown in the GF9101 Block diagram. The sum then passes through a variable delay along with the $\overline{\text{ZERO}}$ and NEGATE signals. The variable delay is provided so that complementary sums from cascaded GF9101's may be added together in the pipelined output stage. The $\overline{\text{ZERO}}$ signal zeros the sum and the NEGATE signal negates the sum.

PIPELINE_IN, PIPELINE_OUT STAGE

The calculated filter sum from the adder tree and delay enters into the pipelined output stage. Figure 5 shows the block diagram for the pipelined structure. FB_SEL determines whether the sum is added to the current PIPELINE_OUT or the registered PIPELINE_IN. The result is then registered at PIPELINE_OUT. When using one GF9101, this configuration can be used to add two partial filter sums from the A and B registers. Another application would be to use the PIPELINE_IN port for adding DC offset or SYNC and BURST signals (i.e. for 4:2:2 to $4f_{SC}$ rate conversion). This can be achieved by clocking in the SYNC and BURST signals from an external PROM connected to the PIPELINE_IN.

By connecting PIPELINE_OUT of one GF9101 device to PIPELINE_IN of another, up to three GF9101's may be cascaded to form larger filters.

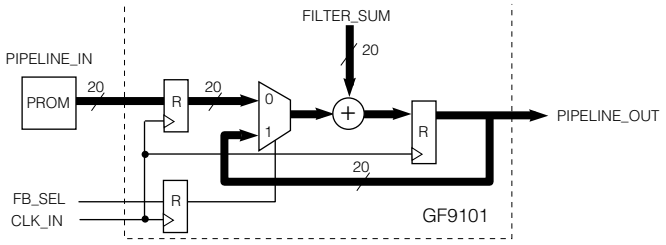


Fig. 5 Block Diagram for Pipelined Output Stage

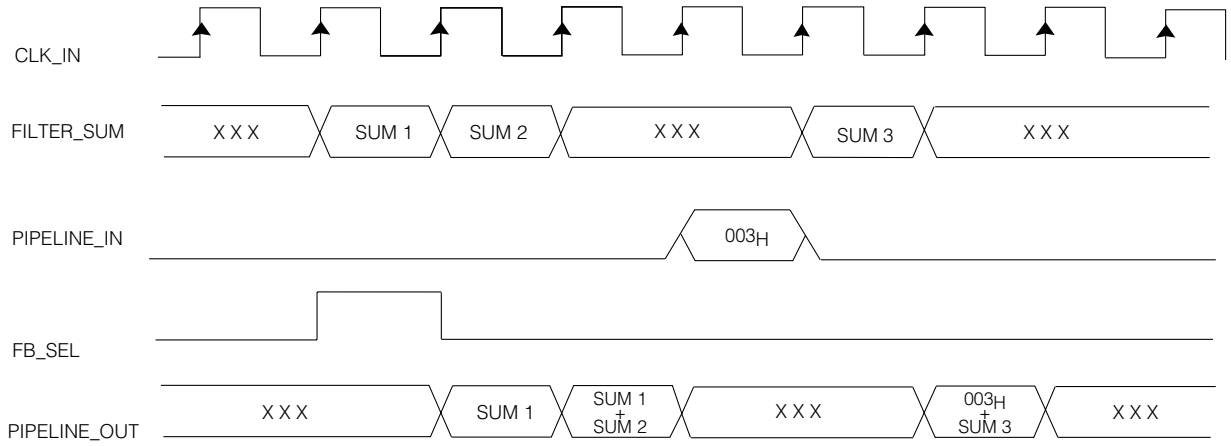


Fig. 6 Timing Diagram for the Pipelined Output Stage

APPLICATION NOTES

Video applications for the GF9101 include video rate conversion and high performance FIR filters. The following section presents a number of examples which show odd and even symmetric and asymmetric filters.

ODD-TAP SYMMETRIC FILTER

The GF9101 can be configured as an Odd-tap symmetric filter. A 23-tap odd-symmetric filter using one GF9101 will be discussed. For an odd-tap symmetric filter, the configuration word is shown in Table 7.

The maximum data rate using this filter configuration is 20 MHz, where the filter is clocked at twice the data rate of 40 MHz, the frequency of CLK_IN. The filter has input data A_n and filter data coefficients Cn (C0 —> C11) as shown in Figure 7. The input enters the filter at DATA_A_IN and exits the filter from DATA_B_OUT. The coefficient C11 is only multiplied by the data in reg. A_12 and reg.B_12 is bypassed. The data is shifted into the register by clocking ENA and ENB at the same time at half the CLK_IN frequency. The filter timing is shown in Figure 8.

TABLE 7: Configuration Word for an Odd-Tap Symmetric Filter

BIT NO.	CONFIGURATION WORD	DESCRIPTION
0	1	Data A and B are both signed data[2]
1	1	
2	0	One register delay
3	0	
4	1	23-tap filter, bypass reg. B_12
5	X	Depending on loading mode.
6	X	(See Table 1)

NOTE:

2: Bits 0 and 1 should have the same value for a 23 or 24 tap filter.

TABLE 8: Internal RAM Addresses and Contents

COEF_ADDR (6-0)	MEMORY CONTENTS
00_H	12 coefficients, for tap 1—> tap 12

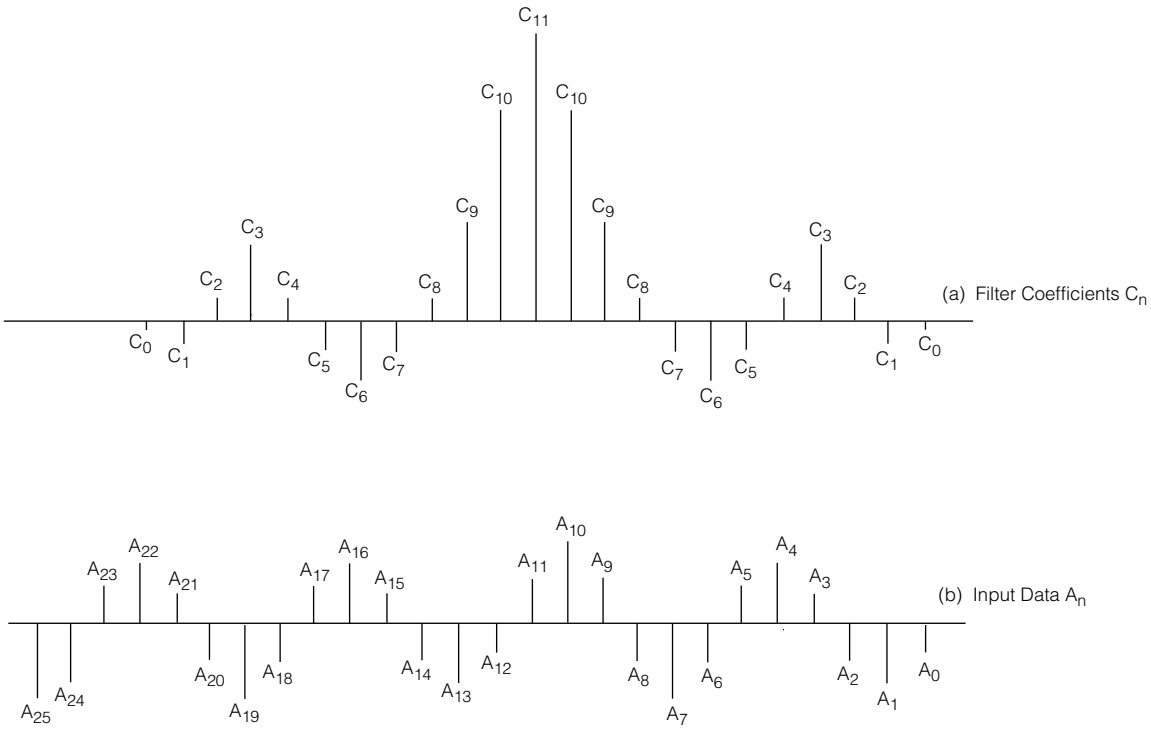


Fig. 7 Input Data A_n and Coefficients C_n

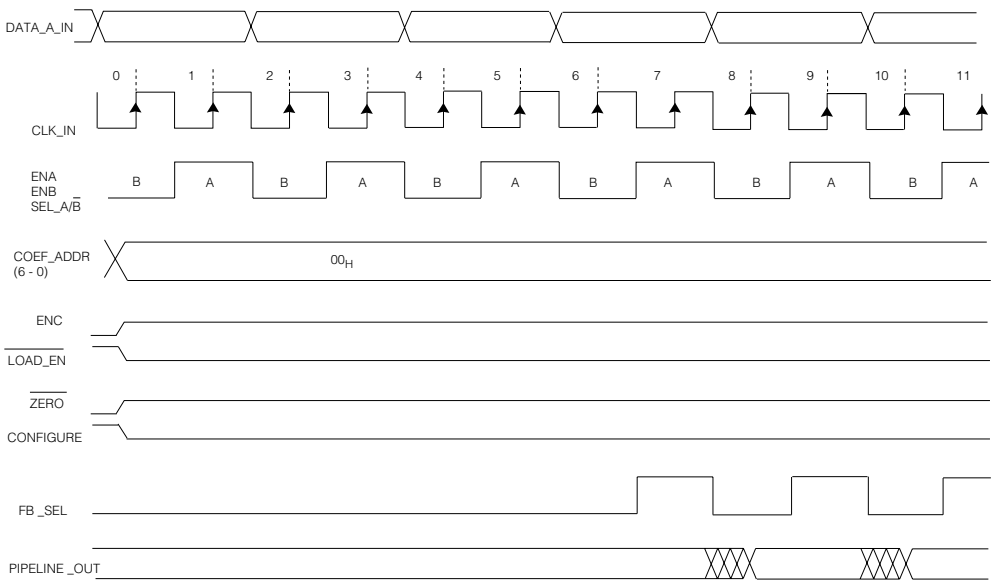


Fig. 8 Timing Diagram for a 23-Tap Odd-Symmetric Filter

Assuming that the data A0 —> A21 has already been shifted into the filter registers, by clocking ENA and ENB the data A22 enters DATA_A_IN (Figure 9a). During the first CLK_IN rising edge, the data in the A registers (A22 —> A11) are selected by SEL_A/$\overline{B}$, to be multiplied by the coefficients, C0 —> C11 in memory location 0, COEF_ADDR 00_H . During the second CLK_IN rising edge the data in B registers (A0 —> A10) are selected by SEL_A/$\overline{B}$, to be multiplied by the coefficients, C0 —>C10 (Figure 9b). After passing through the adder tree and the delay (4 CLK_IN cycles in total), the two sums are added in the pipeline section of the filter. FB_SEL selects PIPELINE_IN during CLK_IN period 5, at which time a DC offset could be introduced at PIPELINE_IN to be added to the sum. During CLK_IN period 6, FB_SEL selects PIPELINE_OUT and the final filter sum is calculated and passed through to PIPELINE_OUT.

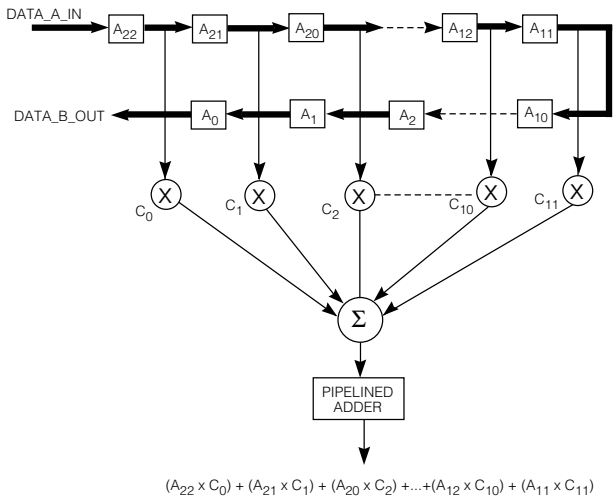


Fig. 9a Data Flow Diagram for a 23 Tap Odd-Symmetric Filter

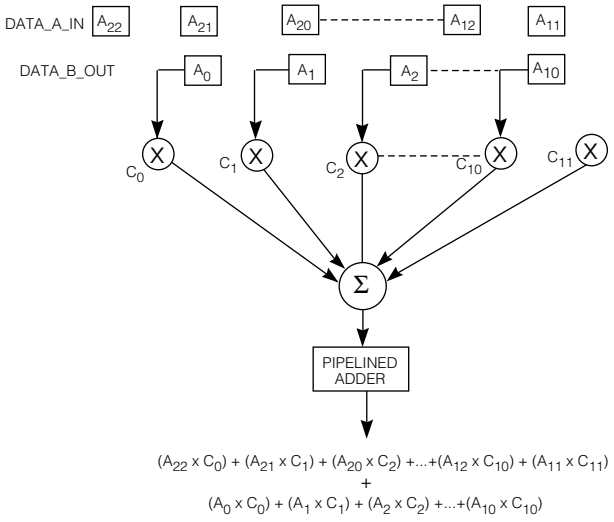


Fig. 9b Data Flow Diagram for a 23 Tap Odd-Symmetric Filter

EVEN-TAP SYMMETRIC FILTER

The GF9101 can be configured as an even-tap symmetric filter. A 24-tap symmetric filter can be configured using one GF9101 by connecting the outputs of DATA_A_OUT to the inputs of DATA_B_IN and taking the output at PIPELINE_OUT. For a 24-tap symmetric filter, the configuration word is shown in Table 9.

TABLE 9: Configuration Word for a 24-tap Symmetric Filter

BIT NO.	CONFIG. WORD	DESCRIPTION
0	1	[3]Data A and B are both signed data
1	1	
2	0	One register delay
3	0	
4	0	24-tap filter, connect the outputs of DATA_A_OUT to the inputs of DATA_B_IN.
5	X	Depending on the loading mode
6	X	See Table 1

NOTE

3. Bits 0 and 1 should have the same value for a 23 or 24 tap filter

The filter coefficients are shown in Figure 10. The timing is verysimilar to that of the even-symmetric case.

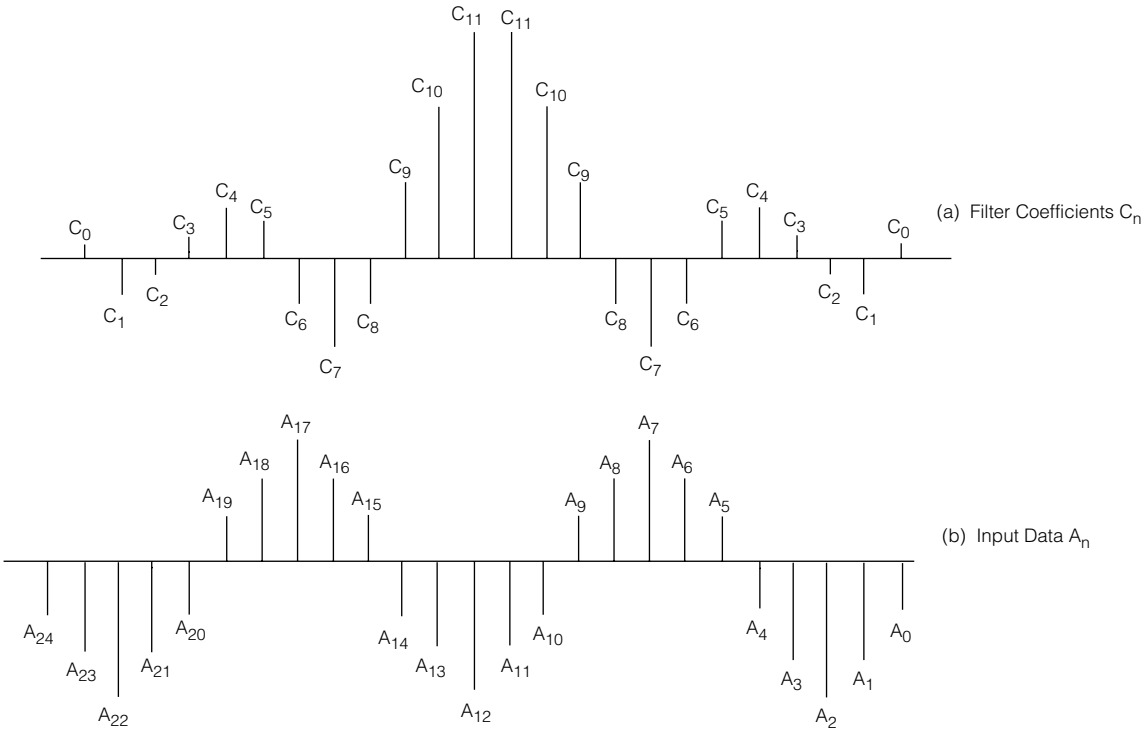


Fig. 10 Input Data A_n and Coefficients C_n

ASYMMETRIC FILTER

The GF9101 can be used as a 24-tap asymmetric filter by configuring it the same way as the even-symmetric case. The difference is in the memory locations since the asymmetric case uses 24 different coefficients, i.e. two sets of filter coefficients. The filter coefficients and the memory locations are shown in Table 10.

The timing diagram is shown in Figure 11. The data flow diagrams are shown in Figures 11a and 11b.

TABLE 10:Internal RAM Address & Contents for a 24-tap Asymmetric Filter

COEF_ADDR (6-0)	MEMORY CONTENTS
00_H	First set of 12 coefficients, C_0 —> C_{11}
01_H	Second set of 12 coefficients, C23 —> C12

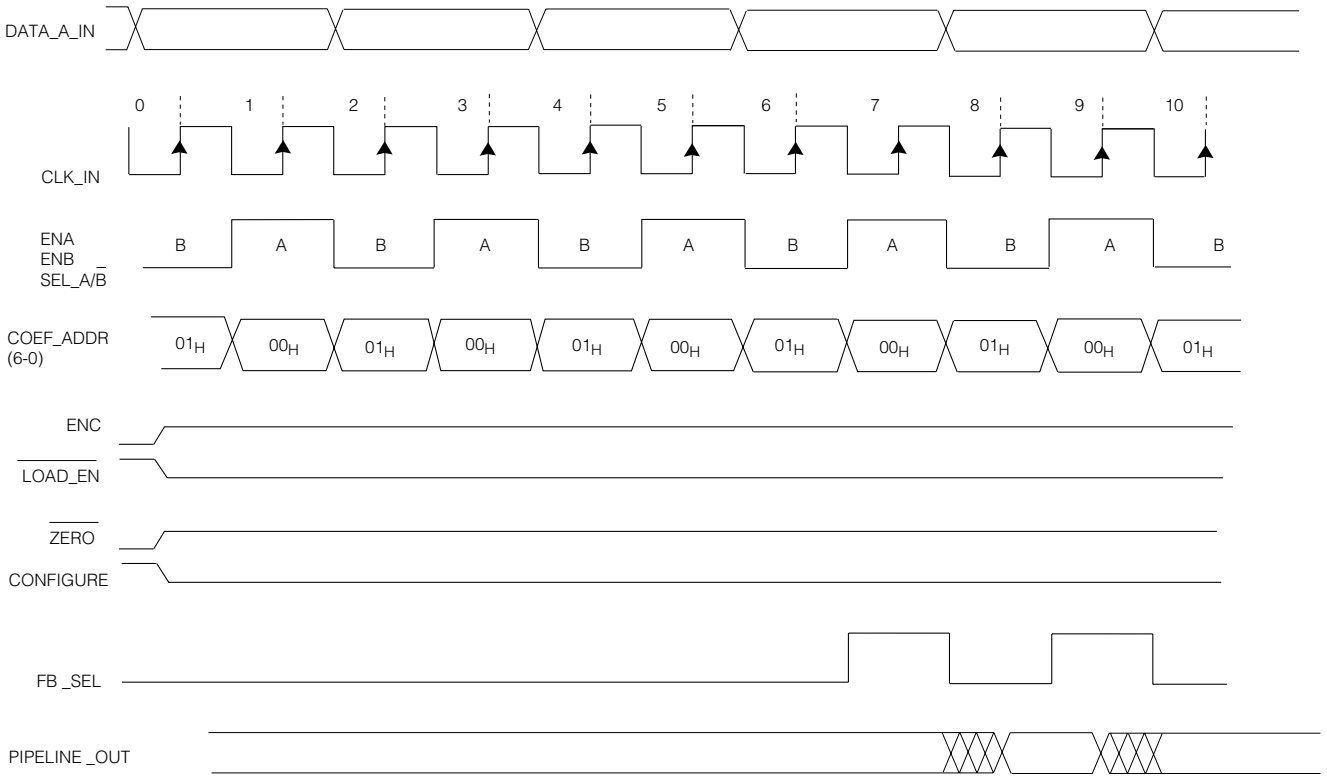


Fig. 11 Timing Diagram for a 24 Tap Asymmetric Filter

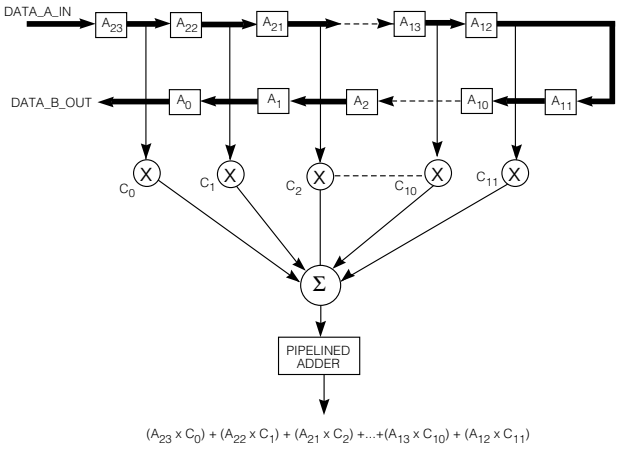


Fig. 11a Data Flow Diagram for a 24 Tap Asymmetric Filter

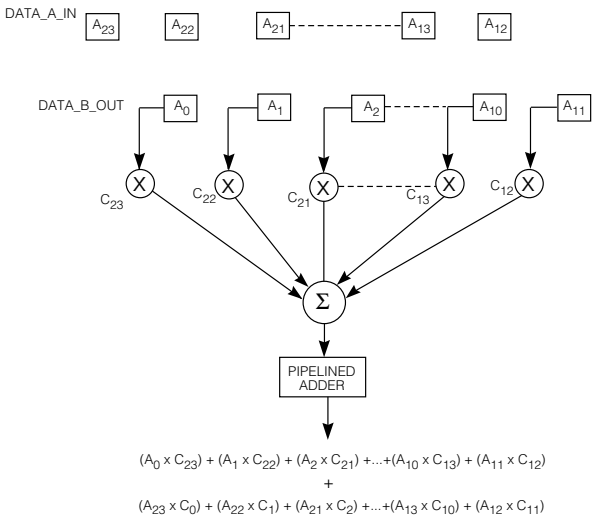


Fig. 11b Data Flow Diagram for a 24 Tap Asymmetric Filter

CASCADING

In the previous section, configuration for a 24 tap filter using only one GF9101 was shown. To realize higher order (>24) filters, up to three GF9101's would allow a 72 tap FIR filter to be configured without any additional hardware. In Figure 13, two GF9101's are cascaded together to obtain a 48 tap filter. The data enters DATA_A_IN (device number 1) and exits from DATA_B_OUT (device number 1). In device number 2, the DATA_A_OUT bus is connected to DATA_B_IN in order to feed the data back in to the B12 register of the same device. The contents of the configuration register will be different for the two devices to compensate for a three register delay introduced when two GF9101's are cascaded to get a 48 tap filter. The configuration register contents are shown in Table 11.

For the 48 tap filter, input data A $_n$ and coefficients C $_n$ are shown in Figure 12. The pipelined output section of the 48 tap filter is shown in Figure 14. Note that two register delays are introduced due to R2 and R3 between the accumulators of device number 1 and number 2. An additional delay is introduced when the filter-sum is fed back to be added to the next sum by selecting FB_SEL_1. The timing diagram for the 48 tap asymmetric filter is shown in Figure 15. The processing clock runs at twice the data rate since the A and B registers of the GF9101 are multiplexed internally..

TABLE 11 Configuration Word for the Cascaded GF9101's

	DEVICE NO. 1	DEVICE NO. 2	
BIT NO.	CONFIG. WORD	CONFIG. WORD	DESCRIPTION
0	1	1	Data A and B are both signed data.
1	1	1	
2	0	0	1 clock cycle delay in device no. 1 and 4 clock delay in device no. 2
3	0	1	
4	0	0	Using each device as 2 x 12 tap filters. Note that in device no. 2 DATA_A_OUT is externally connected to DATA_B_IN.
5	0	0	Assuming serial load mode selected for both devices.
6	0	0	

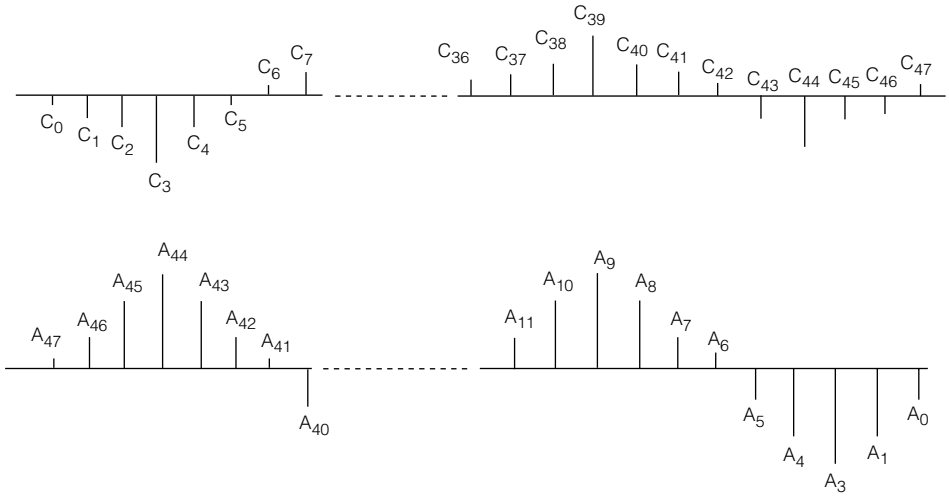


Fig. 12 Input Data A_n and Coefficients C_n

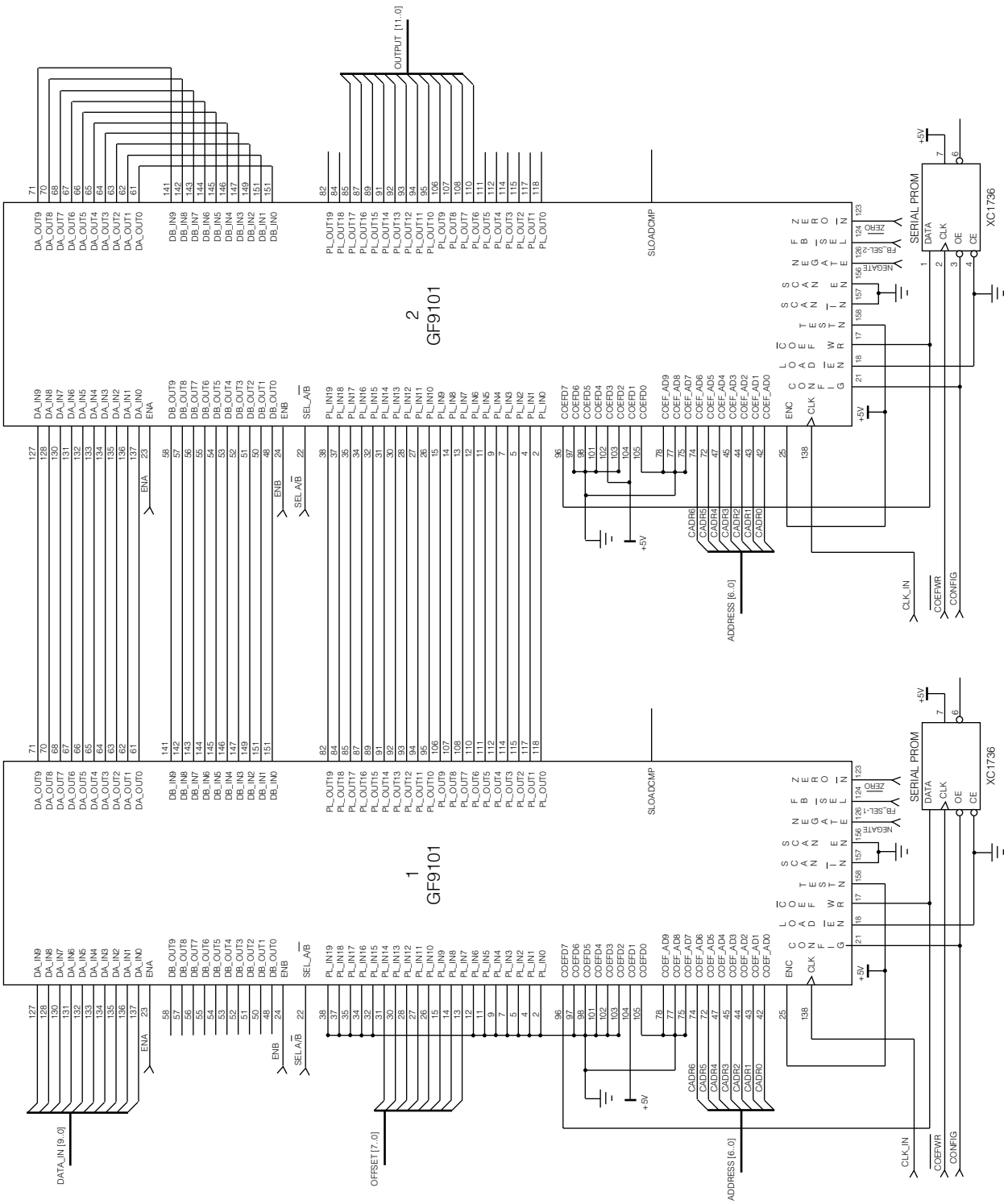

OUTPUT [11..0]
2
GF9101
1
GF9101
SLOADCMP
SERIAL PROM
XC1736
DATA
CLK
OE
CE
+5V
DATA_IN [9..0]
OFFSET [7..0]
ADDRESS [6..0]
CLK_IN
COEFWR
CONFIG

Fig. 13

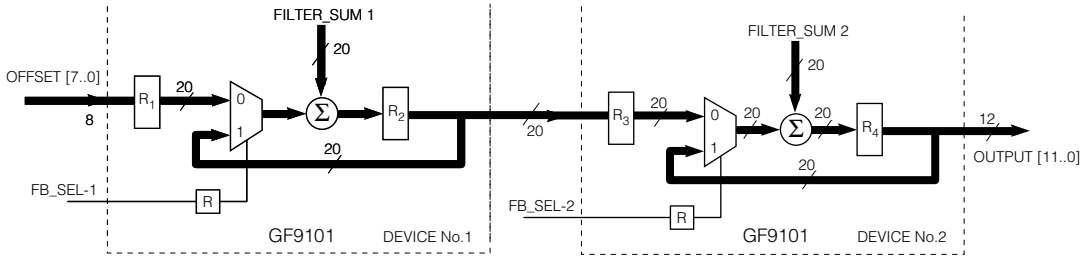


Fig. 14 Pipelined Output Stages for Two Cascaded GF9101's

TABLE 12: Internal RAM Address and Contents for a 48-tap Asymmetric Filter using Two Cascaded GF9101's

COEF_ADDR	INTERNAL RAM CONTENTS	
	Device No. 1	Device No. 2
00_H	C0 —> C11 (registers A1 —> A12)	C12 —> C23 (registers A1 —> A12)
01_H	C47 —> C36 (registers B1 —> B12)	C35 —> C24 (registers B1 —> B12)

Dedicated serial PROM's can be used to load the coefficients into the internal RAM of each GF9101. Note that when data is fed back into DATA_B_IN, it enters register B12 of device number 2. Therefore, while loading the coefficients into the internal RAM for the B registers the coefficients should be arranged as shown in Table 12. If a single source is used for coefficient loading, the $\overline{\text{LOAD\_EN}}$ signal is used to select the appropriate device. Also, the S_LOAD_CMP signal can be used as an indicator for a successful load.

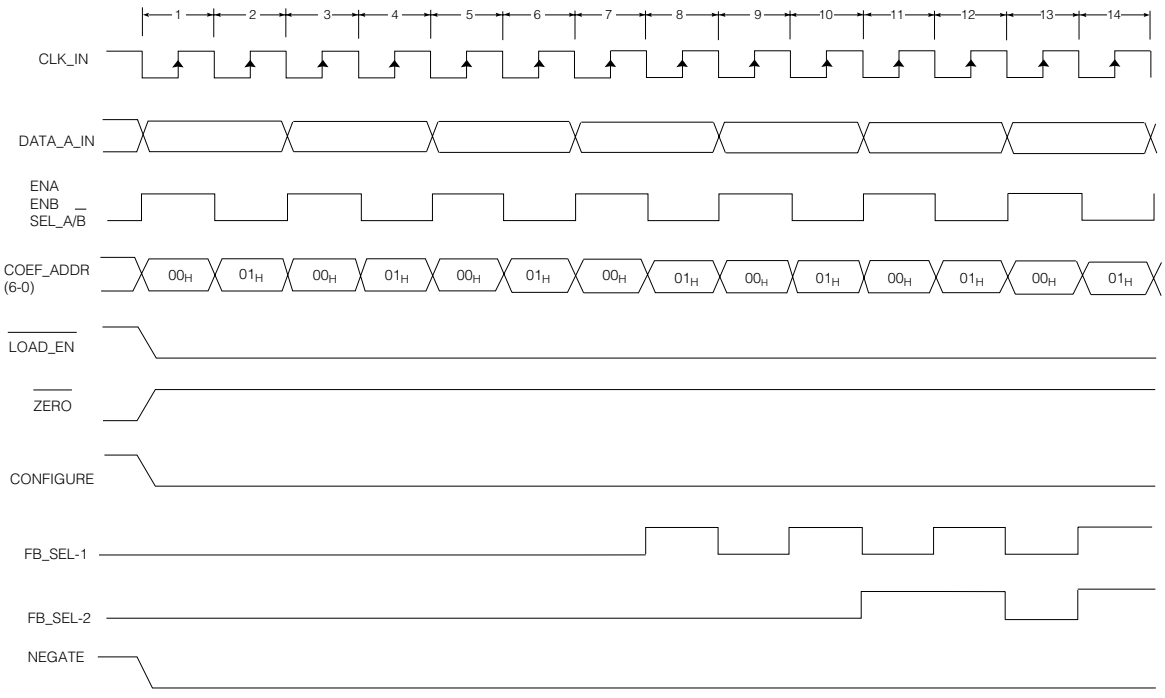
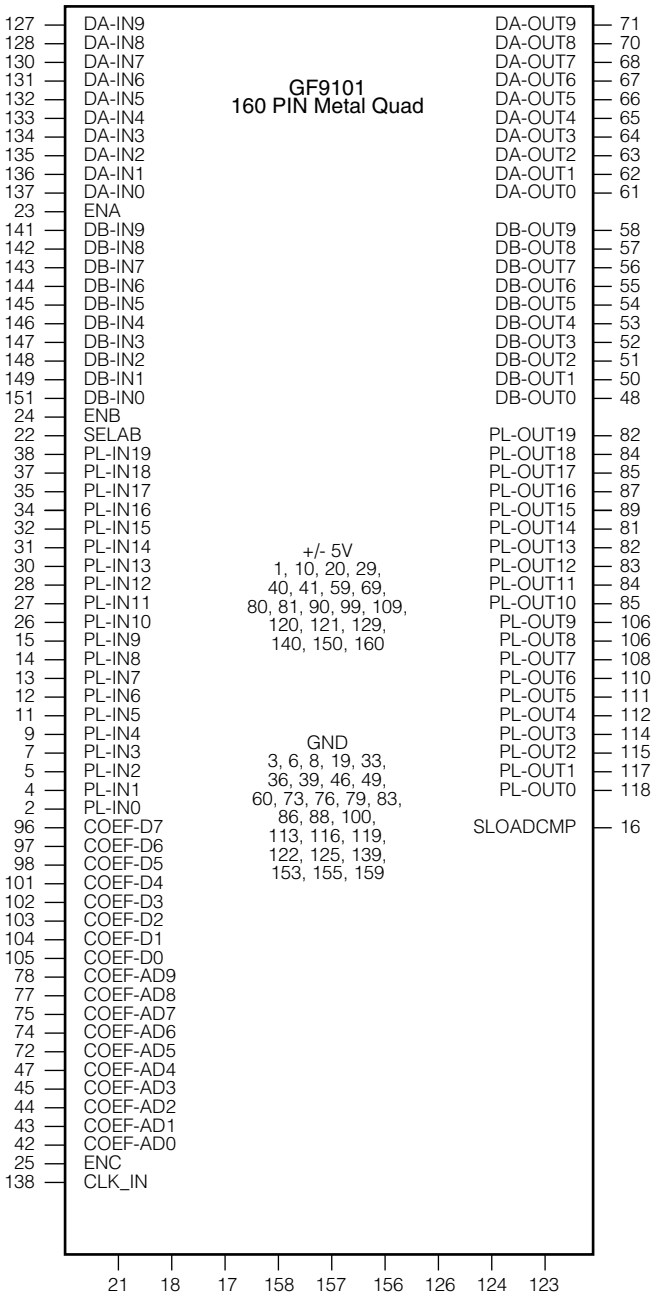


Fig. 15 Timing Diagram for a 48 Tap Asymmetric Filter



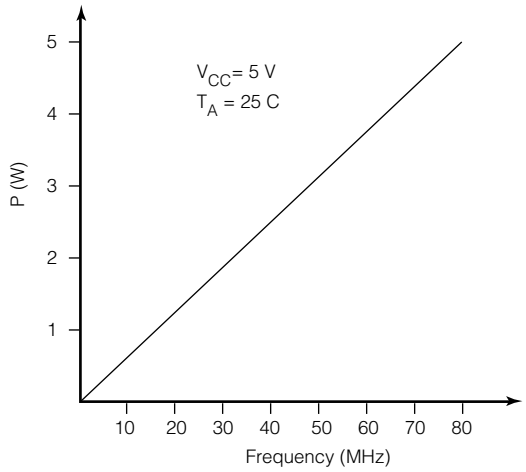
GF9101 Pin Designations

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.3 to +7.0 V
Input Voltage	-0.3 to (V_{DD} +0.3) V
Short Circuit Duration (single output)	1 second
Storage Temp	- 40 to +125 C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
DC Supply Voltage	V_{DD}	+ 3.0 to + 5.5	V
Ambient	T_A	0 to +70	C
Junction	T_J	+150	C



GF9101 Power Consumption vs Clock Rate

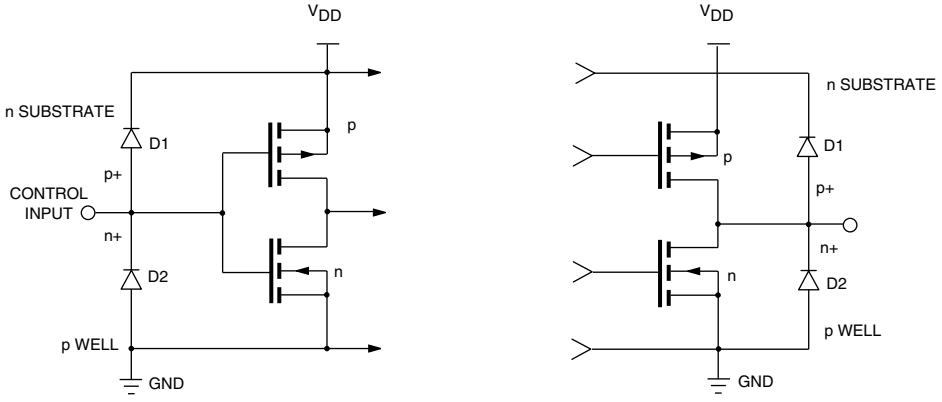


Fig. 16 Equivalent Input/Output Circuit

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, T_A = 0°C to 70°C unless otherwise shown

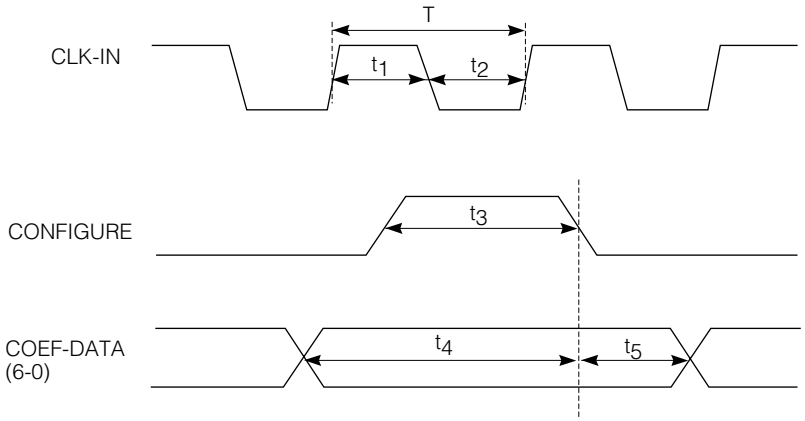
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Input LOW	V_{IL}		-	-	1.5	V
Voltage Input HIGH	V_{IH}		3.5	-	-	V
Voltage Output HIGH	V_{OH}		2.4	4.5	-	V
Switching Threshold	V_T		-	2.5	-	V
Input Current	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}	-10	+/-1	10	µA
Output Current HIGH	I_{OH}	PIPELINE_OUT	-	-	2	mA
	I_{OH}	DATA_A_OUT, DATA_B_OUT	-	-	1	mA
Output Current LOW	I_{OL}	PIPELINE_OUT	-	-	2	mA
	I_{OL}	DATA_A_OUT, DATA_B_OUT	-	-	1	mA
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{DD}$ or V_{SS}	-	12	-	mA
Output Short Circuit Current	I_{OS}	V_{DD} = Max, $V_O = V_{DD}$	30	75	140	mA
		V_{DD} = Max, V_O = 0V	25	70	140	mA
Input Capacitance	C_{IN}		-	4.0	-	pF
Output Capacitance	C_{OUT}		-	3.5	-	pF

SWITCHING CHARACTERISTICS

V_{CC} = 5V ±5%, T_A = 0°C to 70°C unless otherwise shown

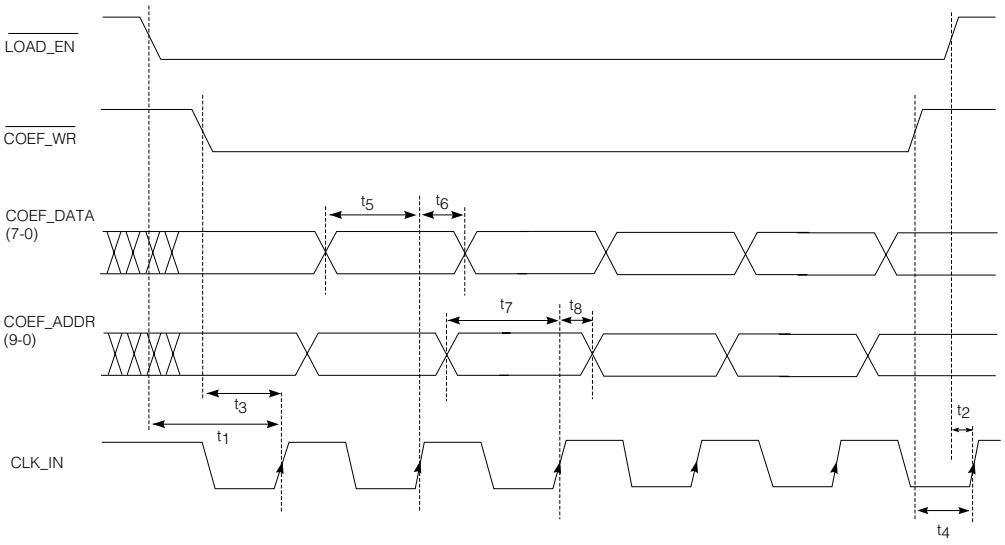
Output Delay	t_D		-	8	-	ns
Setup Time	t_S	All Inputs	2	-	-	ns
Hold Time	t_H	All Inputs	6	-	-	ns
Clock Rate	f_{MAX}		-	-	40	MHz

GF9101 TIMING



Configuration Mode

	DESCRIPTION	SYMBOL	MIN	MAX	UNIT
1	CLK_IN duration time (HIGH)	t_1	12		ns
2	CLK_IN duration time (LOW)	t_2	12		ns
3	CLK_IN period time	T	25		ns
4	CONFIGURE pulse width	t_3	T+10		ns
5	COEF_DATA to configure setup time	t_4	10		ns
6	COEF_DATA to configure hold time	t_5	5		ns

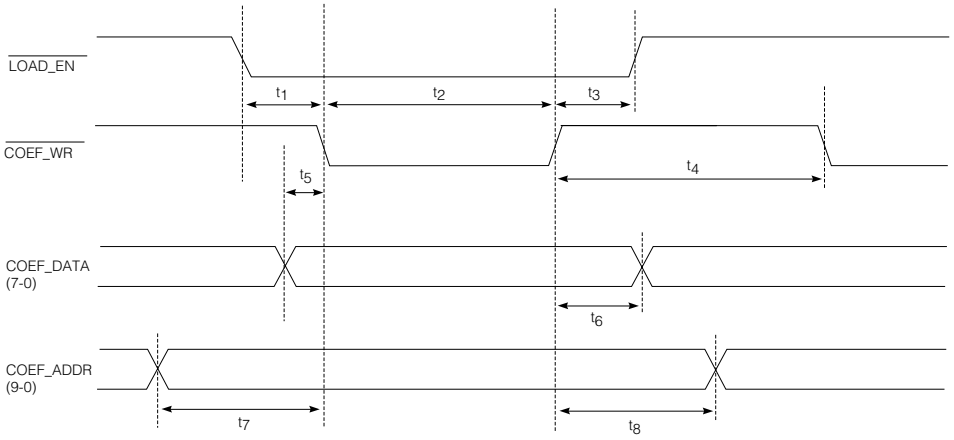


Memory Loading - Parallel Interface

	DESCRIPTION	SYMBOL	MIN	MAX	UNIT
1	$\overline{\text{LOAD\_EN}}$ to CLK_IN set up time*	t_1	4		ns
2	$\overline{\text{LOAD\_EN}}$ to CLK_IN hold time**	t_2	6		ns
3	$\overline{\text{COEF\_WR}}$ to CLK_IN set up time*	t_3	4		ns
4	$\overline{\text{COEF\_WR}}$ to CLK_IN hold time**	t_4	6		ns
5	COEF_DATA to CLK_IN set up time	t_5	2		ns
6	COEF_DATA to CLK_IN hold time	t_6	6		ns
7	COEF_ADDR to CLK_IN set up time	t_7	2		ns
8	COEF_ADDR to CLK_IN hold time	t_8	6		ns

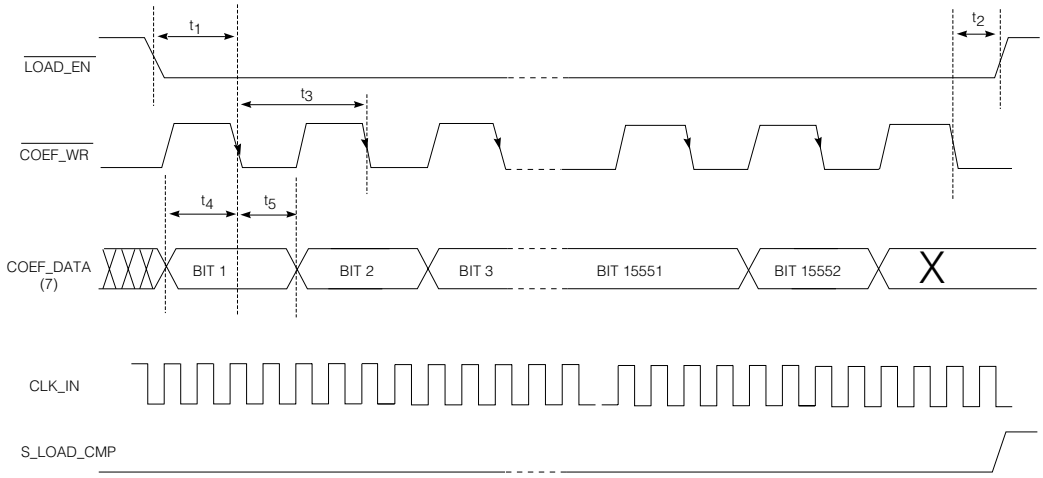
* to enable loading

** to disable loading



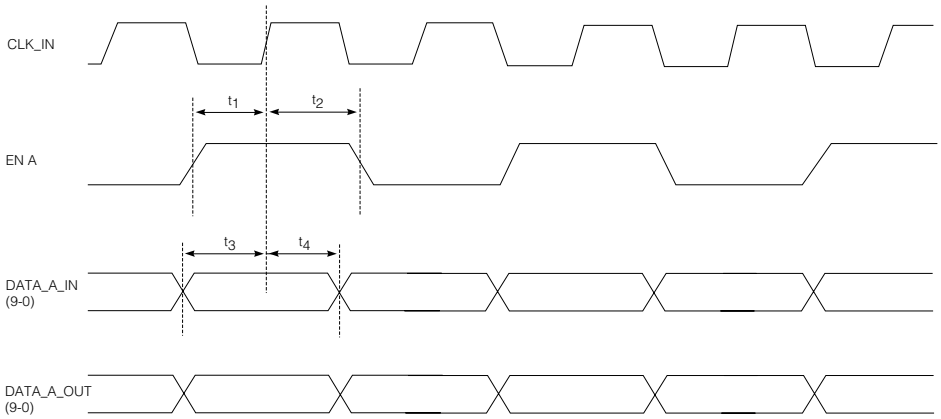
Memory Loading - Microprocessor Interface

	DESCRIPTION	SYMBOL	MIN	MAX	UNIT
1	$\overline{\text{LOAD\_EN}}$ to $\overline{\text{COEF\_WR}}$ set up time	t_1	2		na
2	$\overline{\text{COEF\_WR}}$ puls width low	t_2	80		ns
3	$\overline{\text{LOAD\_EN}}$ to $\overline{\text{COEF\_WR}}$ hold time	t_3	6		ns
4	$\overline{\text{COEF\_WR}}$ pulse width, high	t_4	20		ns
5	COEF_DATA to $\overline{\text{COEF\_WR}}$ set up time	t_5	10		ns
6	COEF_DATA to $\overline{\text{COEF\_WR}}$ hold time	t_6	10		ns
7	COEF_ADDR to $\overline{\text{COEF\_WR}}$ set up time	t_7	2		ns
8	COEF_ADDR to $\overline{\text{COEF\_WR}}$ hold time	t_8	6		ns



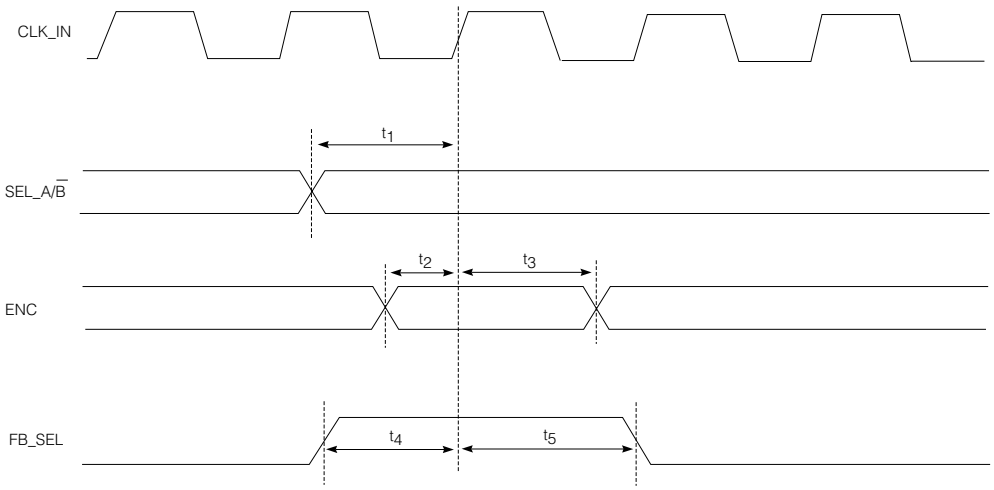
Memory Loading - Serial

	DESCRIPTION	SYMBOL	MIN	MAX	UNIT
1	$\overline{\text{LOAD\_EN}}$ to $\overline{\text{COEF\_WR}}$ set up time	t_1	4		ns
2	$\overline{\text{LOAD\_EN}}$ to $\overline{\text{COEF\_WR}}$ hold time	t_2	6		ns
3	$\overline{\text{COEF\_WR}}$ period	t_3	4xT		ns
4	COEF_DATA(7) to $\overline{\text{COEF\_WR}}$ set up time	t_4	2		ns
5	COEF_DATA(7) to $\overline{\text{COEF\_WR}}$ hold time	t_5	6		ns



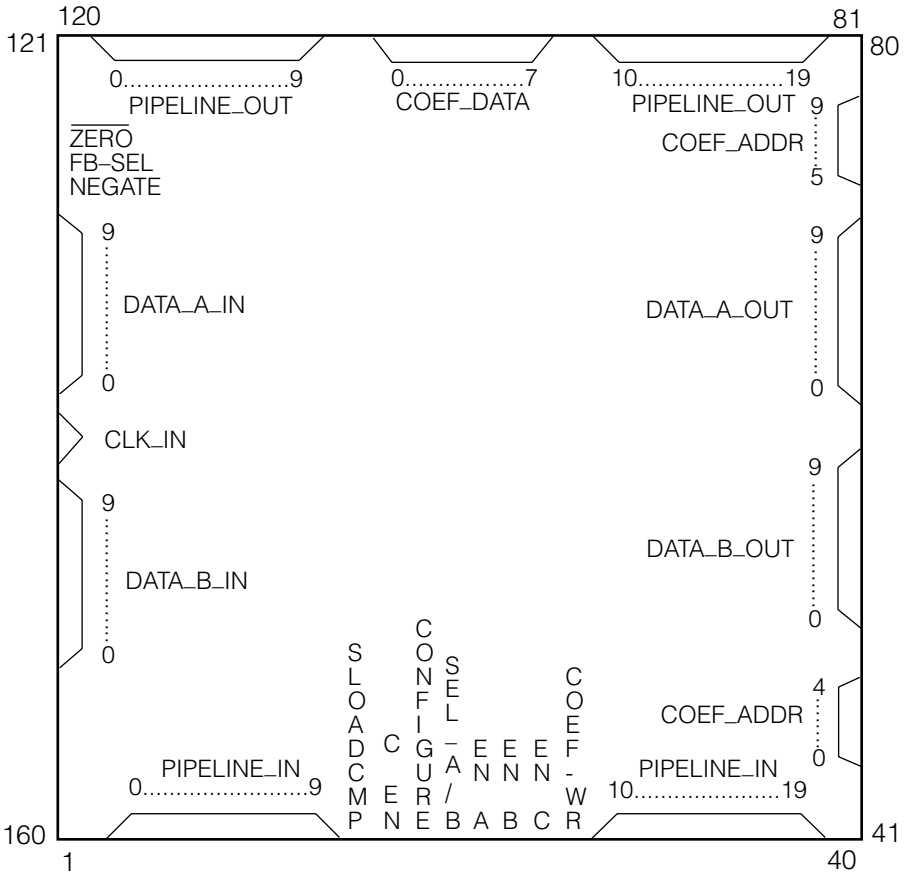
Run Mode

	DESCRIPTION	SYMBOL	MIN	MAX	UNIT
1	ENA to CLK_IN set up time	t_1	2		ns
2	ENA to CLK_IN hold time	t_2	6		ns
3	DATA_A_IN to CLK_IN set up time	t_3	2		ns
4	DATA_A_IN to CLK_IN hold time	t_4	6		ns



Run Mode

DESCRIPTION		SYMBOL	MIN	MAX	UNIT
1	SEL_A/$\overline{B}$ to CLK_IN set up time	t_1	2		ns
2	ENC to CLK_IN set up time	t_2	2		ns
3	ENC to CLK_IN hold time	t_3	6		ns
4	FB_SEL to CLK_IN set up time	t_4	2		ns
5	FB_SEL to CLK_IN hold time	t_5	6		ns



160 pin Metal Quad Pinout

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
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The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

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Remove 'Not Recommended for New Designs' Watermark.
Correct package name to 160 pin Metal Quad.

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