

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change minimum limit of dimension Q for case outline T. Changes in accordance with NOR 5962-R145-97.	96-11-27	Raymond Monnin
B	Add note 4/ to t_{WLQZ} , t_{CDR} , and t_R in table I. Add note 5/ to t_{ELQX} , t_{WHQX} , t_{OLQX} , and t_{OHQZ} in table I. Add case outline 8. Change dimensions b, c, L, and Q for case outline T. Add CAGE 01295 as source of supply for case outlines T and 8. Update boilerplate. Editorial changes throughout.	97-04-17	Raymond Monnin
C	Change minimum dimensions A, b, and E for case outline U. Add CAGE 65786 as a source of supply. Editorial changes throughout. ksr	97-10-24	Raymond Monnin

REV																			
SHEET																			
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28					
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14		
PMIC N/A	PREPARED BY Jeff Bowling						DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316												
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Jeff Bowling						MICROCIRCUIT, MEMORY, DIGITAL, 512K X 8 STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON												
	APPROVED BY Michael A. Frye																		
	DRAWING APPROVAL DATE 96-03-05						SIZE A	CAGE CODE 67268	5962-95600										
	REVISION LEVEL C						SHEET 1 OF 28												

DSCC FORM 2233
APR 97

5962-E244-97

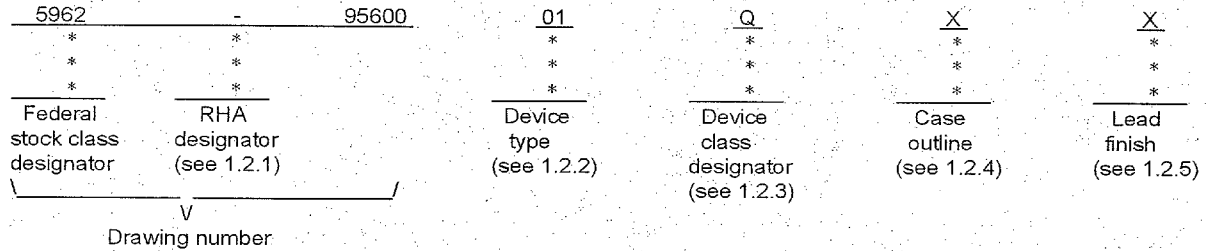
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1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Data retention	Access time
01		512K X 8 CMOS SRAM	No	45 ns
02		512K X 8 CMOS SRAM	No	35 ns
03		512K X 8 CMOS SRAM	No	25 ns
04		512K X 8 CMOS SRAM	No	20 ns
05		512K X 8 CMOS SRAM	Yes	45 ns
06		512K X 8 CMOS SRAM	Yes	35 ns
07		512K X 8 CMOS SRAM	Yes	25 ns
08		512K X 8 CMOS SRAM	Yes	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	GDIP1-T32 or CDIP2-T32	32	dual-in-line
Y	See figure 1	32	TSOP package
Z	See figure 1	32	leadless chip carrier
U	See figure 1	32	SOJ package
T	See figure 1	36	flat pack

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535, as applicable (see 6.6.1 and 6.6.2 herein).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 2

1.2.4 Case outlines - continued.

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
M	See figure 1	36	SOJ package
N	See figure 1	36	leadless chip carrier
9	See figure 1	32	flat pack
8	See figure 1	36	SOJ package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/

Voltage on any input relative to V_{SS}	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	2.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	6°C/W
Cases U, M, and 8	11°C/W
Case T	10°C/W
Cases Z and N	20°C/W
Case 9	22°C/W
Junction temperature (T_J)	+150°C 2/
Output current	40 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH})	2.2 V dc to +6.0 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 3/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	4/ percent
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

3/ V_{IL} minimum = -3.0 V dc for pulse width less than 20 ns.

4/ Values will be added when they become available.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 3

STANDARDS

MILITARY

- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

- MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

- ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

- JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 4

DSCC FORM 2234
APR 97

9004708 0032421 449

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 5

DSCC FORM 2234
APR 97

■ 9004708 0032422 385 ■

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 4.5 V to 5.5 V V _{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current 1/	I _{CC1}	t _{AVAV} = t _{AVAV} (minimum), V _{CC} = 5.5 V, CE = WE = V _{IL} , outputs open	1, 2, 3	All		225	mA
Standby power supply current (TTL)	I _{CC2}	CE ≥ V _{IH} , all other inputs ≤ V _{IL} or ≥ V _{IH} ; V _{CC} = 5.5 V	1, 2, 3	All		60	mA
Standby power supply current (CMOS)	I _{CC3}	CE ≥ V _{CC} - 0.2 V, V _{CC} = 5.5 V, V _{IN} < 0.2 V or > (V _{CC} - 0.2 V)	1, 2, 3	01-04		25	mA
				05-08		10	
Data retention voltage	V _{DR}	CE ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or ≤ 0.2 V	1, 2, 3	05-08	2		V
Data retention current	I _{CC4}	V _{CC} = 2.0 V	1, 2, 3	05-08		2	mA
Input leakage current, any input	I _{ILK}	V _{CC} = 5.5 V, V _{IN} = 0 V to 5.5 V	1, 2, 3	All		±10	μA
Off-state output leakage current	I _{OLK}	V _{CC} = 5.5 V, V _{IN} = 0 V to 5.5 V	1, 2, 3	All		±10	μA
Output high voltage	V _{OH}	I _{OUT} = -4.0 mA, V _{CC} = 4.5 V, V _{IL} = 0.8 V, V _{IH} = 2.2 V	1, 2, 3	All	2.4		V
Output low voltage	V _{OL}	I _{OUT} = 8.0 mA, V _{CC} = 4.5 V, V _{IL} = 0.8 V, V _{IH} = 2.2 V	1, 2, 3	All		0.4	V
Input capacitance	C _{IN}	V _{IN} = 0 V, see 4.4.1e f = 1.0 MHz, T _A = +25°C,	4	All		12	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V, see 4.4.1e f = 1.0 MHz, T _A = +25°C,	4	All		14	pF
Functional testing		See 4.4.1c	7,8A,8B	All			
Chip enable access time	t _{ELQV}	See figure 5 2/3/	9,10,11	01,05		45	ns
				02,06		35	
				03,07		25	
				04,08		20	
Read cycle time	t _{AVAV}		9,10,11	01,05	45		ns
				02,06	35		
				03,07	25		
				04,08	20		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 6

DSCC FORM 2234
APR 97

9004708 0032423 211

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 4.5 V to 5.5 V V _{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address access time	t _{AVQV}	See figure 5 2/3/	9,10,11	01,05		45	ns
				02,06		35	
				03,07		25	
				04,08		20	
Output hold after address change	t _{AVQX}		9,10,11	All	3		ns
Chip enable to output active 4/ 5/	t _{ELQX}		9,10,11	All	3		ns
Chip disable to output inactive 4/ 5/	t _{EHQZ}		9,10,11	01,05	0	20	ns
				02,06	0	15	
				03,07	0	10	
				04,08	0	8	
Output enable to output valid	t _{OLQV}		9,10,11	01,05		25	ns
				02,06		15	
				03,07		12	
				04,08		10	
Output enable to output in low Z 4/ 5/	t _{OLQX}		9,10,11	All	0		ns
Output enable to output in high Z 4/ 5/	t _{OHQZ}		9,10,11	01,05	0	20	ns
				02,06	0	15	
				03,07	0	10	
				04,08	0	8	
Write cycle time	t _{AVAV}	See figure 5 2/	9,10,11	01,05	45		ns
				02,06	35		
				03,07	25		
				04,08	20		
Write pulse width	t _{WLWH} t _{WLEH}		9,10,11	01,05	35		ns
				02,06	30		
				03,07	20		
				04,08	17		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 7

DSCC FORM 2234
APR 97

9004708 0032424 158

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 4.5 V to 5.5 V V _{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable to end of write	t _{ELWH} t _{ELEH}	See figure 5 2/	9,10,11	01,05	35		ns
				02,06	30		
				03,07	20		
				04,08	17		
Data setup to end of write	t _{DVWH} t _{DVEH}		9,10,11	01,05	25		ns
				02,06	20		
				03,07	12		
				04,08	10		
Data hold after end of write 4/	t _{WHDX} t _{EHDX}		9,10,11	All	0		ns
Address valid to end of write	t _{AVWH} t _{AVEH}		9,10,11	01,05	35		ns
				02,06	30		
				03,07	20		
				04,08	17		
Address setup to beginning of write	t _{AVWL} t _{AVEL}		9,10,11	All	0		ns
Address hold after end of write	t _{WHAX} t _{EHAX}		9,10,11	All	1		ns
Write enable to output disable 4/ 5/	t _{WLQZ}		9,10,11	01,05	0	30	ns
				02,06	0	25	
				03,07	0	10	
				04,08	0	8	
Output active after end of write 4/ 5/	t _{WHQX}		9,10,11	All	0		ns
Chip select to data retention time 4/	t _{CDR}	See figure 5 2/ CE ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V	9,10,11	05-08	0		ns
Operation recovery time 4/	t _R		9,10,11	05-08	t _{AVAV}		ns

1/ I_{CC} is dependent upon output loading and cycle rate. The specified values apply with output(s) unloaded.

2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance, unless otherwise specified. Output timing reference is 1.5 V. See figure 4.

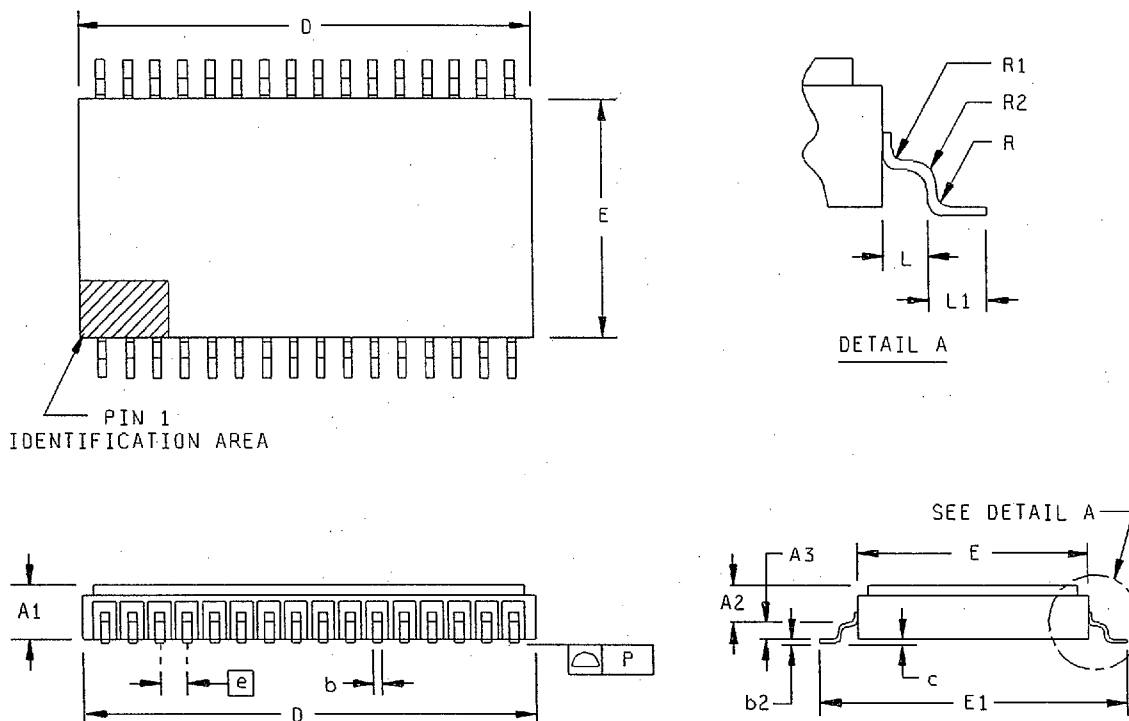
3/ For read cycles, WE is high for entire cycle.

4/ Parameter, if not tested, shall be guaranteed to the limits specified in table I.

5/ Measured ±500 mV from steady-state output voltage. Load capacitance is 5.0 pF.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 8

Case Y (see note)



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A1	2.21	3.00	0.087	0.118	e	1.27 BSC		.050 BSC	
A2	1.27	1.78	0.050	0.070	L	0.51	1.40	0.020	0.055
A3	0.43	1.52	0.017	0.060	L1	0.51	0.76	0.020	0.030
b	0.20	0.61	0.008	0.024	P	—	0.10	—	0.004
b2	0.13	0.20	0.005	0.008	R	0.10	—	0.004	—
c	—	0.25	—	0.010	R1	0.10	0.36	0.004	0.014
D	41.40	42.42	0.820	0.840	R2	0.25	0.51	0.010	0.020
E	10.64	10.85	0.419	0.427	N	32			
E1	14.20	14.40	0.559	0.567					

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

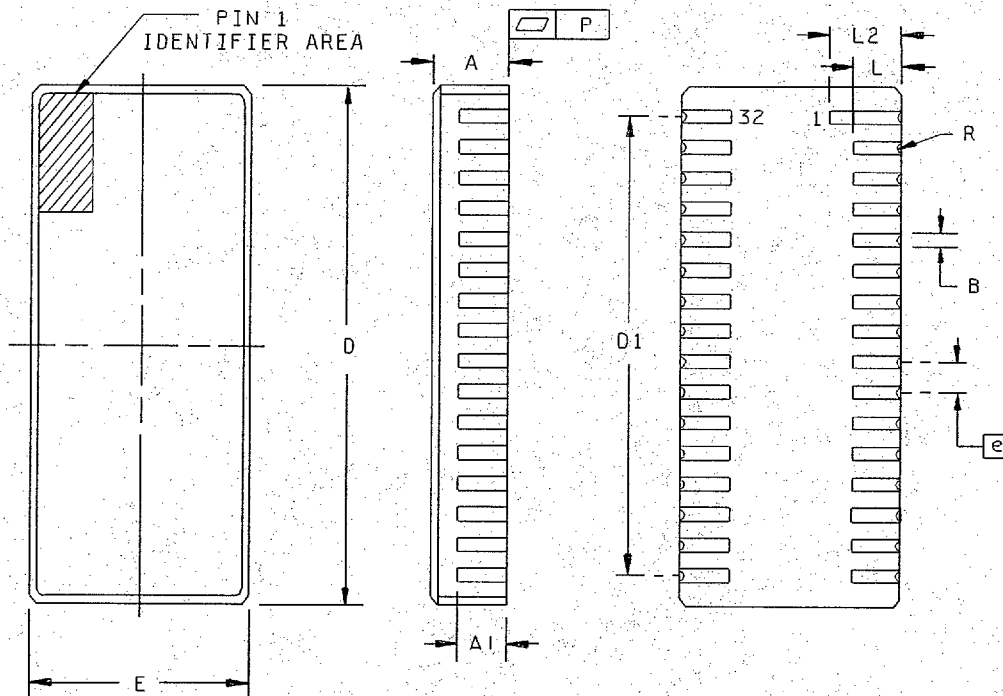
FIGURE 1. Case outlines.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 9

DSCC FORM 2234
APR 97

9004708 0032426 T20

Case Z (see note)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.03	2.54	.080	.100
A1	1.37	1.68	.054	.066
B	0.56	0.71	.022	.028
D	20.70	21.21	.815	.835
D1	18.80	19.30	.740	.760
E	11.18	11.68	.440	.460
e	1.27 BSC		.050 BSC	
L	2.54 REF		.100 REF	
N	32			
P	—	0.15	—	.006
R	0.23 REF		.009 REF	

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

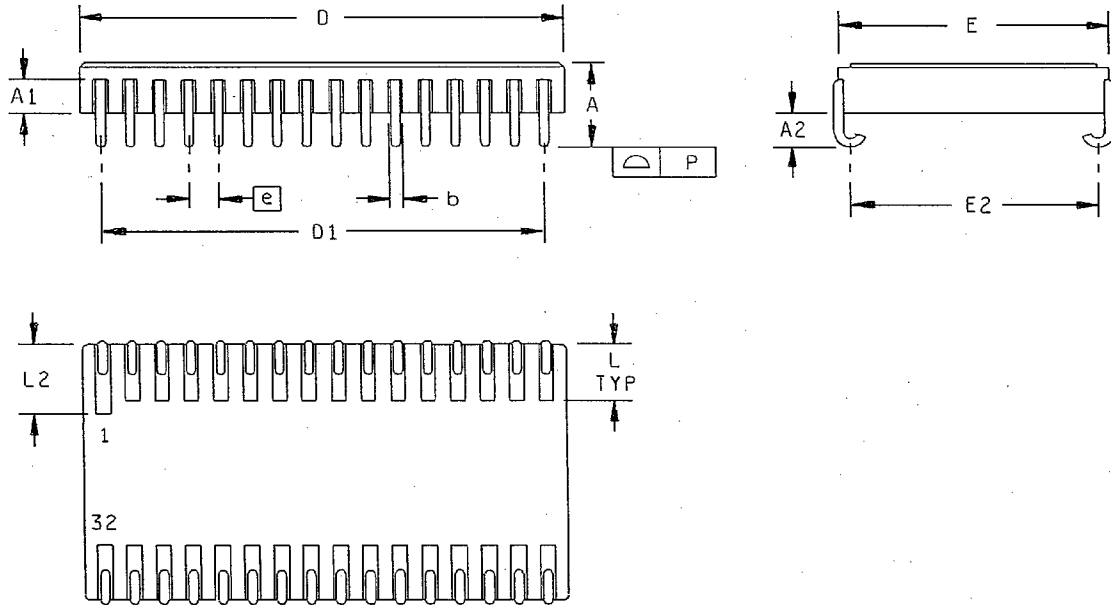
FIGURE 1. Case outlines - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 10

DSCC FORM 2234
APR 97

9004708 0032427 967

Case U (see note)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	4.06	.115	.160
A1	1.37	1.91	.054	.075
A2	0.64	1.60	.025	.063
b	0.38	0.71	.015	.028
D	20.70	21.21	.815	.835
D1	18.80	19.30	.740	.760
E	10.62	11.68	.418	.460
E2	9.42	10.41	.371	.410
e	1.27 BSC		.050 BSC	
L	1.27	1.78	.050	.070
L2	2.92	3.43	.115	.135
N	32			
P	---	0.10	---	.004

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

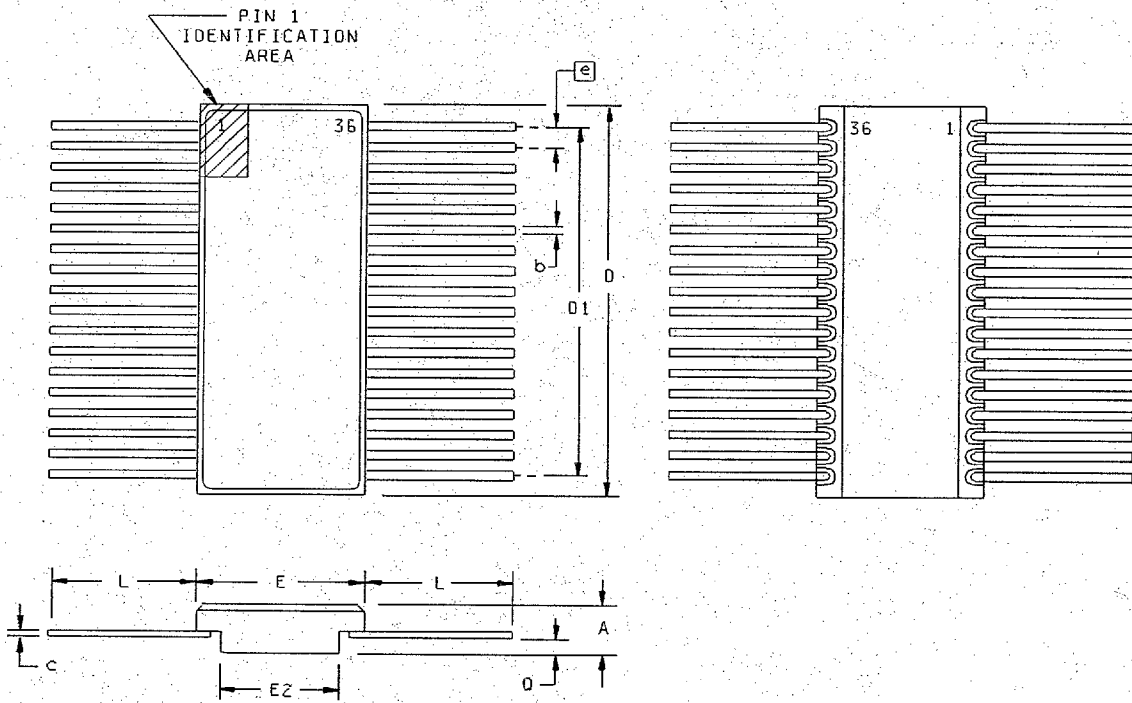
FIGURE 1. Case outlines - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 11

DSCC FORM 2234
APR 97

9004708 0032428 8T3

Case outline T (see note)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.44	3.18	.096	.125
b	0.38	0.56	.015	.022
c	0.08	0.23	.003	.009
D	23.11	23.62	.910	.930
D1	21.34	21.84	.840	.860
E	12.83	13.08	.505	.515
E2	9.78	10.08	.385	.397
e	1.27 BSC		.050 BSC	
L	6.35	9.40	.250	.370
N	36			
Q	0.51	1.14	.020	.045

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

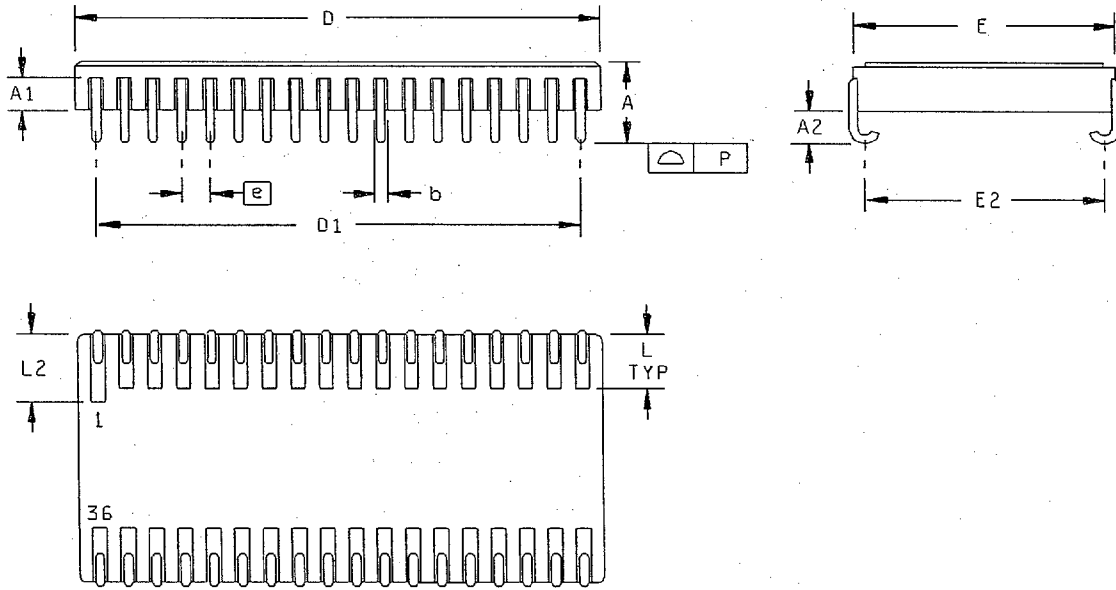
FIGURE 1. Case outlines - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 12

DSCC FORM 2234
APR 97

9004708 0032429 73T

Case outline M (see note)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.56	4.06	.140	.160
A1	1.37	1.91	.054	.075
A2	0.64	1.60	.025	.063
b	0.48	0.71	.019	.028
D	23.11	23.85	.910	.939
D1	21.34	21.84	.840	.860
E	11.02	11.68	.434	.460
E2	9.50	10.41	.374	.410
e	1.27 BSC		.050 BSC	
L	1.27	1.78	.050	.070
L2	2.92	3.43	.115	.135
N	36			
P	—	0.10	—	.004

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

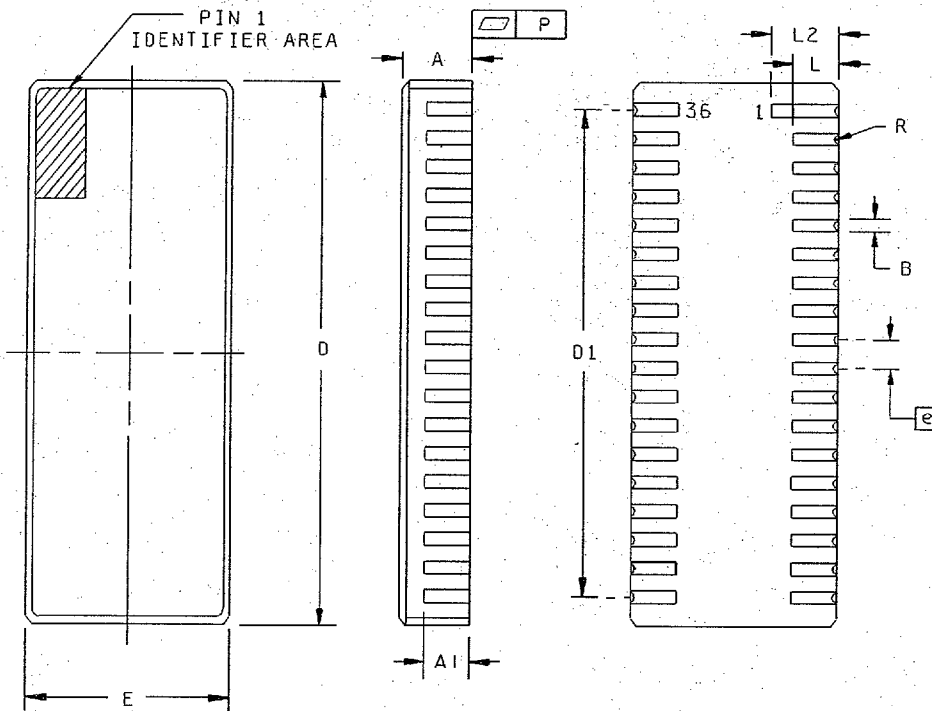
FIGURE 1. Case outlines - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 13

DSCC FORM 2234
APR 97

9004708 0032430 451

Case N (see note)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.03	2.54	.080	.100
A1	1.37	1.68	.054	.066
b	0.56	0.71	.022	.028
D	23.11	23.62	.910	.930
D1	21.34	21.84	.840	.860
E	11.30	11.68	.445	.460
e	1.27 BSC		.050 BSC	
L	2.54 TYP		.100 TYP	
L2	2.92	3.43	.115	.135
N	36			
P	--	0.15	--	.006
R	0.23 TYP		.009 TYP	

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

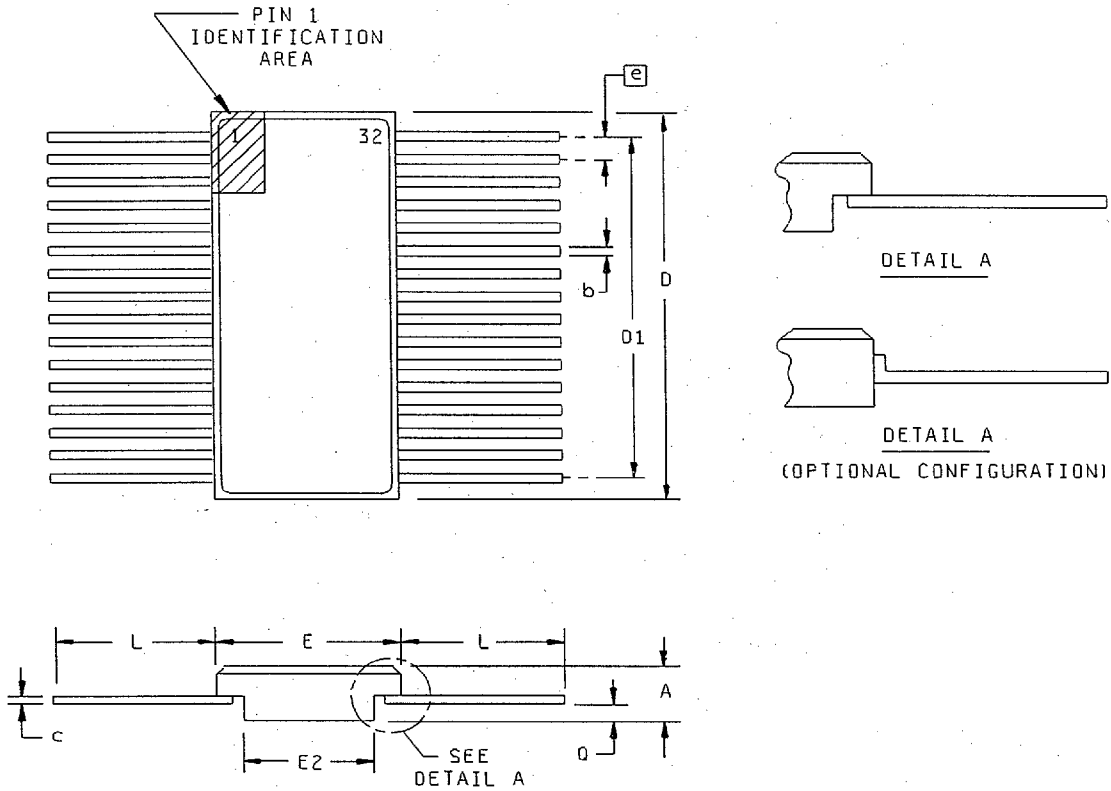
FIGURE 1. Case outlines - Continued.

<p>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316</p>	<p>SIZE A</p>		<p>5962-95600</p>
		<p>REVISION LEVEL C</p>	<p>SHEET 14</p>

DSCC FORM 2234
APR 97

9004708 0032431 398

Case 9 (see notes)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.44	2.90	.096	.114
b	0.20	0.48	.008	.019
c	0.08	0.20	.003	.008
D	20.73	21.29	.816	.838
D1	18.85	19.25	.742	.758
E	10.64	11.68	.419	.460
E2	8.76	10.85	.345	.427
e	1.27 BSC		.050 BSC	
L	7.37	7.87	.290	.310
N	32			
Q	0.61	0.97	.024	.038

NOTES:

1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Dimension E2 does not apply to optional configuration.

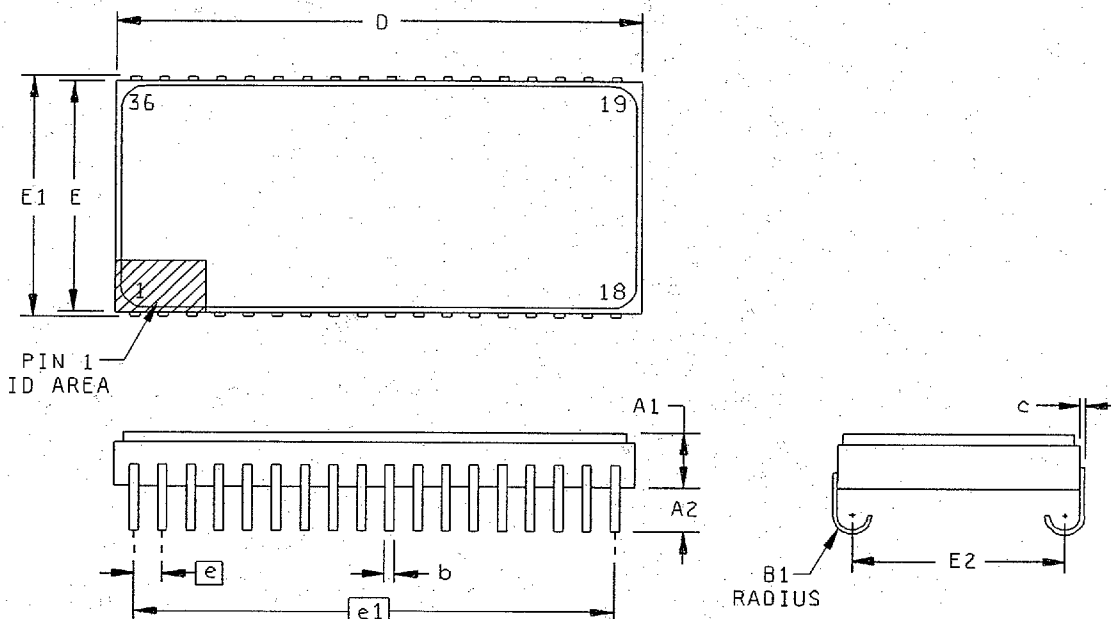
FIGURE 1. Case outlines - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 15

DSCC FORM 2234
APR 97

9004708 0032432 224

Case 8



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A1	2.03	2.79	.080	.110
A2	1.47	1.98	.058	.078
B1	0.64R	0.89R	.025R	.035R
b	0.41	0.58	.016	.023
c	0.15	0.33	.006	.013
D	22.99	23.75	.905	.935
E	10.54	11.05	.415	.435
E1	11.30 REF		.445 REF	
E2	9.17	9.93	.361	.391
e	1.27 BSC		.050 BSC	
e1	21.59 BSC		.850 BSC	
N	36			

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

<p>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316</p>	<p>SIZE A</p>		<p>5962-95600</p>
		<p>REVISION LEVEL C</p>	<p>SHEET 16</p>

DSCC FORM 2234
APR 97

9004708 0032433 160

Device types	All	
Case outlines	X, Y, Z, U, 9	T, M, N, 8
Terminal number	Terminal symbol	
1	A ₁₈	A ₀
2	A ₁₆	A ₁
3	A ₁₄	A ₂
4	A ₁₂	A ₃
5	A ₇	A ₄
6	A ₆	\overline{CE}
7	A ₅	I/O ₁
8	A ₄	I/O ₂
9	A ₃	V _{CC}
10	A ₂	V _{SS}
11	A ₁	I/O ₃
12	A ₀	I/O ₄
13	I/O ₀	WE
14	I/O ₁	A ₅
15	I/O ₂	A ₆
16	V _{SS}	A ₇
17	I/O ₃	A ₈
18	I/O ₄	A ₉
19	I/O ₅	NC
20	I/O ₆	A ₁₀
21	I/O ₇	A ₁₁
22	\overline{CE}	A ₁₂
23	A ₁₀	A ₁₃
24	\overline{OE}	A ₁₄
25	A ₁₁	I/O ₅
26	A ₉	I/O ₆
27	A ₈	V _{CC}
28	A ₁₃	V _{SS}
29	WE	I/O ₇
30	A ₁₇	I/O ₈
31	A ₁₅	\overline{OE}
32	V _{CC}	A ₁₅
33	--	A ₁₆
34	--	A ₁₇
35	--	A ₁₈
36	--	NC

NC = No connection

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 17

DSCC FORM 2234
APR 97

■ 9004708 0032434 DT7 ■

\overline{OE}	\overline{CE}	\overline{WE}	Mode	I/O	Power
X	H	X	Standby	High Z	Standby
H	L	H	Output deselect	High Z	Active
L	L	H	Read	D _{OUT}	Active
X	L	L	Write	D _{IN}	Active

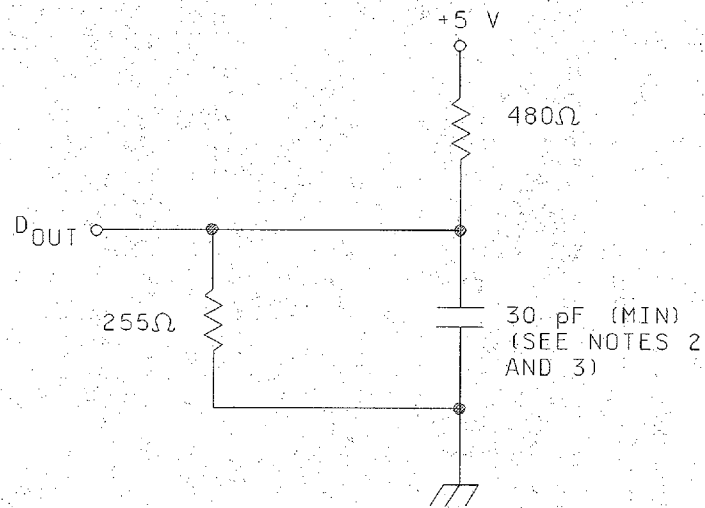
H = Logic "1" state
L = Logic "0" state
X = Don't care

FIGURE 3. Truth table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 18

DSCC FORM 2234
APR 97

9004708 0032435 T33



- NOTES:
1. Use these output load circuits or equivalent for testing.
 2. Including scope and jig.
 3. Minimum of 5 pF for t_{ELQX} , t_{EHQZ} , t_{OLQX} , t_{OHQZ} , t_{WLQZ} , and t_{WHQX} .

AC test conditions:

Input pulse levels	GND to 3.0 V
Input rise, fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuits.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 19

DSCC FORM 2234
APR 97

9004708 0032436 97T

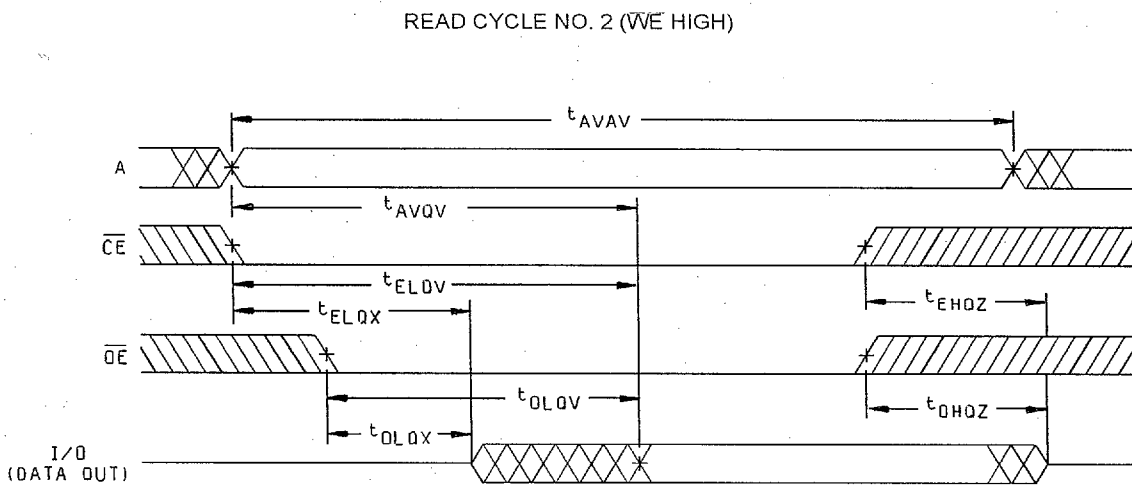
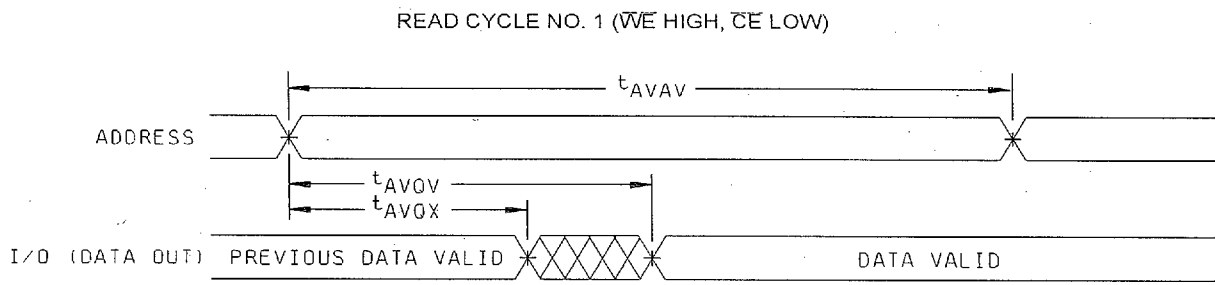


FIGURE 5. Timing waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 20

DSCC FORM 2234
APR 97

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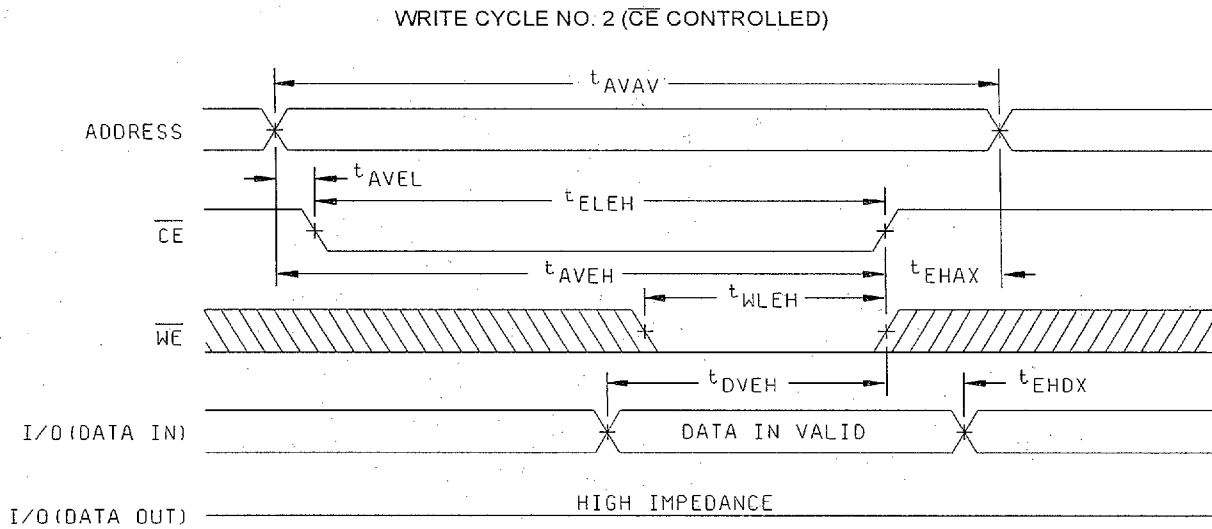
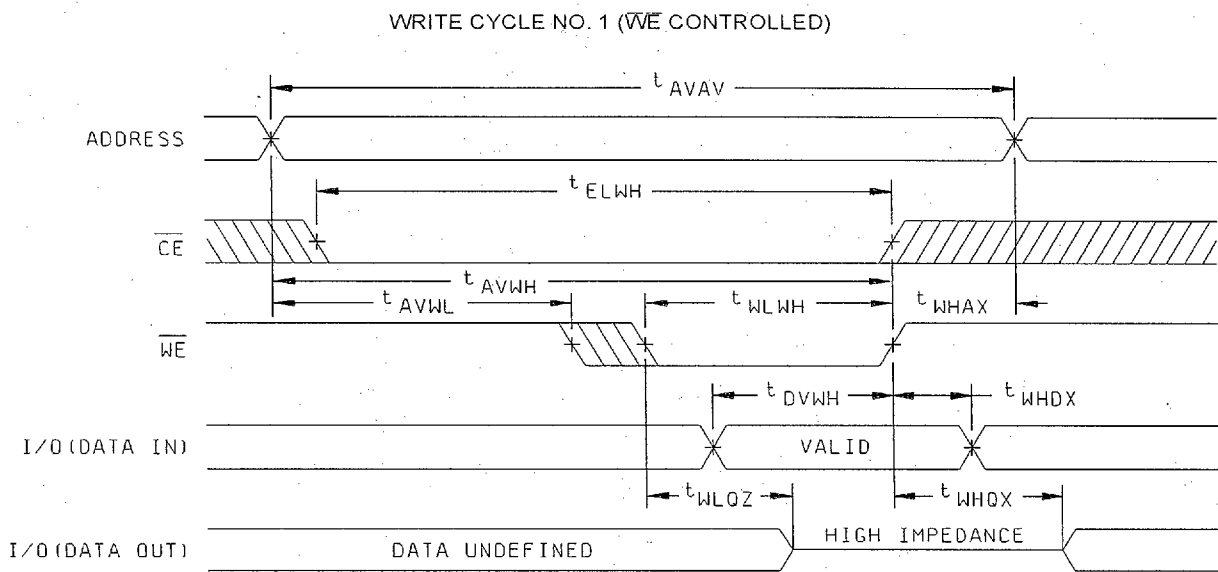


FIGURE 5. Timing waveforms - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A	5962-95600
		REVISION LEVEL C

DSCC FORM 2234
APR 97.

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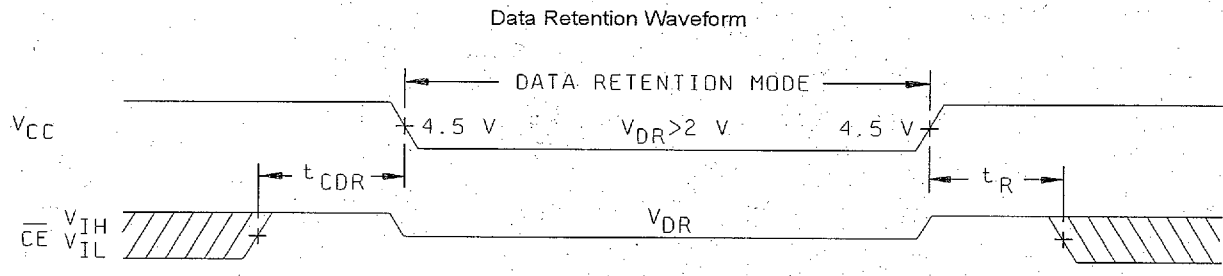


FIGURE 5. Timing waveforms - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 22

DSCC FORM 2234
APR 97

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

- 1/ Blank spaces indicate tests are not applicable.
- 2/ Any or all subgroups may be combined when using high-speed testers.
- 3/ Subgroups 7 and 8 functional tests shall verify the truth table.
- 4/ * indicates PDA applies to subgroup 1 and 7.
- 5/ ** see 4.4.1e.
- 6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
- 7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I _{CC3} standby	±10%
I _{ILK} , I _{OLK}	±10%

- 1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 23

DSCC FORM 2234
APR 97

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4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. OV (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 24

DSCC FORM 2234
APR 97

9004708 0032441 237

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 25

DSCC FORM 2234
APR 97

■ 9004708 0032442 173 ■

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows.

C_{IN}, C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{ILK}	Input leakage current.
I_{OLK}	Output leakage current.
T_C	Case temperature.
V_{CC}	Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 26

DSCC FORM 2234
APR 97

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APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 27

DSCC FORM 2234
APR 97

■ 9004708 0032444 T46 ■

APPENDIX

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316	SIZE A		5962-95600
		REVISION LEVEL C	SHEET 28

DSCC FORM 2234
APR 97

■ 9004708 0032445 982 ■

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-10-24

Approved sources of supply for SMD 5962-95600 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535, as applicable, during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560001MXA	66301	EDI88512CA45CB
	0EU86	AS5C4008CW-45
5962-9560001MYA	66301	EDI88512CA45B32B
5962-9560001MZA	0EU86	AS5C4008EC-45
5962-9560001MUA	66301	EDI88512CA45NB
	0EU86	AS5C4008ECJ-45
	65786	CY7C1048-45FJMB
5962-9560001MTA	66301	EDI88512CA45F36B
	0EU86	AS5C512K8F-45
5962-9560001MMA	66301	EDI88512CA45N36B
	0EU86	AS5C512K8ECJ-45
5962-9560001MNA	0EU86	AS5C512K8EC-45
5962-9560001M9A	66301	EDI88512CA45F32B
	0EU86	AS5C4008F-45
5962-9560002MXA	66301	EDI88512CA35CB
	0EU86	AS5C4008CW-35
5962-9560002MYA	66301	EDI88512CA35B32B
5962-9560002MZA	0EU86	AS5C4008EC-35
5962-9560002MUA	66301	EDI88512CA35NB
	0EU86	AS5C4008ECJ-35
	65786	CY7C1048-35FJMB
5962-9560002MTA	66301	EDI88512CA35F36B
	0EU86	AS5C512K8F-35
	01295	SMJ684002-35HKEM
5962-9560002MMA	66301	EDI88512CA35N36B
	0EU86	AS5C512K8ECJ-35
5962-9560002MNA	0EU86	AS5C512K8EC-35
5962-9560002M9A	66301	EDI88512CA35F32B
	0EU86	AS5C4008F-35
5962-9560002M8A	01295	SMJ684002-35HJAM
5962-9560003MXA	66301	EDI88512CA25CB
	0EU86	AS5C4008CW-25

See footnote at end of list.

9004708 0032446 819

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560003MYA	66301	EDI88512CA25B32B
5962-9560003MZA	0EU86	AS5C4008EC-25
5962-9560003MUA	66301	EDI88512CA25NB
	0EU86	AS5C4008ECJ-25
	65786	CY7C1048-25FJMB
5962-9560003MTA	66301	EDI88512CA25F36B
	0EU86	AS5C512K8F-25
	01295	SMJ684002-25HKEM
5962-9560003MMA	66301	EDI88512CA25N36B
	0EU86	AS5C512K8ECJ-25
5962-9560003MNA	0EU86	AS5C512K8EC-25
5962-9560003M9A	66301	EDI88512CA25F32B
	0EU86	AS5C4008F-25
5962-9560003M8A	01295	SMJ684002-25HJAM
5962-9560004MXA	66301	EDI88512CA20CB
	0EU86	AS5C4008CW-20
5962-9560004MYA	66301	EDI88512CA20B32B
5962-9560004MZA	0EU86	AS5C4008EC-20
5962-9560004MUA	66301	EDI88512CA20NB
	0EU86	AS5C4008ECJ-20
	65786	CY7C1048-20FJMB
5962-9560004MTA	66301	EDI88512CA20F36B
	0EU86	AS5C512K8F-20
	01295	SMJ684002-20HKEM
5962-9560004MMA	66301	EDI88512CA20N36B
	0EU86	AS5C512K8ECJ-20
5962-9560004MNA	0EU86	AS5C512K8EC-20
5962-9560004M9A	66301	EDI88512CA20F32B
	0EU86	AS5C4008F-20
5962-9560004M8A	01295	SMJ684002-20HJAM
5962-9560005MXA	66301	EDI88512LPA45CB
	0EU86	AS5C4008CW-45L0
5962-9560005MYA	66301	EDI88512LPA45B32B
5962-9560005MZA	0EU86	AS5C4008EC-45L
5962-9560005MUA	66301	EDI88512LPA45NB
	0EU86	AS5C4008ECJ-45L
	65786	CY7C1048L-45FJMB
5962-9560005MTA	66301	EDI88512LPA45F36B
	0EU86	AS5C512K8F-45L

See footnote at end of table.

9004708 0032447 755

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560005MMA	66301	EDI88512LPA45N36B
	0EU86	AS5C512K8ECJ-45L
5962-9560005MNA	0EU86	AS5C512K8EC-45L
5962-9560005M9A	66301	EDI88512LPA45F32B
	0EU86	AS5C4008F-45L
5962-9560006MXA	66301	EDI88512LPA35CB
	0EU86	AS5C4008CW-35L
5962-9560006MYA	66301	EDI88512LPA35B32B
5962-9560006MZA	0EU86	AS5C4008EC-35L
5962-9560006MUA	66301	EDI88512LPA35NB
	0EU86	AS5C4008ECJ-35L
	65786	CY7C1048L-35FJMB
5962-9560006MTA	66301	EDI88512LPA35F36B
	0EU86	AS5C512K8F-35L
	01295	SMJ684002-35HKEM
5962-9560006MMA	66301	EDI88512LPA35N36B
	0EU86	AS5C512K8ECJ-35L
5962-9560006MNA	0EU86	AS5C512K8EC-35L
5962-9560006M9A	66301	EDI88512LPA35F32B
	0EU86	AS5C4008F-35L
5962-9560006M8A	01295	SMJ684002-35HJAM
5962-9560007MXA	66301	EDI88512LPA25CB
	0EU86	AS5C4008CW-25L
5962-9560007MYA	66301	EDI88512LPA25B32B
5962-9560007MZA	0EU86	AS5C4008EC-25L
5962-9560007MUA	66301	EDI88512LPA25NB
	0EU86	AS5C4008ECJ-25L
	65786	CY7C1048L-25FJMB
5962-9560007MTA	66301	EDI88512LPA25F36B
	0EU86	AS5C512K8F-25L
	01295	SMJ684002-25HKEM
5962-9560007MMA	66301	EDI88512LPA25N36B
	0EU86	AS5C512K8ECJ-25L
5962-9560007MNA	0EU86	AS5C512K8EC-25L
5962-9560007M9A	66301	EDI88512LPA25F32B
	0EU86	AS5C4008F-25L
5962-9560007M8A	01295	SMJ684002-25HJAM
5962-9560008MXA	66301	EDI88512LPA20CB
	0EU86	AS5C4008CW-20L

See footnote at end of list.

9004708 0032448 691

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9560008MYA	66301	EDI88512LPA20B32B
5962-9560008MZA	0EU86	AS5C4008EC-20L
5962-9560008MUA	66301	EDI88512LPA20NB
	0EU86	AS5C4008ECJ-20L
	65786	CY7C1048L-20FJMB
5962-9560008MTA	66301	EDI88512LPA20F36B
	0EU86	AS5C512K8F-20L
	01295	SMJ684002-20HKEM
5962-9560008MMA	66301	EDI88512LPA20N36B
	0EU86	AS5C512K8ECJ-20L
5962-9560008NA	0EU86	AS5C512K8EC-20L
5962-9560008M9A	66301	EDI88512LPA20F32B
	0EU86	AS5C4008F-20L
5962-9560008M8A	01295	SMJ684002-20HJAM

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>
66301	Electronic Design Inc. 1 Research Drive Westborough, MA 01581-3906
0EU86	Austin Semiconductor 8701 Cross Park Drive Austin, TX 78754-4566
01295	Texas Instruments, Inc. 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75266-0199 Point of contact: P.O. Box 60448 Midland, TX 79711-0448
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134-1599

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