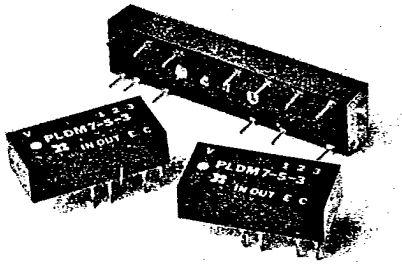
TTL PROGRAMMABLE LOGIC DELAY MODULES

The "DIP SERIES" PLDM offered by Rhombus Industries was developed to allow the design engineer a viable method by which to obtain final delay adjustments, during and/or after installation in a circuit. These programmable delay modules incorporate all necessary driving and pick off circuitry, to allow full compatibility with Schottky TTL and DTL circuits. The design includes compensation for propagation delays and incorporates internal termination at the output. No additional external components are necessary to obtain the required delay. The logic delay modules are digitally programmed by the presence of either a "1" or a "0" at each of the programming pins. Since the input and output terminals are fixed, programming is accomplished through DC voltage levels present at the programming pins. Programming may be accomplished by remote switching; computer generated data; or when no need exists in the application to change the delay time during normal use, by ground pads through all programming pins. Programming can then be accomplished by cutting off those pins which are to remain at a state "1" prior to insertion of the PLDM into the printed circuit board. When the enable input is high, the output is low.

The PLDM is offered in a 3 & 4 bit version giving 8 & 16 programming steps according to their respective truth tables. Tolerance on minimum delay, delay change per step, and deviation from programmed delay are all summarized on their respective data sheets. Delay time is measured at the 1.5 volt level on the leading edge. Rise time for all modules is 4.0ns maximum when measured from 0.75v to 2.4v. Temperature coefficient of delay is better than +500ppm/°C over the operating temperature range of 0 thru 70°C.

The PLDM accepts either a Logic "1" or Logic "0" and will reproduce these levels at the output without inversion. Each module has the capability of driving up to 10 TTL loads.



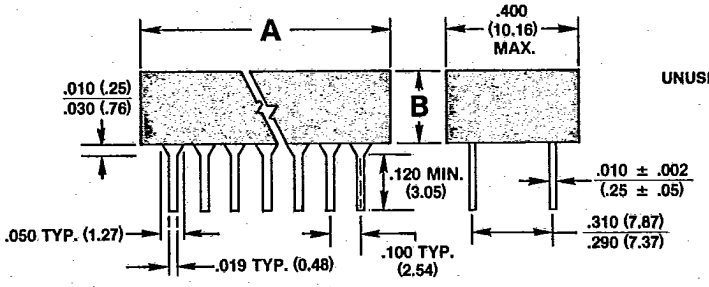
OPERATING SPECIFICATIONS

Vcc Supply Voltage: ..... 4.75 to 5.25 VDC
Logic "1" Input:
  Voltage ..... 2v min.; 5.5v max.
  Current ..... 100μa @ 2.4v, 2ma @ 5.5v
Logic "0" Input:
  Voltage ..... .8v max.
  Logic "1" Voltage Out: ..... 2.4v min.
  Logic "0" Voltage Out: ..... .4v max.
Rise Time Out: ..... 4ns max.
Storage Temp Range: ..... −55° to +125°C
Operating Temp Range: ..... 0° to 70°C

TEST CONDITIONS

Input Pulse Width: ..... Min. 40% of max. delay
Input Pulse Rise Time: 3ns
Input Pulse Voltage: 3.2v
Vcc Supply Voltage: ..... 5.0 VDC
Vcc Supply Current: ..... 60 ma typ.

PHYSICAL DIMENSIONS

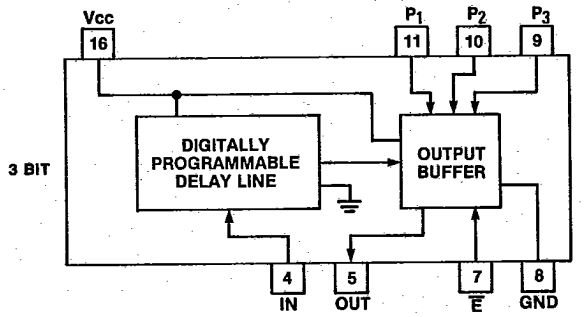


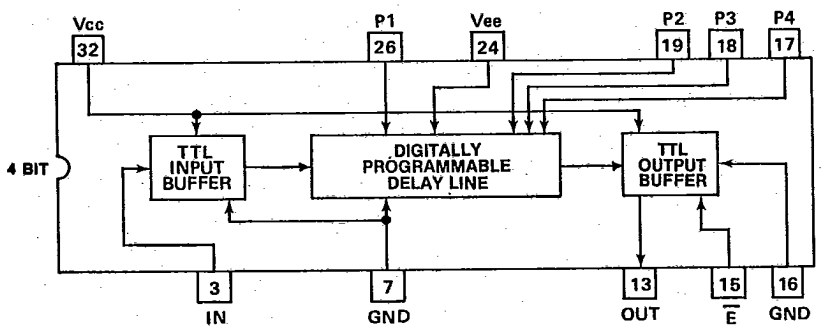
UNUSED LEADS ARE OMITTED.

PART NUMBER	CONFIGURATION	"A" DIMENSION (MAX.) Inches (mm)	"B" DIMENSION (MAX.) Inches (mm)
PLDM7-XX	16 Pin, 3 Bit	0.800 (20.32)	0.250 (6.35)
PLDMXX-XX	32 Pin, 4 Bit	1.600 (40.64)	0.230 (5.84)

BLOCK DIAGRAMS WITH PINOUTS

WHITE DOT (NOTCH) DENOTES PIN 1.





Factory orders should include complete part numbers as explained below:

PLDM XX — XX

- Programmable TTL Delay Module
- Initial Delay in ns (Step 0)
- XX = 7 only for 3 Bit
- Step Delay

TABLE I 4 BIT

PART NUMBER	MIN. DELAY TIME	MAX. DELAY TIME (NOM.)	MAX. DEV. FROM PROGRAMMING DELAY	DELAY CHANGE PER STEP
PLDM 15-1	15ns ± 1ns	30ns	± 1ns	1ns ± .5ns
PLDM 15-2	12ns ± 1ns	45ns	± 1ns	2ns ± .8ns
PLDM 15-3	15ns ± 1ns	60ns	± 2ns	3ns ± 1ns
PLDM 15-5	15ns ± 1ns	90ns	± 2ns	5ns ± 1ns
PLDM 15-10	15ns ± 1ns	165ns	± 4ns	10ns ± 1ns
PLDM 15-16	15ns ± 1ns	255ns	± 4ns	16ns ± 2ns
PLDM 30-1	30ns ± 2ns	45ns	± 2ns	1ns ± .5ns
PLDM 45-1	45ns ± 2ns	60ns	± 2.5ns	1ns ± .5ns
PLDM 60-1	60ns ± 2ns	75ns	± 2.5ns	1ns ± .5ns
PLDM 75-1	75ns ± 3ns	90ns	± 3.0ns	1ns ± .5ns
PLDM 90-1	90ns ± 3ns	105ns	± 3.5ns	1ns ± .5ns

TRUTH TABLE

Programming Pins 4 3 2 1 / PART NUMBER	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
PLDM 15-1	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
PLDM 15-2	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45
PLDM 15-3	15	18	21	24	27	30	33	36	39	42	45	48	51	54	57	60
PLDM 15-5	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90
PLDM 15-10	15	25	35	45	55	65	75	85	95	105	115	125	135	145	155	165
PLDM 15-16	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
PLDM 30-1	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
PLDM 45-1	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
PLDM 60-1	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
PLDM 75-1	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
PLDM 90-1	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105

TABLE II 3 BIT

PART NUMBER	MIN. DELAY TIME	MAX. DELAY TIME (NOM.)	MAX. DEV. FROM PROGRAMMING DELAY	DELAY CHANGE PER STEP
PLDM 7 - 1	7ns ± 1ns	14ns	± 4ns	1ns ± .3ns
PLDM 7 - 2	7ns ± 1ns	21ns	± .6ns	2ns ± .4ns
PLDM 7 - 3	7ns ± 1ns	28ns	± .8ns	3ns ± .5ns
PLDM 7 - 4	7ns ± 1ns	35ns	± .9ns	4ns ± .5ns
PLDM 7 - 5	7ns ± 1ns	42ns	± 1.0ns	5ns ± .5ns
PLDM 7 - 10	7ns ± 1ns	77ns	± 2.0ns	10ns ± 1.0ns

TRUTH TABLE

Programming Pins 3 2 1 / PART NUMBER	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
PLDM 7 - 1	7	8	9	10	11	12	13	14
PLDM 7 - 2	7	9	11	13	15	17	19	21
PLDM 7 - 3	7	10	13	16	19	22	25	28
PLDM 7 - 4	7	11	15	19	23	27	31	35
PLDM 7 - 5	7	12	17	22	27	32	37	42
PLDM 7 - 10	7	17	27	37	47	57	67	77

Other delays readily available. Please consult the factory.