DS501-00001-2v0-E

Memory FRAM

16 K (2 K × 8) Bit I²C

MB85RC16

■ DESCRIPTION

The MB85RC16 is an FRAM (Ferroelectric Random Access Memory) chip in a configuration of 2,048 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MB85RC16 is able to retain data without using a data backup battery.

The memory cells used in the MB85RC16 have at least 10^{10} Read/Write operation endurance per bit, which is a significant improvement over the number of read and write operations supported by other nonvolatile memory products.

The MB85RC16 can provide writing in one byte units because the long writing time is not required unlike Flash memory and E²PROM. Therefore, the writing completion waiting sequence like a write busy state is not required.

■ FEATURES

- Bit configuration : 2,048 words × 8 bits
- Operating power supply voltage : 2.7 V to 3.6 V
- Operating frequency : 1 MHz (Max)
- Two-wire serial interface : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating temperature range : − 40 °C to + 85 °C
- Data retention : 10 years (+ 75 °C)
- Read/Write endurance : 10^{10} times
- Package : Plastic / SOP, 8-pin (FPT-8P-M02)
- Low power consumption : Operating current 0.1mA (Max: @1 MHz), Standby current 0.1 μA (Typ)

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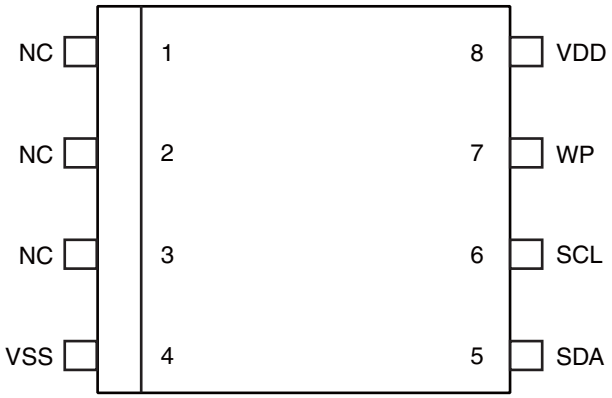
■ PIN ASSIGNMENT

(TOP VIEW)

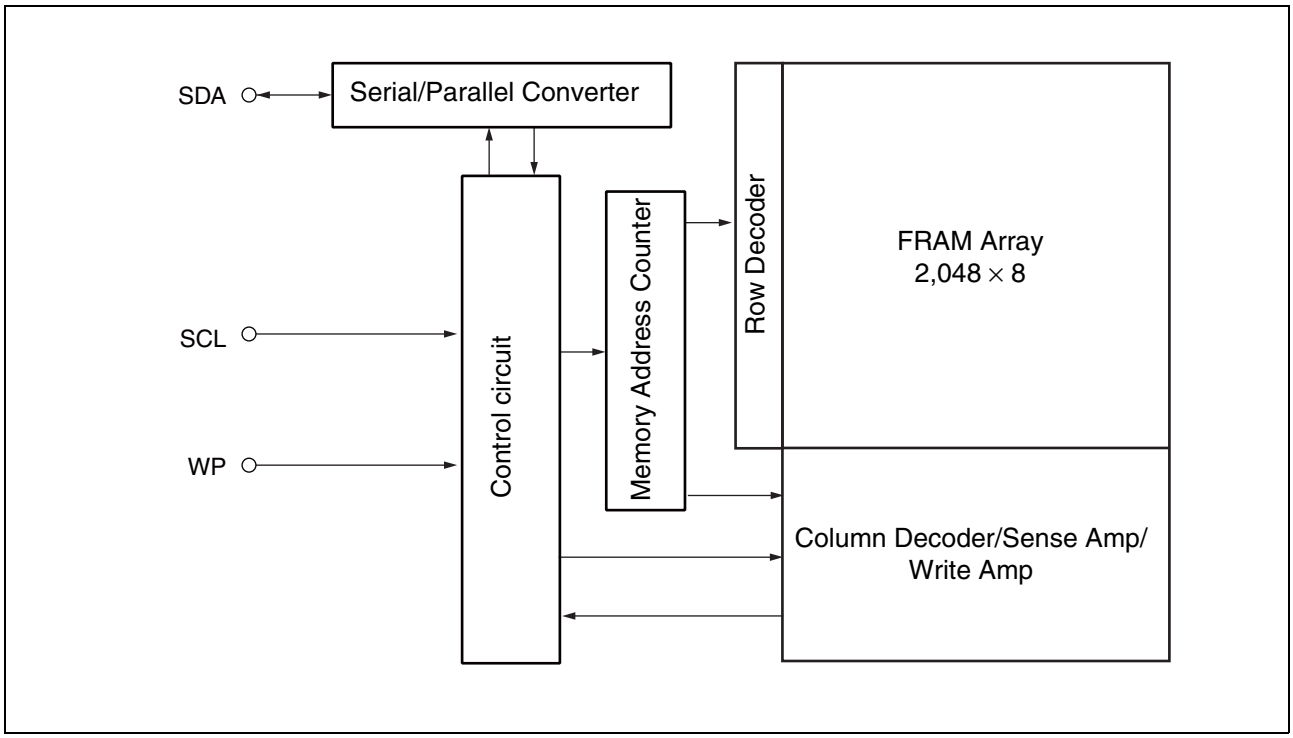


(FPT-8P-M02)

■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 3	NC	Unconnected pins Leave it unconnected.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin of serial data for performing bidirectional communication of memory address and writing or reading data. It is possible to connect some devices. It is an open drain output, so a pull-up resistance is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output timing serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When Write Protect pin is “H” level, writing operation is disabled. When Write Protect pin is “L” level, the entire memory region can be overwritten. Reading operation is always enabled regardless of the Write Protect pin state. The write protect pin is internally pulled down to VSS pin, and that is recognized as “L” level (the state that writing is enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

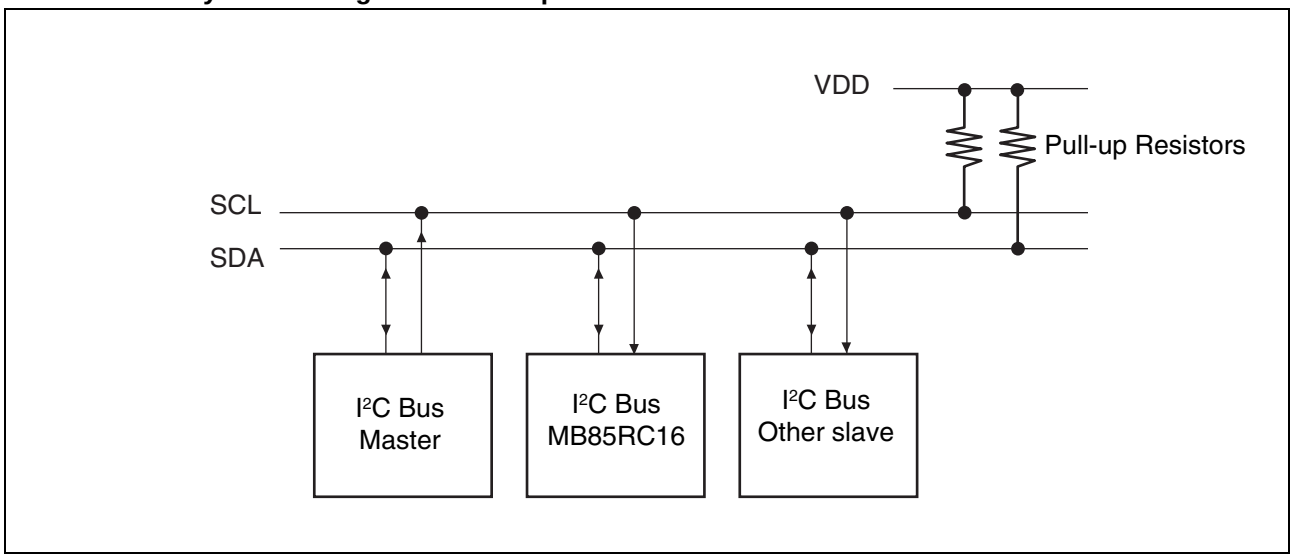
■ BLOCK DIAGRAM



■ I²C (Inter-Integrated Circuit)

The MB85RC16 has the two-wire serial interface and the I²C bus, and operates as a slave device.
The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, a I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration.

• I²C Interface System Configuration Example

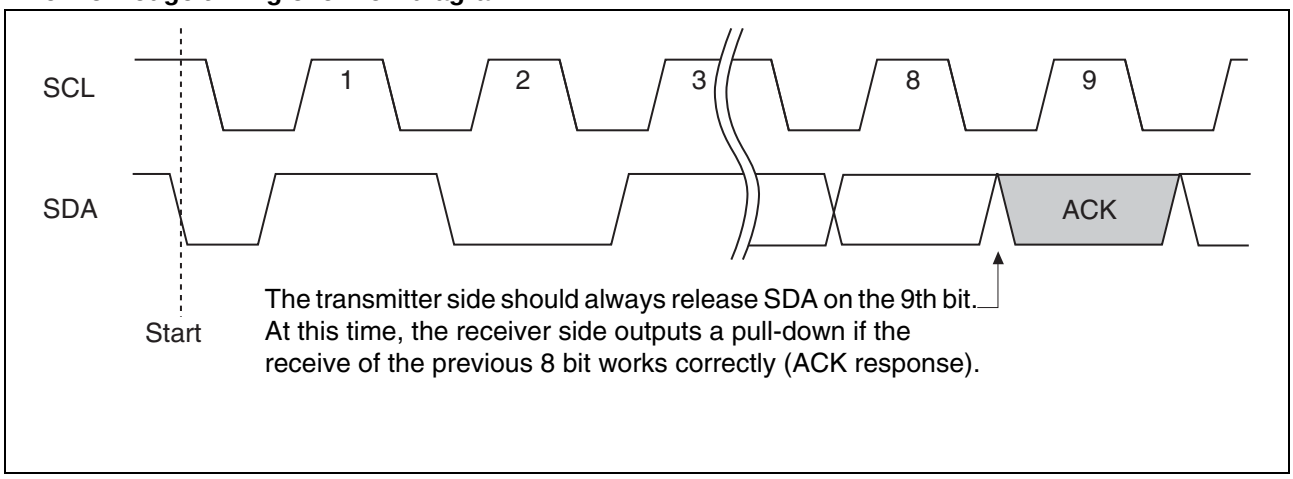


■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including memory address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after every 8 bits are successfully transmitted. On the transmitter side, the bus is temporarily released on this 9th clock to allow the acknowledge signal to be received and checked. During this released period, the receiver side pulls the SDA line down to indicate that the communication works correctly.

If the receiver side receives the stop condition before transmitting the acknowledge “L” level, the read operation ends and the I²C bus enters the standby state. If the acknowledge “L” level is not detected, and the Stop condition is not sent, the bus remains in the released state without doing anything.

• Acknowledge timing overview diagram



■ MEMORY ADDRESS STRUCTURE

The MB85RC16 has the memory address buffer to store the 11-bit information for the memory address.

As for byte write, page write and random read commands, the complete 11-bit memory address is configured by inputting the memory upper address (3 bits) and the memory lower address (8 bits), and saving to the memory address buffer and access to the memory is performed.

As for a current address read command, the complete 11-bit memory address is configured by inputting the memory upper address (3 bits) and by the memory address lower 8-bit which has saved in the memory address buffer, and saving to the memory address buffer and access to the memory is performed.

■ DATA STRUCTURE

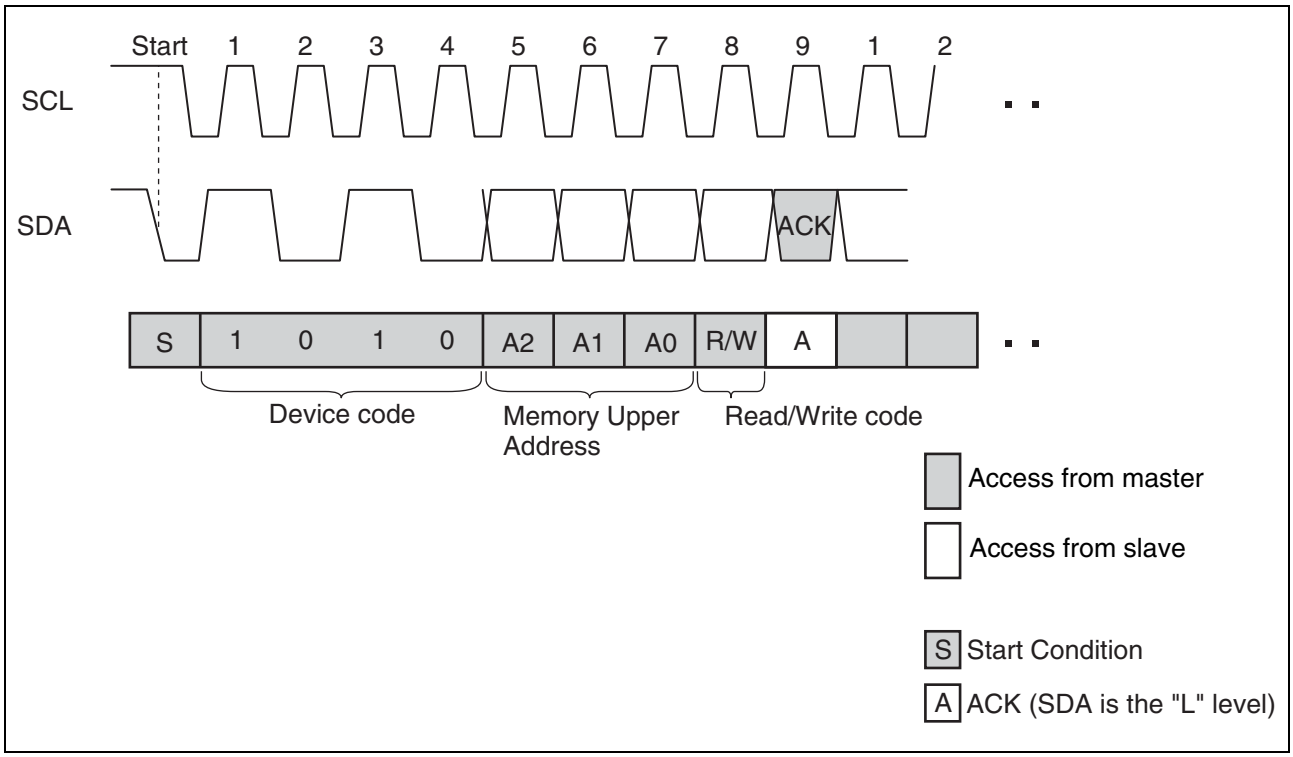
The master inputs the device address word (8 bits) following the start condition, and then the slave outputs the Acknowledge “L” level on the ninth bit. After confirming the Acknowledge response, the sequential 8-bit memory lower address is input, to the byte write, page write and random read commands.

As for the current address read command, inputting the memory lower address is not performed, and the address buffer lower 8-bit is used as the memory lower address.

When inputting the memory lower address finishes, the slave outputs the Acknowledge “L” level on the ninth bit again.

Afterwards, the input and the output data continue in 8-bit units, and then the Acknowledge “L” level is output for every 8-bit data.

• Device Address Word



■ FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC16 performs the high speed write operations, so any waiting time for an ACK* by the acknowledge polling does not occur.

*: In E^2PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

■ WRITE PROTECT (WP)

The entire memory array can be write protected by setting the WP pin to the “H” level. When the WP pin is set to the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

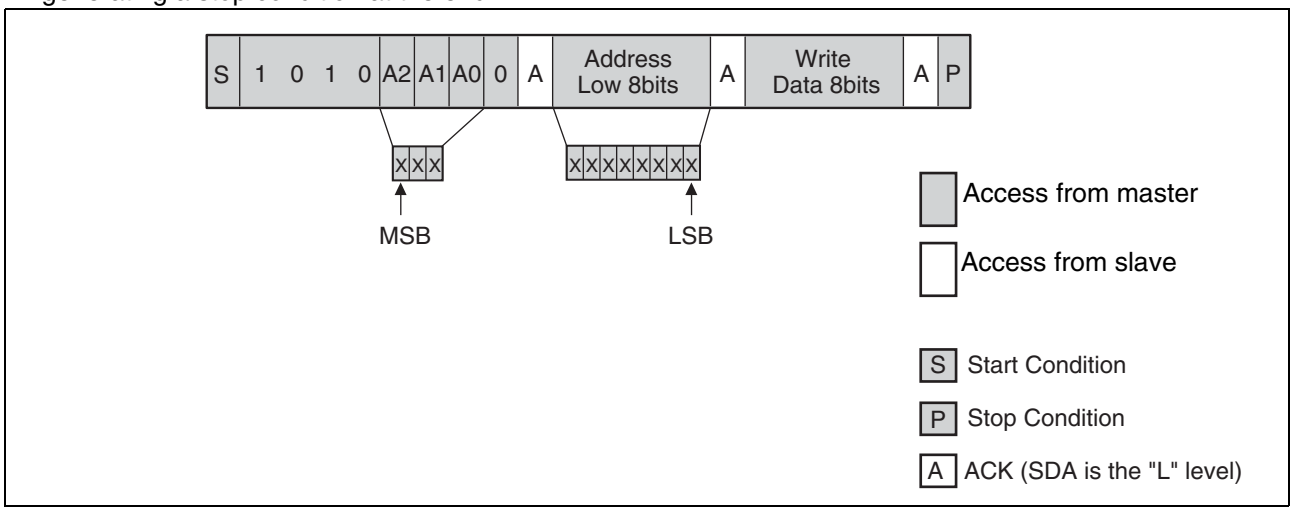
Do not change the WP signal level during the communication period from the start condition to the stop condition.

Note : The WP pin is pulled down internally to VSS pin, therefore if the WP pin is open, the pin status is detected as the “L” level (write enabled).

■ COMMAND

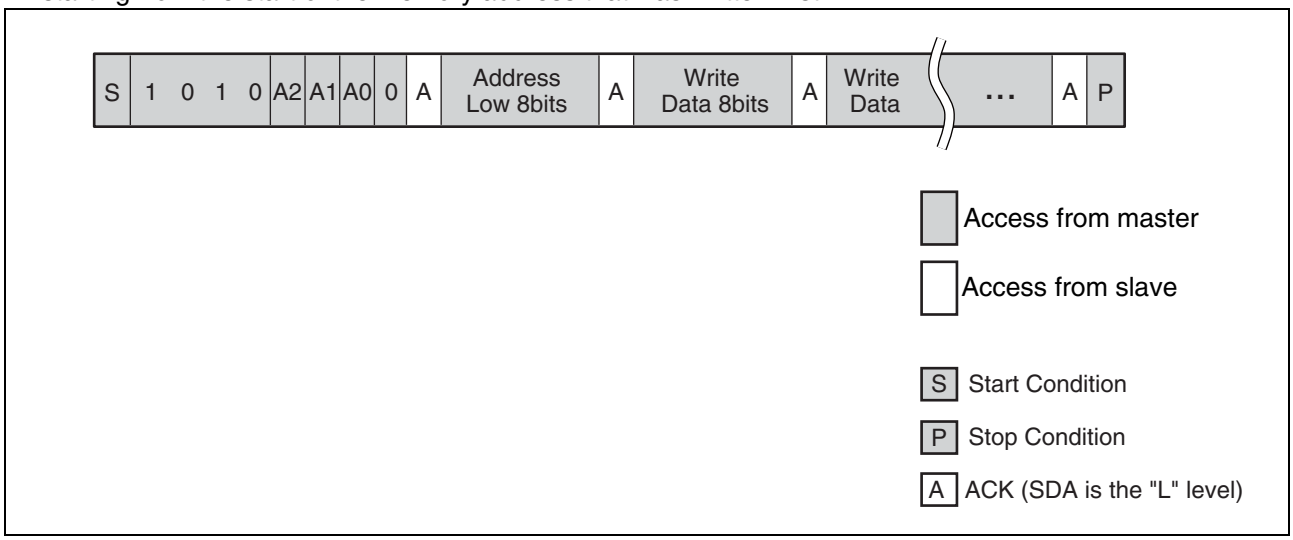
• Byte Write

If the device address word (R/W “0” input) is sent after the start condition, an ACK responds from the slave. After this ACK, write memory addresses and write data are sent in the same way, and the write ends by generating a stop condition at the end.



• Page Write

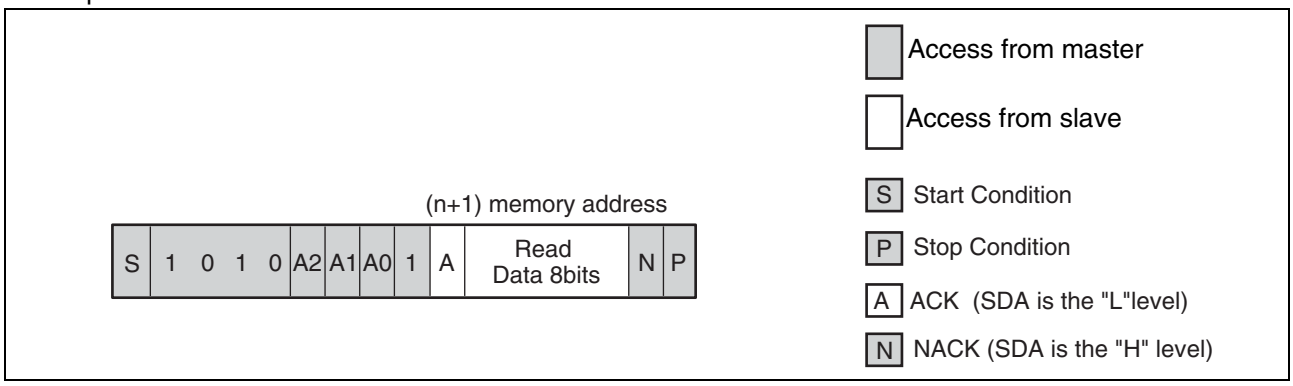
If data is continuously sent after the following address when the same command (expect stop condition) as Byte Write was sent, a page write is performed. The memory address rolls over to first memory address (000_H) at the end of the address. Therefore, if more than 2 Kbytes are sent, the data is overwritten in order starting from the start of the memory address that was written first.



• Current Address Read

If the last write or read operation finishes correctly up to the end of stop condition, the memory address that was accessed last remains in the memory address buffer (the length is 11 bits).

When sending this command without turning the power off, it is possible to read from the memory address n+1 which adds 1 to the total 11-bit memory address n, which consists of the memory upper address 3-bit from the device address word input and the lower 8-bit of the memory address buffer. If the memory address n is the last address, it is possible to read with rolling over to the head of the memory address (000_H). The current address (address that the memory address buffer indicates) is undefined immediately after turning the power on.

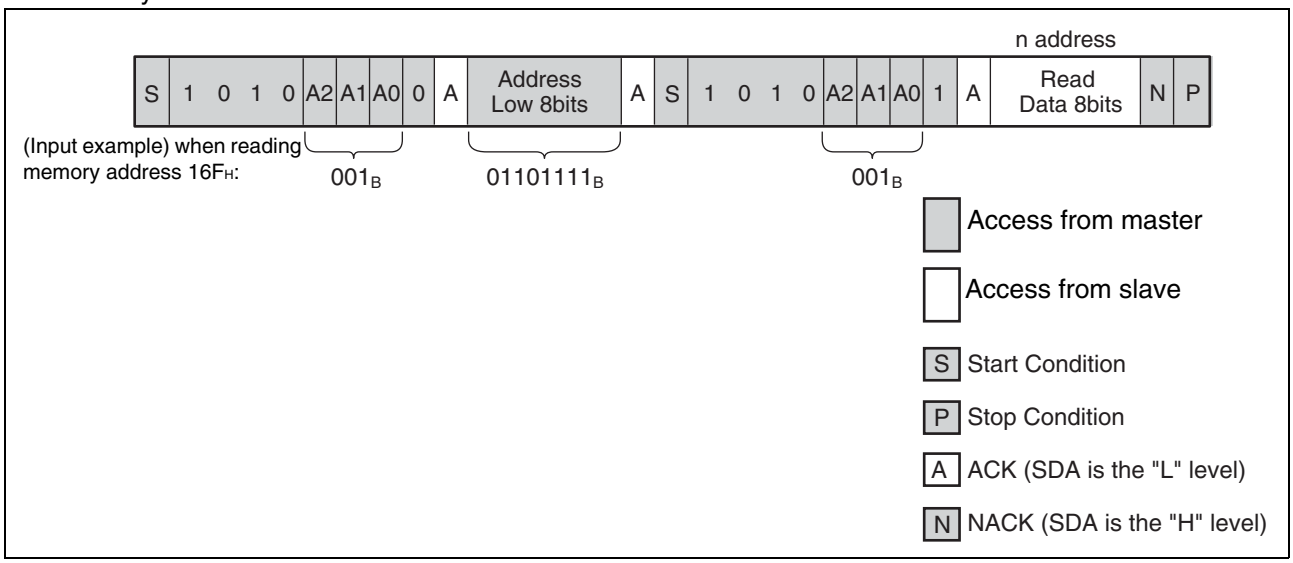


• Random Read

The one byte of data from the memory address as saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

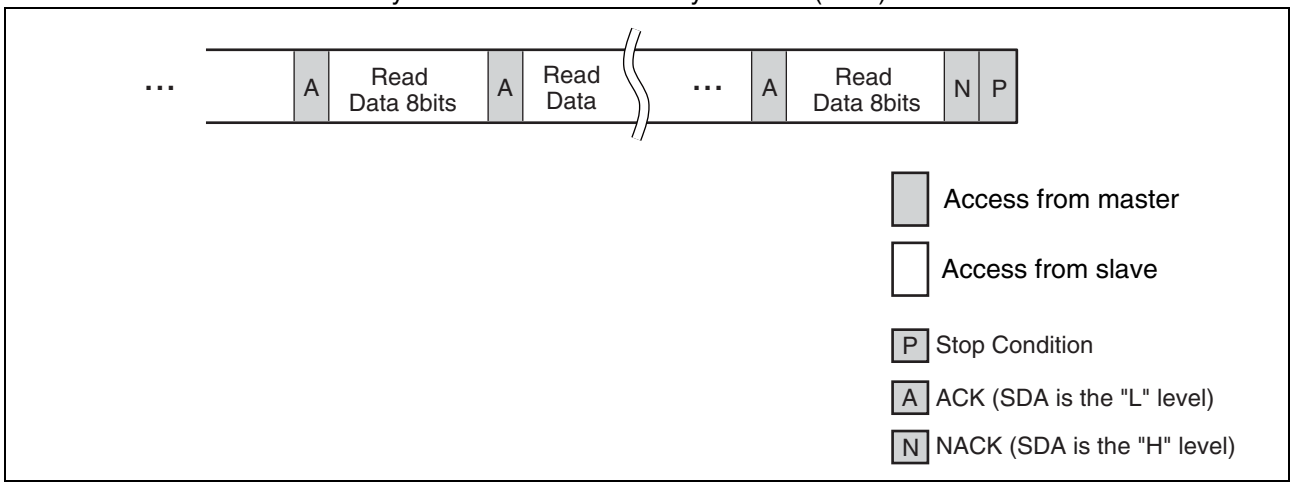
Setting values for the first and the second memory upper address codes should be the same.

The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



• Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address for the MB85RC16, the read address automatically rolls over to first memory address (000_H).



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 40	+ 125	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	2.7	3.3	3.6	V
“H” level input voltage*	V_{IH}	$V_{DD} \times 0.8$	—	V_{DD} + 0.5 (≤ 4.0)	V
“L” level input voltage*	V_{IL}	− 0.5	—	+ 0.6	V
Ambient temperature	T_A	− 40	—	+ 85	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	1	µA
Output leakage current*2	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	—	—	1	µA
Operating power supply current	I_{CC}	SCL = 1 MHz	—	70	100	µA
Standby current	I_{SB}	SCL, SDA = V_{DD} WP = 0V or V_{DD} or OPEN T_A = + 25 °C	—	0.1	1	µA
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
Input resistance for WP pin	R_{IN}	V_{IN} = V_{IL} (Max)	50	—	—	kΩ
		V_{IN} = V_{IH} (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

2. AC Characteristics

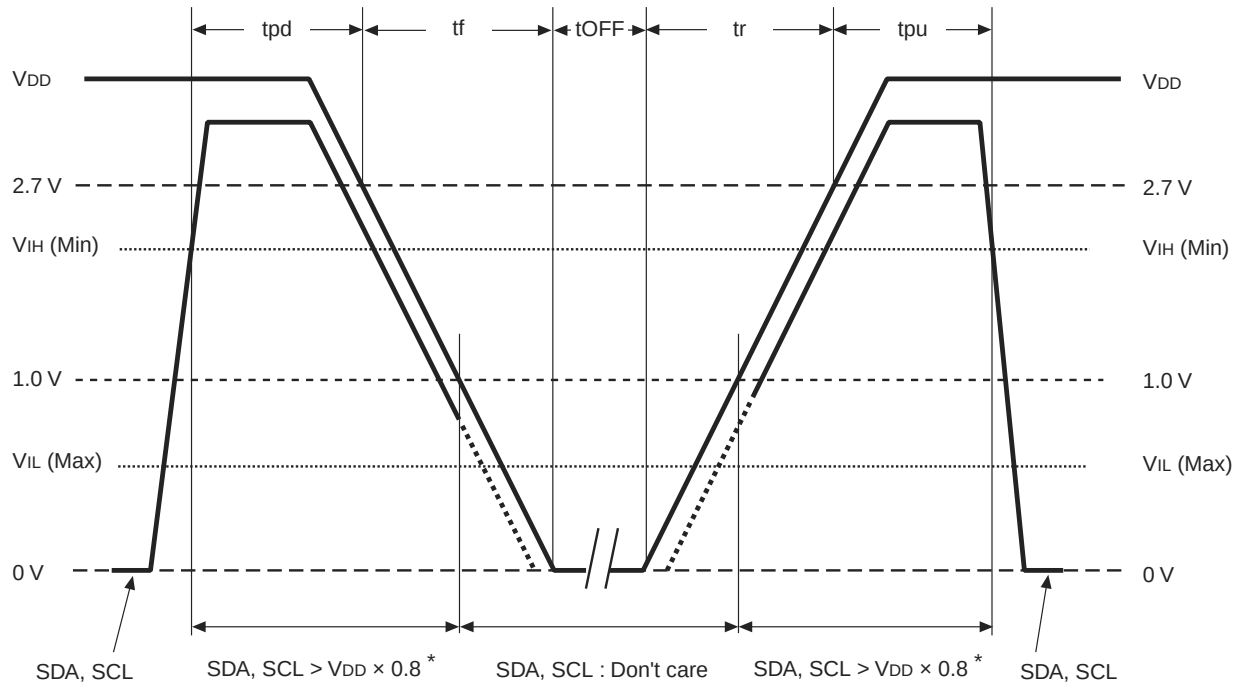
(within recommended operating conditions)

Parameter	Symbol	Value				Unit
		STANDARD MODE		FAST MODE		
		Min	Max	Min	Max	
SCL clock frequency	FSCL	0	400	0	1000	kHz
Clock high time	T_{HIGH}	600	—	400	—	ns
Clock low time	T_{LOW}	1300	—	600	—	ns
SCL/SDA rise time	T_r	—	300	—	300	ns
SCL/SDA fall time	T_f	—	300	—	100	ns
Start condition hold	$T_{HD:STA}$	600	—	250	—	ns
Start condition setup	$T_{SU:STA}$	600	—	250	—	ns
SDA input hold	$T_{HD:DAT}$	0	—	0	—	ns
SDA input setup	$T_{SU:DAT}$	100	—	100	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	0	—	ns
Stop condition setup	$T_{SU:STO}$	600	—	250	—	ns
SDA output access after SCL fall	T_{AA}	—	900	—	550	ns
Pre-charge time	T_{BUF}	1300	—	500	—	ns
Noise suppression time constant on SCL, SDA	T_{SP}	—	50	—	50	ns

AC characteristics were measured under the following measurement conditions.

Power supply voltage : 2.7 V to 3.6 V
Operating temperature : – 40 °C to + 85 °C
Input voltage amplitude : 0.3 V to 2.7 V
Input rise time : 5 ns
Input fall time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

POWER ON SEQUENCE



* : SDA, SCL (Max) < V_{DD} + 0.5 V

Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85		ns
SDA, SCL level hold time during power up	tpu	85		ns
Power supply rise time	tr	0.01	50	ms
Power supply fall time	tf	0.01	50	ms
Power off time	tOFF	50		ms

NOTES ON USE

- Data written before performing IR reflow is not guaranteed after IR reflow.
- V_{DD} is required to be rising from 0 V because turning the power on from an intermediate level may cause malfunctions, when the power is turned on.

MEMO

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