

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.5Ω (+2.7V Supply)
- Wide V_{CC} Range: +1.65V to +4.2V ±10%
- I_{CC} = 0.3μA @ T_A = +25°C
- Rail-to-Rail switching throughout Signal Range
- Fast Switching Speed: 20ns max. at 3.3V
- High Off Isolation: -65dB @ 100 kHz
- Crosstalk Rejection: -65dB @ 100 kHz
- Extended Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green):
 - 16-contact TQFN (ZL16), 2.5mm x 2.5mm
 - 16-contact TQFN (ZH16), 3.0mm x 3.0mm

Applications

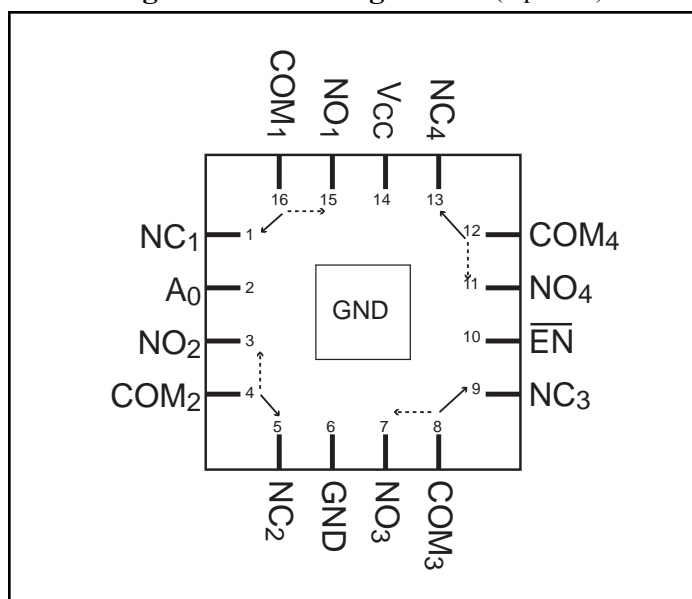
- Cell Phones
- PDAs
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals
- Audio & Video Signal Routing
- PCMCIA Cards
- Modems
- Hard Drives
- JTAG Testing

Description

The PI3A412E is a Quad single-pole double-throw (SPDT) CMOS switch with enable. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, +1.65V to +4.2V, the switch has an On-Resistance of 0.5Ω at 2.7V.

Control inputs, A₀ to $\overline{\text{EN}}$, tolerates input drive signals up to 5V, independent of supply voltage.

Block Diagram / Pin Configuration (top view)



Pin Description

Pin #	Name	Description
4, 8, 12, 16	COM _X	Common Output / Data Port
1, 5, 9, 13	NC _X	Data Port (normally connect)
3, 7, 11, 15	NO _X	Data Port (normally open)
10	$\overline{\text{EN}}$	Enable
2	A ₀	Logic Input Control
6	GND	Ground
14	V _{CC}	Positive Power Supply

Note :

1. X = 1, 2, 3, or 4

Function Table

$\overline{\text{EN}}$	A ₀	Function
1	X	No Switch Connected, All I/O = Hi-Z
0	0	NC _X Connected to COM _X
0	1	NO _X Connected to COM _X

Note :

1. X = 1, 2, 3, or 4.

Absolute Maximum Ratings

Voltages Referenced to GND

V_{CC} -0.5V to +4.6V

V_{NC} , V_{NO} , V_{COM} ⁽¹⁾ -0.5V to V_{+} +0.3V
 or 30mA, whichever occurs first

Current (any terminal)..... ±400mA

Peak Current

(Pulsed at 1ms, 10% duty cycle)..... ±500mA

Thermal Information

Continuous Power Dissipation

16-pin Tin TQFN (derate 7.1mW/°C above +70°C) 0.5W

Storage Temperature -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note 1: Signals on NC, NO, COM, or \overline{EN}_1 , A_0 exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Single +4.2V Supply

($V_{CC} = +4.2V \pm 10\%$, GND = 0V, $V_{IH} = 1.4V$, $V_{IL} = 0.7V$) ($T_A = -40^\circ C$ to $+85^\circ C$)

Parameter	Symbol	Conditions	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch						
Analog Signal Range ⁽³⁾	V_{ANALOG}		0		V_{CC}	V
On Resistance	R_{ON}	$V_{CC} = 4.0V$, $I_{COM} = 100mA$, $V_{NC} = +1.5V$		0.4	0.5	Ω
On-Resistance Match Between Channels ⁽⁴⁾	ΔR_{ON}			0.01	0.03	
On-Resistance Flatness ⁽⁵⁾	$R_{FLAT(ON)}$			0.06	0.15	
Off Leakage Current ⁽⁶⁾	$I_{NO(OFF)}$, or $I_{NC(OFF)}$	$V_{CC} = 4.4V$, V_{NO} or $V_{NC} = 0.3V$, 3.3V	-200		200	nA
On Leakage Current ⁽⁶⁾	$I_{COM(ON)}$	$V_{CC} = 4.4V$, V_{NO} or $V_{NC} = 0.3V$, 3.3V	-200		200	

Notes:

- The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
- Typical values are $T_A = 25^\circ C$, $V_{CC} = 4.2V$ unless otherwise specified.
- Guaranteed by design.
- $\Delta R_{ON} = R_{ON}$ match between channels
- Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
- Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at $+25^\circ C$.

Electrical Specifications - Single +4.2V Supply

(V_{CC} = +4.2V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.7V) (T_A = -40°C to +85°C)

Description	Param- eters	Test Conditions	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Logic Input						
Input High Voltage	V _{IH}	Guaranteed logic High Level	1.4			V
Input Low Voltage	V _{IL}	Guaranteed logic Low Level			0.7	
Input Current with Voltage High	I _{AH}	V _A = 1.4V, all others = 0.5V	−1		1	μA
Input Current with Voltage Low	I _{AL}	V _A = 0.5V, all other = 1.4V	−1		1	
Dynamic						
Turn-On Time	t _{ON}	V _{CC} = 4.2V, V _{NO} = 2.0V, Figure 1 & 2		20	25	ns
Turn-Off Time	t _{OFF}			12	15	
Break-Before-Make	t _{BBM}	V _{NO} = 1.5V, R _L = 50Ω, C _L = 35pF, See Figure 3	1	12	15	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 4		100		pC
Off Isolation ⁽⁴⁾	O _{IRR}	R _L = 50Ω, f = 100 kHz, Figure 5		-65		dB
Cross Talk ⁽⁵⁾	X _{TALK}	R _L = 50Ω, f = 100 kHz, Figure 6		-65		
3dB Bandwidth	f _{3db}	See Test Circuit Figure 9		40		MHz
Off Capacitance	C _{NO(OFF)}	f = 1 MHz, Figure 7		45		pF
Off Capacitance	C _{NC(OFF)}			45		
On Capacitance	C _{ON}	f = 1 MHz, Figure 8		150		
Supply						
Power-Supply Range	V _{CC}		1.5		4.6	V
Positve Supply Current	I _{CC}	V _{CC} = 4.4V, V _{COM} = 0V or V _{CC}			0.4	μA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are V_{CC} = 4.2V unless otherwise specified.
3. Guaranteed by design.
4. Off Isolation = 20log₁₀ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
5. Between any two switches. See Figure 5.

Electrical Specifications - Single +3.3V Supply

($V_{CC} = +3.3V \pm 10\%$, $GND = 0V$, $V_{IH} = 1.3V$, $V_{IL} = 0.5V$) ($T_A = -40^\circ C$ to $+85^\circ C$)

Parameter	Symbol	Conditions	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch						
Analog Signal Range ⁽³⁾	V_{ANALOG}		0		V_{CC}	V
On Resistance	R_{ON}	$V_{CC} = 2.7V$, $I_{COM} = 100mA$, $V_{NC} = +1.5V$		0.5	0.65	Ω
On-Resistance Match Between Channels ⁽⁴⁾	ΔR_{ON}			0.02	0.05	
On-Resistance Flatness ⁽⁵⁾	$R_{FLAT(ON)}$			0.05	0.15	
Off Leakage Current ⁽⁶⁾	$I_{NO(OFF)}$, or $I_{NC(OFF)}$	$V_{CC} = 3.6V$, V_{NO} or $V_{NC} = 0.3V, 3.3V$	-150		150	nA
On Leakage Current ⁽⁶⁾	$I_{COM(ON)}$	$V_{CC} = 3.6V$, V_{NO} or $V_{NC} = 0.3V, 3.3V$	-150		150	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are $V_{CC} = 3.3V$ unless otherwise specified.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ match between channels
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at $+25^\circ C$.

Electrical Specifications - Single +3.3V Supply

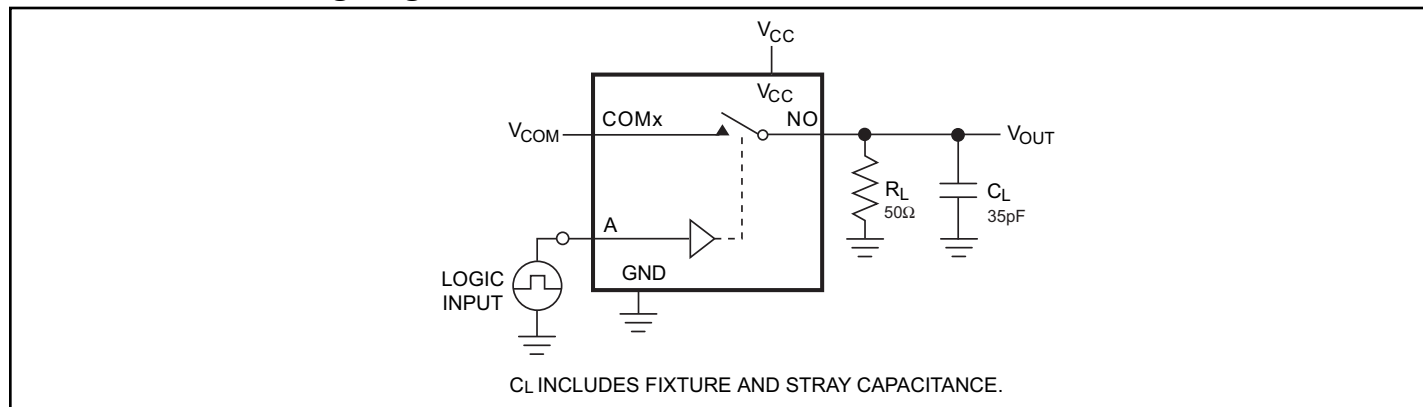
(V_{CC} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.3V, V_{IL} = 0.5V) (T_A = -40°C to +85°C)

Description	Parameters	Test Conditions	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Logic Input						
Input High Voltage	V _{IH}	Guaranteed logic High Level	1.3			V
Input Low Voltage	V _{IL}	Guaranteed logic Low Level			0.5	
Input Current with Voltage High	I _{AH}	V _A = 1.4V, all others = 0.5V	−1		1	μA
Input Current with Voltage Low	I _{AL}	V _A = 0.5V, all other = 1.4V	−1		1	
Dynamic						
Turn-On Time	t _{ON}	V _{CC} = 3.3V, V _{NO} = 2.0V, Figure 1 & 2		20	25	ns
Turn-Off Time	t _{OFF}			12	15	
Break-Before-Make	t _{BBM}	V _{NO} = 1.5V, R _L = 50Ω, C _L = 35pF, See Figure 3	1	12	15	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 4		100		pC
Off Isolation ⁽⁴⁾	O _{IRR}	R _L = 50Ω, f = 100 kHz, Figure 5		-65		dB
Cross Talk ⁽⁵⁾	X _{TALK}	R _L = 50Ω, f = 100 kHz, Figure 6		-65		
3dB Bandwidth	f _{3db}	See Test Circiut Figure 9		40		MHz
Off Capacitance	C _{NO(OFF)}	f = 1 MHz, Figure 7		45		pF
Off Capacitance	C _{NC(OFF)}			45		
On Capacitance	C _{ON}	f = 1 MHz, Figure 8		150		
Supply						
Power-Supply Range	V _{CC}		1.5		4.6	V
Positve Supply Current	I _{CC}	V _{CC} = 3.6V, V _{COM} = 0V or V _{CC}			0.3	μA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are T_A = 25°C, V_{CC} = 3.3V unless otherwise specified.
3. Guaranteed by design.
4. Off Isolation = 20log₁₀ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
5. Between any two switches. See Figure 5.

Test Circuits and Timing Diagrams



Notes:

Unused Bx inputs must be grounded.

Figure 1. AC Test Circuit

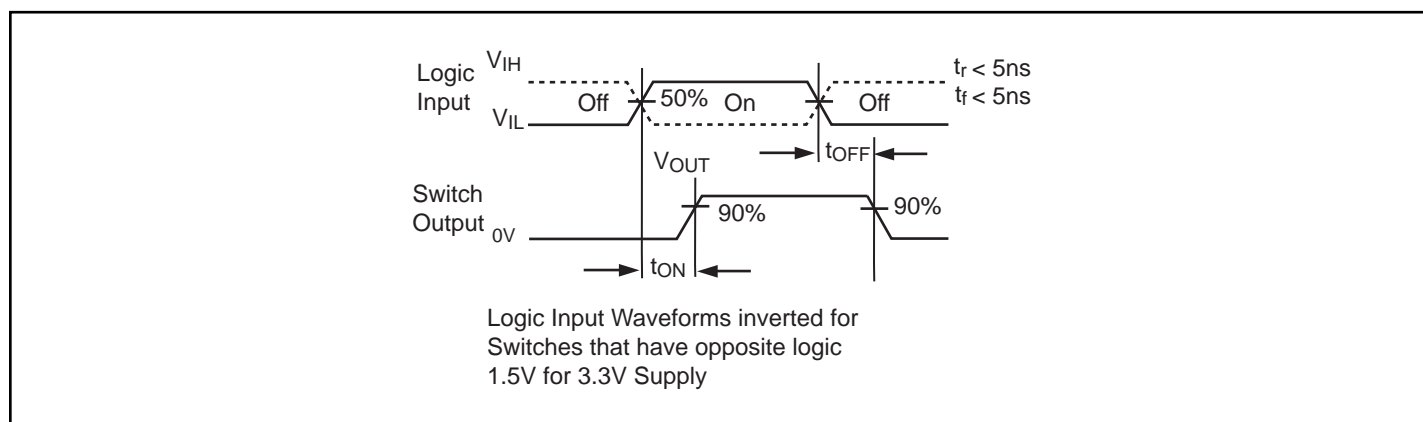


Figure 2. AC Waveforms

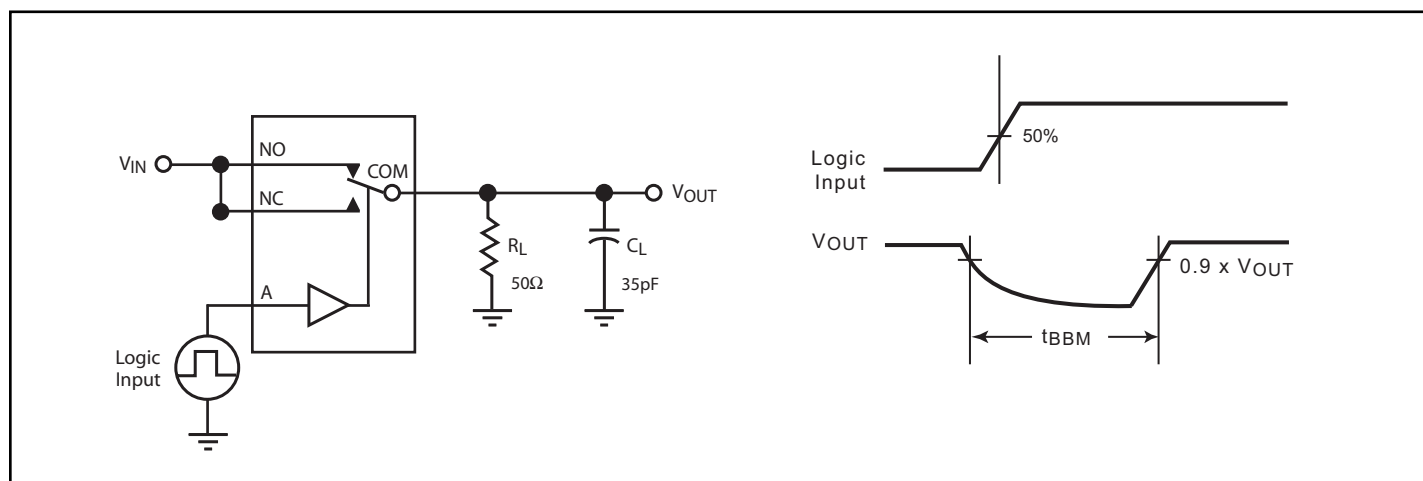


Figure 3. Break Before Make Interval Timing

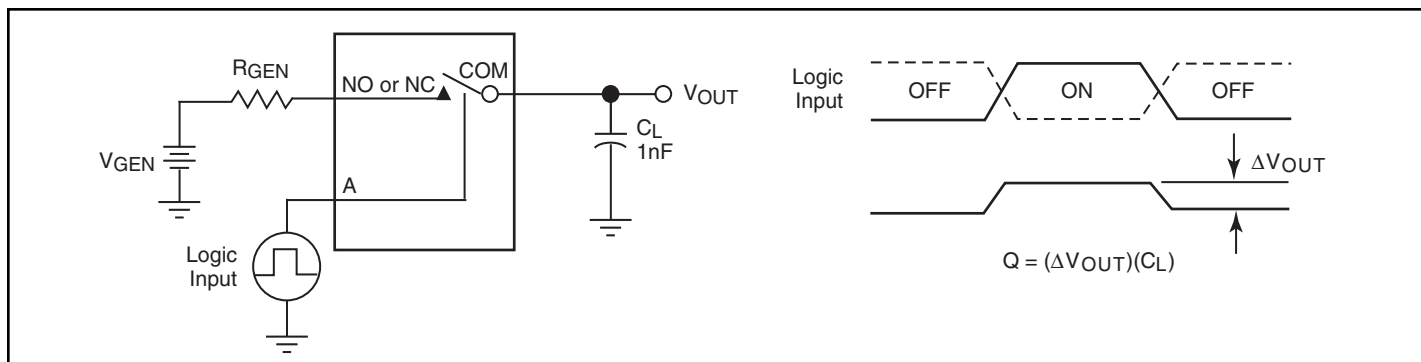


Figure 4. Charge Injection Test

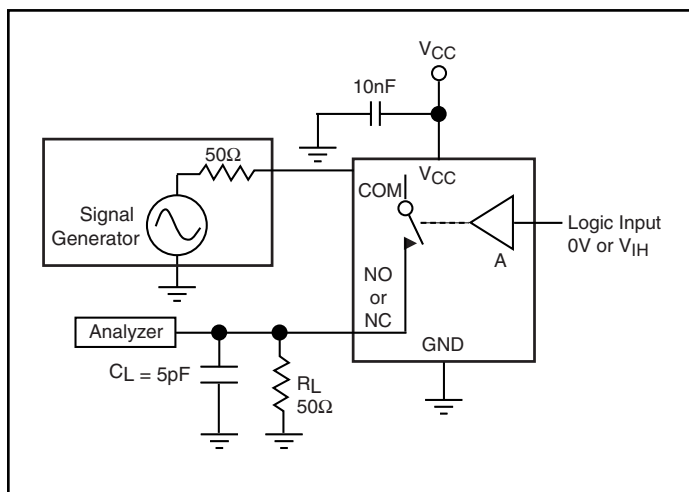


Figure 5. Off Isolation

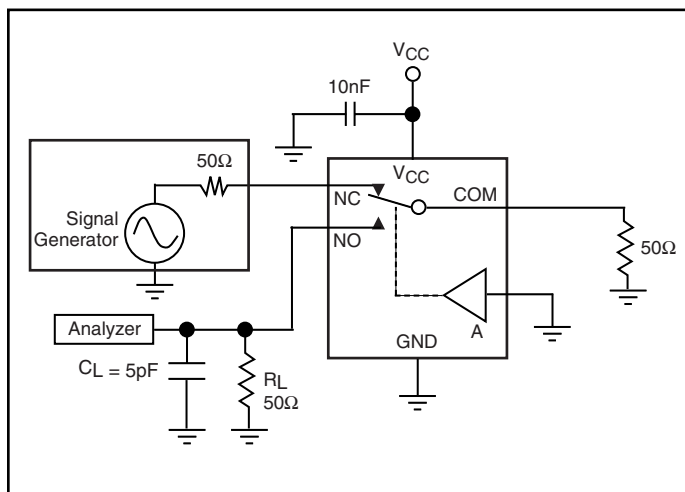


Figure 6. Crosstalk

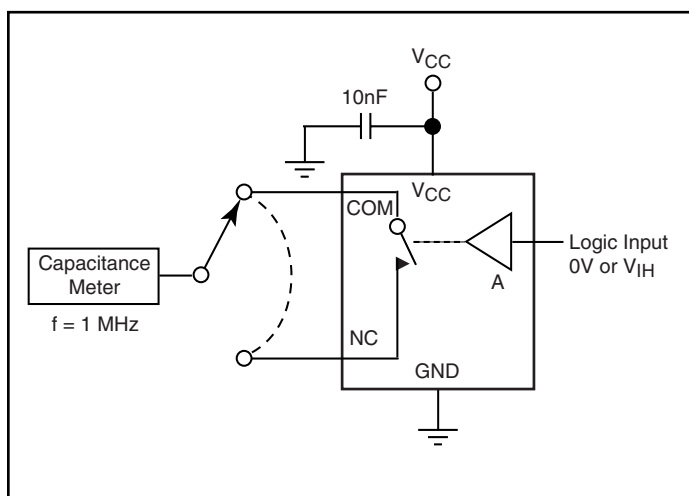


Figure 7. Channel Off Capacitance

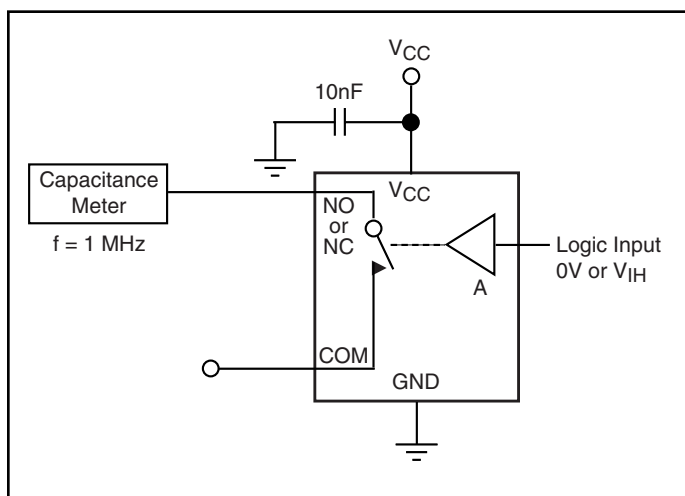


Figure 8. Channel On Capacitance

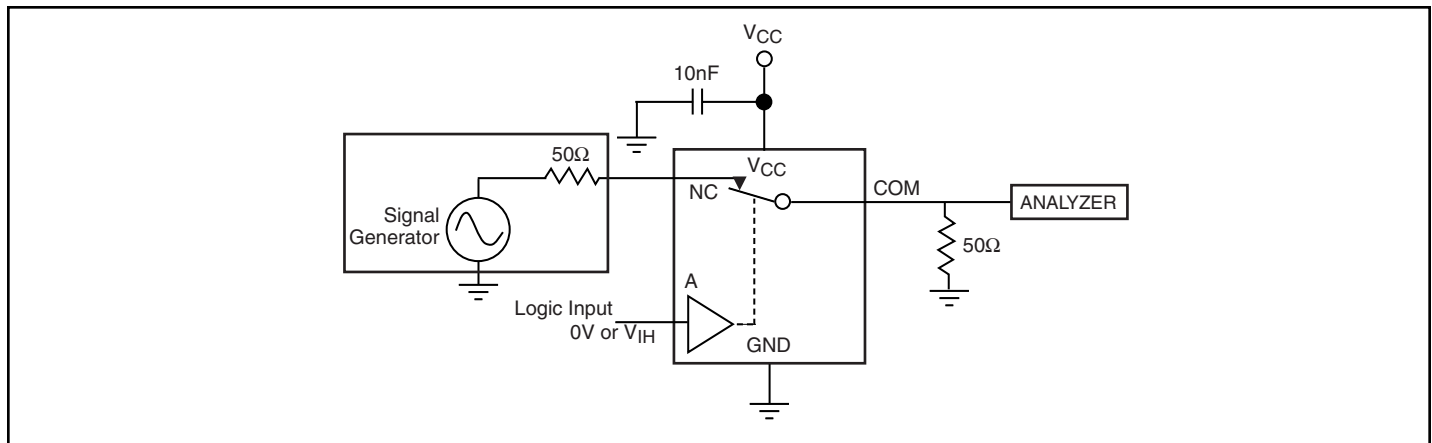
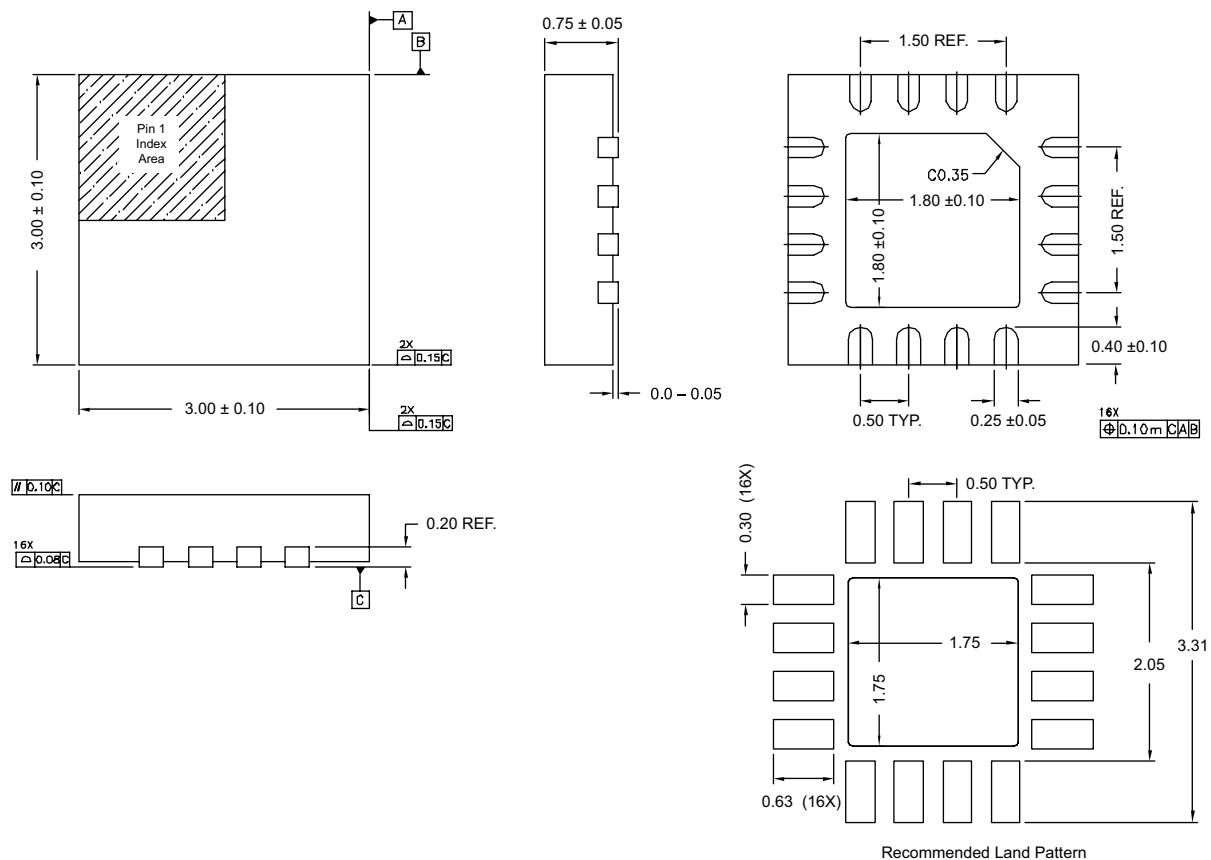


Figure 9. Bandwidth



Notes:

- 1) All dimensions are in millimeters
- 2) Ref JEDEC: MO-220J (WEED)
- 3) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals



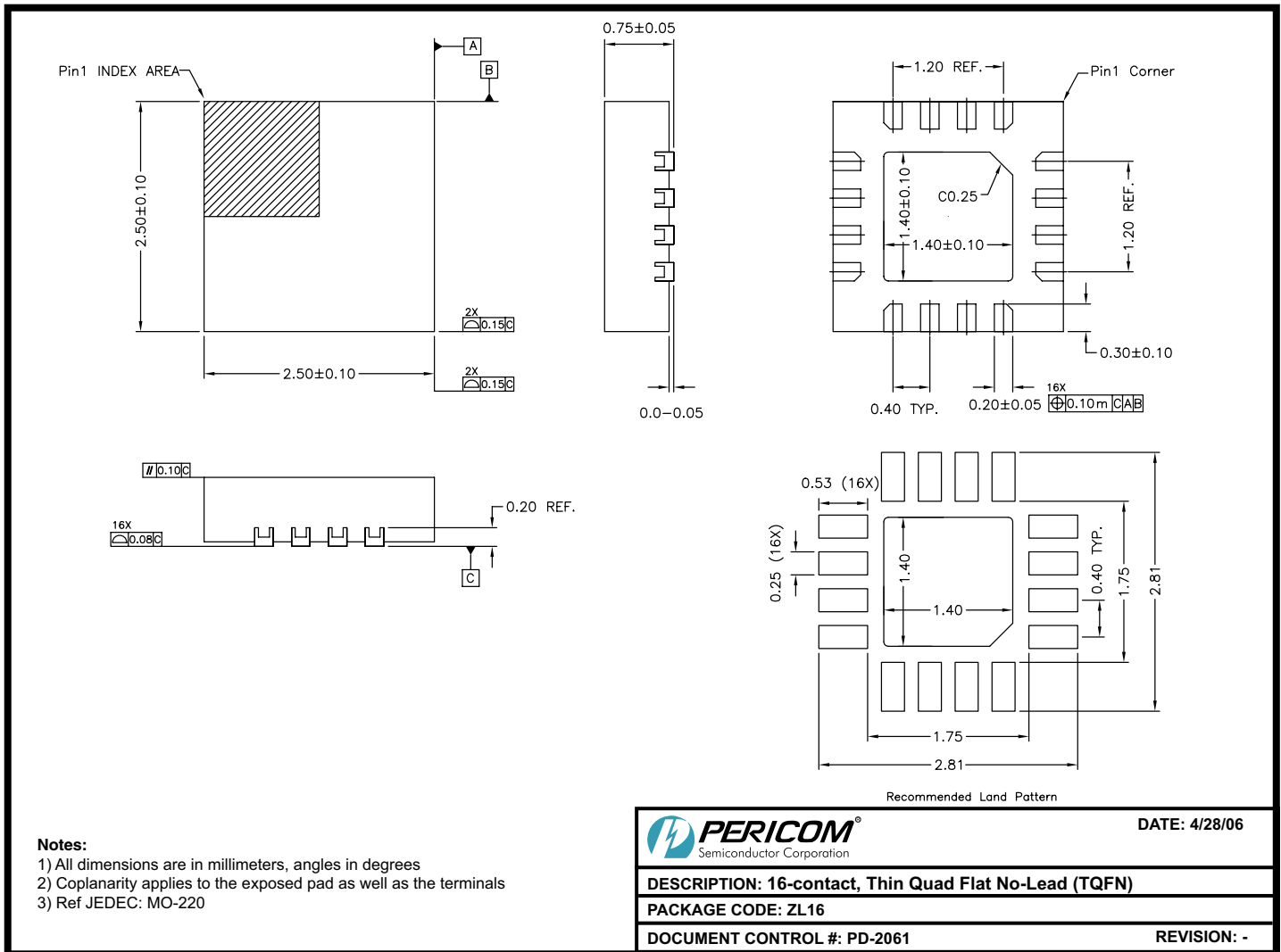
DATE: 03/16/06

DESCRIPTION: 16-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH16)

DOCUMENT CONTROL #: PD-2047

REVISION: A



Ordering Information

Ordering Code	Package Code	Package Description
PI3A412EZLE	ZL	Pb-free & Green, 16-contact TQFN
PI3A412EZHE	ZH	Pb-free & Green, 16-contact TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding X suffix = Tape/Reel